GL339/339A
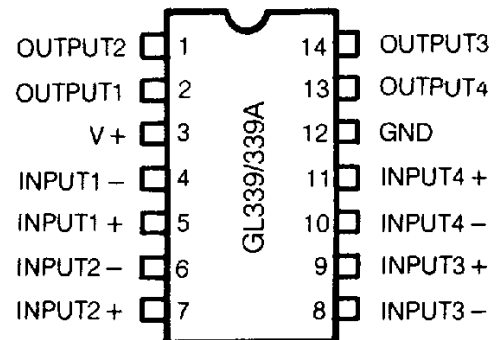## LOW POWER, LOW OFFSET VOLTAGE QUAD COMPARATORS

Description

The GL339 consists of four independent precision voltage comparators designed specifically to operate from a single power supply Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stage allows the input common-mode voltage to include ground.

Features

- **Single Supply Operation +2.0V to +36V**
- **Dual Supply Operation ±1.0V to ±18V**
- **Compatible with All forms of Logic**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 800 μA TYP**
- **Low Input Bias Current 25nA TYP**
- **Low Input Offset Current ±5 nA TYP**
- **Low Offset Voltage ±2mV**

Pin Configuration

OUTPUT2	1	14 OUTPUT3
OUTPUT1	2	13 OUTPUT4
V+	3	12 GND
INPUT1−	4	11 INPUT4+
INPUT1+	5	10 INPUT4−
INPUT2−	6	9 INPUT3+
INPUT2+	7	8 INPUT3−

GL339/339A

Absolute Maximum Ratings

Supply Voltage. V+	+36V or ±18V
Differential Input Voltage	36V
Input Voltage Range	—0 3V to +36V
Power Pissipation	1000 mW
Input current (V_{IN}<—0 3V)	50 mA
Operating Temperature Range	·0°C to +70°C
Storage Temperature Range	—55°C to +125°C
Pin Temperature	. 260°C

Shematic Diagram
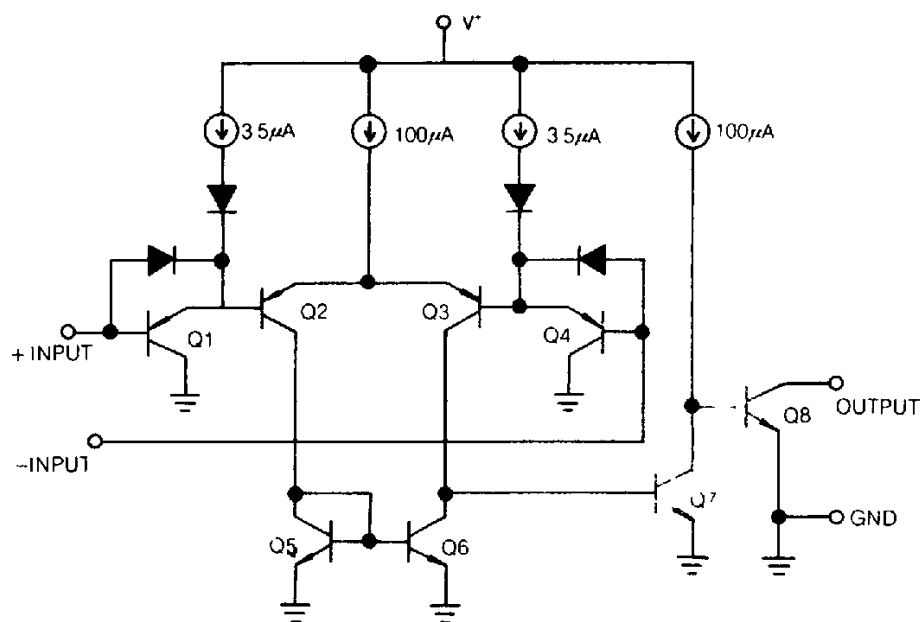
**Electrical Characteristics:** $V^+ = 5V, T_A = 25°C$, unless otherwise specified)

| PARAMETER	Test Conditions		GL339			GL339A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offest Voltage	At out switch point $V_O = 1.4$, $R_S = 0$ $V_{REF} = 1.4V$			±2	±5		±1	±2	mV
		$0°C \leqslant T_A \leqslant 70°C$			9			4	
Input Bias Current (1)	Output in linear range			25	250		25	250	nA
		$0°C \leqslant T_A \leqslant 70°C$			400			400	
Input Offset Current				±5	±50		±5	±50	nA
		$0°C \leqslant TA \leqslant 70°C$			±150			±150	
Input Common-Mode Voltage Range (2)			0		$V^+ -1.5$	0		$V^+ -1.5$	V
		$0°C \leqslant TA \leqslant 70°C$	0		$V^+ -2.0$	0		$V^+ -2.0$	
Supply Current	$R_L = \infty$			0.8	2.0		0.8	2.0	mA
Supply Current	$V_{CC} = 30V$, $R_L = \infty$				2.5			2.5	mA
Voltage Gain	$R_L \geqslant 15K\Omega$, $V^+ = 15V$		93	106		93	106		dB
Large Signal Response Time	$V_{IN} = TTL$ logic swing $V_{REF} = 1.4V$, $R_L = 5.1K\Omega$ $V_{RL} = 5V$			300			300		ns
Response Time (3)	$V_{RL} = 5V$, $R_L = 5.1K\Omega$			1.3			1.3		μs
Ouptur Sink Current	$V_{IN(-)} \geqslant 1V$, $V_{IN(+)} = 0V$, $V_O \leqslant 1.5V$		6	16		6	16		mA
Output Saturation	$V_{IN(-)} \geqslant 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leqslant 4mA$			250	400		250	400	mV
		$0°C \leqslant TA \leqslant 70°C$			700			700	
Output Leakage	$V_{IN(+)} \geqslant 1V$ $V_{IN(-)} = 0V$			0.1			0.1		nA
		$0°C \leqslant TA \leqslant 70°C$			1000			1000	
Differential Input Voltage	All $V_{IN} \geqslant 0V$ (or V^- if split supply is used) $0°C \leqslant T_A \leqslant 70°C$			V^+			V^+		V

NOTES:

(1) The direction of the current is out of the IC due to the PNP input stage This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs This conditions is not destructive providing the input current is limited to less than 50mA

(3) The response time specified is for a 100mA input step with 5mV overdrive For larger overdrive signals 300 nsec can be obtained
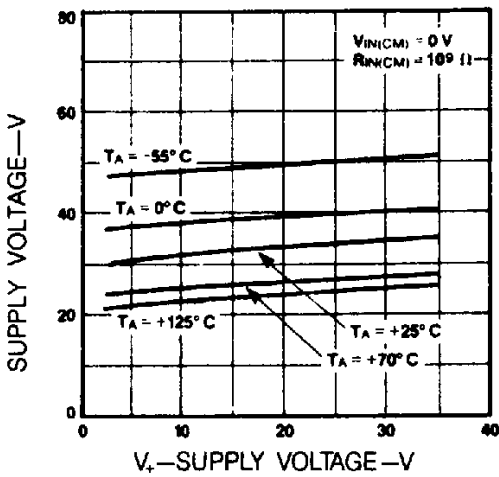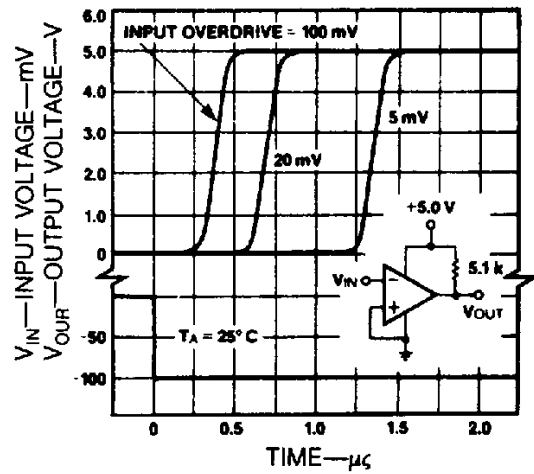
TYPICAL PREFORMANCE CURVES

Supply Current
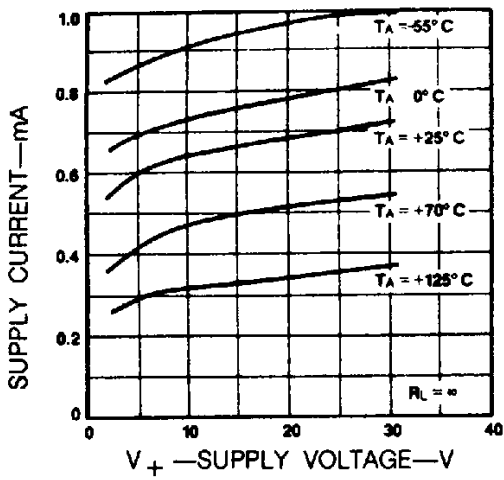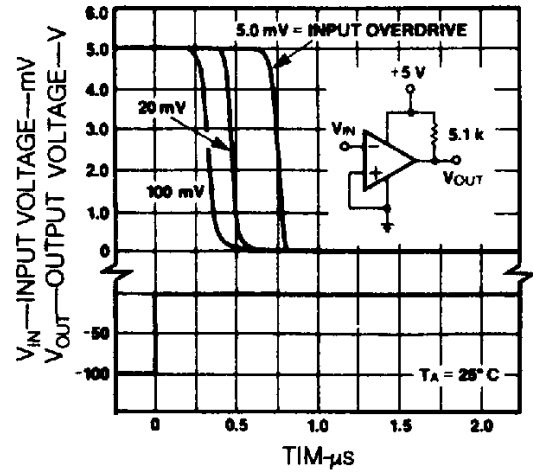
Input Current

Output Saturation Voltage

Reaponse Time for Various input Overdrives—Negative Transition

Response Time for Various Input Overdrives—Positive Transition
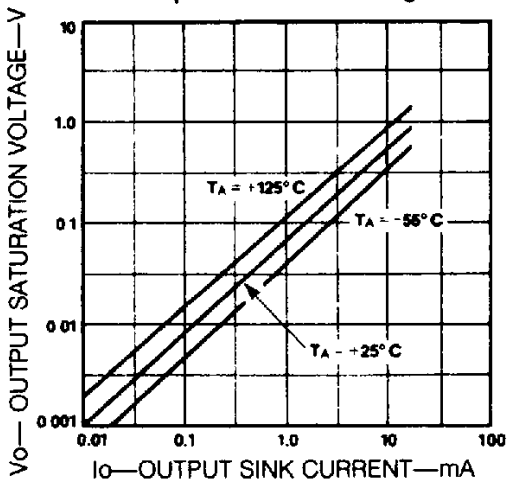
APPLICATION NOTE

The GL339/A are high-gain, wide-bandwidth devices which, like most comparators, can easy oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the GL339/A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V

It is usually unnecessary to use a bypass capacitor across the power supply line
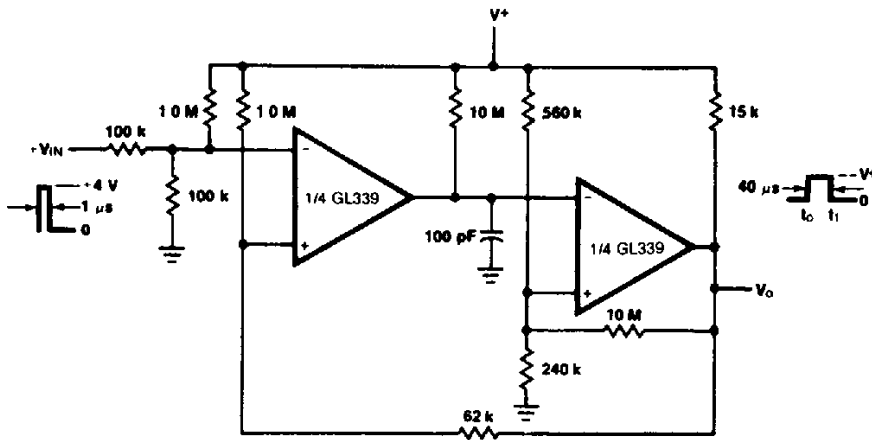
The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than–0.3V (at 25°C). An input clamp diode can be used as shown in the applications section

The output of the GL339/A is the uncommitted collector of a grounded-emitter npn output transistor Many collectors can be tied together to provide an output ORing function An output pull-up resistor can be connected to any availabale power supply voltage within the permitted supply voltage range and there is no restriction on this voltagae due to the magnitude of the voltage which is applied to the V+ terminal of the GL339/A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive availabale (which is independent of V+) and the β of this device When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents
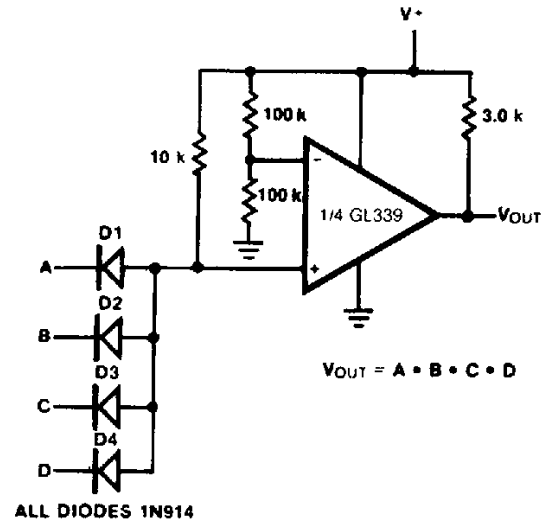
1. TYPICAL APPLICATIONS (V+ = 15 V)

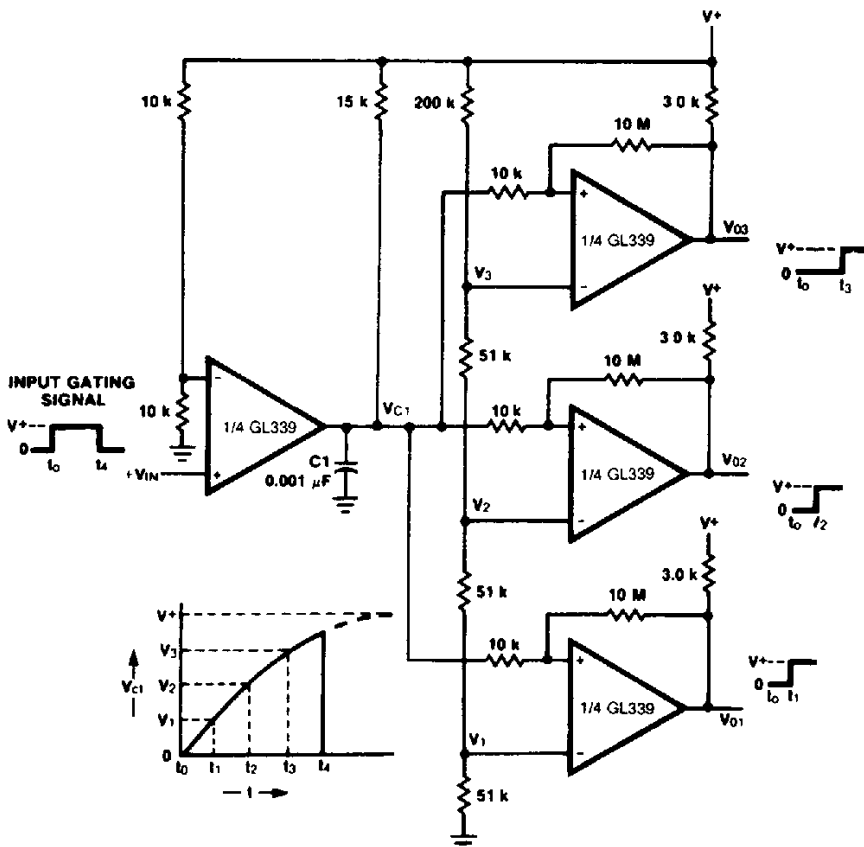### AND GATE

OR GATE

ONE-SHOT MULTIVIBRATOR

BI-STABLE MULTIVIBRATOR

DataSheet.in
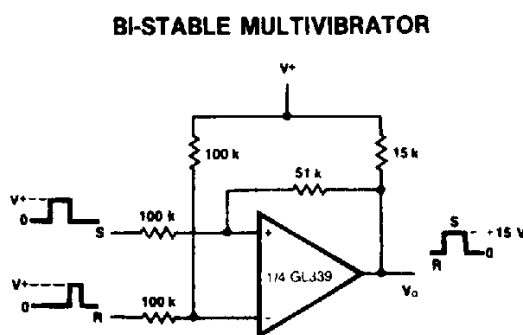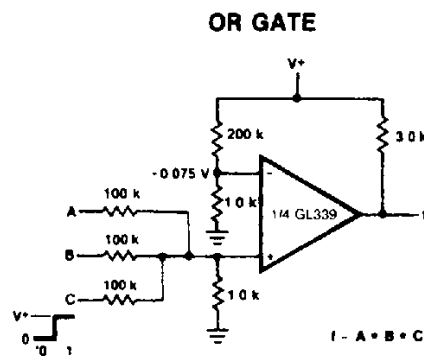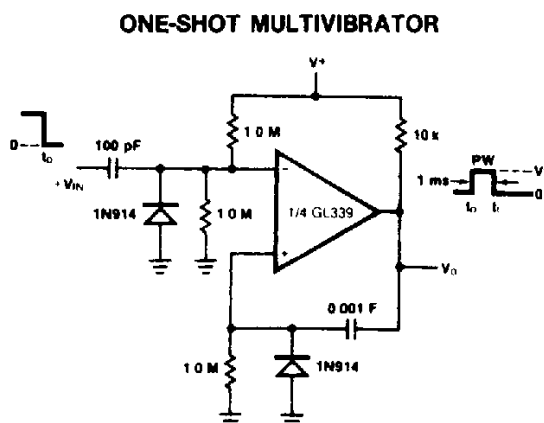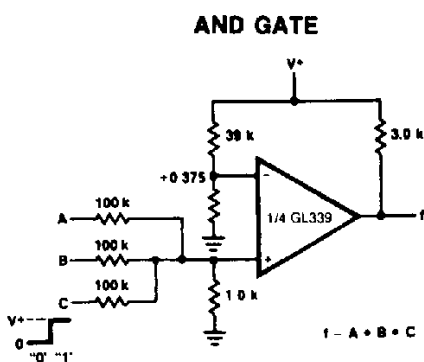
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT

LARGE FAN-IN AND GATE

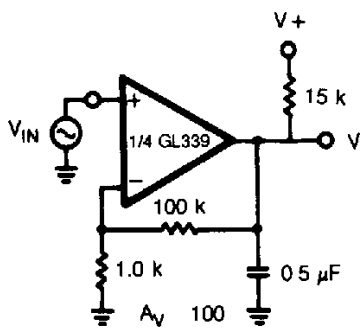$V_{OUT} = A \cdot B \cdot C \cdot D$

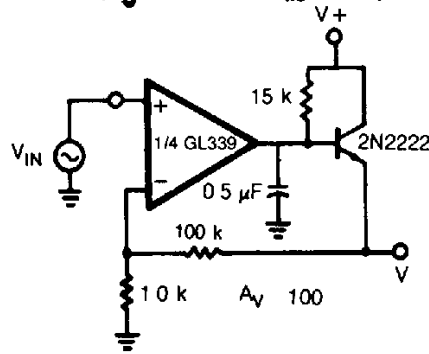ALL DIODES 1N914

TIME DELAY GENERATOR
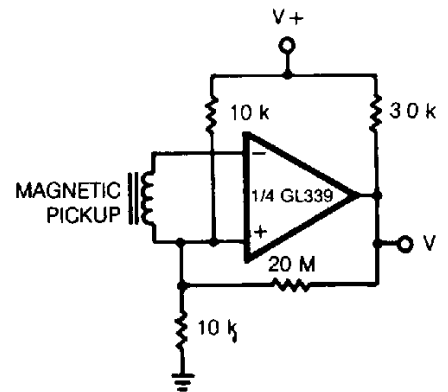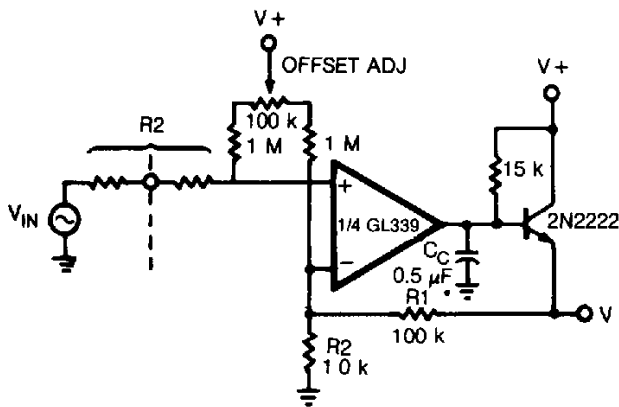
ORING THE OUTPUTS
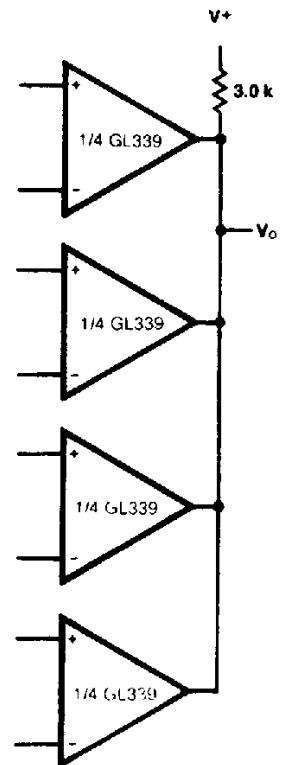
LOW FREQUENCY OP AMP

LOW FREQUENCY OP AMP
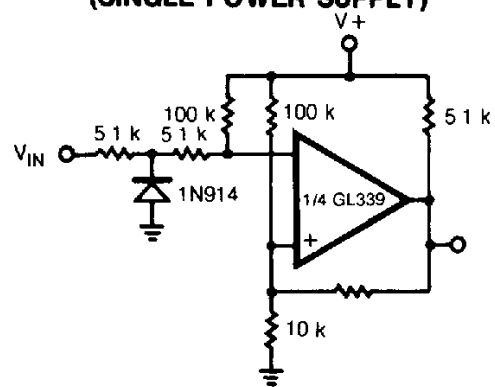($V_O = 0$ V FOR $V_{IN} = 0$ V)

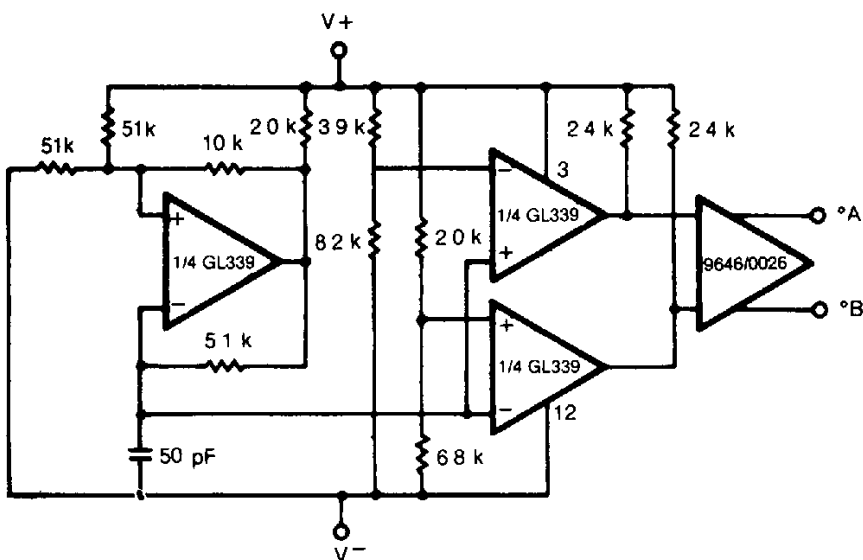**TRANSDUCER AMPLIFIER**

LOW FREQUENCY OP AMP WITH OFFSET ADJUST
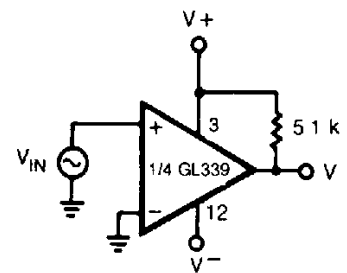

**ZERO CROSSING DETECTOR
(SINGLE POWER SUPPLY)**

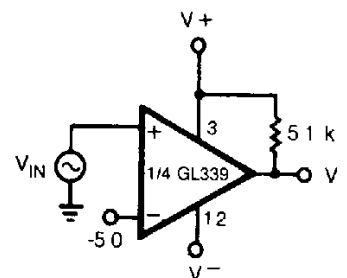**2. SPLIT-SUPPLY APPLICATIONS** $V^+ = +15V$ and $V^- = -15V$
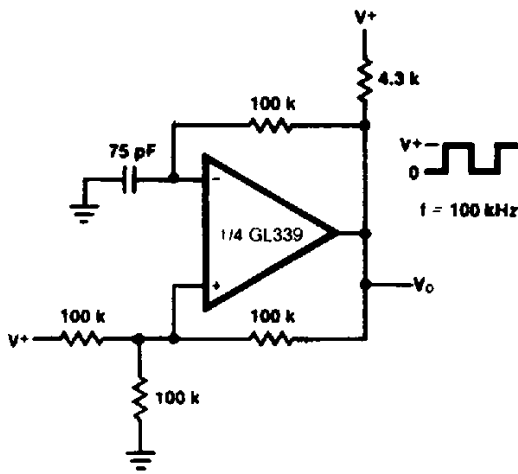
MOS CLOCK DRIVER
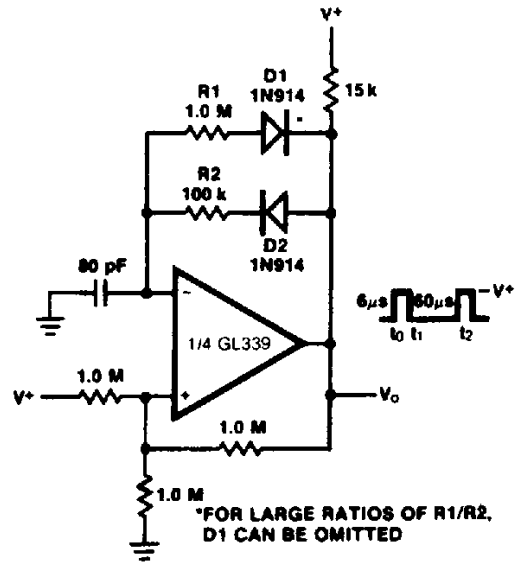

ZERO CROSSING DETECTOR

COMPARATOR WITH A NEGATIVE REFERENCE

SQUAREWAVE-OSCILLATOR

PULSE GENERATOR

*FOR LARGE RATIOS OF R1/R2,
D1 CAN BE OMITTED
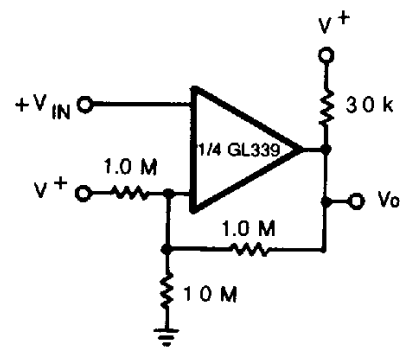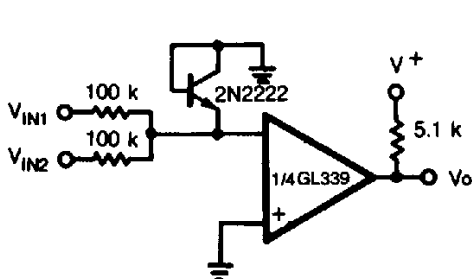
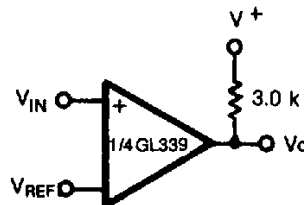## NON-INVERTING COMPARATOR WITH HYSTERESIS
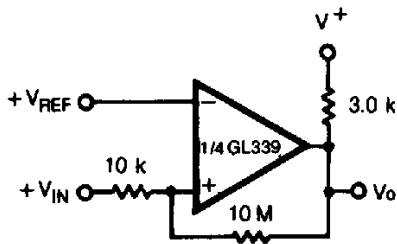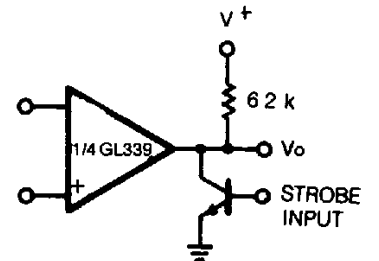
INVERTING COMPARATOR WITH HYSTERESIS

COMPARING INPUT VOLTAGES
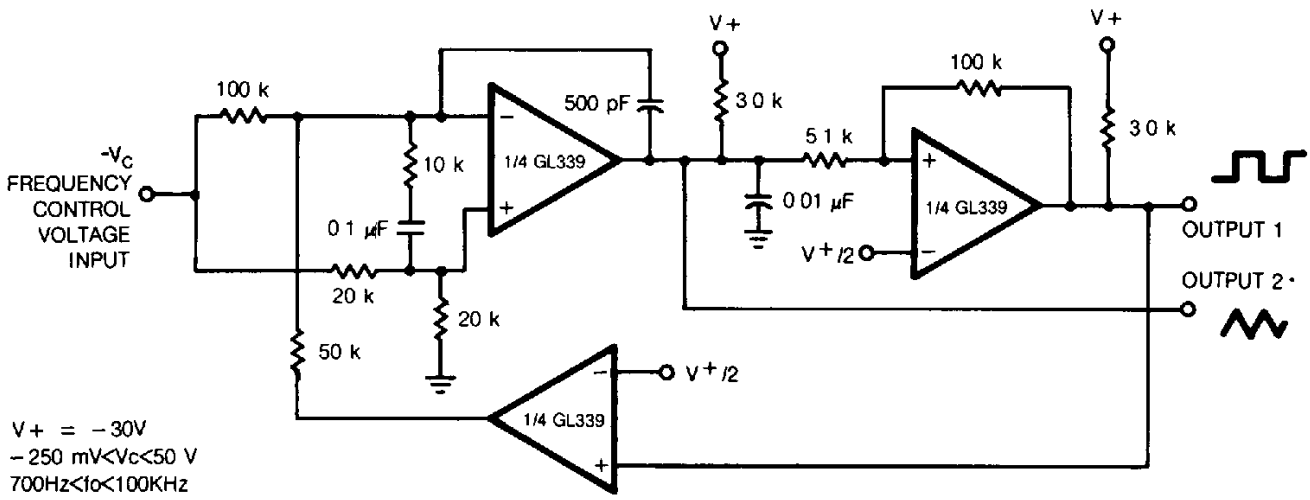## OF OPPOSITE POLARITY

BASIC COMPARATOR

OUTPUT STROBING

OR LOGIC GATE WITHOUT
PULL-UP RESISTOR

TWO-DECADE HIGH-FREQUENCY VCO

$V+ = -30V$
$-250\ mV < V_C < 50\ V$
$700Hz < fo < 100KHz$

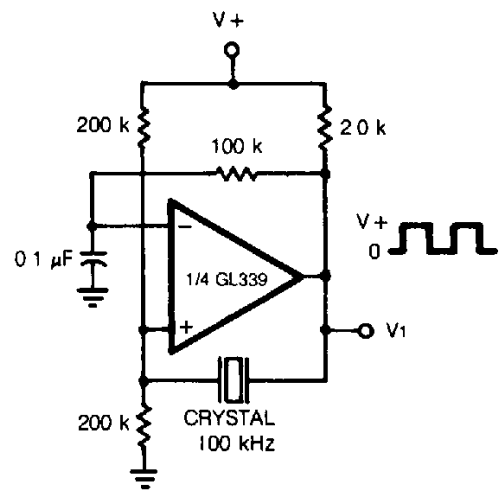## LIMIT COMPARATOR
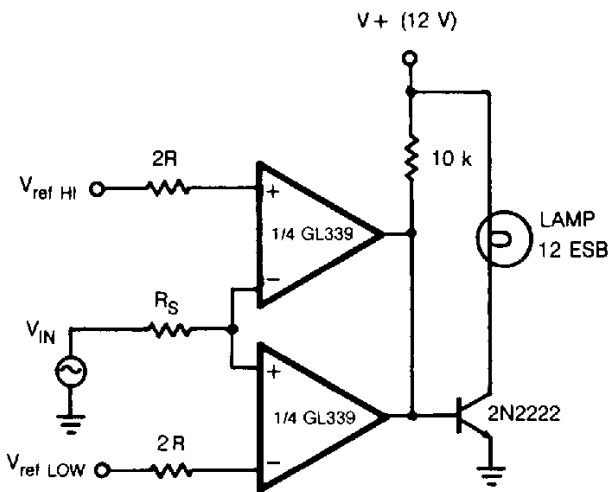
CRYSTAL CONTROLLED OSCILLATOR

GL393/393A
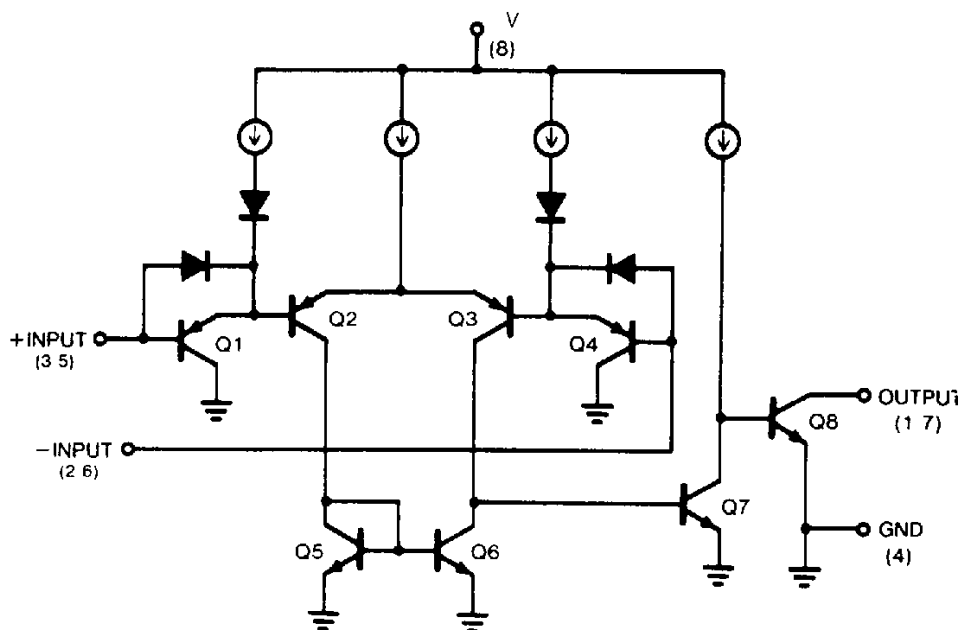## LOW POWER, LOW OFFSET VOLTAGE DUAL COMPARATORS

Description

The GL393 consists of two independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range, Darlington connected pnp input stage allows the input common-mode voltage to include ground.
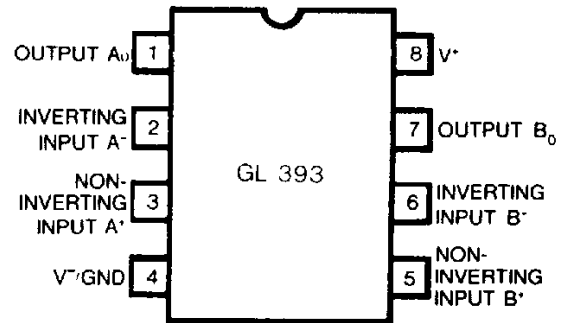
Features

- **Single Supply Operation +2.0V to +36V**
- **Dual Supply Operation ±1.0V to ±18V**
- **Compatible with All forms of Logic**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 400 μA TYP**
- **Low Input Bias Current 25nA TYP**
- **Low Input Offset Current ±5 nA TYP**
- **Low Offset Voltage ±2mV**

Pin Configuration

OUTPUT A₀	1	8	V⁺
INVERTING INPUT A⁻	2	7	OUTPUT B₀
NON-INVERTING INPUT A⁺	3	6	INVERTING INPUT B⁻
V⁻/GND	4	5	NON-INVERTING INPUT B⁺

GL 393

Absolute Maximum Ratings

Supply Voltage, V⁺	+36V or ±18V
Differential Input Voltage	36V
Input Voltage Range	−0.3V to +36V
Power Pissipation	500mW
Input Current (V$_{IN}$<−0.3V)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	260°C

Shematic Diagram

Electrical Characteristics: $V^+ = 5V$ $T_A = 25°C$, unless otherwise specified)

PARAMETER	Test Conditions		GL393			GL393A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	At out. switch point $V_o = 1\,4$; $R_s = 0$ $V_{REF} = 1.4V$			±2	±5		±1	±2	mV
		$0°C \leqslant T_A \leqslant 70°C$			9			4	
Input Bias Current (1)	Output in linear range			25	250		25	250	nA
		$0°C \leqslant T_A \leqslant 70°C$			400			400	
Input Offset Current				±5	±50		±5	±50	nA
		$0°C \leqslant T_A \leqslant 70°C$			±150			±150	
Input Common-Mode Voltage Range (2)			0		V^+-1.5	0		V^+-1.5	V
		$0°C \leqslant T_A \leqslant 70°C$	0		V^+-2	0		V^+-2	
Supply Current	$R_L = \infty$			0.4	1		0.4	1	mA
Supply Current	$V_{CC} = 30V$, $R_L = \infty$				2.5			2.5	mA
Voltage Gain	$R_L \geqslant 15K\Omega$, $V^+ = 15V$		93	106		93	106		dB
Large Signal Response Time	V_{IN} = TTL logic swing, $V_{REF} = +1.4V$; $R_L = 5.1K\Omega$ $V_{RL} = 5V$			300			300		ns
Response Time (3)	$V_{RL} = 5V$; $R_L = 5.1k\Omega$			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geqslant 1V$; $V_{IN(+)} = 0V$; $V_o \leqslant 1.5V$		6	16		6	16		mA
Output Saturation	$V_{IN(-)} \geqslant 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leqslant 4mA$			150	400		150	400	mV
		$0°C \leqslant T_A \leqslant 70°C$			700			700	
Output Leakage	$V_{IN(+)} \geqslant 1V$ $V_{IN(-)} = 0V$			0.1			0.1		nA
		$0°C \leqslant T_A \leqslant 70°C$			1000			1000	
Differential Input Voltage	All $V_{IN} \geqslant 0V$ (or V^- if split supply is used) $0°C \leqslant T_A \leqslant 70°C$			V^+			V^+		V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines

(2) If either input of any comparators goes more negative than 0 3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs This conditions is not destructive providing the input current is limited to less than 50mA

(3) The response time specified is for a 100mV input step with 5mV overdrive For larger overdrive signals 300 nsec can be obtained
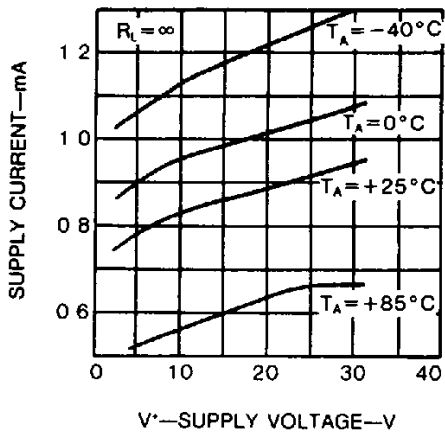
Typical Performance Curves

Figure 1— Supply Current
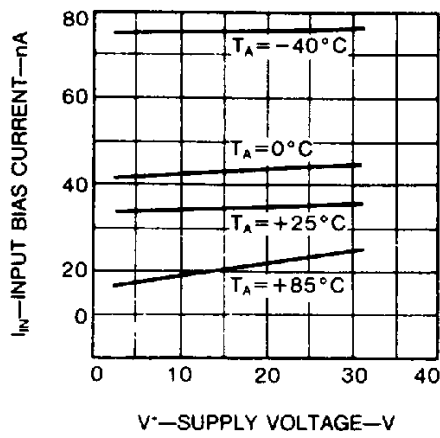

Figure 2— Input Current
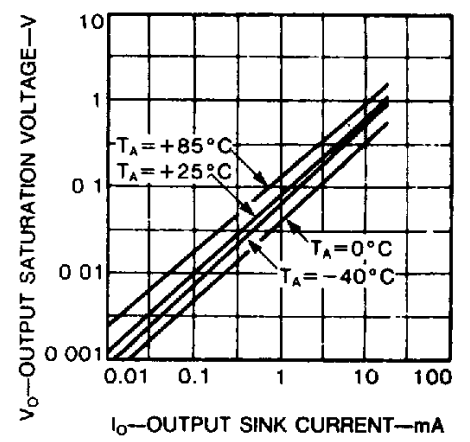

Figure 3—Output Saturation Voltage

Figure 4 — Response Time for Various Input Overdrives Negative Transition
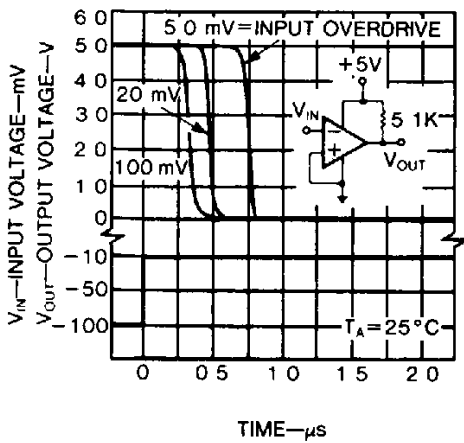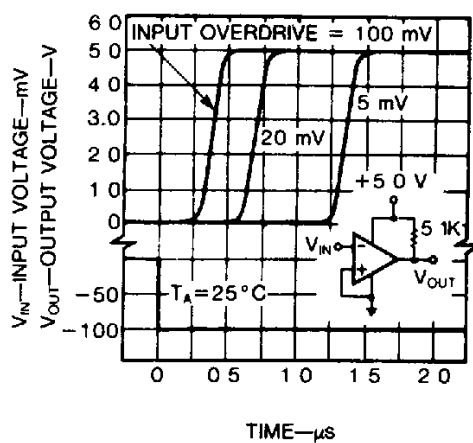

Figure 5— Response Time for Various Input Overdrives Positive Transition

Applications

These dual comparators feature high gain, wide band width characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situa-

tion input resistors < 10kΩ should be used. The addition of positive feedback (<10mV) is also recommended. It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −0.3V should not be used
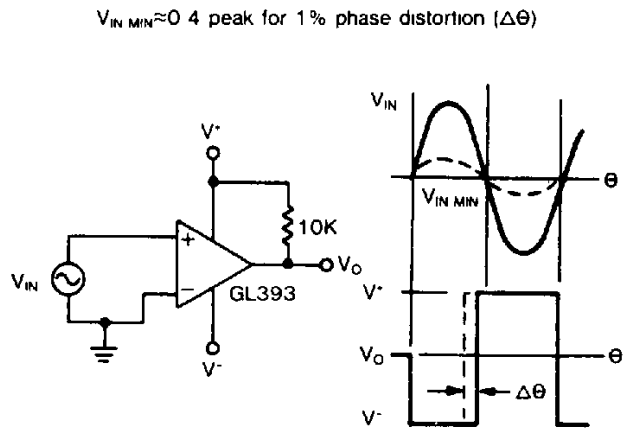
**Figure 6-Zero Crossing Detector
(Single Supply)**
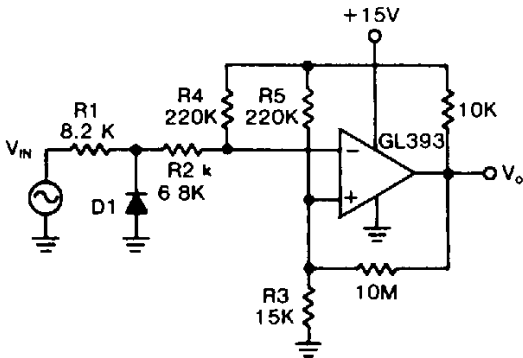
D1 prevents input from going negative by more than 0 6V

$$R1+R=R3$$

$$R3 < \frac{R5}{10} \text{ for small error in zero crossing}$$

**Figure 7-Zero Crossing Detector
(Split Supplies)**

$V_{IN\ MIN} \approx 0\ 4$ peak for 1% phase distortion (Δθ)

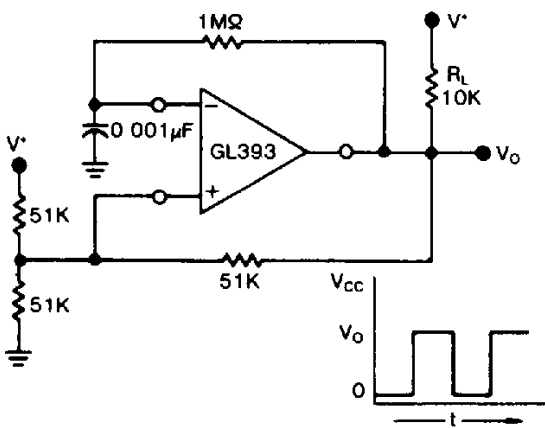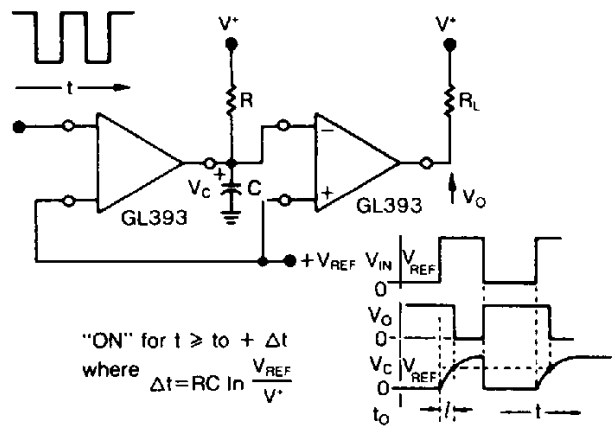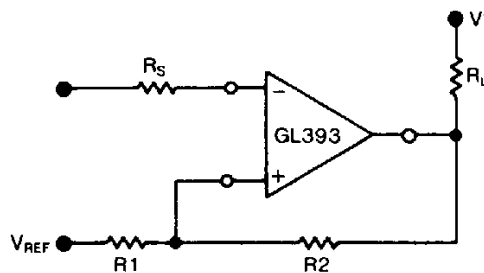**Figure 8-Free-Running Square-Wave Oscillator**

Figure 9-Time Delay Generator

"ON" for $t \geqslant t_0 + \Delta t$

where $\Delta t = RC \ln \dfrac{V_{REF}}{V^*}$

Figure 10-Comparator With Hysteresis

$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{REF} + \frac{(V_{CC} - V_{REF})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{REF} + \frac{(V_{REF} - V_O\ Low)\ R1}{R1 + R2 + R_L}$$