DATA SHEET

HM 65770

4 K x 4
HIGH SPEED CMOS SRAM
WITH OUTPUT ENABLE

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FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25/35/45 ns (max)
  COMMERCIAL : 20/25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (max)
  STANDBY : 27.5 mW (max)
- **WIDE TEMPERATURE RANGE :**
  - 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **OUTPUT ENABLE**

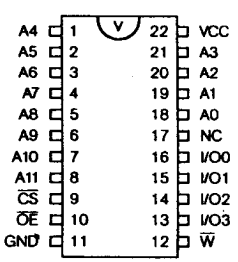
DESCRIPTION

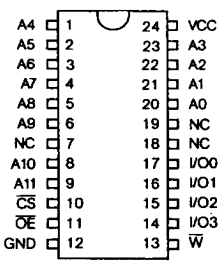
The HM 65770 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65770 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 90 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65770 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65770 is processed following the test methods of MIL STD 883C.

PACKAGES

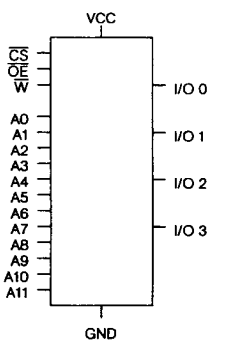
Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.
SO 300 mils, 24 pins, DIL.

Pinout DIL 22/24 pins (top view)

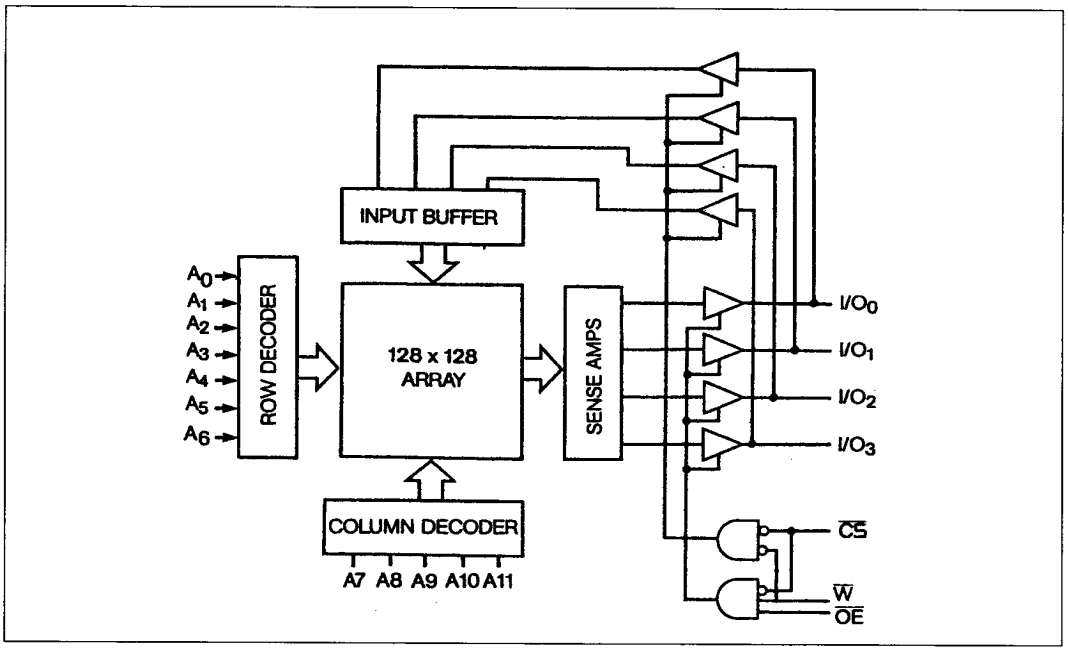




LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I/O0–I/O3	: Input/Output	$\overline{W}$	: Write enable
Vcc	: Power	$\overline{OE}$	: Output enable
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V. These parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

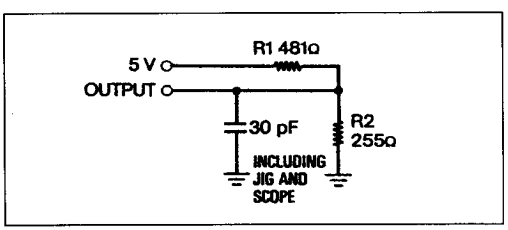


Fig. 1a.

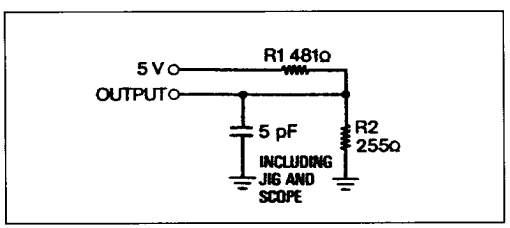
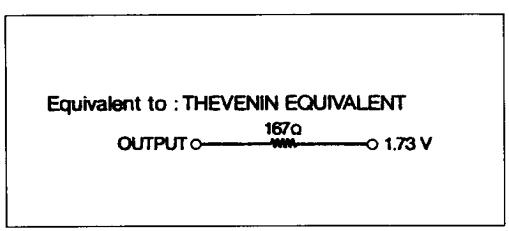


Fig. 1b.



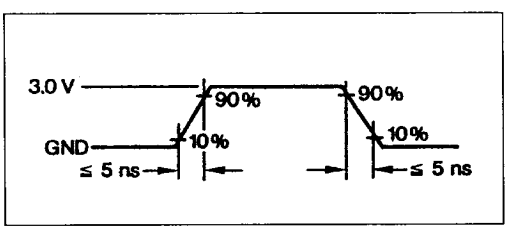


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 50.0	–	50.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA .
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL		PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	90	90	90	90	mA	max

Consumption for Military specification :

SYMBOL		PARAMETER	65770 H-2	65772 K-2	65770 M-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	120	120	120	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

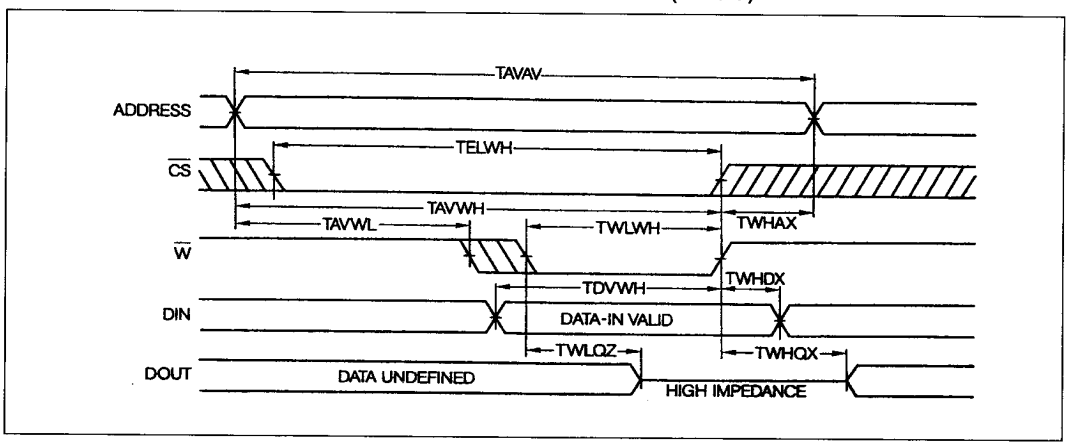
SYMBOL	PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	30	35	ns	min
TDVWH	Data set-up time	10	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	35	35	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	20	ns	max
TWLWH	Write pulse width	15	20	30	35	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	3	ns	min
TWHQX (8)	Write high to low Z	3	6	6	6	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65770 H-2	65770 K-2	65770 M-2	UNIT	VALUE
TAVAV	Write cycle time	25	35	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	35	ns	min
TDVWH	Data set-up time	10	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	35	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	20	30	35	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	3	ns	min
TWHQX (8)	Write high to low Z	6	6	6	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 : $\overline{W}$ Controlled (note 9)



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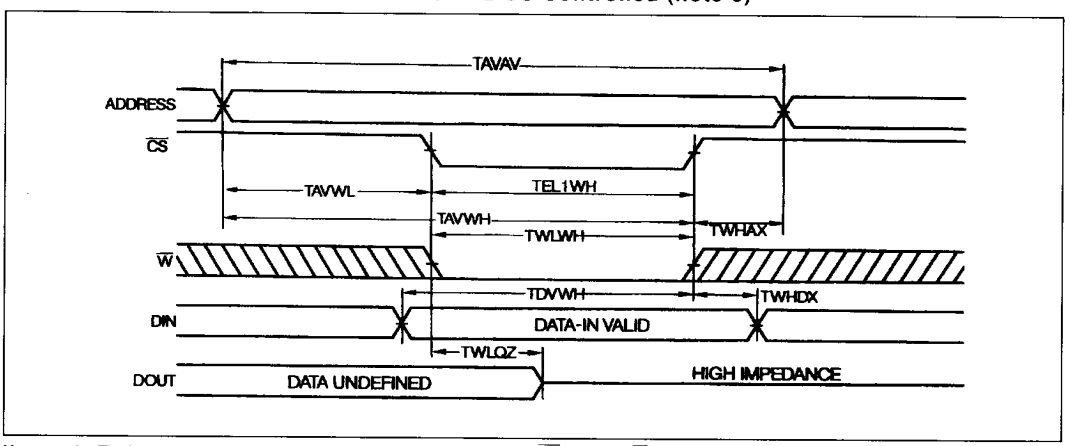
WRITE CYCLE 2 $\overline{CS}$ Controlled (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65770 F-5	65770 H-5	65770 K-5	65770 M-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	max
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	15	15	25	30	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	25	30	ns	max
TGLQV	Output Enable access time	12	15	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	2	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	12	15	15	15	ns	max

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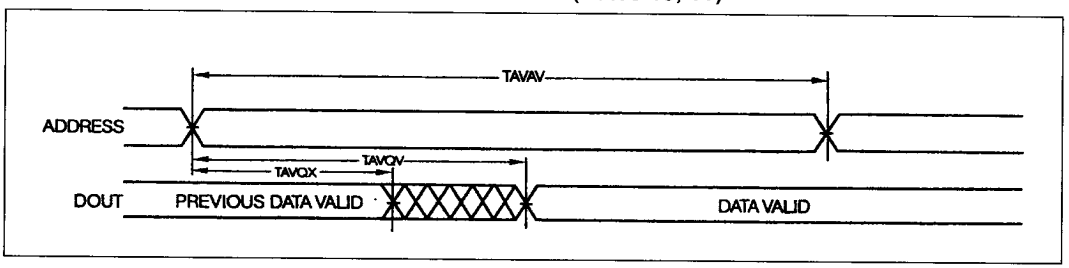
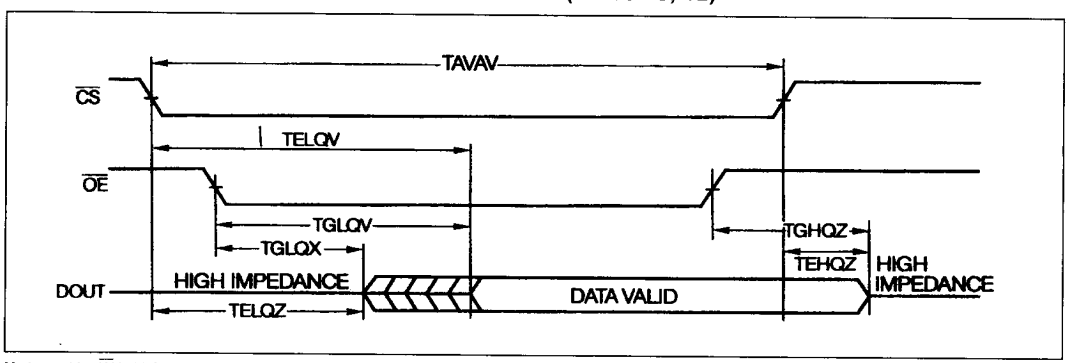
READ CYCLE : Military specification

SYMBOL	PARAMETER	65770 H-2	65770 K-2	65770 M-2	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	ns	max
TGLQV	Output Enable access time	15	15	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	20	ns	max

READ CYCLE nb 1 : (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL and $\overline{OE}$ = VIL.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65770	K	– 5
0 - Chip form 1 - Ceramic 22 pins 3 - Plastic 22 pins T - SO 24 pins	4 k x 4 high speed static RAM with Output Enable	F = 20 ns H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins : X41
Ceramic, 300 mils, 20 pins : C33
SOIC DIL 300 mils, 24 pins : TBD.