Empowered by Innovation

New ASIC Solution Platform

ISSP™

ISSP1 Series

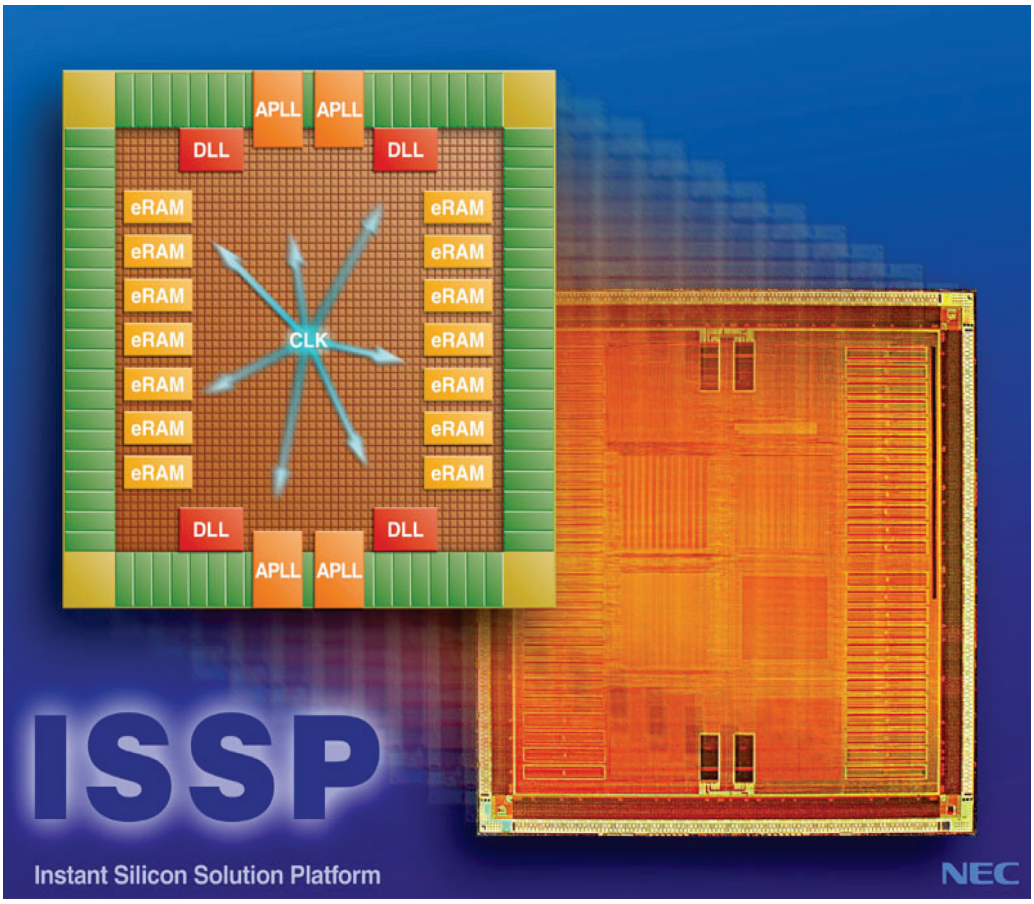
ISSP1-STD Series

ISSP1-HSI Series

ISSP90 Series

ISSP90-STD Series New product

ISSP90-HSI Series Preliminary



<A New Platform Never Seen Before>
- High-performance LSIs realized quickly, easily, and at low cost -

NEC Electronics

ISSP

ISSP (Instant Silicon Solution Platform) is a new ASIC platform device that helps you create high-performance LSIs quickly, easily, and at low cost.

As a designer today, you face shorter deadlines for designing LSI products than ever before.

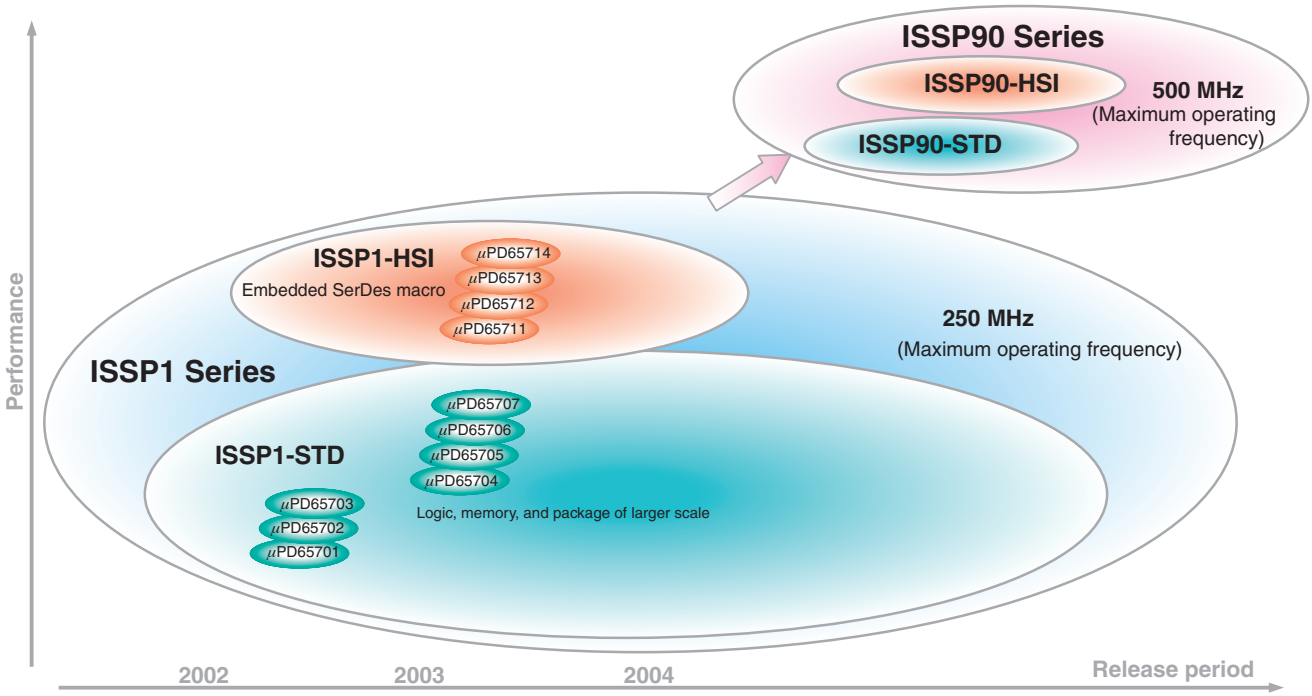
ISSP offers you a risk management solution that enables fast time to market and lower total costs. This solution helps NEC Electronics satisfy needs that could not be satisfied by conventional ASIC products and FPGA.

ISSP Lineup

The ISSP1-STD Series, NEC Electronics' first-generation ISSP, is a standard type platform that integrates large-scale SRAM, and APLL and DLL circuits. The ISSP1-STD Series realizes an operating frequency of up to 250 MHz by employing 5-layer AL routing technology using a 0.15 μm CMOS process. The main applications of this ISSP include high-speed and high-capacity (broadband) communications or network equipment, computer peripheral equipment, high-performance measuring instruments, and consumer electronic systems.

The ISSP1-HSI Series is a high-speed interface core version of the first-generation ISSP. It supports high-speed interfaces including PCI Express, Gigabit Ethernet, and Fibre Channel, by embedding a high-performance 2.5 Gbps SerDes (Serializer/Deserializer). In addition, IP cores necessary for communications and networks such as SPI4.2 (Dynamic), 10/100M Ethernet MAC, 1G Ethernet MAC, POS PHY Level 3, and UTOPIA are available as firmware macros, providing the ideal solution for high-speed, high-capacity (broadband) communications, network equipment, and server equipment.

The ISSP90 Series, NEC Electronics' second-generation ISSP, employs a state-of-the-art 90 nm CMOS process. The internal operating frequency of this series is as high as 500 MHz. In addition, the number of user gates is to 6.5 million gates, four times the number of the first generation, and the SRAM capacity has been increased three-fold to 11.5 Mb. An embedded SerDes core with a data transmission rate of up to 10 Gbps is also available, as are the IP cores already provided with the ISSP1 Series. This core can realize a serial interface standard of up to10 Gb and a Serial ATA high-speed interface of 3 Gb. A 10 Gbps Ethernet MAC is also available.



Features of ISSP

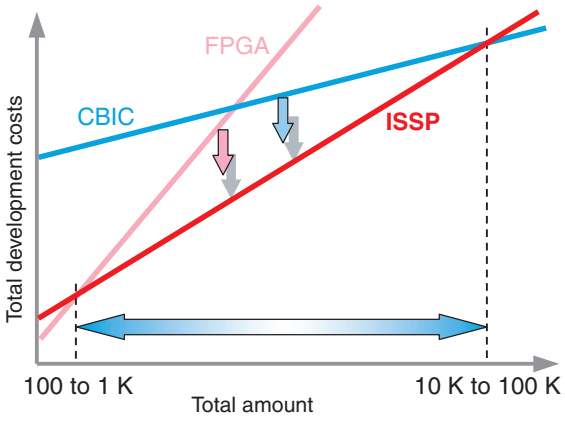
(1) Can realize high-performance system LSIs at lower cost than conventional ASIC/FPGA
(2) Substantially easier design through employment of new architecture
(3) Many IP cores and high-speed interfaces available
(4) High-mix low volume production possible in a short time.

Low Development Risk

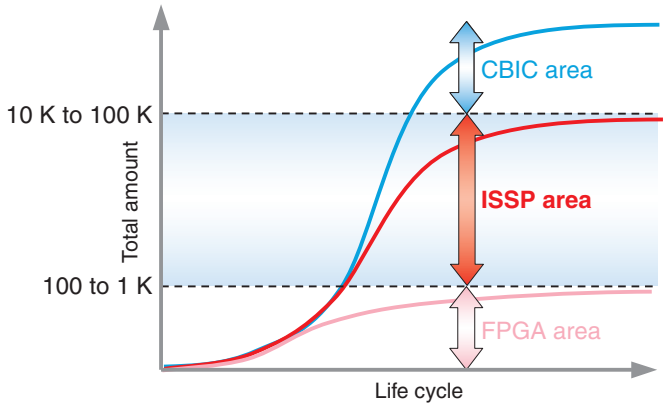
Progress in ASIC process technology has accelerated in recent years and ASICs with improved performance and functionality are now widely available to satisfy an ever diverse range of demands. In the meantime, however, new problems have arisen. For example, an increase in the number of process steps means a larger number of masks are required. This leads directly to higher development costs. Test design, clock design, and signal integrity problems also lengthen the development period, further raising the development costs, and the risk to the developer. In the development stage of a new product, an increase in initial costs makes it difficult to estimate payback of investment, placing heavy pressure on the developer's cash flow. In some cases, mass production does not justify the investment.

ISSP can reduce such investment risks by supplying high-performance system LSIs at an initial cost equivalent to that of gate arrays.

Total number of mass-produced products vs. total costs



Optimal mass production amount for each device



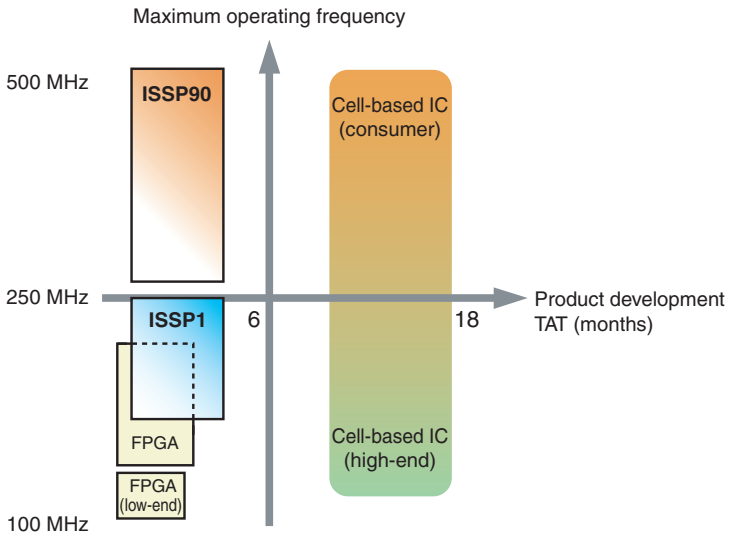
Total development costs = Labor costs + NRE + Total amount x Unit price

Short Development Period

The main causes that extend the development period of conventional ASICs are problems of test design and mutual interference of signals (signal integrity) resulting from increased miniaturization. FPGAs, on the other hand, require a long time to verify circuits if high-speed circuits exceeding 100 MHz are to be designed. If the cell utilization rate is high, the design convergence degrades and, in the worst case, the specifications must be reviewed.

With ISSP, the user can concentrate on designing circuits without having to be aware of test design because a test circuit is embedded in advance in the base wafer. In addition, the design period can be shortened due to the employment of a leading-edge process and an embedded clock tree, which increase the performance, and by a new cell structure that counters signal integrity.

Product development TAT (start of development to mass production)



IP Core Lineup

Macro		ISSP1			ISSP90	
		STD Series		HSI Series	STD Series	HSI Series
		μPD65701 to μPD65703	μPD65704 to μPD65707			
DDR Controller	133 MHz, 64 bit	√√	√√	√	√	√
10/100 M Ethernet MAC		√√	√√	√√	√	√
10/100/1000 M Ethernet MAC	MAC (Triple)	√√	√√	√√	√	√
	TBI (125 MHz, 10 bit)	√√	√√	√√	√	√
10 G Ethernet MAC		–	–	–	–	√
SPI4.2	Static	√√	–	√	–	–
	Dynamic	–	√√	√	√	√
POS PHY/UTOPIA Level 3		√√	√√	√√	√	√
PCI-X	I/O only	–	√√	√√	√	√
SerDes	Up to 2.5 G bps	–	–	√√	–	√
	Up to 10 G bps	–	–	–	–	√
PCI Controller	66 MHz, 32 bit	√√	√√	√√	√	√
PCI Express	PCS	–	–	√√	–	√
XAUI	PCS	–	–	–	–	√
Fibre Channel	PCS	–	–	√	–	√

√√ : Supported √ : To be supported – : Not supported

Embedded APLL/DLL

♦ APLL

High-speed version: Functions: Clock skew control function, clock multiplication function, phase shift function, DDR interface
Input frequency: 25 MHz to 400 MHz
Output frequency: 25 MHz to 800 MHz

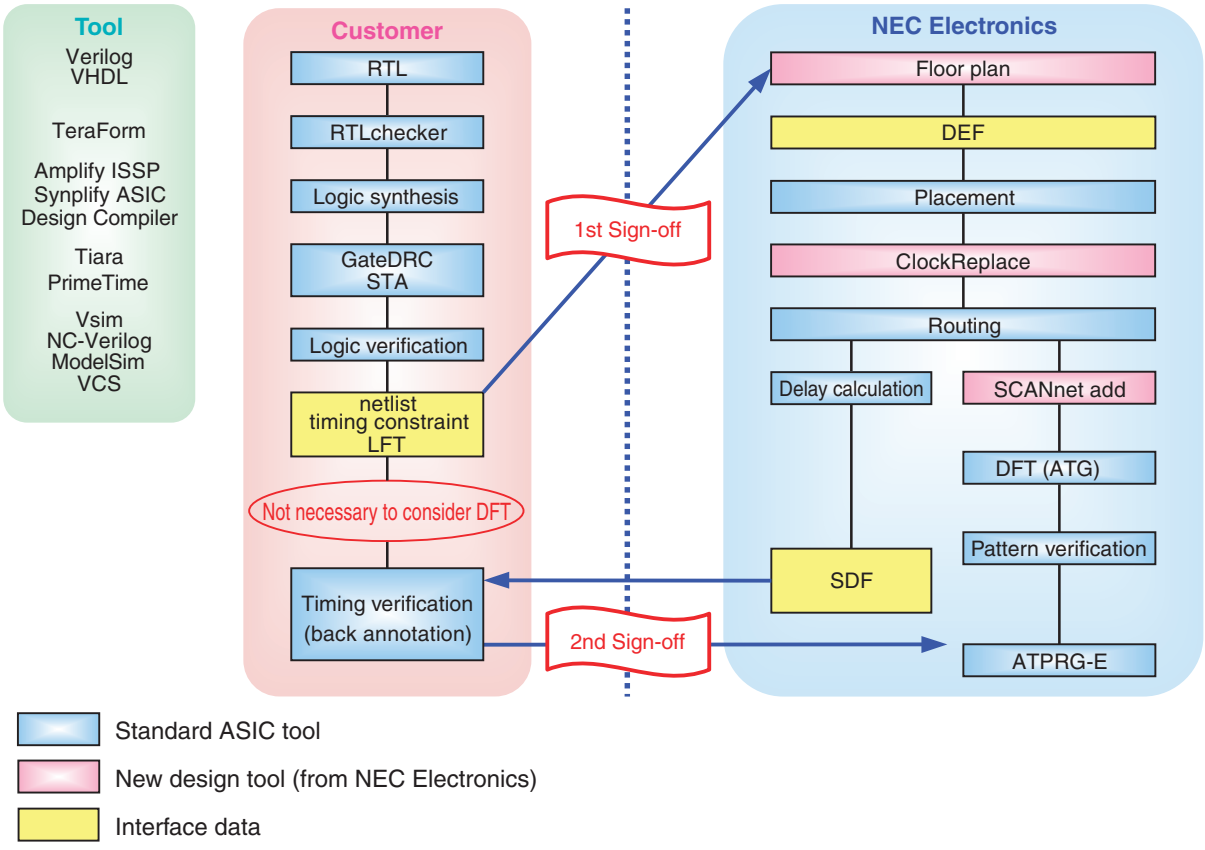
Medium-speed version: Functions: Clock skew control function, clock multiplication function
Input frequency: 12.5 MHz to 400 MHz
Output frequency: 12.5 MHz to 400 MHz

♦ DDL Functions: DDR interface
Input frequency: 100 MHz to 175 MHz
Output frequency: 100 MHz to 175 MHz

ISSP (Tool Environment)

Function	Tool	
	NEC Electronics	Third party
Framework	OPENCAD™ ISSP	–
RTL check	–	Teraform®
Schematic editor	Vdraw	–
Synthesis	–	Design Compiler, Synplify® ASIC, Amplify® ASIC
Physical synthesis	–	Amplify ISSP
Wave editor	Wave Editor	–
Logic verification	V.sim	ModelSim, NC-Verilog, VCS
STA	Tiara	PrimeTime
Design rule check	GateDRC, STADRC	–
Formal verification	Zero	Conformal-LEC, Formality
Floor plan	Galet, Ace-Floor Plan	Amplify ISSP, SoC ENCOUNTER
Place & route	Galet, Y-Place	Amplify ISSP, SoC ENCOUNTER

ISSP (Development Flow)



ISSP1-STD Series

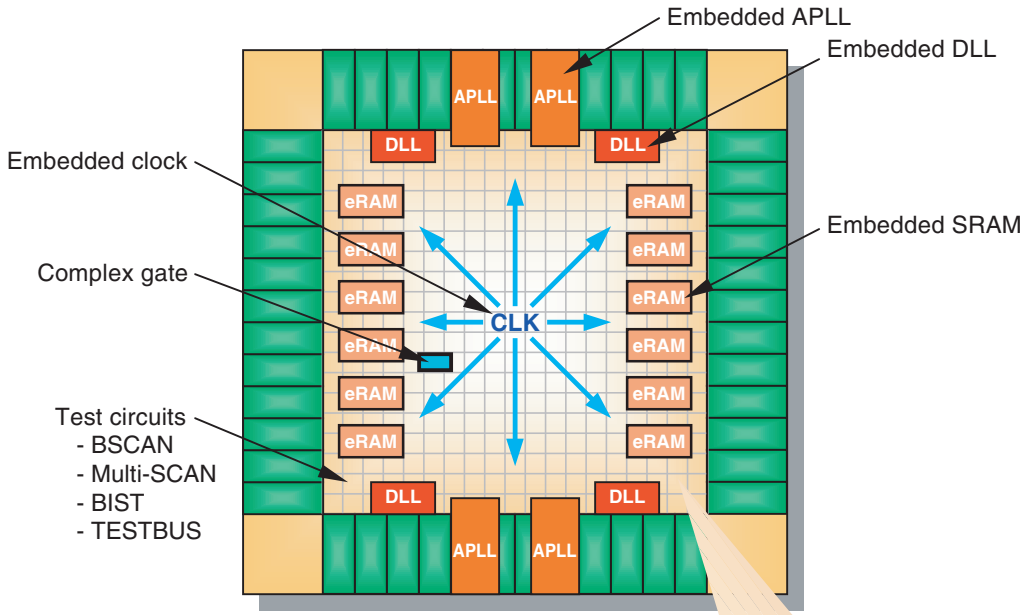
Product Overview

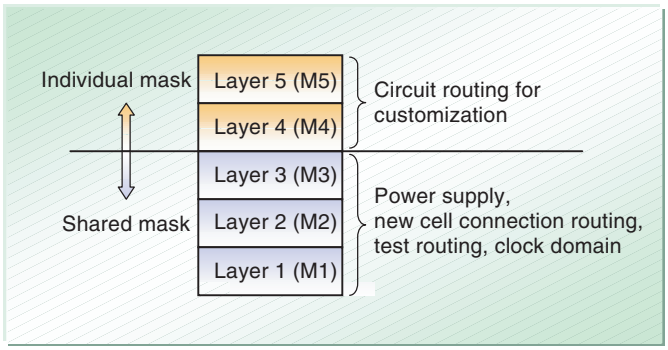
The ISSP1-STD Series includes large-scale SRAM and APLL and DLL circuits, and employs 5-layer AL routing technology using a 0.15 μm CMOS process, realizing an operation speed of up to 250 MHz.

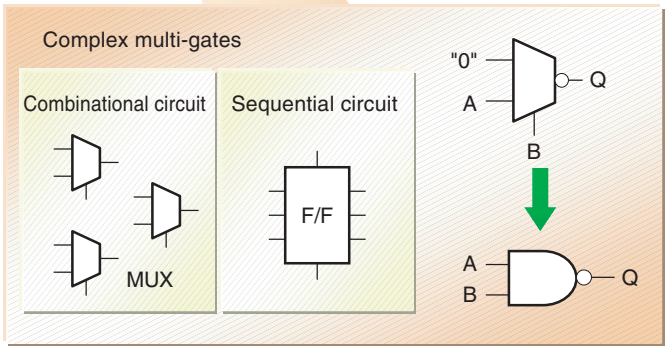
A newly developed complex gate structure is employed for the cells. The lower three routing layers are embedded in advance in the base wafer as complex gate routing, core connection routing, test circuit routing, clock tree routing, and power routing. As a result, the user does not have to consider test design and can concentrate on designing circuits. This results in a substantially shorter design period. In addition, the development costs can also be reduced because the user can customize the circuit by using just the higher two routing layers.

The main applications of the ISSP1-STD Series include high-speed, high-capacity (broadband) communications and network systems, computer peripheral equipment, high-performance measuring instruments, and consumer electronic equipment.

Chip Image of ISSP1-STD Series







ISSP1-STD Series

Master Lineup

Master	Number of Usable ISSP Gates	SRAM Size (Bits)	SRAM		APLL		DLL	Package
			16 K	4 K	High-speed version	Medium-speed version		
μPD65701	214 K	262 K	16	0	3	1	8	TBGA: 532/420 pins
μPD65702	407 K	786 K	48	0	3	1	8	TBGA: 420/500/576/680 pins
μPD65703	941 K	1 M	64	0	3	1	16	TBGA: 500/576/680/768 pins
μPD65704	1 M	3.7 M	216	32	4	0	32	ABGA: 500/756/888 pins
μPD65705	1.7 M	2.2 M	128	32	4	0	32	
μPD65706	1 M	3.7 M	216	32	4	0	32	FCBGA: 1155/1521Note pins
μPD65707	1.7 M	2.2 M	128	32	4	0	32	

Note Under development

Specifications

Item		Specification
Process		0.15 μm process, Si gate CMOS, 2-layer customized routing
Maximum number of usable gates		1.7 M gates (number of usable ISSP gates) 3.7 Mb (RAM capacity)
Package	TBGA	352/420/500/576/768 pins
	ABGA	500/756/888 pins
	FCBGA	1155/1521 pins
Supply voltage	I/O block	Conforms to 3.3 V, 2.5 V, and other high-speed interface standards
	Internal block	1.5 V
Power consumption (internal gates)	Combinational circuit	0.0267 μW/MHz/gate
	Sequential circuit	0.0215 μW/MHz/gate (data line cycle/clock line cycle = 4)
Maximum operating frequency (system clock)		250 MHz (166 MHz) (Maximum operating frequency differs depending on the circuit configuration)
Interface level		3.3 V/2.5 V LVTTL 3.3 V PCI, PCI-X LVDS, HSTL, SSTL, PECL, etc.
Embedded macro	SRAM	1- or 2-port compiled synchronous
	APLL	High-speed type, medium-speed type
	DLL	For high-speed SDRAM interface
Other macros		SRAM: Distributed compiled synchronous SRAM SPI4.2 (Dynamic), 10/100/1000 M Ethernet MAC, 10/100 M Ethernet MAC, POS PHY Level 3, UTOPIA, DDR controller, PCI controller
Embedded clock		Global clock: 2 lines Local clock: 2 to 32 lines
Embedded test-related		Scan path test, boundary scan, BIST, test bus

Remark The usable package/macro differs depending on the scale of the master.

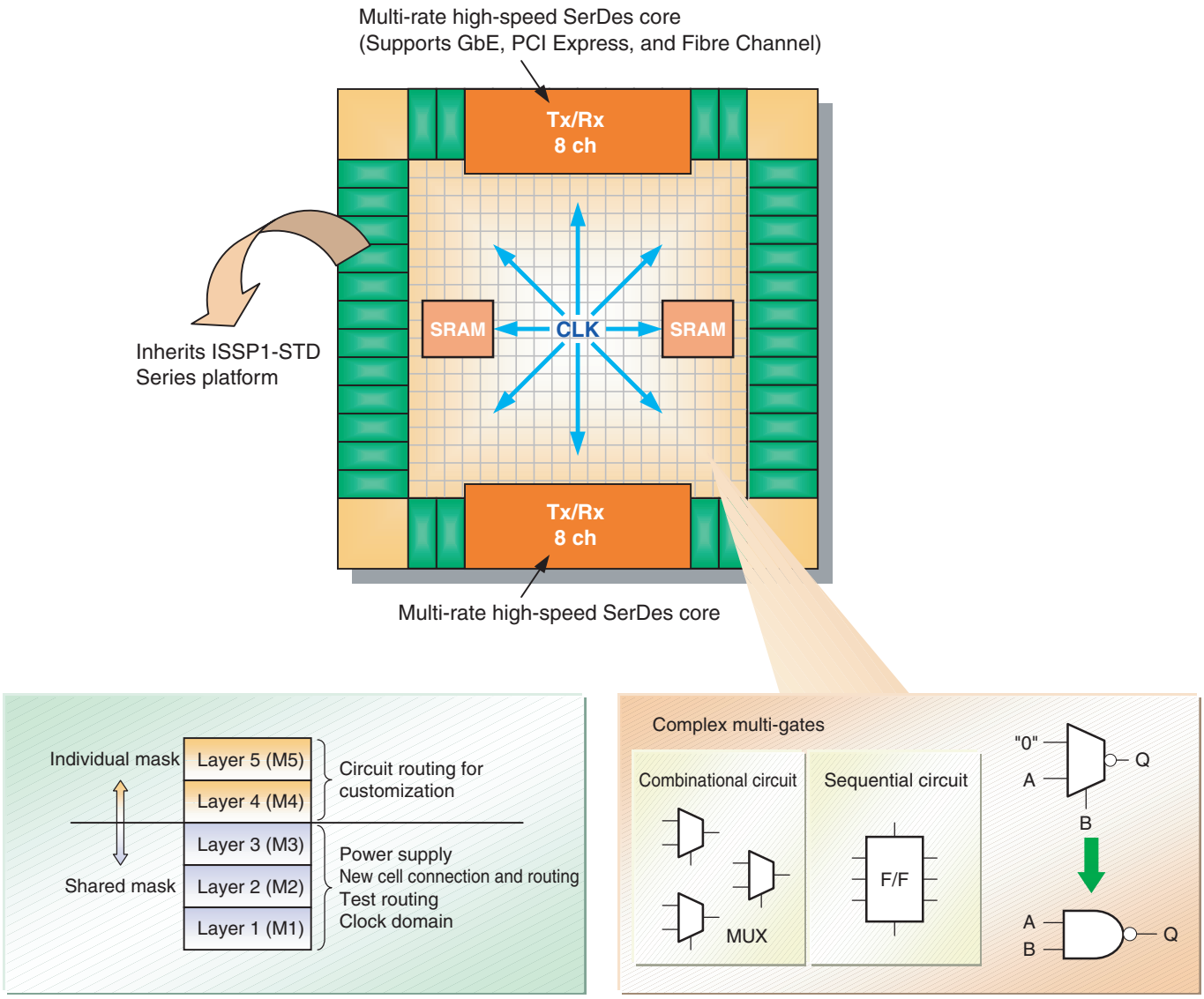
ISSP1-HSI Series

Product Overview

The ISSP1-HSI Series supports high-speed interfaces including PCI Express, Gigabit Ethernet (GbE), and Fibre Channel, by embedding up to 16 high-performance 2.5 Gbps SerDes (Serializer/Deserializer) cores, as well as the functions of the ISSP1-STD Series.

In addition, IP cores necessary for communications and networks such as SPI4.2 (Dynamic), 10/100 M Ethernet MAC, 1 G Ethernet MAC, POS PHY Level 3, and UTOPIA are available as firmware macros, providing an ideal solution for high-speed, high-capacity (broadband) communications and network equipment and server equipment. The same high-performance 0.15 μm CMOS process as the existing ISSP1-STD Series is used. Circuits can also be customized by using just two routing layers. Test circuits and clock tree routing are prepared in advance. Therefore, the design and production periods can be dramatically shortened and development costs reduced.

ISSP1-HSI Series Chip Image



Master Lineup

Master	Number of Usable ISSP Gates	SRAM Size (Bits)	SRAM			APPL (High-Speed Version)	DLL	Number of SerDes Channels	Package
			16 K	4 K	128				
μPD65711	695 K	729 K	42	0	32	4	8	8	ABGA: 576/756 pins
μPD65712	1 M	1 M	56	0	64	4	16	16	ABGA: 576/756/888 pins
μPD65713	1.4 M	2 M	112	20	64	4	32	16	ABGA: 756/888 pins
μPD65714	1.4 M	2 M	112	20	64	4	32	16	FCBGA: 1155 pins

Specifications

Item		Specification
Process		0.15 μm process, Si gate CMOS, 2 layer customized routing
Maximum number of usable gates		1.4 M gates (number of usable ISSP gates) 2 Mb (RAM capacity)
Package	ABGA	576/756/888 pins
	FCBGA	1155 pins
Supply voltage	I/O block	Conforms to 3.3 V, 2.5 V, and other high-speed interface standards
	Internal block	1.5 V
Power consumption (internal gate)	Combinational circuit	0.0267 μW/MHz/gate
	Sequential circuit	0.0215 μW/MHz/gate (data line cycle/clock line cycle = 4)
Maximum operating frequency (system clock)		250 MHz (166 MHz) (Maximum operating frequency differs depending on circuit configuration)
Interface level		3.3 V/2.5 V LVTTL 3.3 V PCI, PCI-X LVDS, HSTL, SSTL, PECL, etc.
Embedded high-speed interface macro		SerDes: Supports GbE/PCI Express/Fibre Channel
Embedded macro	SRAM	1- or 2-port compiled synchronous type
	APLL	High-speed type
	DLL	For high-speed SDRAM interface
Other macros		SPI4.2 (Dynamic), 10/100/1000 M Ethernet MAC, 10/100 M Ethernet MAC, POS PHY Level 3, UTOPIA, DDR controller, PCI controller
Embedded clock		Global clock: 2 lines Local clock: 2 to 32 lines
Embedded test-related		Scan path test, boundary scan, BIST, test bus

Remark The usable package/macro differs depending on the scale of the master.

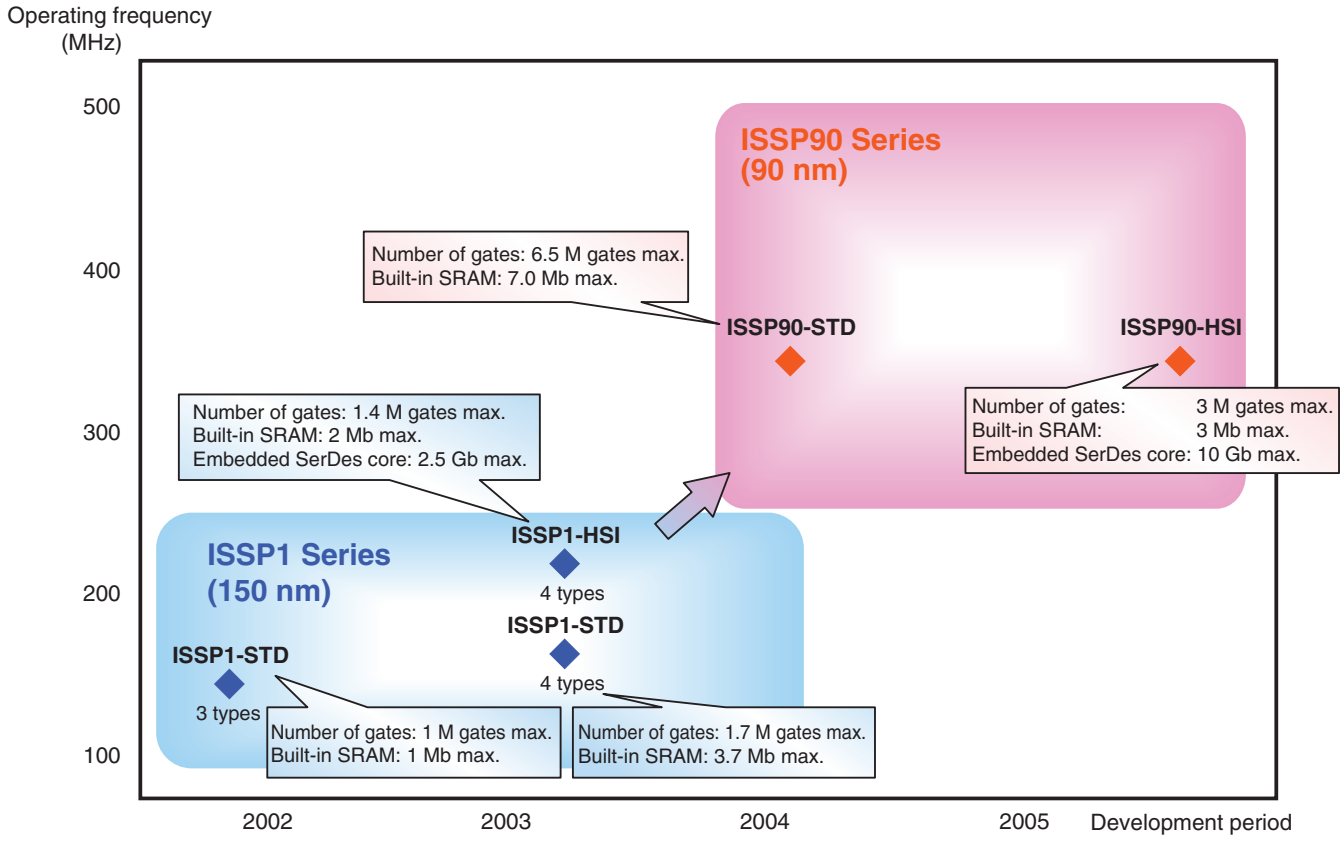
ISSP90 Series

Product Overview

The ISSP90 Series employs a leading-edge 90 nm CMOS process and features an operating frequency of 500 MHz, double that of the ISSP1 Series. In addition, the number of user gates is four times higher (6.5 million gates), and a two-fold SRAM capacity of 7.0 Mb is provided.

In addition to the IP cores available in the ISSP1 Series, the ISSP90 Series supplies a SerDes embedded core with a data transmission rate of 10 Gbps as a high-speed interface indispensable for next-generation applications such as communications, server, and storage. This core can realize a high-speed serial interface standard of 10 Gb and high-speed Serial ATA interface of 3 Gb. A 10 Gbps Ethernet MAC is also available.

Development of ISSP90 Series



Remark SerDes (Serializer/Deserializer): Serial/parallel converter

Master Lineup

New product

I/O Interface	Master	Number of Usable ISSP Gates	SRAM Size (Bits)	I/O Lineup	Maximum Clock[Note]/ Maximum System Clock[Note]	Package (FCBGA)
3.3 V	μPD69551	1.74 M	1.11 M	SSTL2 (2.5 V)	333 MHz/ 250 MHz (High density version)	729 pins
	μPD69552	2.68 M	1.92 M	SSTL18 (1.8 V)		1155 pins
	μPD69553	3.45 M	2.95 M	DDR2 (1.8 V)		1155 pins
	μPD69554	4.00 M	1.77 M	HSTL18 (1.8 V)		1521 pins
	μPD69555	4.67 M	4.20 M	PECL (2.5 V)		
	μPD69556	5.53 M	2.36 M	LVDS (High speed:3.3 V only)		
	μPD69557	5.40 M	5.68 M			1155 pins
	μPD69558	6.50 M	3.02 M	LVDS (Middle and low speed:2.5 V only)		1521 pins
2.5 V	μPD69559	5.23 M	7.08 M			1849 pins
3.3 V	μPD69561	0.87 M	0.77 M	SSTL2 (2.5 V)	500 MHz/ 333 MHz (High speed version)	729 pins
	μPD69562	1.34 M	1.34 M	SSTL18 (1.8 V)		1155 pins
	μPD69563	1.73 M	2.06 M	DDR2 (1.8 V)		1155 pins
	μPD69564	2.00 M	1.24 M	HSTL18 (1.8 V)		1521 pins
	μPD69565	2.34 M	2.94 M	PECL (2.5 V)		
	μPD69566	2.76 M	1.65 M	LVDS (High speed: 3.3 V only)		
	μPD69567	2.70 M	3.97 M			1155 pins
	μPD69568	3.25 M	2.12 M	LVDS (Middle and low speed: 2.5 V only)		1521 pins
2.5 V	μPD69569	2.62 M	4.94 M			1849 pins

Note Depends on the circuit configuration.

Specifications

Item		Specification
Process		90 nm CMOS process, 7 layers (2 customized routing layers)
Maximum number of usable gates		6.5 M gates (number of usable ISSP gates) 7.0 Mb (RAM capacity)
Package	FCBGA	729/1155/1521/1849 pins
Supply voltage	I/O block	Conforms to 3.3 V, 2.5 V, 1.8 V, and other high-speed interface standards
	Internal block	1.0 V
Maximum operating frequency (system clock)		500 MHz (333 MHz) (Maximum operating frequency differs depending on circuit configuration)
Interface level		2.5 V LVCMOS, LVPECL 2.5 input, 3.3 V LVTTL, 2.5 V LVDS, HSTL class 1/HSTL class 3, SSTL2 class 1/SSTL2 class 2, SSTL18.
Embedded macro	SRAM	2-port compiled synchronous type
	APLL	High-speed type
	DLL	For high-speed SDRAM interface (3.3 V master only)
Other macros		SPI4.2 (Dynamic), 10 G Ethernet MAC, 10/100/1000 M Ethernet MAC, 10/100 M Ethernet MAC, POS PHY Level 3, UTOPIA, DDR controller, PCI controller
Embedded test-related		Scan path test, boundary scan, BIST, test bus

Remark The usable package/macro differs depending on the scale of the master.

Specifications

Preliminary

Item		Specification
Process		90 nm CMOS process, 7 layers (2 customized routing layers)
Maximum number of usable gates		3 M gates (number of usable ISSP gates) 3 Mb (RAM capacity)
Package	FCBGA	729/1155/1521/1849 pins
Supply voltage	I/O block	Conforms to 3.3 V, 2.5 V, 1.8 V, and other high-speed interface standards
	Internal block	1.0 V
Maximum operating frequency (system clock)		500 MHz (333 MHz) (Maximum operating frequency differs depending on circuit configuration)
Interface level		2.5 V LVCMOS, LVPECL 2.5 input, 3.3 V LVTTL, 2.5 V LVDS, HSTL class 1/HSTL class 3, SSTL2 class 1/SSTL2 class 2, SSTL18.
High-speed interface embedded macro		SerDes: Supports 10 G serial interface standard (such as 10 G BASE-R)/3 G serial ATA/XAUI/GbE/InfiniBand/PCI Express/Fibre Channel.
Embedded macro	SRAM	2-port compiled synchronous type
	APLL	High-speed type
	DLL	For high-speed SDRAM interface (3.3 V master only)
Other macros		SPI4.2 (Dynamic), 10 G Ethernet MAC, 10/100/1000 M Ethernet MAC, 10/100 M Ethernet MAC, POS PHY Level 3, UTOPIA, DDR controller, PCI controller
Embedded test-related		Scan path test, boundary scan, BIST, test bus

Remark The usable package/macro differs depending on the scale of the master.

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