WD1100-12 Improved MFM Generator

DESCRIPTION

The WD1100-12 Improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION

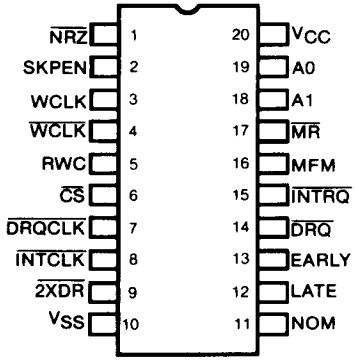
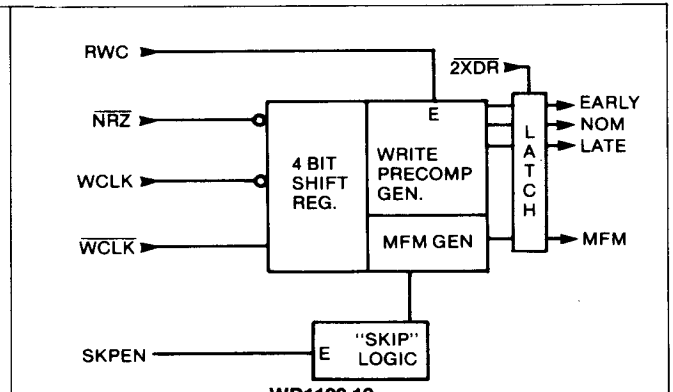


Figure 1.
WD1100-12 Pin Connections



WD1100-12
Figure 2. Block Diagram MFM Generator

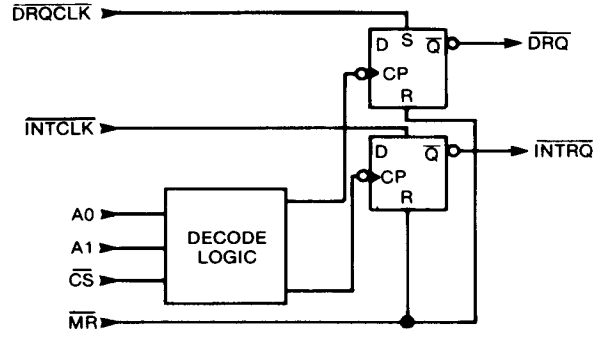


Figure 3.
WD1100-12 Block Diagram Interrupt Control Logic

Powered by ICminer.com Electronic-Library Service CopyRight 2003

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK
4	$\overline{WCLK}$	WRITE CLOCK	(pin 3).
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	2 TIMES DATA RATE	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompenstion Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) goes/ is low.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18,19	A_0,A_1	ADDRESS 0,1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ² 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the NRZ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data / clock pattern as an Address Mark, using AI_{16} data with OA_{16} clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data paterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias.....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS}.....-0.2V to +7.0V
Power Dissipation.....1 Watt

STORAGE TEMPERATURE:
PLASTIC.....-55°C (-67°F) to +125°C (257°F)
CERAMIC....-55°C (-67°F) to +150°C (302°F)

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%; V_{SS} = OV

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All outputs open
I_{IH}	Current Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	μA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%; V_{SS} = OV

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t.↓WCLK	10			nsec	"Per Figure 4"
t_{DH}	Data hold w.r.t.↓WCLK	25			nsec	"Per Figure 4"
t_{TM}	↑2XDR to ↑ MFM			115	nsec	"Per Figure 4"
t_{MR}	Master reset pulse width	50			nsec	"Per Figure 5"
t_{MD}	↓$\overline{MR}$ to ↑DRQ			150	nsec	"Per Figure 5"

Powered by ICminer.com Electronic-Library Service CopyRight 2003

SYMBOL	PARAMTER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑INTRQ			150	nsec	"Per Figure 5"
t_{DQ}	DRQCLK pulse width	50			nsec	"Per Figure 7"
t_{IQ}	INTCLK pulse width	50			nsec	"Per Figure 8"
t_{DD}	↓DRQCLK to DRQ			120	nsec	"Per Figure 7"
t_{II}	↓INTCLK to INTRQ			120	nsec	"Per Figure 8"
t_{AD}	↓AX to ↑DRQ			145	nsec	"Per Figure 6"
t_{AI}	↑ AX to ↑INTRQ			160	nsec	
t_{CD}	↓CS to ↑DRQ			145	nsec	"Per Figure 6"
t_{CI}	↓CS to ↑INTRQ			180	nsec	"Per Figure 6"
t_{RN}	↑RWC to ↓NOM			145	nsec	"Per Figure 4"
t_{TE}	↑2XDR to ↑EARLY			115	nsec	"Per Figure 4"
t_{TN}	↑2XDR to ↑ NOM			115	nsec	"Per Figure 4"
t_{TL}	↑2XDR to ↑ LATE			115	nsec	"Per Figure 4"

NOTES: 1. Typical Values are for $T_A = 25°C$ (77°F) and $V_{CC} = +5.0V$.

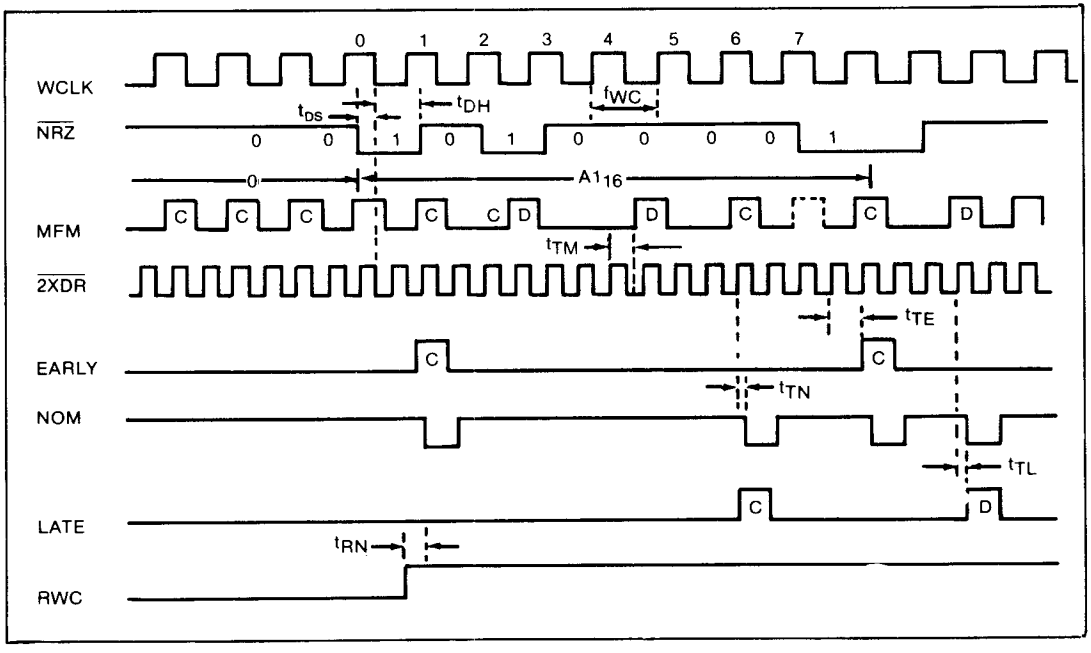


Figure 4. WD1100-12 MFM GENERATOR TIMING

Powered by ICminer.com Electronic-Library Service CopyRight 2003

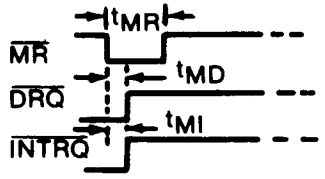


Figure 5

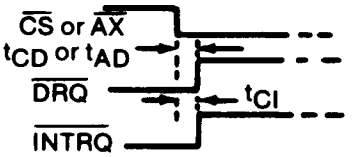


Figure 6

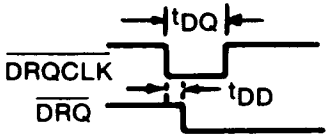


Figure 7

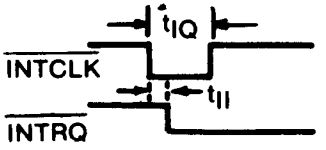


Figure 8

Powered by ICminer.com Electronic-Library Service CopyRight 2003