SONY CXK784862Q-50 50MHz

256K-byte Single Chip Cache Subsystem for 486 CPU

Description

The Sony Cache CXK784862Q is a single chip cache subsystem designed to work with the 486SX/DX/DX2 microprocessors at frequencies up to 50MHz. This device is designed utilizing Sony's proprietary Memory-intensive ASIC (MASIC™) technology. Using MASIC, the CXK784862Q integrates 256K-bytes of cache memory, tag RAM and associated control logic on a single chip. As a look-aside secondary cache, this device can be incorporated into various systems using different core-logic chipsets. This device can be designed onto a motherboard as a standard or an upgradeable feature. Multiple CXK784862Q chips can be cascaded to provide different levels of cache sizes and performance. A proprietary Enhanced Cascade Mode allows cascading at high speed without using external glue logic. High performance, high integration and low power characteristics render this device ideal for high performance desktop and mobile computing applications.

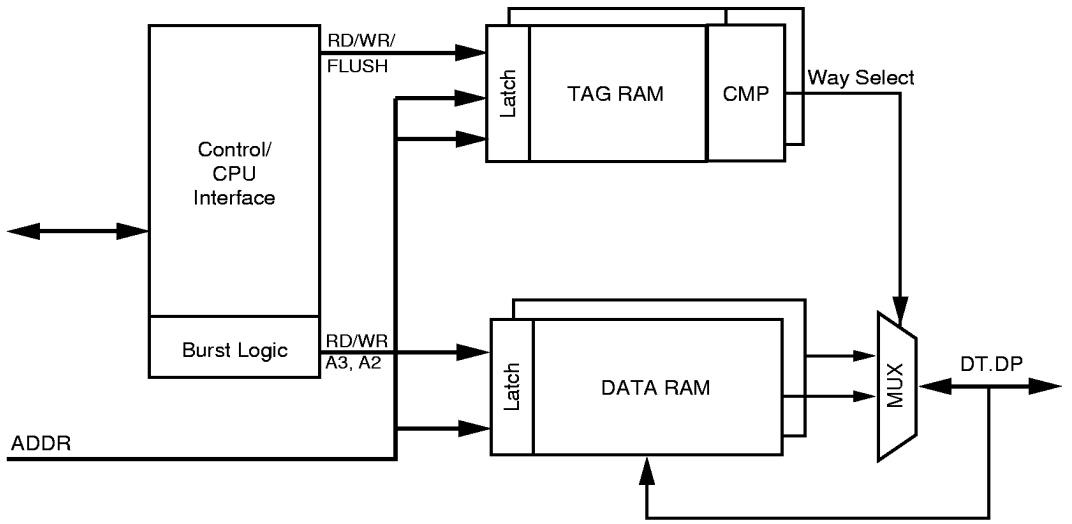
Features

- Look-aside architecture
- Write-through cache operation
- 50MHz operating frequency
- 256K-byte two-way-set associativity
- Supports MESI protocol
- Cascadable up to 1M bytes
- Enhanced cascade mode
- Zero wait state burst mode (2-1-1-1)
- PC compatible
- 160-pin PQFP

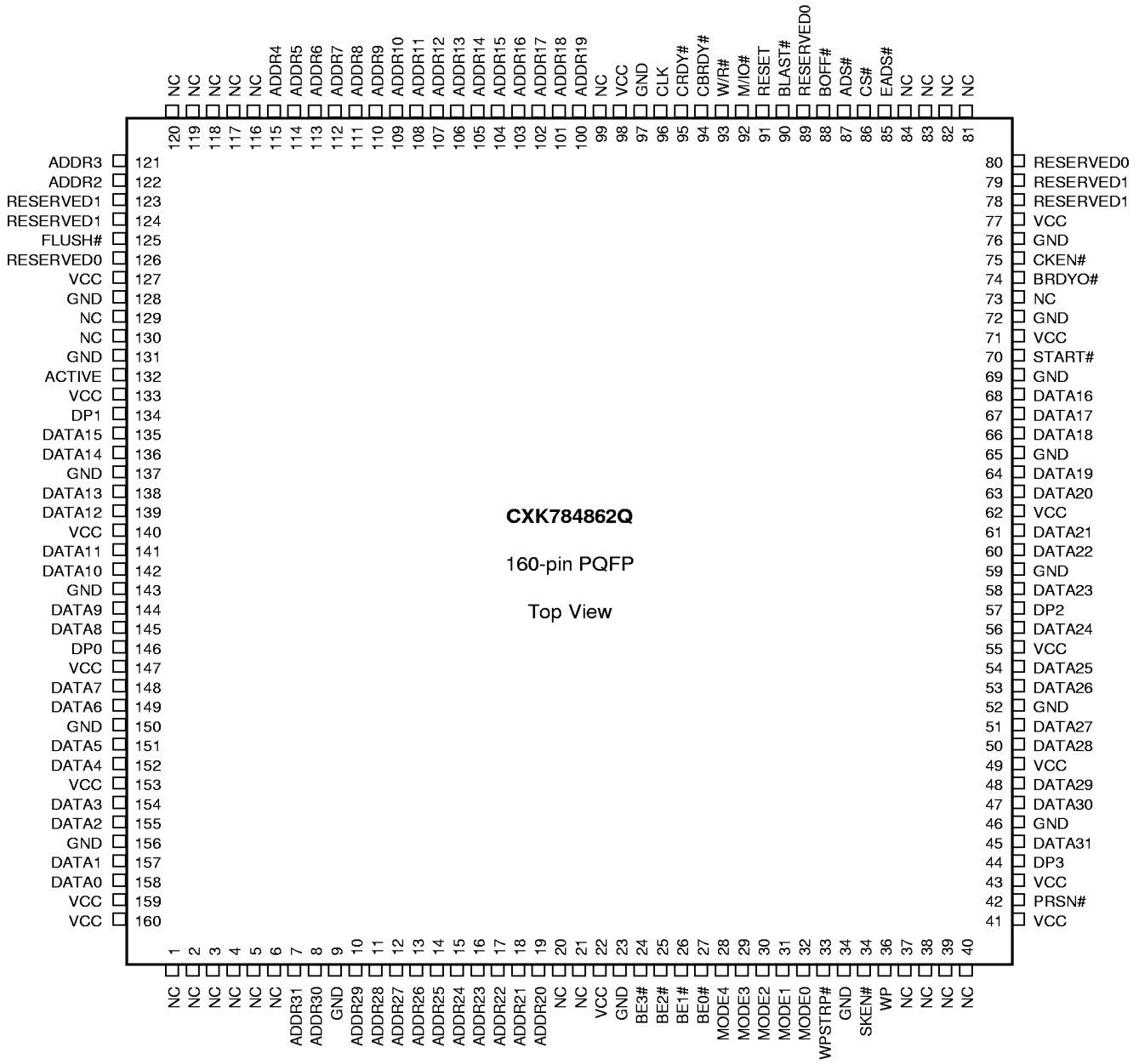
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration



NOTES:

"RESERVED_0" pins should be connected to GND through resistive pull-down.

"RESERVED_1" pins should be connected to V_{CC} through resistive pull-up.

"NC" pins should not be connected externally. Some of these pins may be driven by the CXK784862Q.

Table of Package Pin Numbers and Pin Names

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	NC	41	VCC	81	NC	121	ADDR3
2	NC	42	PRSN#	82	NC	122	ADDR2
3	NC	43	VCC	83	NC	123	RESERVED_1
4	NC	44	DP3	84	NC	124	RESERVED_1
5	NC	45	DATA31	85	EADS#	125	FLUSH#
6	NC	46	GND	86	CS#	126	RESERVED_0
7	ADDR31	47	DATA30	87	ADS#	127	VCC
8	ADDR30	48	DATA29	88	BOFF#	128	GND
9	GND	49	VCC	89	RESERVED_0	129	NC
10	ADDR29	50	DATA28	90	BLAST#	130	NC
11	ADDR28	51	DATA27	91	RESET	131	GND
12	ADDR27	52	GND	92	M/IO#	132	ACTIVE
13	ADDR26	53	DATA26	93	W/R#	133	VCC
14	ADDR25	54	DATA25	94	CBRDY#	134	DP1
15	ADDR24	55	VCC	95	CRDY#	135	DATA15
16	ADDR23	56	DATA24	96	CLK	136	DATA14
17	ADDR22	57	DP2	97	GND	137	GND
18	ADDR21	58	DATA23	98	VCC	138	DATA13
19	ADDR20	59	GND	99	NC	139	DATA12
20	NC	60	DATA22	100	ADDR19	140	VCC
21	NC	61	DATA21	101	ADDR18	141	DATA11
22	VCC	62	VCC	102	ADDR17	142	DATA10
23	GND	63	DATA20	103	ADDR16	143	GND
24	BE3#	64	DATA19	104	ADDR15	144	DATA9
25	BE2#	65	GND	105	ADDR14	145	DATA8
26	BE1#	66	DATA18	106	ADDR13	146	DP0
27	BE0#	67	DATA17	107	ADDR12	147	VCC
28	MODE4	68	DATA16	108	ADDR11	148	DATA7
29	MODE3	69	GND	109	ADDR10	149	DATA6
30	MODE2	70	START#	110	ADDR9	150	GND
31	MODE1	71	VCC	111	ADDR8	151	DATA5
32	MODE0	72	GND	112	ADDR7	152	DATA4
33	WPSTRP#	73	NC	113	ADDR6	153	VCC
34	GND	74	BRDYO#	114	ADDR5	154	DATA3
35	SKEN#	75	CKEN#	115	ADDR4	155	DATA2
36	WP	76	GND	116	NC	156	GND
37	NC	77	VCC	117	NC	157	DATA1
38	NC	78	RESERVED_1	118	NC	158	DATA0
39	NC	79	RESERVED_1	119	NC	159	VCC
40	NC	80	RESERVED_0	120	NC	160	VCC

Pin Description

Pin Name	Pin Number	I/O	Description
Address			
ADDR[31:2]	7-8, 10-19, 100-115, 121-122	I	Address pins shared by the CPU and the cache subsystem on the host bus.
BE#[3:0]	24-27	I	Byte enable. These signals allow individual bytes within a doubleword to be updated independently. They are ignored in all read cycles.
Data			
DATA[31 :0]	45, 47-48, 50-51, 53-54, 56, 58, 60-61, 63-64, 66-68, 135-136, 138-139, 141-142, 144-145, 148-149, 151-152, 154-155, 157-158	I/O	Data pins on the host bus.
DP[3:0]	44, 57, 134, 146	I/O	Data parity. One parity bit for each data byte. The CXK784862Q does not perform parity check. These bits are read and written like other data bits.
Control			
ACTIVE	132	O	This signal serves as an indicator in Enahnced Cascade mode to indicate which CXK784862Q chip has been selected to handle memory access. This pin should be used for debugging purposes only and should not be used during normal oper ation.
ADS#	87	I	Address strobe. An input from the CPU to indicate the start of an access cycle. The ADDR[31:2], BE#[3:0], CS#, M/IO# and W/R# signals must be valid when ADS# is active.
BLAST#	90	I	End-of-Burst indicator. Driven by the CPU to indicate the end of a burst cycle.
BOFF#	88	I	BOFF# is an input generated by the system logic to back-off the CPU and the CXK784862Q from the host bus. Any on-going bus access is aborted in the next cycle when BOFF# is active.
BRDYO#	74	I/O	Burst ready is generated by the CXK784862Q to indicate that a read hit has occurred and that data is being returned on the data bus. It also indicates that the CXK784862Q can transfer the entire cache line by using burst mode. Burst ready is normally tri-stated. During read hit, it is asserted by the CXK784862Q until the read cycle is terminated, and then driven high for one cycle before being tri-stat ed. It is an I/O pin during Enhanced Cascade mode.
CBRDY#	94	I	Cache data burst ready. Generated by the system logic to indicate that one cycle of data transfer has been completed and that burst mode can be used to transfer more data. This pin can be connected externally to BRDYO# to form an I/O pin that can be directly connected to the BRDY# input of the CPU. See appendix for more detail.
CKEN#	75	O	Cache Enable. This pin is driven by the CXK784862Q to indicate to the CPU if the read hit data from the CXK784862Q is cacheable in the CPU's internal cache. It can be sampled by the CPU in the same way as it samples KEN#. A CXK784862Q cache line is not cacheable in the CPU only if it is write protected and the write protect strap option is on.
CLK	96	I	System clock. Same as the 486 1X clock.
CRDY#	95	I	Cache data ready. Generated by the system logic to terminate the current bus cycle and to stop the burst transfer.
CS#	86	I	Chip Select. This signal must be asserted with ADS# and EADS#; otherwise ADS# and EADS# are ignored. When Enhanced Cascade Mode is used, CS# must be tied low.
EADS#	85	I	External Address Strobe. The CXK784862Q performs a snoop cycle when EADS# is active. The snoop address is sampled at the same time as EADS# is sampled low. If the snoop address hits a cache line, that cache line is invalidated internally.

Pin Name	Pin Number	I/O	Description
FLUSH#	125	I	FLUSH# invalidates all the cache lines in the CXK784862Q. This can be used to ensure than any stale data, if present, will be purged from the cache.
M/IO#	92	I	Memory and I/O selector. Memory is selected if this signal is high, otherwise I/O is selected.
MODE[4:0]	28-32	I	Operation mode selector. Static input pins. Selects between normal mode, Enhanced Cascade mode and test mode. MODE[4:0] Description 00000 Normal mode, 256K-byte 00100 Enhanced Cascade mode, 1024K, chip0 00101 Enhanced Cascade mode, 1024K, chip1 00110 Enhanced Cascade mode, 1024K, chip2 00111 Enhanced Cascade mode, 1024K, chip3 01100 Enhanced Cascade mode, 512K, chip0 01101 Enhanced Cascade mode, 512K, chip1 all other mode pin combinations are reserved.
NC	1-6, 20-21, 37-40, 73, 81-84, 99, 116-120, 129-130	—	These pins must be left unconnected to any external signal. Some of these signals may be driven by the CXK784862Q.
PRSN#	42	O	This is a static output pin that always drives low. It allows the system logic to detect the presence of the CXK784862Q chip.
RESET	91	I	Resets the CXK784862Q to the initial state and invalidates all the tag entries. The CXK784862Q must be reset after power-up or after mode pin changes.
RESERVED_0	80, 89, 126	I	These pins must be tied low through pull-down resistors.
RESERVED_1	78, 79, 123-124	I	These pins must be tied high through pull-up resistors.
SKEN#	35	I	Cacheability indicator. This signal is sampled by the CXK784862Q to determine if a line fill is cacheable. It is sampled twice during a line fill. It is first sampled one clock cycle before the first CBRDY#. It is sampled again one clock cycle before the last CBRDY# of the line fill. SKEN# must be active during both sampling points; otherwise the line fill is not cacheable.
START#	70	I/O	The START# pin indicates to the system memory that a read miss or memory write has occurred. The system memory is required to handle these cycles.
W/R#	93	I	Read/Write select. High indicates a write cycle and low indicates a read cycle.
WP	36	I	The Write Protect signal indicates if a cache line is write protected. It is sampled at the third cycle of a cache line fill. If WP is high and the write protect strap option is on, the line is write protected and any further attempts to write to this location will be ignored.
WPSTRP#	33	I	Write Protect Strap. It is sampled at the falling edge of RESET. It must be stable for two clocks before and after the falling edge of RESET. If WPSTRP# is sampled active, the write protect strap option is turned on. The CXK784862Q will use the WP pin to determine the write protection of the cache line. If WPSTRP# is sample inactive, the WP input will have no effect.

Functional Descriptions

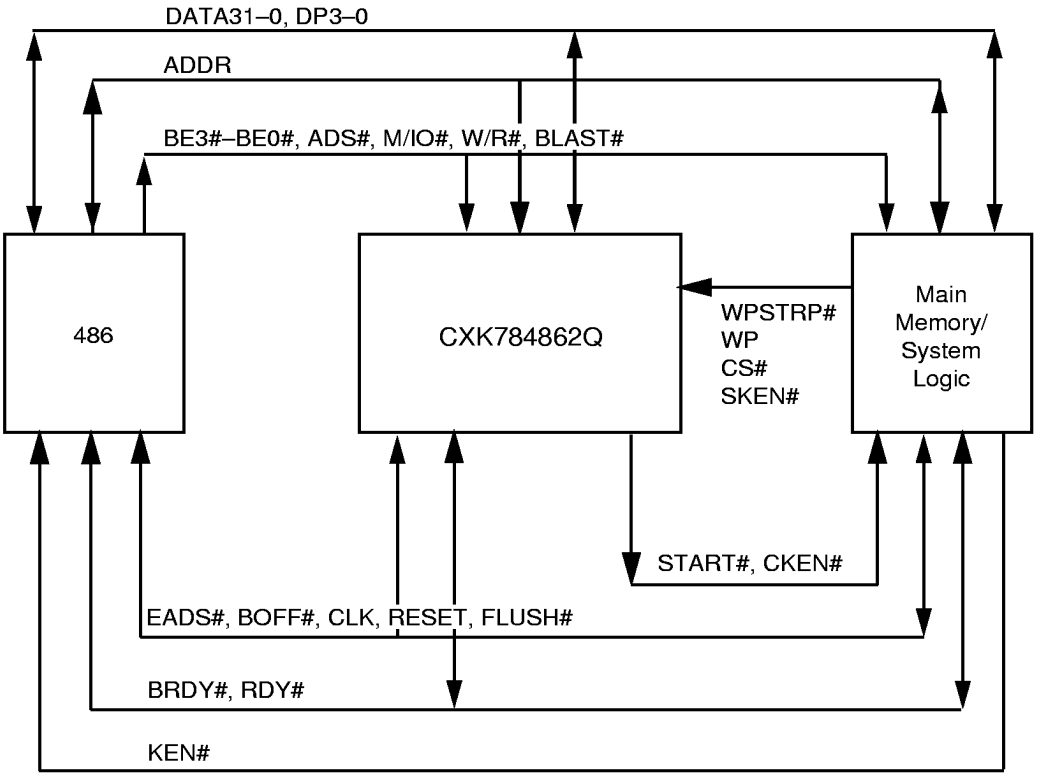
Introduction

The Sony Cache CXK784862Q is designed to work with the 486 microprocessor in a "look aside" configuration. Data and address buses from the CPU are routed to the system memory and the CXK784862Q in parallel. If data read by the CPU is present in the CXK784862Q, i.e. cache hit, the CXK784862Q returns its cache data to the CPU without requiring services from the system memory.

If data needed by the CPU is not in the CXK784862Q, it will start a memory cycle. The CXK784862Q will monitor the transactions between the CPU and memory. Data returned from the memory is captured by the CPU and the CXK784862Q at the same time. The control logic within the CXK784862Q caches the newly returned data automatically. Future references to the same data will produce a cache hit in the CXK784862Q so that data can be transferred to the CPU with zero wait state.

The CXK784862Q is a write-through cache so that all write data will be written into the system memory and, for write hit, to the CXK784862Q simultaneously. The write-through design guarantees data consistency between the cache and system memory whenever data is written by the CPU.

The CXK784862Q interface logic understands the CPU bus cycles for memory accesses. It monitors all the transactions between the CPU and external cache/memory but does not generate bus transactions of its own. This near-transparent design minimizes overheads for cache fill and allows the CXK784862Q to be incorporated into any motherboard design with minimum design changes. A motherboard can be designed with the CXK784862Q as a plug-in option to offer different levels of performance. The figure below shows a typical system configuration with the CXK784862Q cache subsystem.



Typical System Configuration

Internal Architecture

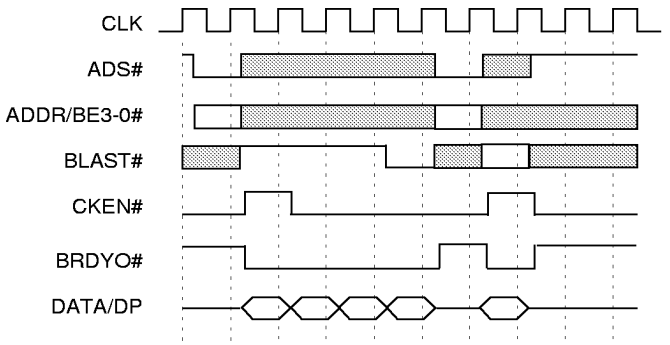
The CXK784862Q is a 256k-byte 2-way-set-associative cache system with line size of 16 bytes. Each WAY contains 4k tags and each tag controls two lines of cache memory. The upper address bits, ADDR[31:17] are stored in the tag when data is written into the cache. The next lower address bits, ADDR[16:5] select one of the 4k tags and the address bits ADDR[4:2] select the line and the doubleword within the cache line.

Since the cache is 2-way-set-associative, there are two possible locations for each data line to be stored in the cache. During a read, address bits 16 to 5 access the two tag entries simultaneously and the two tags are compared with the address bits 31 to 17. The matched tag indicates the corresponding data are stored in the cache; thus a cache hit is generated. Once a cache hit is detected, memory reads for any of the bytes within the cache line can be read from the cache. If neither of the tags matches the address bits or the tags are invalid, then a cache miss is generated and data must be read from system memory.

When a data line is read from system memory, it is cached into the CKX784862Q and the CPU at the same time. A Least Recently Used (LRU) algorithm is used to select one of the two WAYs to store the new data. An LRU bit is maintained for each of the 4k tags for cache update. Since the CKX784862Q is a write-through cache, there is no need to copy the existing data to the system memory during cache replacement.

Interface to CPU

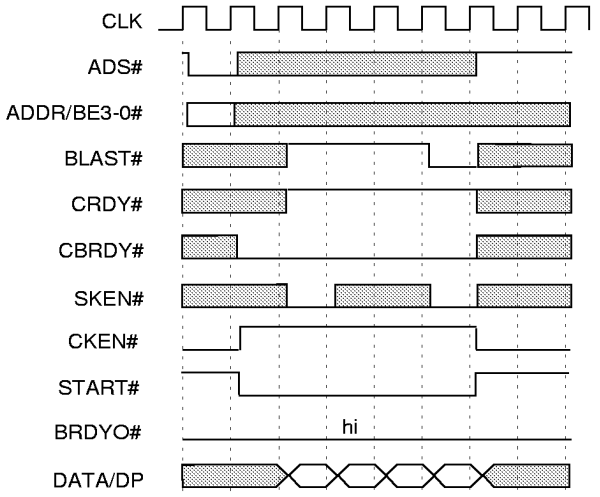
The CXK784862Q is designed specifically for a 486-based motherboard and it understands the memory access cycles generated by the CPU. It monitors ADS#, CS#, M/IO#, W/R#, and ADDR to initiate a cache read. If the read address produces a cache hit, the CXK784862Q returns data with zero wait states. Since the entire cache line is valid in the CXK784862Q, it transfers data to the CPU using burst mode by asserting BRDYO#. If the CPU indicates it is also ready to accept more data by deasserting BLAST#, the burst sequence will continue and the remaining doublewords of the cache line will be sent to the CPU with zero wait state until BLAST# is asserted. Data returned from the CXK784862Q is cacheable in the CPU's internal cache unless the WP (Write Protect) bit of the cache tag is set and the WSTRP option is on. The figure below is a timing diagram of a read hit cycle.



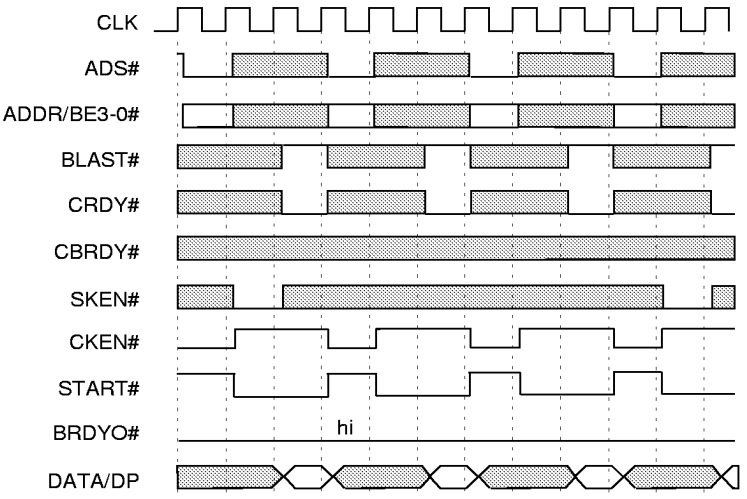
Cache Hit with CPU Reading Four Words Followed by Cache Hit with CPU Reading One Word

Interface to System Memory

If a memory read produces a cache hit, the CXK784862Q will return data directly to the CPU without alerting the system memory. However, if the read access produces a cache miss, system memory is called upon by the CXK784862Q to serve the memory read. It indicates a cache miss to the system memory by asserting START#. Other control signals such as M/IO#, W/R# and ADDR are available to the system memory directly from the CPU. The CXK784862Q monitors the ready signals, CRDY# and CBRDY#, from system memory to read data from the DATA bus. The system memory can use burst or non-burst mode to return data to the CPU and the CXK784862Q. Data from the system memory is cacheable in the CXK784862Q only if the SKEN# input is driven active one clock cycle before the first data returns from the system memory and one clock cycle before the last data. If a cache line fill is aborted before it is completed, the CXK784862Q will not update its cache line. The next two figures show the interactions between the CXK784862Q, system memory and the CPU during cache misses.



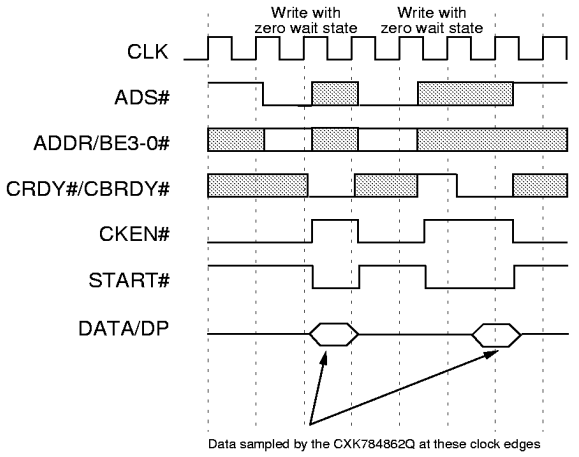
Line Fill with Burst Mode and No Wait State



Read Miss with Non-Burst Line Fill

Write Sequences

A write-through cache design implies that every time the CPU writes data into memory, the cache and the system memory are updated at the same time. If the write data is already in the cache (write hit), the CXK784862Q updates its cache line and activates START# to initiate the memory update. If the write data is not in the cache (write miss), the CXK784862Q activates START# but does not operate on the data. The figure below shows the timing sequences of write cycles.



Write Hit Cycle

Cache Line Snoop

In order to support external bus master and DMA transfers efficiently, the CXK784862Q has the capability of invalidating an individual cache line when the line is updated by a master other than the CPU. To invalidate a cache line, the external master performs a snoop cycle by asserting EADS# and drives the valid address on to ADDR[31:4]. The CXK784862Q checks its tags for a cache hit. The line is invalidated if it is found in the cache. The CXK784862Q can be snooped once every two clock cycles. It requires one cycle for reading the tag entries and one cycle for invalidating the tag. Invalidation can run at the same time the CXK784862Q is doing a line fill since ADDR[31:4] and EADS# are not used during a line fill. A cache access after the current line fill, however, can be delayed if the line fill and invalidation cycles are running in parallel. The figure below illustrates the timing sequences.

Time	T1	T2	T2	T2	T2	T2	T1	T2
	Tag Search	Activates START#	Start Line Fill			Validate Tag for Line Fill	Tag Search	START#

Normal START#

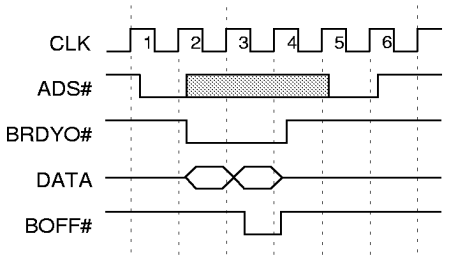
Time	T1	T2	T2	T2	T2	T2			T1	T2
	Tag Search	Activates START#	Start Line Fill			EADS# Tag Search	Validate Tag	Validate Tage for Line Fill	Tag Search	START#

Invalidation delays START#

Timing of START# Signal

Backoff

To further support multiple bus master systems and to avoid deadlock, a backoff feature is incorporated. With this feature, the external master can assert the BOFF# input to the CXK784862Q anytime during operation. The CXK784862Q immediately relinquishes the bus and aborts any read or write cycle it may be running at the time. After BOFF# has been de-asserted, it waits for the CPU to start a new operation. The figure to the right is an example of asserting BOFF# during read hit.



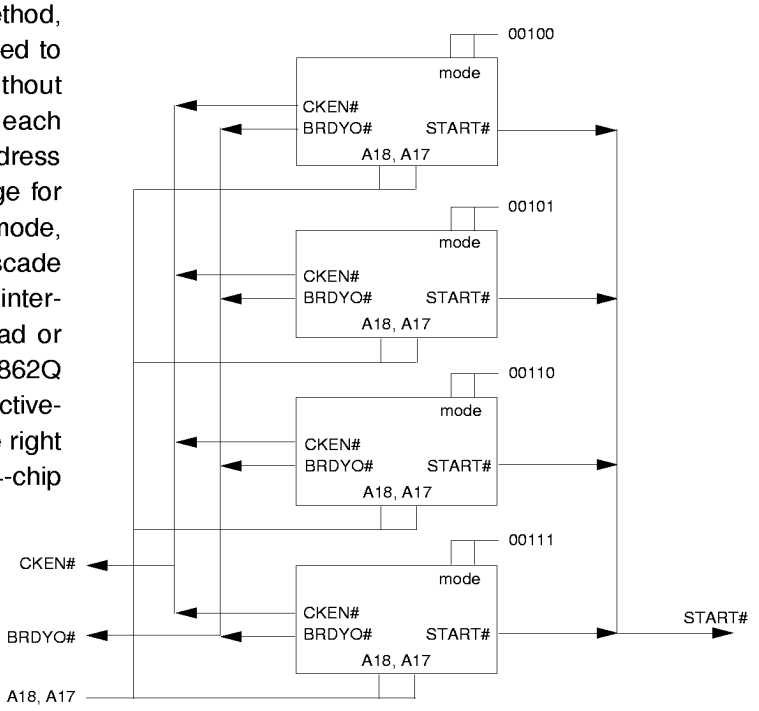
NOTES:

1. BOFF# may be asserted at any cycle. Current memory access is aborted and will not be restarted after BOFF# is de-asserted.
2. Asserting ADS# at Cycle 5 starts a new memory access.

BOFF# Asserted During Read Hit

Enhanced Cascade Modes

Multiple CXK784862Q chips can be cascaded together to increase cache size. A special cascading method, called the Enhanced Cascade Mode, was developed to cascade multiple CXK784862Q chips together without using any external glue logic. Under this mode, each CXK784862Q chip in the system decodes the address internally and responds to a specific address range for read, write and snoop cycles. In 2-chip cascade mode, ADDR17 is used as internal select. In 4-chip cascade mode, ADDR[18:17] are both used to decode the internal select. The chips that are not selected for read or write are disabled. Outputs from all 2 or 4 CXK784862Q chips can be wired together since only one chip is actively driving during normal operation. The figure to the right illustrates the Enhanced Cascade mode used in a 4-chip cascade design.



Enhanced Cascade Mode with No External Glue Logic

Electrical Characteristics

Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_D	2.7(1)	W
Ambient (operating) temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	–55 to +150	°C

DC Characteristics

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{CC}	4.75	5.25	V
Input low voltage	V_{IL}	–0.3(1)	+0.8	V
Input high voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Output low voltage @4.5mA	V_{OL}	—	0.4	V
Output high voltage @–1.0mA	V_{OH}	2.4	—	V
Input leakage current	I_{LI}	–1	1	µA
Output leakage current	I_{LO}	–1	1	µA
Supply current @ 33MHz	I_{CC1}	—	500	mA
Supply current @ 50MHz	I_{CC2}	—	700	mA
Capacitance: PQFP	Cin			
Clock pin			9	pF
Other input pins			7	pF
Output pins			9	pF
I/O pins			9	pF

NOTE:

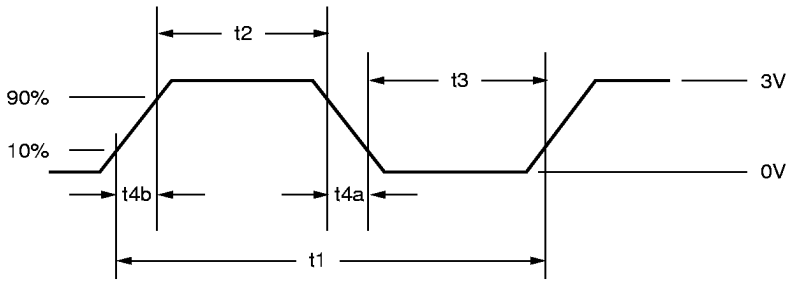
1. V_{IL} = –1V min. for 3ns per cycle.

AC Characteristics Operating Conditions: 5V Vcc, ±5%, 0 to +70°C

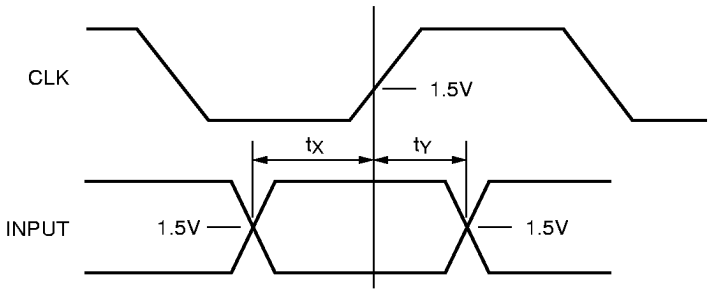
Symbol	Parameter	Min. (ns)	Max. (ns)
t_1	CLK Period	20	
t_2	CLK HIGH Time	6	
t_3	CLK LOW Time	6	
t_{4a}	CLK Fall Time		3
t_{4b}	CLK Rise Time		3
t_{5a}	ADDR, BE0#-BE3# Setup (non-Snoop)	5	
t_{5b}	ADDR, BE0#-BE3# Hold (non Snoop)	3	
t_{6a}	ADS#, M/IO#, W/R# Setup	5	
t_{6b}	ADS#, M/IO#, W/R# Hold	3	
t_{7a}	BLAST# Setup	5	
t_{7b}	BLAST# Hold	3	
t_{8a}	CRDY#, CBRDY# Setup	4	
t_{8b}	CRDY#, CBRDY# Hold	3	
t_{9a}	SKEN# Setup	4	
t_{9b}	SKEN# Hold	3	
t_{10a}	DATA, DP0-DP3 Setup	4	
t_{10b}	DATA, DP0-DP3 Hold	3	
t_{11a}	WP Setup	5	
t_{11b}	WP Hold	3	
t_{12a}	BOFF# Setup	5	
t_{12b}	BOFF# Hold	3	
t_{13a}	EADS# Setup	4	
t_{13b}	EADS# Hold	3	
t_{14a}	ADDR Setup (invalidation)	4	
t_{14b}	ADDR Hold (invalidation)	3	
t_{15a}	RESET, FLUSH# Setup	4	
t_{15b}	RESET, FLUSH# Hold	3	
t_{16}	BRDY)# Valid	3	13
t_{17}	CKEN# Valid	3	9
t_{18}	START# Valid	3	15
t_{19}	DATA Valid (Read Hit)	4	13
t_{20a}	CS# Setup	4	
t_{20b}	CS# Hold	3	
t_{22a}	BRDYO# Enable	0	
t_{22b}	BRDYO Disable		13

NOTE:

All AC measurements are made with input switching from 0V to 3V. Input and output reference points are at 1.5V.

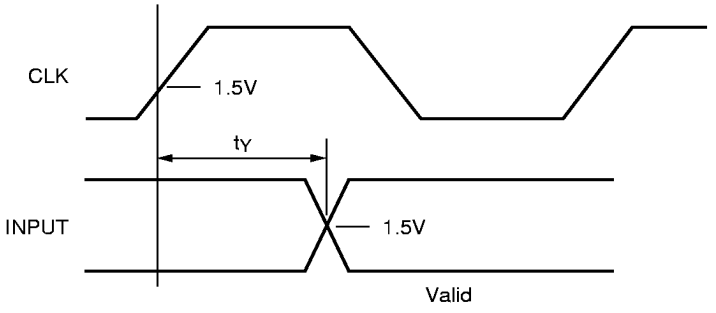


Clock Waveform



$t_X = t_{5a, 6a, 7a, 8a, 9a, 10a, 11a, 12a, 13a, 14a, 15a, 20a}$
$t_Y = t_{5b, 6b, 7b, 8b, 9b, 10b, 11b, 12b, 13b, 14b, 15b, 20b}$

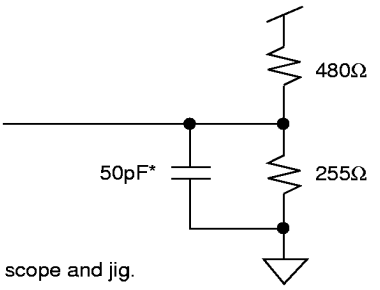
Setup and Hold Timings



$t_Y = t_{16, 17, 18, 19}$

Valid Delay Timings

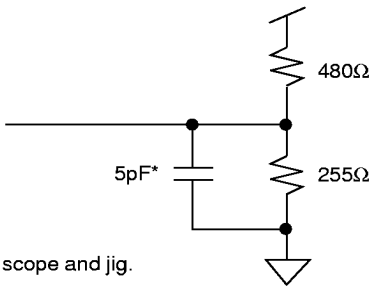
Output Load (1) for DT and DP



*Including scope and jig.

Output Load for Valid Delay

Output Load (2)



*Including scope and jig.

NOTES:

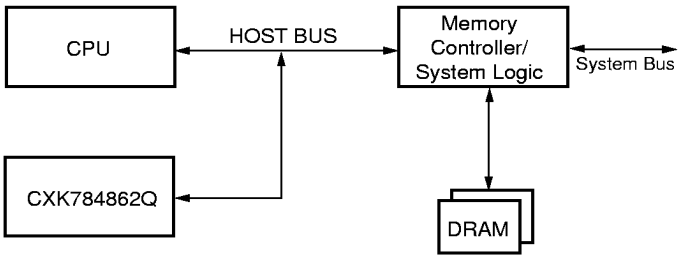
1. Transition is measured ±200mV from steady voltage with specified loading.
2. Float delay is sampled and is not 100% tested.

Output Load for Float Delay

Appendix

This appendix is organized as a design guide for using the CXK784862Q in typical system design. It first describes the special features such as Enhanced Cascade Mode and the usage of the mode pins. The next section describes typical design issues. Due to the simplicity of the look-aside architecture, the CXK784862Q can work with most PC systems without major design changes. However, some of the interface signals between the CPU and the system logic may be affected by the presence of the CXK784862Q. This section describes how some of these signals should be connected. The last section describes the restriction sin snoop cycle.

System Block Diagram



Mode Pin Usage

The mode pins define the operation mode of the CXK784862Q. These pins are static input pins tied to either logic-1 or logic-0 according to the desired operation mode. The mode pins are defined as the following:

MODE[4]:

This pin can be defined independently of the other mode pins. If this pin is tied to logic-0, the BRDYO# output will be tri-stated one cycle after each low-to-high transition. BRDYO# is enabled automatically when it dries low. If MODE[4] is tied to logic-1, the BRDYO# and output are always enabled regardless of output state.

MODE[3:0]

MODE[3]	MODE[2]	MODE[1]	MODE[0]	Operation Mode
0	0	0	0	256K-byte normal mode
1	0	0	0	Data RAM test mode
1	0	0	1	Tag RAM test mode
0	1	0	0	Enhanced cascade mode, 1024K, chip0
0	1	0	1	Enhanced cascade mode, 1024K, chip1
0	1	1	0	Enhanced cascade mode, 1024K, chip2
0	1	1	1	Enhanced cascade mode, 1024K, chip3
1	1	0	0	Enhanced cascade mode, 512K, chip0
1	1	0	1	Enhanced cascade mode, 512K, chip1
1	1	1	1	128K-byte scale-down mode

The test modes are used for production testing and should not be used in the system. The 256K-byte normal mode should be used in normal non-cascade design. If MODE[3:0] are all connected to 1, the CXK784862Q emulates a 128K-byte cache system. Internally half of the data RAM and the tag RAM are disabled, so it would have the same performance as a 128K-byte cache. No address scrambling is required.

If two or four CXK784862Q chips are cascaded in a system to form a larger cache using enhanced cascade mode, all the CXK784862Q chips on the system should have MODE[3:0] tied to cascade mode setting. For example, if two CXK784862Q chips are cascaded in a system to form a 512K-byte cache, one of the CXK784862Q chips should be designated as chip0 and its MODE[3:0] pins tied to “1100”. The other CXK784862Q chip should have MODE[3:0] tied to “1101”.

Enhanced Cascade Mode

The Enhanced Cascade mode allows 2 or 4 CXK784862Q chips to work together to form a larger cache without using any external logic gates. When used in enhanced cascade more, most of the inputs (except the MODE pins) and outputs (except the ACTIVE pin) are wired to all the CXK784862Q chips in parallel. For example, the BRDYO# pin from all the CXK784862Q chips on the system are wired together to form the BRDYO# signal. When the system is powered-on or after reset, all the CXK784862Q chips on the system drive the outputs to the idle states. Since each output is driven to the same value by all the CXK784862Q chips, there is no signal conflict. Each memory access from the CPU would select one of the CXK784862Q chips as the active chip based on the value of ADDR18 and ADDR17. The unselected chips tri-state their outputs so that the active chip has total control of the output and I/O signals. The selected chip remains active until the next memory access which will start the select process again.

The ACTIVE output pin from each CXK784862Q should not be wired together. This pin is used for debugging only. When a CXK784862Q chip is selected, it asserts its ACTIVE output signal. If a chip is not selected, its ACTIVE pin is driven low.

The CS# input cannot be used during cascade mode. The CS# input to all the CXK784862Q chips must be connect to logic-0.

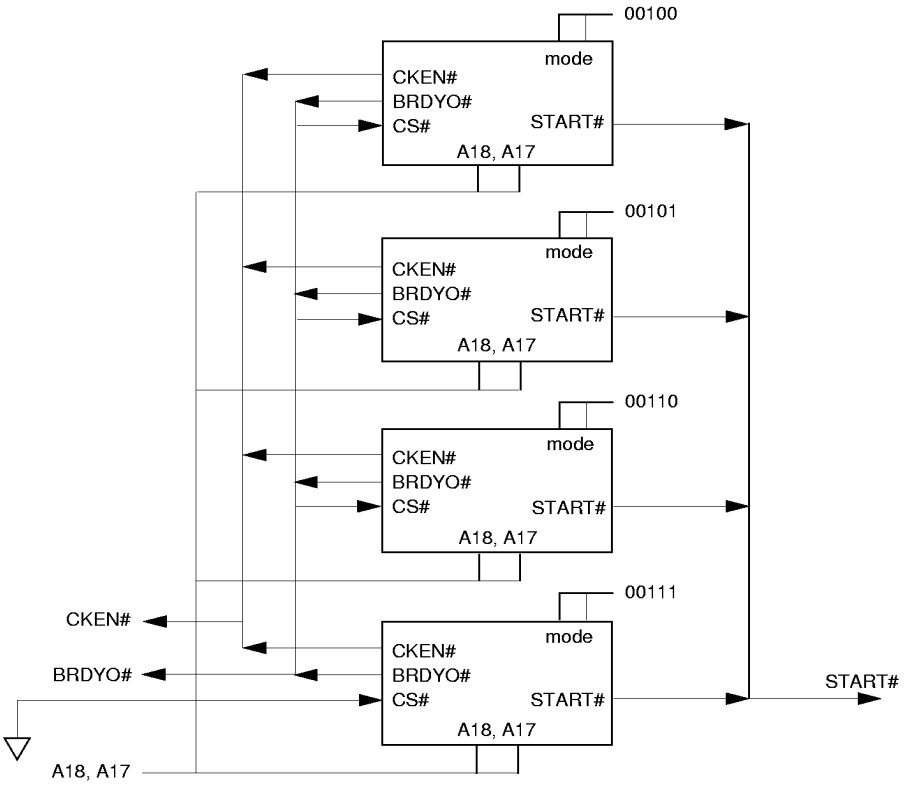


Figure A1. Enhanced Cascade Mode

Interface Signal Generation

CKEN# and SKEN#

SKEN# is driven by the system logic and received by the CXK784862Q to determine cacheability of a line fill. CKEN# is driven by the CXK784862Q to determine cacheability of a CPU line fill when data is provided by CXK784862Q (read hit). Data provided by the CXK784862Q is normally cacheable internal to the CPU with the exception of write protected lines. There are two methods to generate KEN# to the CPU through SKEN# and CKEN#.

The first method uses an external AND gate as shown in Figure A2. SKEN# is driven by the system logic according to data cacheability during read miss cycles. During read hit cycles, the SKEN# signal should be high so that the KEN# input of the CPU is controlled by the CKEN# output.

The alternative method is shown in Figure A3. The method is applicable if the write-protect feature of the CXK784862Q is not used. In the absence of write-protected data, all read hits on CXK784862Q are cacheable in the CPU. The system logic should always drive KEN# low except during read miss or write cycles. KEN# should be driven according to the cacheability of the data during read miss cycles.

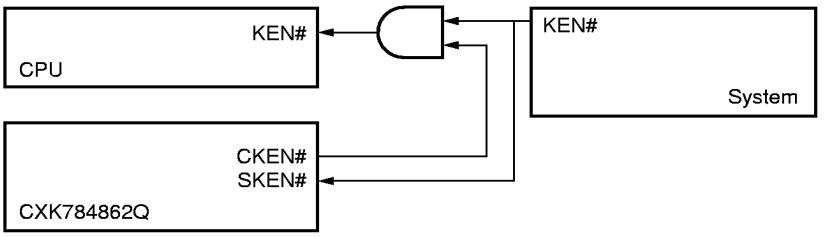


Figure A2. KEN# Generation

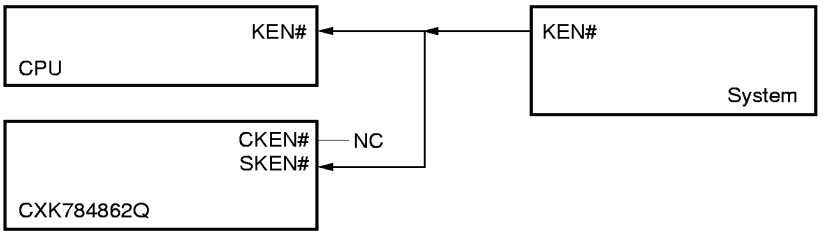


Figure A3. KEN# Generation, Alternative Method

BRDY#

If MODE[4] pin is tied to "0", BRDYO# from the CKX784862Q is normally tri-stated except during read hit cycle when the CKX784862Q drives this signal active (low). In the clock cycle after read hit is finished, the CKX784862Q drives BRDYO# high for one cycle and then it is tri-stated. A pull-up resistor should be used to maintain BRDYO# at high level when it is tri-stated. The BRDY# signal from the system should be driven low only during read miss, write and I/O cycles. In all other cycles it should be driven high and then tri-stated. The CPU's BRDY# input can be generated by wire_AND the BRDYO# signal from the system and from the CKX784862Q. CBRDY# and BRDYO# of the CKX784862Q can also be wired together to form an I/O pin.

START#

START# is used by the CKX784862Q to signal any cycle that requires services from the system memory. These cycles are read miss, write miss and write through cycles. The system memory controller can monitor this signal instead of the ADS# signal from the CPU to activate the system memory. The system logic should still monitor the ADS# signal from the CPU to detect I/O cycles.

CS#

The Chip Select signal should be tied low (active) during normal operation. If CS# is driven high, the CXK784862Q does not respond to any memory access or snoop cycle.

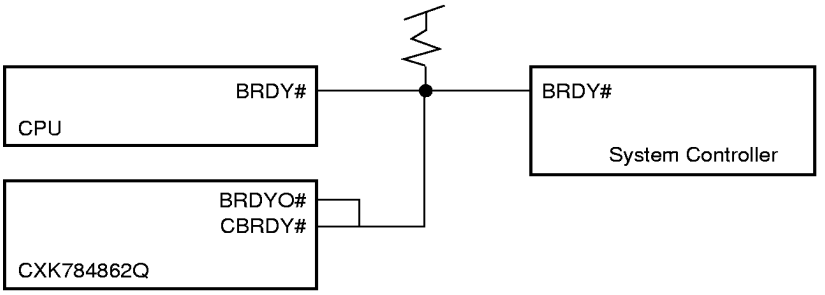


Figure A4. BRDY# Signal Generation

EADS# During Line Fill

Invalidation by EADS# during line fill may cause problems if not handled properly. Figure A5 is one example that invalidation will fail. The line fill completes at cycle 6 and validatio of the cache line is supposed to take place at the same cycle. But, since the EADS# request has higher priority, the validation of the cache line at 0000 is delayed until cycle 9, after the completion of EADS# at cycles 5 and 7. The EADS# request at cycle 7, even though it specifies address 0000, failed to invalidate the cache line at 0000 because it has taken place before the validation is performed. Furthermore, because internal tag RAM is used for invalidation, the ADS# at cycle 9 is delayed until cycle 11 before the corresponding START# is generated.

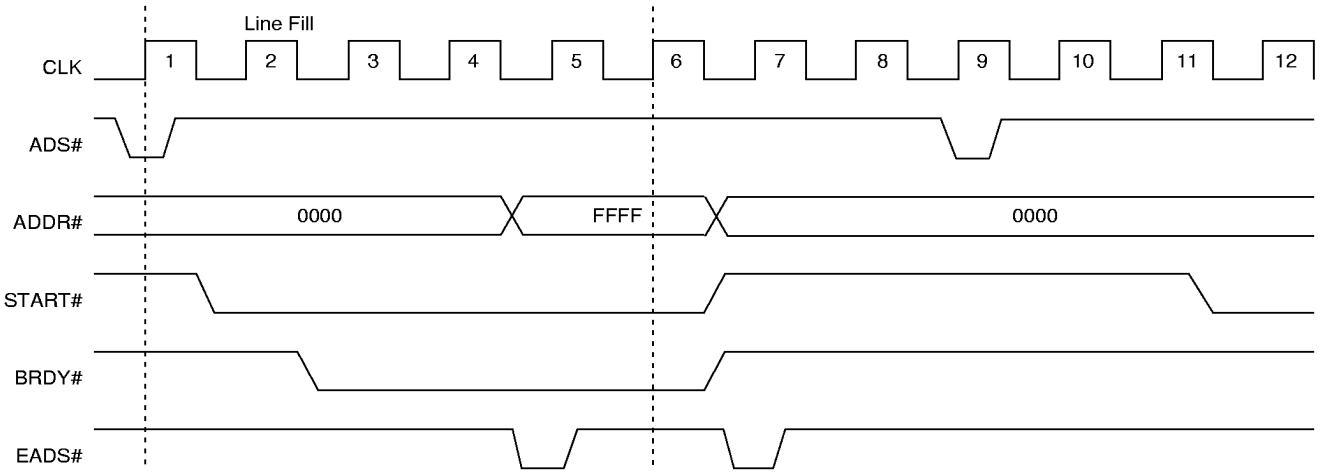


Figure A5. EADS# Causing Problem During Line Fill

The EADS# problem also exists in the following case:

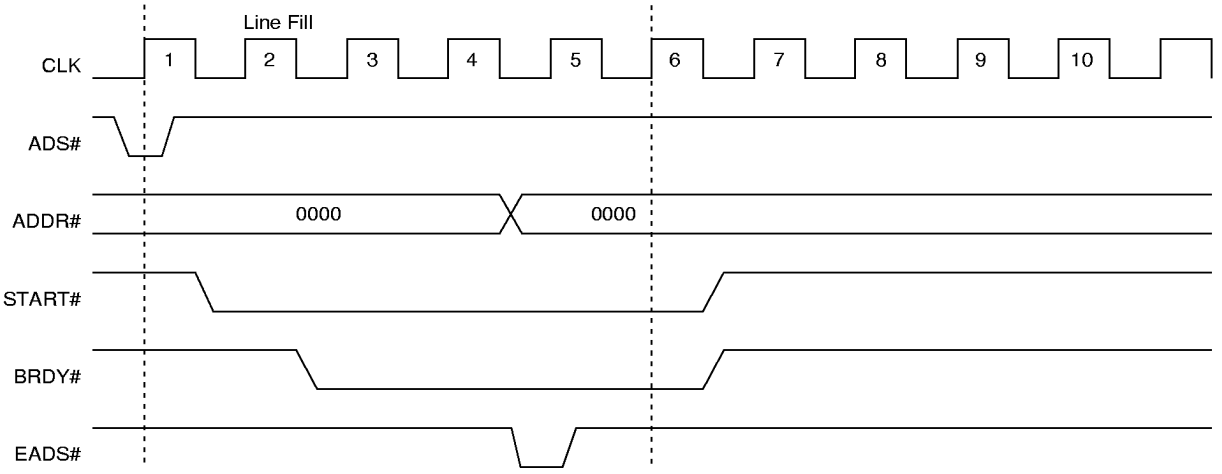
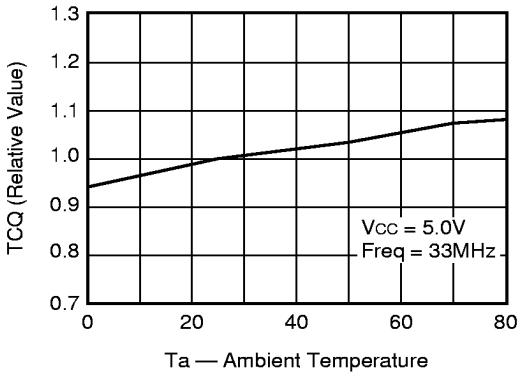


Figure A6. EADS# Causing Problem During Line Fill

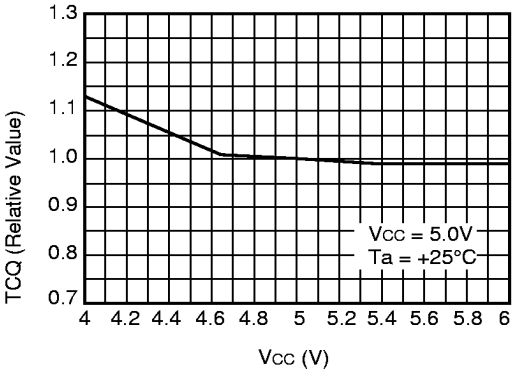
There are three different ways to avoid the problems shown in Figures A5 and A6:

1. Do not allow EADS# from the cycle that line fill has started until the last doubleword has returned. This applies even if the line fill is of non-burst type.
2. If EADS# is activated during line fill, do not assert SKEN# before the last doubleword of the line fill. This way the cache line will not be validated.
3. Activate EADS# request only during back-off. The back-off cycle aborts all line fill in progress.

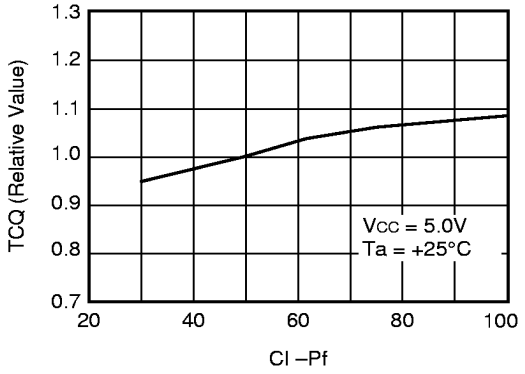
TCQ vs Ambient Temperature



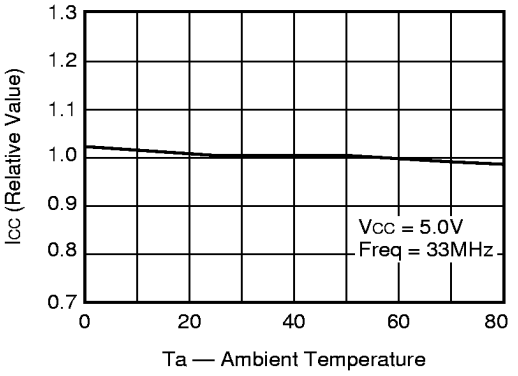
TCQ vs Supply Voltage



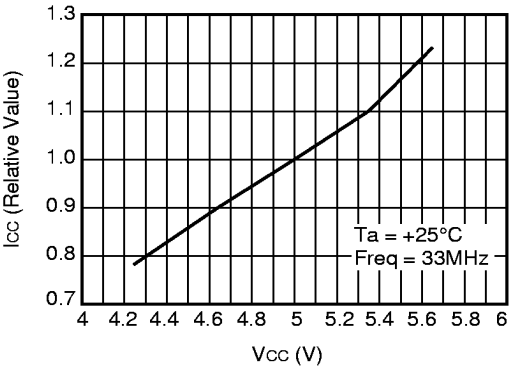
TCQ vs Output Load



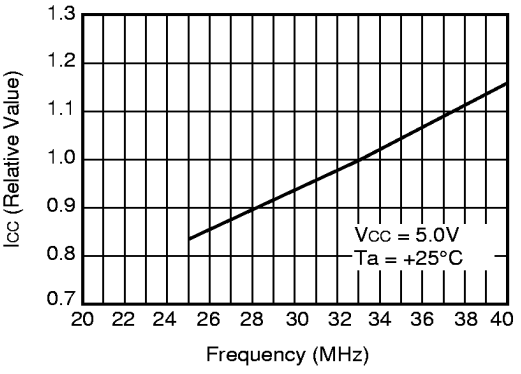
Supply Current vs Ambient Temperature



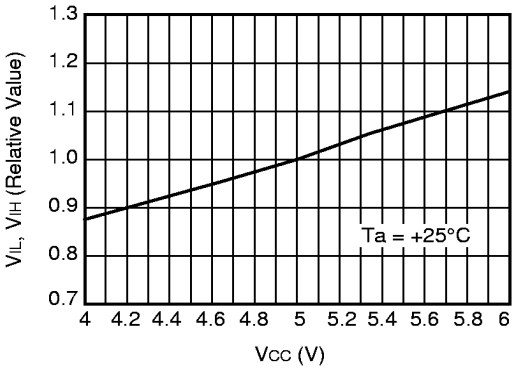
Supply Current vs Supply Voltage



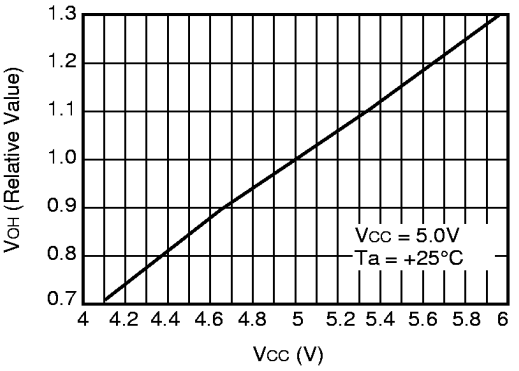
Supply Current vs Frequency



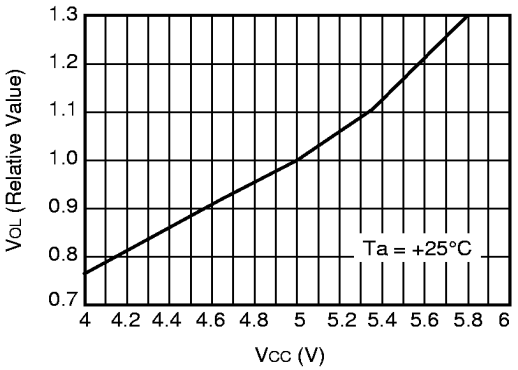
Input Voltage Level vs Supply Voltage



VOH vs Supply Voltage

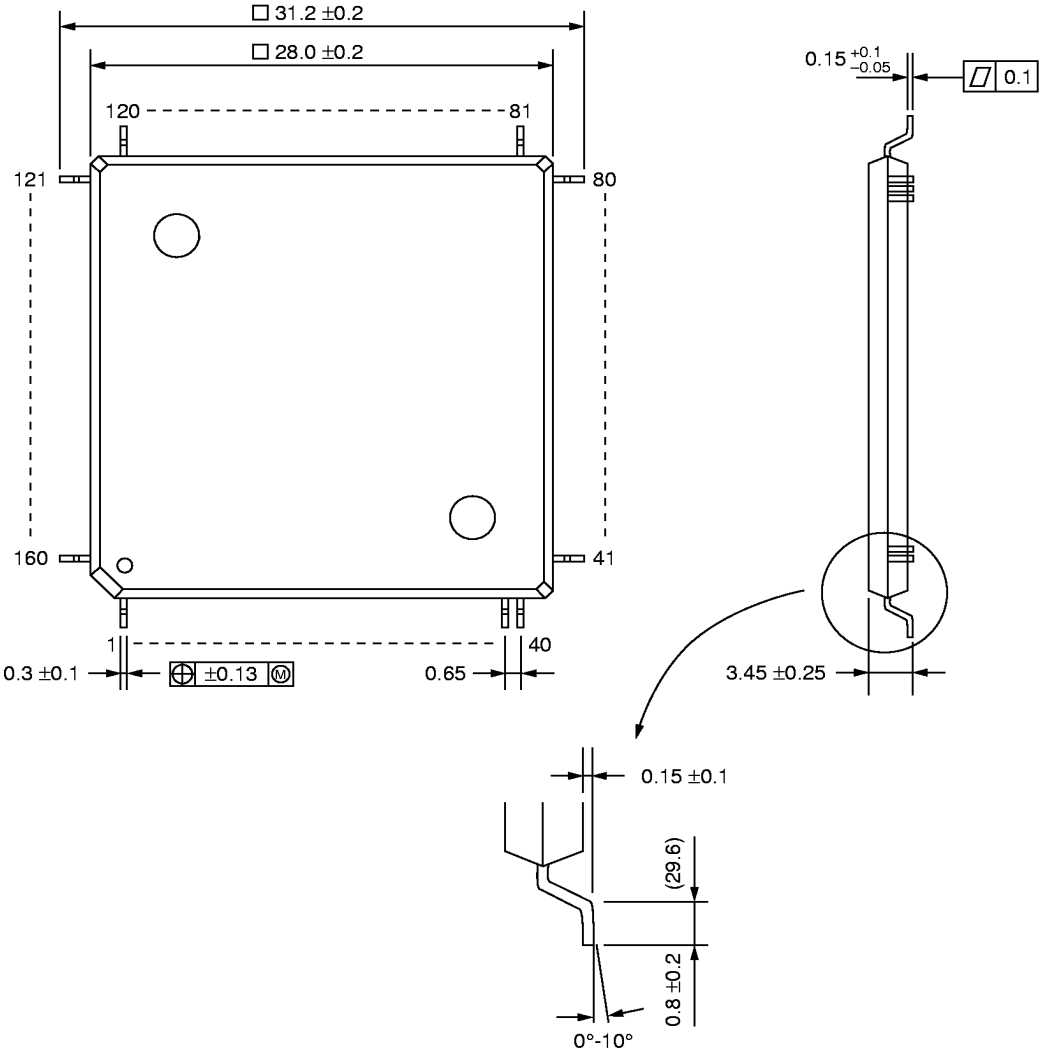


VOL vs Supply Voltage



Package Dimensions Unit: mm

160 Pin QFP (Plastic)



SONY CODE	QFP-160P-L01
EIAJ CODE	*QFP160-P-2828-A
JEDEC CODE	—

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER/42 ALLOY
PACKAGE WEIGHT	4.9g