DSP56300 Family Manual Addendum

This document provides updated information for revision 3.0 of the *DSP56300 Family Manual (DSP56300FM/AD)*. The updates include the following:

- Change in required instructions to ensure that no maskable interrupts occur during a non-interruptible code sequence
- Modified stack extension description
- Operating Mode Register (OMR) bit 11 definition
- System stack configuration description
- Added note about the DSP56321 DPLL and clock modules
- Updated VCO description
- Modified design guidelines for ripple and PCAP
- Modified Port A descriptions
- Added note about DRAM support
- Clarified BLH bit description and modified trailing wait state definition for DSP56321 only
- Added note for the DRAM control register
- Redefined DMA end-of-block transfer operation
- Modified X0 register description example for the INSERT instruction

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1 Non-Interruptible Code Sequence

Area to Change	Change Description
Section 2.3.2, p. 2-17	There is a change in the number of prior instructions required to ensure that non-interruptible code runs correctly. Replace the second sentence from the top of the page with the following: Due to pipeline latency, any changes to IPL masking in the SR are not reflected in code processing until 15 clock cycles after the change is made. Therefore, after any change in IPL masking, particularly if the masking level is increased, add 15 NOP instructions immediately after the instruction that writes the new IPL masking to ensure proper operation. **Note:** The two preferable scenarios in which interrupt disabling should not require additional precautions are: — Within an ISR of the same or higher interrupt priority, if you are sure that an interrupt of the same priority will not occur. — During background processing, but only when you are sure that no interrupt will occur, such as during the time before the interrupt source is initialized.

2 Stack Extension Definition

Area to Change	Change Description
Section 4.3.2, p. 4-5	Replace the first two sentences with the following: The stack extension is in an area in internal memory (extending the hardware stack, thus the name). The stack extension exists in either the X data memory or the Y data memory, as selected by the XYS bit in the Operating Mode Register (OMR) (refer to **Chapter 5**, *Program Control Unit*, for a detailed description of the OMR).

3 Operating Mode Register Bit 11 Definition

Area to Change	Change Description
Table 5-2, p. 5-9	For bit 11, change the row contents to the following:

11	TAS	0	**$\overline{\text{TA}}$ Synchronize Select** Selects the synchronization method for the input Port A pin—$\overline{\text{TA}}$ (Transfer Acknowledge). At operating frequencies ≤ 100 MHz, you can use $\overline{\text{TA}}$ with external synchronization with respect to CLKOUT or asynchronously (which synchronizes the $\overline{\text{TA}}$ signal with the clock internally) depending on the setting of the TAS bit in the Operating Mode Register (OMR). If external synchronous mode is selected (TAS = 0), you are responsible for ensuring that $\overline{\text{TA}}$ transitions occur synchronous to CLKOUT to ensure correct operation. External synchronous operation is not supported above 100 MHz; therefore, when using $\overline{\text{TA}}$ above 100 MHz, the OMR[TAS] bit must be set to synchronize the $\overline{\text{TA}}$ signal internally with the system clock.

4 System Stack Configuration

Area to Change	Change Description
Section 5.4.3, p. 5-19	Two sentences in this section may create confusion about the definition of the system stack. A more complete definition exists on the following page. Therefore, starting on line 4, delete the following two sentences: The system stack is extended in the data memory in a space specified by the stack control registers that monitor system stack accesses. This hardware copies the least recently used (LRU) location of the system stack to data memory if the on-chip hardware stack is full and brings data from data memory when the on-chip hardware stack is empty.

5 PLL and Clock Generator

Area to Change	Change Description
Chapter 6, p. 6-1	Add the following note after the chapter heading: **Note:** The DSP56321 device uses a digital phase-lock loop (DPLL) and a different clock module than other members of the DSP56300 family. Refer to **Chapter 5** of the *DSP56321 Reference Manual*.

6 Voltage Controlled Oscillator (VCO)

Area to Change	Change Description
Section 6.2.3, p. 6-3	Replace all the text in the section with the following: The Voltage Controlled Oscillator (VCO) operates at frequencies from 30 MHz to twice the maximum device operating frequency. The minimum frequency is required to ensure VCO stability. See **Table 2-6** in the device-specific *Technical Data* sheet for the maximum frequency for each device. Also refer to **Table 2-5** in the same *Technical Data* sheet for the external clock signal characteristics. **Note:** When the PLL is enabled, the maximum device operating frequency is half the VCO frequency. Because the reset value of all clock dividers and multiplier is 1, if EXTAL is less than 30 MHz, the VCO cannot operate correctly during reset and the PLL must be disabled. For such cases, the hardware design must hold the PINIT input low during reset to disable the PLL. After reset, the software can change the pre-divider (PD) and MF to the desired values (ensuring that the input to the VCO is not less than 30 MHz) and then set the PCTL[PEN] bit to enable the PLL. **Note:** The DSP56321 has a DPLL clock circuit that is different from the rest of the DSP56300 family. Its VCO operates differently from this description. Refer to **Section 5.5** in the *DSP56321 Reference Manual*.

7 Design Guidelines for Ripple and PCAP

Area to Change	Change Description
Figure 6-3, p. 6-11	At the top of the figure, change V_{CC} = 5 V to V_{CC}. **Note:** More recent versions of DSP56300 devices use lower voltage levels for V_{CC}.

8 External Memory Interface (Port A)

Area to Change	Change Description
Table 9-2, p. 9-2	Change the title for the third column to **State During Reset**[1,2]. Add notes that state: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated internally. However, some DSP56300 devices have internal keeper circuits that maintain last output level even when the internal drivers are tri-stated. Refer to the specific device technical data sheet, user's manual, or reference manual for details. **2.** The Wait processing state does not affect the signal state.
Table 9-3, p. 9-2	Change the title of the third column to **State During Reset, Stop, or Wait**. Change the first row of the table to the following:

AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the OMR, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals. Unlike address lines, these lines are deasserted between external accesses. See **Section 9.6.1** *Address Attribute Registers (AAR[0–3])* for details. **Row Address Strobe**—When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for the DRAM interface. These signals are tri-statable outputs with programmable polarity. **Note:** DRAM access is not supported above 100 MHz. Also, the DSP56321 does not support DRAM at any frequency.
$\overline{\text{RAS}}$[0–3]	Output		

Area to Change **Change Description**

Table 9-3, p. 9-3 Change the $\overline{TA}$ signal row to the following:

$\overline{TA}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56300 device is the bus master and there is no external bus activity, or the device is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, asserted to enable completion of the bus cycle, and deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is deasserted. The number of wait states is determined by the $\overline{TA}$ input or by the BCR, whichever is longer. The BCR sets the minimum number of wait states in external bus cycles. In order to use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{TA}$ deassertion. At operating frequencies ≤ 100 MHz, $\overline{TA}$ can operate synchronously (with respect to CLKOUT) or asynchronously depending on the setting of the TAS bit in the Operating Mode Register (OMR). If synchronous mode is selected, the user is responsible for ensuring that $\overline{TA}$ transitions occur synchronous to CLKOUT to ensure correct operation. Synchronous operation is not supported above 100 MHz and the OMR[TAS] bit must be set to synchronize the $\overline{TA}$ signal with the internal clock. **Note:** Do not use $\overline{TA}$ while performing DRAM accesses; otherwise, improper operation may result. Also, when the DSP56300 device is the bus master, but $\overline{TA}$ is not used for external bus control, $\overline{TA}$ must be pulled down (asserted).

Area to Change **Change Description**

Table 9-3, p. 9-3 Change the $\overline{BR}$ signal row to the following:

$\overline{BR}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BCR[BRH] bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56300 family device is a bus master or not. Bus “parking” allows bus access without asserting $\overline{BR}$ (see the descriptions of bus “parking” in **Section 9.5.3.4** and **Section 9.5.3.6**). The Bus Request Hold (BRH) bit in the Bus Control Register (BCR) allows $\overline{BR}$ to be asserted under software control, even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbiter that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted; arbitration is reset to the bus slave state.

Area to Change **Change Description**

Table 9-3, p. 9-4 Change $\overline{BB}$ signal row to the following:

$\overline{BB}$	Input/ Output	Ignored input	**Bus Busy**—Indicates that the bus is active. $\overline{BB}$ must be asserted and deasserted synchronous to CLKOUT. Only after $\overline{BB}$ is deasserted can a pending bus master become the bus master (and assert $\overline{BB}$). Some designs allow a bus master to keep $\overline{BB}$ asserted after ceasing bus activity. This is called “bus parking” and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus (see **Section 9.5.3.4** and **Section 9.5.3.6**). Deassertion of $\overline{BB}$ uses an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). **Note:** $\overline{BB}$ requires an external pull-up resistor.

Area to Change	Change Description
Table 9-3, pp. 9-4	Change the $\overline{\text{CAS}}$ signal row to the following:

$\overline{\text{CAS}}$	Output	Tri-stated	**Column Address Strobe**—When the DSP is the bus master, $\overline{\text{CAS}}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated. **Note:** DRAM access is not supported above 100 MHz. Also, the DSP56321 does not support DRAM at any frequency.

Area to Change	Change Description
Table 9-3, pp. 9-4 to 9-5	Change the last two rows in the table to the following:

BCLK	Output	Tri-stated	**Bus Clock** When the DSP is the bus master, BCLK is active when the ATE bit in the Operating Mode Register is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle. You can use the rising edge of BCLK to sample the address lines to determine where an internal Program memory access is occurring. **Note:** At operating frequencies above 100 MHz, this signal produces a low-amplitude waveform that is not usable externally by other devices. Also, the DSP56321 does not support BCLK at any frequency.
$\overline{\text{BCLK}}$	Output	Tri-stated	**Bus Clock Not** When the DSP is the bus master, $\overline{\text{BCLK}}$ is the inverse of the BCLK signal. Otherwise, the signal is tri-stated. **Note:** At operating frequencies above 100 MHz, this signal produces a low-amplitude waveform that is not usable externally by other devices. Also, the DSP56321 does not support $\overline{\text{BCLK}}$ at any frequency.

9 DRAM Support

Area to Change	Change Description
Section 9.2.3, p. 9-8	After the section heading, add the following note: **Note:** DSP56300 devices do not support the DRAM interface above 100 MHz. The DSP56321 does not support DRAM at any frequency.

10 Bus Control Register

Area to Change	Change Description
Table 9-5, p. 9-19	After the description for bit 22 (BLH), add the following note: **Note:** This bit is not supported by all DSP56300 devices.
Table 9-5, p. 9-19 to 9-20	After the descriptions for bits 20–16 (BDFW), bits 15–13 (BA3W), bits 12–10 (BA2W), bits 9–5 (BA1W), and bits 4–0 (BA0W) add the following note: **Note:** For the DSP56321 device, when three through seven wait states are selected, one additional wait state is inserted at the end of the access.

11 DRAM Control Register

Area to Change	Change Description
Section 9.6.3, p. 9-21	After the section heading, add the following note: **Note:** DSP56300 devices do not support the DRAM interface above 100 MHz. The DSP56321 does not support DRAM at any frequency.

12 DMA End-of-Block Transfer

Area to Change	Change Description
Section 10.4.1.2, p. 10-9 to 10-10	Replace the last sentence in the section with the following: When operating in a mode in which DE is not cleared at the end of the block transfer (that is, if DTM = 100 or 101), the DMA end-of-block transfer interrupt may not be latched when the bus grant ($\overline{BG}$) signal is asserted by the external bus arbiter. This causes the end-of-block interrupt to be lost.
Table 10-5, p. 1-17	Delete the notes at the end of the descriptions for DTM = 100 and 101 in the table that state: "The DMA End-of-Block-Transfer Interrupt cannot be used in this mode."

13 INSERT Instruction Example

Area to Change	Change Description
Chapter 13, p. 13-79	For the X0 register (shown just below the middle of the page), change 47 to 23 and 24 to 0. The correct range for the register is bits 23–0.

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