

FX060 Frequency Translator



Features

- 19.44 MHz and 155.52 MHz Clock Outputs Locked to an 8 kHz or 1.544 MHz Input Clock
- Commercial or Industrial Temperature Range
- Surface Mount Option Available
- Single 5.0 Vdc Supply
- AC/HCMOS Compatible Inputs and Outputs
- Lock Detect Circuit
- <10 ps rms Output Jitter at 19.44 MHz
- 19 ps rms Typical Output Jitter at 155.52 MHz
- ±70 ppm Input Frequency Tolerance

Applications

- Clock Frequency Translation
- SONET/SDH/ATM
- Clock Distribution

Description

Vectron s FX060 frequency translator is a low noise, narrow band PLL that generates 155.52 MHz and 19.44 MHz output clocks locked to an input 8 kHz or 1.544 MHz reference clock. The 19.44 MHz clock is generated by a low noise VCXO. The 155.52 MHz signal is a multiplied representation of the 19.44 MHz output.

Lock Detect 8 kHz User Input 19.44 MHz Phase Loop 19.44 MHz connection Detector Filter VCXO Output when 1.544 MHz Frequency 155.52 MHz input is Frequency Multiplier Output used 8 kHz Divider Output Frequency 1.544 MHz Divider Input

*This Bulletin is provided for informational purposes to enable early engineering discussions.

It should not be assumed that the product described in this document is qualified or available for manufacture.

Block Diagram

FX060 Frequency Translator

Performance Characteristics

Table 1. Performance Characteristics							
Parameter	Symbol	Minimum	Typical	Maximum	Units		
Supply Voltage	Vdd	4.75	5.0	5.25	V		
Supply Current	lod	-	60	100	mA		
Input Signal	CLKIN		AC/HCMOS		-		
Output Load	CLKOUT	AC/HCMOS		-			
Output Symmetry	DC	45	50	55	%		
19.44 MHz Output Clock Edge Jitter	J 19.44	-	-	10	ps rms		
155.52 MHz Output Clock Jitter	J 155.52	-	19	-	ps rms		
Rise/Fall Time of 19.44 MHz Output	TR/F	-	-	7	ns		
Rise/Fall Time of 155.52 MHz Output	TR/F	-	-	2	ns		
Input Frequency Tolerance	-	-70	-	+70	ppm		
Output Frequency Stability		Tracks reference stability when locked					





Table 2. Pin Function					
Pin	Symbol	Function			
1	OUT19	19.44 MHz Clock Output			
3	OUT155	155.52 MHz Clock Output			
10	LOCK	Lock Detect Output. Lock indicated by Logic High. When not locked output toggles at a rate proportional to the phase difference between the input clock and the internal crystal oscillator			
14	OUT8	8 kHz Clock Output from 1.544 MHz reference clock			
15	IN8	8 kHz Reference Clock Input.			
22	IN1.5	1.544 MHz Reference Clock Input*			
24	VDD	5 Vdc ±5% Supply			
2,6,12,19	GND	Case Ground			
4,5,7,8,9, 11,13,16, 17,18,20, 21,23	N/C	No User Connection			

* Note: For 1.544 MHz input reference, tie pins 14 and 15 together and use pin 22 input

Handing Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.

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