# DRAM MODULE

# 2 MEG x 64

16 MEGABYTE, 3.3V, FAST PAGE OR EDO PAGE MODE

## FEATURES

- JEDEC- and industry-standard pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 8mW standby; 1,600mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms or
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V-tolerant inputs and I/Os (5.5V maximum $V_{IH}$ level)

## OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - 168-pin DIMM (gold) — G

## KEY TIMING PARAMETERS

EDO Operating Mode

| SPEED | $t_{RC}$ | $t_{RAC}$ | $t_{PC}$ | $t_{AA}$ | $t_{CAC}$ | $t_{CAS}$ |
|---|---|---|---|---|---|---|
| -6 | 105ns | 60ns | 25ns | 35ns | 20ns | 12ns |
| -7 | 125ns | 70ns | 30ns | 40ns | 25ns | 12ns |

FPM Operating Mode

| SPEED | $t_{RC}$ | $t_{RAC}$ | $t_{PC}$ | $t_{AA}$ | $t_{CAC}$ | $t_{RP}$ |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 35ns | 20ns | 40ns |
| -7 | 130ns | 70ns | 40ns | 40ns | 25ns | 50ns |

## PART NUMBERS

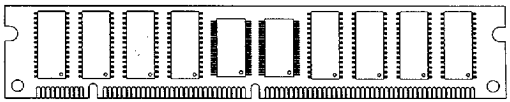
| PART NUMBER | DESCRIPTION |
|---|---|
| MT8LD264G-xx | 2 Meg x 64, FPM |
| MT8LD264G-xx X | 2 Meg x 64, EDO |

xx = speed

## PIN ASSIGNMENT (Front View)

### 168-Pin DIMM

(DE-6) SOJ Version



| PIN # | SYMBOL | PIN # | SYMBOL | PIN # | SYMBOL | PIN # | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 43 | Vss | 85 | Vss | 127 | Vss |
| 2 | DQ0 | 44 | $\overline{OE2}$ | 86 | DQ32 | 128 | RFU |
| 3 | DQ1 | 45 | $\overline{RAS2}$ | 87 | DQ33 | 129 | NC |
| 4 | DQ2 | 46 | $\overline{CAS4}$ | 88 | DQ34 | 130 | $\overline{CAS5}$ |
| 5 | DQ3 | 47 | $\overline{CAS6}$ | 89 | DQ35 | 131 | $\overline{CAS7}$ |
| 6 | Vcc | 48 | $\overline{WE2}$ | 90 | Vcc | 132 | $\overline{PDE}$ |
| 7 | DQ4 | 49 | Vcc | 91 | DQ36 | 133 | Vcc |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | DQ16 | 94 | DQ39 | 136 | DQ48 |
| 11 | NC | 53 | DQ17 | 95 | NC | 137 | DQ49 |
| 12 | Vss | 54 | Vss | 96 | Vss | 138 | Vss |
| 13 | DQ8 | 55 | DQ18 | 97 | DQ40 | 139 | DQ50 |
| 14 | DQ9 | 56 | DQ19 | 98 | DQ41 | 140 | DQ51 |
| 15 | DQ10 | 57 | DQ20 | 99 | DQ42 | 141 | DQ52 |
| 16 | DQ11 | 58 | DQ21 | 100 | DQ43 | 142 | DQ53 |
| 17 | DQ12 | 59 | Vcc | 101 | DQ44 | 143 | Vcc |
| 18 | Vcc | 60 | DQ22 | 102 | Vcc | 144 | DQ54 |
| 19 | DQ13 | 61 | RFU | 103 | DQ45 | 145 | RFU |
| 20 | DQ14 | 62 | RFU | 104 | DQ46 | 146 | RFU |
| 21 | DQ15 | 63 | RFU | 105 | DQ47 | 147 | RFU |
| 22 | NC | 64 | RFU | 106 | NC | 148 | RFU |
| 23 | Vss | 65 | DQ23 | 107 | Vss | 149 | DQ55 |
| 24 | NC | 66 | NC | 108 | NC | 150 | NC |
| 25 | NC | 67 | DQ24 | 109 | NC | 151 | DQ56 |
| 26 | Vcc | 68 | Vss | 110 | Vcc | 152 | Vss |
| 27 | $\overline{WE0}$ | 69 | DQ25 | 111 | RFU | 153 | DQ57 |
| 28 | $\overline{CAS0}$ | 70 | DQ26 | 112 | $\overline{CAS1}$ | 154 | DQ58 |
| 29 | $\overline{CAS2}$ | 71 | DQ27 | 113 | $\overline{CAS3}$ | 155 | DQ59 |
| 30 | $\overline{RAS0}$ | 72 | DQ28 | 114 | NC | 156 | DQ60 |
| 31 | $\overline{OE0}$ | 73 | Vcc | 115 | RFU | 157 | Vcc |
| 32 | Vss | 74 | DQ29 | 116 | Vss | 158 | DQ61 |
| 33 | A0 | 75 | DQ30 | 117 | A1 | 159 | DQ62 |
| 34 | A2 | 76 | DQ31 | 118 | A3 | 160 | DQ63 |
| 35 | A4 | 77 | NC | 119 | A5 | 161 | NC |
| 36 | A6 | 78 | Vss | 120 | A7 | 162 | Vss |
| 37 | A8 | 79 | PD1 | 121 | A9 | 163 | PD2 |
| 38 | A10 | 80 | PD3 | 122 | NC | 164 | PD4 |
| 39 | NC | 81 | PD5 | 123 | NC | 165 | PD6 |
| 40 | Vcc | 82 | PD7 | 124 | Vcc | 166 | PD8 |
| 41 | RFU | 83 | ID0 | 125 | RFU | 167 | ID1 |
| 42 | RFU | 84 | Vcc | 126 | B0 | 168 | Vcc |

## GENERAL DESCRIPTION

The MT8LD264(X) is a randomly accessed solid-state memory containing 2,097,152 words organized in a x64 configuration. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 21 address bits. The address is entered first by $\overline{RAS}$ latching 11 bits and then $\overline{CAS}$ latching 10 bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An EARLY WRITE occurs when $\overline{WE}$ is taken LOW prior to $\overline{CAS}$ falling. A LATE WRITE or READ-MODIFY-WRITE occurs when $\overline{WE}$ falls after $\overline{CAS}$ was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of $\overline{OE}$. During LATE WRITE or READ-MODIFY-WRITE cycles, $\overline{OE}$ must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping $\overline{OE}$ LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

## FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

## EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time ($^{t}$CP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

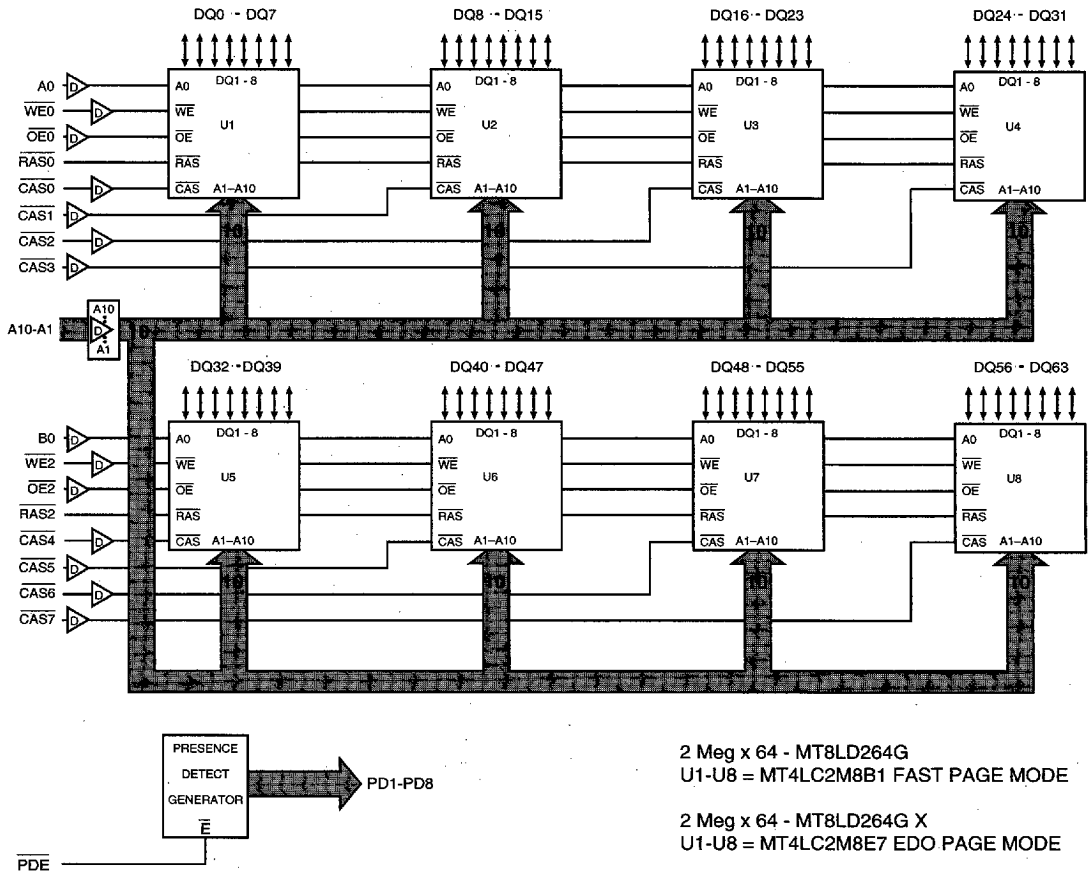
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after $^{t}$OFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last (reference the MT4LC2M8E7 DRAM data sheet for additional information on EDO functionality).

## REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle, and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Correct memory cell data is preserved by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

## FUNCTIONAL BLOCK DIAGRAM




2 Meg x 64 - MT8LD264G
U1-U8 = MT4LC2M8B1 FAST PAGE MODE

2 Meg x 64 - MT8LD264G X
U1-U8 = MT4LC2M8E7 EDO PAGE MODE

**NOTE:** 1. All inputs with the exception of $\overline{RAS}$ are redriven.
2. D = line buffers.

DRAM DIMM

## PIN DESCRIPTIONS

| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 30, 45 | $\overline{RAS0}$, $\overline{RAS2}$ | Input | Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks. |
| 28, 29, 46, 47, 112, 113, 130, 131 | $\overline{CAS0}$-7 | Buffered Input | Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration. |
| 27, 48 | $\overline{WE0}$, $\overline{WE2}$ | Buffered Input | Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle. |
| 31, 44 | $\overline{OE0}$, $\overline{OE2}$ | Buffered Input | Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles. |
| 33-38, 117-121, 126 | A0-A10, B0 | Buffered Input | Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63. |
| 2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160 | DQ0-DQ63 | Input/ Output | Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location. |
| 79-82, 163-166 | PD1-PD8 | Buffered Output | Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to $V_{OH}$ (1) or they will be driven to $V_{OL}$ (0). |
| 41-42, 61-64, 111, 115, 125, 128, 145-148 | RFU | — | RFU: These pins should be left unconnected (reserved for future use). |
| 6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168 | $V_{CC}$ | Supply | Power Supply: +3.3V ± 0.3V |
| 1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152,162 | $V_{SS}$ | Supply | Ground |

## PIN DESCRIPTIONS (continued)

| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 83, 167 | ID0, ID1 | Output | ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss). |
| 132 | $\overline{PDE}$ | Input | Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins. |
| 11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150,161 | NC | — | No connect. |

## TRUTH TABLE

| FUNCTION | | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{PDE}$ | ADDRESSES $^tR$ | ADDRESSES $^tC$ | DATA-IN/OUT DQ0-63 |
|---|---|---|---|---|---|---|---|---|---|
| Standby | | H | H→X | X | X | X | X | X | High-Z |
| READ | | L | L | H | L | X | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | X | X | ROW | COL | Data-In |
| READ WRITE | | L | L | H→L | L→H | X | ROW | COL | Data-Out, Data-In |
| EDO/FAST-PAGE-MODE READ | 1st Cycle | L | H→L | H | L | X | ROW | COL | Data-Out |
| | 2nd Cycle | L | H→L | H | L | X | n/a | COL | Data-Out |
| | Any Cycle (X version) | L | L→H | H | L | X | n/a | n/a | Data-Out |
| EDO/FAST-PAGE-MODE EARLY-WRITE | 1st Cycle | L | H→L | L | X | X | ROW | COL | Data-In |
| | 2nd Cycle | L | H→L | L | X | X | n/a | COL | Data-In |
| EDO/FAST-PAGE-MODE READ-WRITE | 1st Cycle | L | H→L | H→L | L→H | X | ROW | COL | Data-Out, Data-In |
| | 2nd Cycle | L | H→L | H→L | L→H | X | n/a | COL | Data-Out, Data-In |
| $\overline{RAS}$-ONLY REFRESH | | H | X | X | X | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | L | X | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | X | X | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | X | X | High-Z |
| READ PRESENCE-DETECTS | | X | X | X | X | L | X | X | Not Affected |

## PRESENCE-DETECT TRUTH TABLE

| CHARACTERISTICS | | | | | PRESENCE-DETECT PIN (PDx) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Module Density | Module Organization | Row/Column Addresses | ID0 | ID1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0MB | No module installed | X | | | 1 | 1 | 1 | 1 | | | | |
| 8MB | 1 Meg x 64/72 | 10/9 | | | 1 | 1 | 0 | 0 | | | | |
| 8MB | 1 Meg x 64/72 | 10/10 | | | 0 | 0 | 1 | 0 | | | | |
| 16MB | 2 Meg x 64/72 | 10/10 | | | 1 | 0 | 1 | 0 | | | | |
| • 16MB | 2 Meg x 64/72 | 11/10 | | | 1 | 0 | 0 | 1 | | | | |
| 32MB | 4 Meg x 64/72 | 11/10 | | | 0 | 1 | 0 | 1 | | | | |
| 32MB | 4 Meg x 64/72 | 12*/11* | | | 1 | 1 | 0 | 1 | | | | |
| 64MB | 8 Meg x 64/72 | 12/10 | | | 0 | 0 | 1 | 0 | | | | |
| Page Mode | | Fast Page Mode | | | | | | | 0 | | | |
| | | EDO Page Mode | | | | | | | 1 | | | |
| Access Timing | | 70ns | | | | | | | | 0 | 1 | |
| | | 60ns | | | | | | | | 1 | 1 | |
| | | 50ns | | | | | | | | 0 | 0 | |
| Refresh Control | | Standard | | Vss | | | | | | | | |
| Data Width, Parity | | x64, No Parity | Vss | | | | | | | | | 1 |
| | | x72, ECC | Vss | | | | | | | | | 0 |

**NOTE:** Vss = ground; 0 = $V_{OL}$; 1 = $V_{OH}$.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ Pin Relative to $V_{SS}$ ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to $V_{SS}$ ..... -1V to +5.5V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation ..... 8W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) ($V_{CC}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | 3.0 | 3.6 | V | |
| Input High (Logic 1) Voltage, all inputs | | $V_{IH}$ | 2.0 | 5.5 | V | |
| Input Low (Logic 0) Voltage, all inputs | | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ 5.5V<br>(All other pins not under test = 0V) | $\overline{CAS0}$ - $\overline{CAS7}$<br>A0-A10, B0, $\overline{PDE}$<br>$\overline{WE0,2}$, $\overline{OE0,2}$ | $I_{I1}$ | -2 | 2 | µA | |
| | $\overline{RAS0,2}$ | $I_{I2}$ | -8 | 8 | µA | |
| OUTPUT LEAKAGE CURRENT<br>(Q is disabled; 0V ≤ $V_{OUT}$ ≤ 5.5V) | DQ0 - DQ63<br>PD1-PD8 | $I_{OZ}$ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -2mA) | | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 2mA) | | $V_{OL}$ | | 0.4 | V | |

| PARAMETER/CONDITION | SYMBOL | SIZE | MAX -6 | MAX -7 | UNITS | NOTES |
|---|---|---|---|---|---|---|
| STANDBY CURRENT: (TTL)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | $I_{CC1}$ | 16MB | 16 | 16 | mA | 26 |
| STANDBY CURRENT: (CMOS)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ -0.2V) | $I_{CC2}$ | 16MB | 4 | 4 | mA | 26 |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | 16MB | 1,040 | 960 | mA | 3, 26, 29 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, address cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC4}$ | 16MB | 720 | 640 | mA | 3, 26, 29 |
| OPERATING CURRENT: EDO PAGE MODE (X version only)<br>Average power supply current<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, address cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC5}$<br>(X only) | 16MB | 960 | 880 | mA | 3, 26, 29 |
| REFRESH CURRENT: $\overline{RAS}$ ONLY<br>Average power supply current<br>($\overline{RAS}$ cycling, $\overline{CAS}$ = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | 16MB | 1,040 | 960 | mA | 3, 26, 30 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC7}$ | 16MB | 1,040 | 960 | mA | 3, 4, 26 |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A10, B0, $\overline{PDE}$ | $C_{I1}$ | | 9 | pF | 2 |
| Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$ | $C_{I2}$ | | 9 | pF | 2 |
| Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$ | $C_{I3}$ | | 40 | pF | 2 |
| Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$ | $C_{I4}$ | | 9 | pF | 2 |
| Input/Output Capacitance: DQ0 - DQ63 | $C_{IO}$ | | 10 | pF | 2 |
| Output Capacitance: PD1-PD8 | $C_O$ | | 10 | pF | 2 |

## FAST PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +3.3V ±0.3V)

DRAM DIMM

| AC CHARACTERISTICS - FAST PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column-address | $^tAA$ | | 35 | | 40 | ns | 23 |
| Column-address hold time (referenced to $\overline{RAS}$) | $^tAR$ | 48 | | 53 | | ns | 22 |
| Column-address setup time | $^tASC$ | 2 | | 2 | | ns | 21 |
| Row-address setup time | $^tASR$ | 5 | | 5 | | ns | 23 |
| Column-address to $\overline{WE}$ delay time | $^tAWD$ | 57 | | 62 | | ns | 21, 28 |
| Access time from $\overline{CAS}$ | $^tCAC$ | | 20 | | 25 | ns | 14, 23 |
| Column-address hold time | $^tCAH$ | 15 | | 20 | | ns | 23 |
| $\overline{CAS}$ pulse width | $^tCAS$ | 15 | 10,000 | 20 | 10,000 | ns | |
| $\overline{CAS}$ hold time (CBR REFRESH) | $^tCHR$ | 13 | | 13 | | ns | 4, 22 |
| $\overline{CAS}$ to output in Low-Z | $^tCLZ$ | 5 | | 5 | | ns | 21, 30 |
| $\overline{CAS}$ precharge time | $^tCP$ | 10 | | 10 | | ns | 15 |
| Access time from $\overline{CAS}$ precharge | $^tCPA$ | | 40 | | 45 | ns | 23 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $^tCRP$ | 10 | | 10 | | ns | 23 |
| $\overline{CAS}$ hold time | $^tCSH$ | 58 | | 68 | | ns | 22 |
| $\overline{CAS}$ setup time (CBR REFRESH) | $^tCSR$ | 7 | | 7 | | ns | 4, 21 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $^tCWD$ | 42 | | 47 | | ns | 21, 28 |
| Write command to $\overline{CAS}$ lead time | $^tCWL$ | 15 | | 20 | | ns | |
| Data-in hold time | $^tDH$ | 15 | | 20 | | ns | 23, 27 |
| Data-in hold time (referenced to $\overline{RAS}$) | $^tDHR$ | 45 | | 55 | | ns | |
| Data-in setup time | $^tDS$ | -2 | | -2 | | ns | 22, 27 |
| Output disable | $^tOD$ | 3 | 15 | 3 | 20 | ns | 30 |
| Output enable | $^tOE$ | | 15 | | 20 | ns | |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | $^tOEH$ | 13 | | 13 | | ns | 22 |

## FAST PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS - FAST PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Output buffer turn-off delay | $^tOFF$ | 5 | 20 | 5 | 25 | ns | 19, 25, 33 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | $^tORD$ | 0 | | 0 | | ns | 19 |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 35 | | 40 | | ns | |
| $\overline{PDE}$ to valid presence-detect data | $^tPD$ | | 10 | | 10 | ns | 32 |
| $\overline{PDE}$ inactive to presence-detects inactive | $^tPDOFF$ | 2 | | 2 | | ns | 31 |
| FAST-PAGE-MODE READ-WRITE cycle time | $^tPRWC$ | 87 | | 97 | | ns | 21 |
| Access time from $\overline{RAS}$ | $^tRAC$ | | 60 | | 70 | ns | 13 |
| $\overline{RAS}$ to column-address delay time | $^tRAD$ | 13 | 25 | 13 | 30 | ns | 17, 24 |
| Row-address hold time | $^tRAH$ | 8 | | 8 | | ns | 22 |
| Column-address to $\overline{RAS}$ lead time | $^tRAL$ | 35 | | 40 | | ns | 23 |
| $\overline{RAS}$ pulse width | $^tRAS$ | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{RAS}$ pulse width (FAST PAGE MODE) | $^tRASP$ | 60 | 100,000 | 70 | 100,000 | ns | |
| Random READ or WRITE cycle time | $^tRC$ | 110 | | 130 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $^tRCD$ | 18 | 40 | 18 | 45 | ns | 16, 24 |
| Read command hold time (referenced to $\overline{CAS}$) | $^tRCH$ | 2 | | 2 | | ns | 18, 21 |
| Read command setup time | $^tRCS$ | 2 | | 2 | | ns | 21 |
| Refresh period (2,048 cycles) | $^tREF$ | | 32 | | 32 | ms | |
| $\overline{RAS}$ precharge time | $^tRP$ | 40 | | 50 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $^tRPC$ | 0 | | 0 | | ns | |
| Read command hold time (referenced to $\overline{RAS}$) | $^tRRH$ | 0 | | 0 | | ns | 18 |
| $\overline{RAS}$ hold time | $^tRSH$ | 20 | | 25 | | ns | 23 |
| READ WRITE cycle time | $^tRWC$ | 155 | | 185 | | ns | 23 |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $^tRWD$ | 87 | | 97 | | ns | 21, 28 |
| Write command to $\overline{RAS}$ lead time | $^tRWL$ | 20 | | 25 | | ns | 23 |
| Transition time (rise or fall) | $^tT$ | 3 | 50 | 3 | 50 | ns | |
| Write command hold time | $^tWCH$ | 15 | | 20 | | ns | 23 |
| Write command hold time (referenced to $\overline{RAS}$) | $^tWCR$ | 43 | | 53 | | ns | 22 |
| $\overline{WE}$ command setup time | $^tWCS$ | 2 | | 2 | | ns | 21, 28 |
| Write command pulse width | $^tWP$ | 10 | | 15 | | ns | |
| $\overline{WE}$ hold time (CBR REFRESH) | $^tWRH$ | 8 | | 8 | | ns | 22 |
| $\overline{WE}$ setup time (CBR REFRESH) | $^tWRP$ | 12 | | 12 | | ns | 21 |

## EDO PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

| AC CHARACTERISTICS - EDO PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Access time from column-address | tAA | | 35 | | 40 | ns | 23 |
| Column-address setup to $\overline{CAS}$ precharge during writes | tACH | 15 | | 15 | | ns | |
| Column-address hold time (referenced to $\overline{RAS}$) | tAR | 43 | | 48 | | ns | 22 |
| Column-address setup time | tASC | 2 | | 2 | | ns | 21 |
| Row-address setup time | tASR | 5 | | 5 | | ns | 23 |
| Column-address to $\overline{WE}$ delay time | tAWD | 57 | | 62 | | ns | 21, 28 |
| Access time from $\overline{CAS}$ | tCAC | | 20 | | 25 | ns | 14, 23 |
| Column-address hold time | tCAH | 15 | | 17 | | ns | 23 |
| $\overline{CAS}$ pulse width | tCAS | 12 | 10,000 | 12 | 10,000 | ns | |
| $\overline{CAS}$ hold time (CBR REFRESH) | tCHR | 8 | | 10 | | ns | 4, 22 |
| $\overline{CAS}$ to output in Low-Z | tCLZ | 2 | | 2 | | ns | 21 |
| Data output hold after $\overline{CAS}$ LOW | tCOH | 5 | | 5 | | ns | 21 |
| $\overline{CAS}$ precharge time | tCP | 10 | | 10 | | ns | 15 |
| Access time from $\overline{CAS}$ precharge | tCPA | | 40 | | 45 | ns | 23 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | tCRP | 10 | | 10 | | ns | 23 |
| $\overline{CAS}$ hold time | tCSH | 48 | | 53 | | ns | 22 |
| $\overline{CAS}$ setup time (CBR REFRESH) | tCSR | 7 | | 7 | | ns | 4, 21 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | tCWD | 37 | | 42 | | ns | 21, 28 |
| Write command to $\overline{CAS}$ lead time | tCWL | 15 | | 15 | | ns | |
| Data-in hold time | tDH | 15 | | 17 | | ns | 23, 27 |
| Data-in hold time (referenced to $\overline{RAS}$) | tDHR | 45 | | 55 | | ns | |
| Data-in setup time | tDS | -2 | | -2 | | ns | 22, 27 |
| Output disable | tOD | 0 | 15 | 0 | 15 | ns | |
| Output enable | tOE | | 15 | | 20 | ns | |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | tOEH | 10 | | 10 | | ns | 22 |
| $\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH | tOEHC | 10 | | 10 | | ns | |
| $\overline{OE}$ HIGH pulse width | tOEP | 10 | | 10 | | ns | |
| $\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time | tOES | 5 | | 5 | | ns | |
| Output buffer turn-off delay | tOFF | 5 | 20 | 5 | 20 | ns | 19, 25, 33 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | tORD | 0 | | 0 | | ns | 19 |
| EDO-PAGE-MODE READ or WRITE cycle time | tPC | 25 | | 30 | | ns | |
| $\overline{PDE}$ to valid presence-detect data | tPD | | 10 | | 10 | ns | 32 |
| $\overline{PDE}$ inactive to presence-detects inactive | tPDOFF | 2 | | 2 | | ns | 31 |
| EDO-PAGE-MODE READ-WRITE cycle time | tPRWC | 77 | | 87 | | ns | 21 |
| Access time from $\overline{RAS}$ | tRAC | | 60 | | 70 | ns | 13 |
| $\overline{RAS}$ to column-address delay time | tRAD | 10 | 25 | 10 | 30 | ns | 17, 24 |
| Row-address hold time | tRAH | 8 | | 8 | | ns | 22 |
| Column-address to $\overline{RAS}$ lead time | tRAL | 35 | | 40 | | ns | 23 |
| $\overline{RAS}$ pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{RAS}$ pulse width (EDO PAGE MODE) | tRASP | 60 | 125,000 | 70 | 125,000 | ns | |
| Random READ or WRITE cycle time | tRC | 105 | | 125 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 12 | 40 | 12 | 45 | ns | 16, 24 |
| Read command hold time (referenced to $\overline{CAS}$) | tRCH | 2 | | 2 | | ns | 18, 21 |

## EDO PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

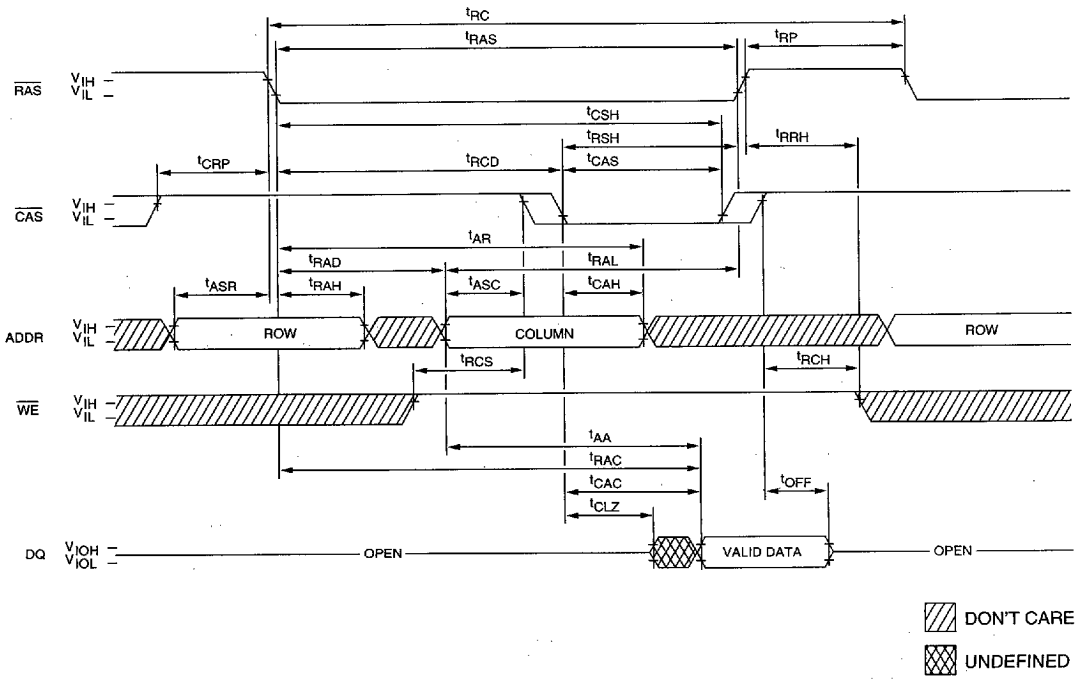
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS - EDO PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Read command setup time | tRCS | 2 | | 2 | | ns | 21 |
| Refresh period (2,048 cycles) | tREF | | 32 | | 32 | ms | |
| $\overline{RAS}$ precharge time | tRP | 40 | | 50 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | tRPC | 5 | | 5 | | ns | |
| Read command hold time (referenced to $\overline{RAS}$) | tRRH | 0 | | 0 | | ns | 18 |
| $\overline{RAS}$ hold time | tRSH | 18 | | 20 | | ns | 23 |
| READ WRITE cycle time | tRWC | 150 | | 175 | | ns | 23 |
| $\overline{RAS}$ to $\overline{WE}$ delay time | tRWD | 82 | | 92 | | ns | 21, 28 |
| Write command to $\overline{RAS}$ lead time | tRWL | 20 | | 20 | | ns | 23 |
| Transition time (rise or fall) | tT | 2 | 50 | 2 | 50 | ns | |
| Write command hold time | tWCH | 15 | | 17 | | ns | 23 |
| Write command hold time (referenced to $\overline{RAS}$) | tWCR | 43 | | 53 | | ns | 22 |
| $\overline{WE}$ command setup time | tWCS | 2 | | 2 | | ns | 21, 28 |
| Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH) | tWHZ | 2 | 18 | 2 | 20 | ns | 25 |
| Write command pulse width | tWP | 10 | | 12 | | ns | |
| $\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH | tWPZ | 10 | | 12 | | ns | |
| $\overline{WE}$ hold time (CBR REFRESH) | tWRH | 8 | | 8 | | ns | 22 |
| $\overline{WE}$ setup time (CBR REFRESH) | tWRP | 12 | | 12 | | ns | 21 |

## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = +3.0V; f = 1 MHz.
3. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $^{t}REF$ refresh requirement is exceeded.
7. AC characteristics assume $^{t}T$ = 5ns for FPM and 2.5ns for EDO.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If $\overline{CAS}$ = $V_{IH}$, data output is High-Z.
11. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V.
13. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If $^{t}RCD$ is greater than the maximum recommended value shown in this table, $^{t}RAC$ will increase by the amount that $^{t}RCD$ exceeds the value shown.
14. Assumes that $^{t}RCD \geq ^{t}RCD$ (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for $^{t}CPN$.
16. Operation within the $^{t}RCD$ (MAX) limit ensures that $^{t}RAC$ (MAX) can be met. $^{t}RCD$ (MAX) is specified as a reference point only; if $^{t}RCD$ is greater than the specified $^{t}RCD$ (MAX) limit, access time is controlled exclusively by $^{t}CAC$.
17. Operation within the $^{t}RAD$ (MAX) limit ensures that $^{t}RAC$ (MIN) can be met. $^{t}RAD$ (MAX) is specified as a reference point only; if $^{t}RAD$ is greater than thespecified $^{t}RAD$ (MAX) limit, access time is controlled exclusively by $^{t}AA$.
18. Either $^{t}RCH$ or $^{t}RRH$ must be satisfied for a READ cycle.
19. $^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
21. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by one-half when used in the x32 mode.
27. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. $^{t}WCS$, $^{t}RWD$, $^{t}AWD$ and $^{t}CWD$ are not restrictive operating parameters. $^{t}WCS$ applies to EARLY WRITE cycles. $^{t}RWD$, $^{t}AWD$ and $^{t}CWD$ apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq ^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq ^{t}RWD$ (MIN), $^{t}AWD \geq ^{t}AWD$ (MIN) and $^{t}CWD \geq ^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. $^{t}WCS$, $^{t}RWD$, $^{t}CWD$ and $^{t}AWD$ are not applicable in a LATE WRITE cycle.
29. Column-address changed once each cycle.
30. The 3ns minimum is a parameter guaranteed by design.
31. $^{t}PDOFF$ MAX is determined by the pullup resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
32. Measured with the specified current load and 100pf.
33. For FAST PAGE MODE option, $^{t}OFF$ is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, $^{t}OFF$ on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
34. Applies to both EDO and FAST PAGE MODEs.

## READ CYCLE
(FAST PAGE MODE Module)

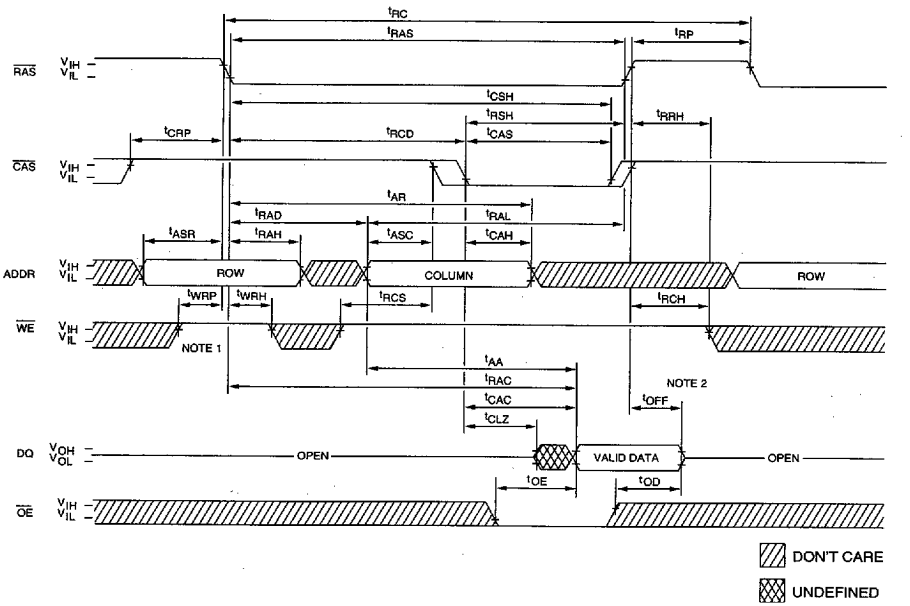



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 5 | | 5 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tOFF | 5 | 20 | 5 | 25 | ns |
| tRAC | | 60 | | 70 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 110 | | 130 | | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRCH | 2 | | 2 | | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 20 | | 25 | | ns |

## READ CYCLE
(EDO PAGE MODE Module)



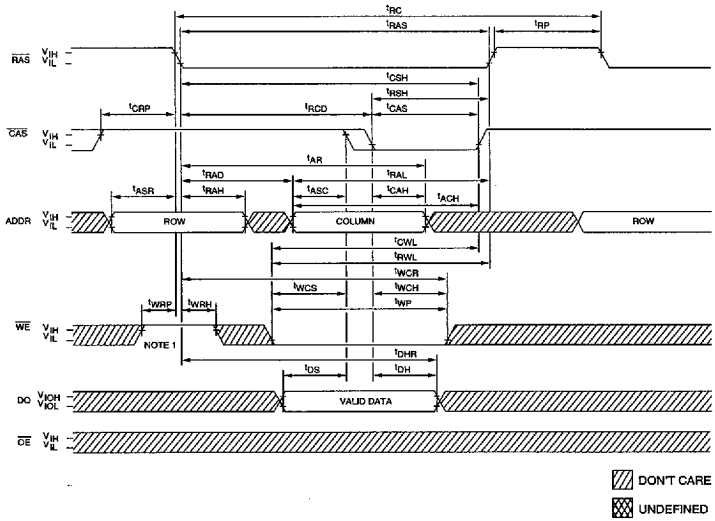

**NOTE:**
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 17 | | ns |
| tCAS | 12 | 10,000 | 12 | 10,000 | ns |
| tCLZ | 2 | | 2 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 48 | | 53 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |
| tOE | | 15 | | 20 | ns |
| tOFF | 5 | 20 | 5 | 20 | ns |
| tRAC | | 60 | | 70 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAD | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 105 | | 125 | | ns |
| tRCD | 12 | 40 | 12 | 45 | ns |
| tRCH | 2 | | 2 | | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 18 | | 20 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## EARLY WRITE CYCLE [34]



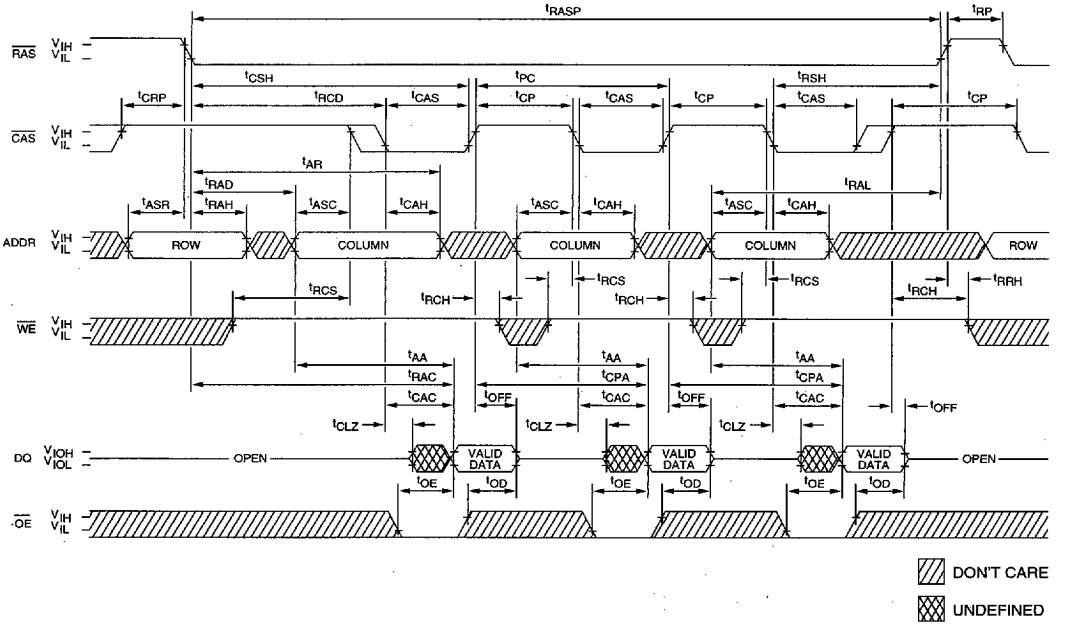

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tACH (EDO) | 15 | | 15 | | ns |
| tAR (FPM) | 48 | | 53 | | ns |
| tAR (EDO) | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAH (FPM) | 15 | | 20 | | ns |
| tCAH (EDO) | 15 | | 17 | | ns |
| tCAS (FPM) | 15 | 10,000 | 20 | 10,000 | ns |
| tCAS (EDO) | 12 | 10,000 | 12 | 10,000 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH (FPM) | 58 | | 68 | | ns |
| tCSH (EDO) | 48 | | 53 | | ns |
| tCWL (FPM) | 15 | | 20 | | ns |
| tCWL (EDO) | 15 | | 15 | | ns |
| tDH (FPM) | 15 | | 20 | | ns |
| tDH (EDO) | 15 | | 17 | | ns |
| tDHR | 45 | | 55 | | ns |
| tDS | -2 | | -2 | | ns |
| tRAD (FPM) | 13 | 25 | 13 | 30 | ns |
| tRAD (EDO) | 10 | 25 | 10 | 30 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC (FPM) | 110 | | 130 | | ns |
| tRC (EDO) | 105 | | 125 | | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH (FPM) | 20 | | 25 | | ns |
| tRSH (EDO) | 18 | | 20 | | ns |
| tRWL (FPM) | 20 | | 25 | | ns |
| tRWL (EDO) | 20 | | 20 | | ns |
| tWCH (FPM) | 15 | | 20 | | ns |
| tWCH (EDO) | 15 | | 17 | | ns |
| tWCR | 43 | | 53 | | ns |
| tWCS | 2 | | 2 | | ns |
| tWP (FPM) | 10 | | 15 | | ns |
| tWP (EDO) | 10 | | 12 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## FAST-PAGE-MODE READ CYCLE



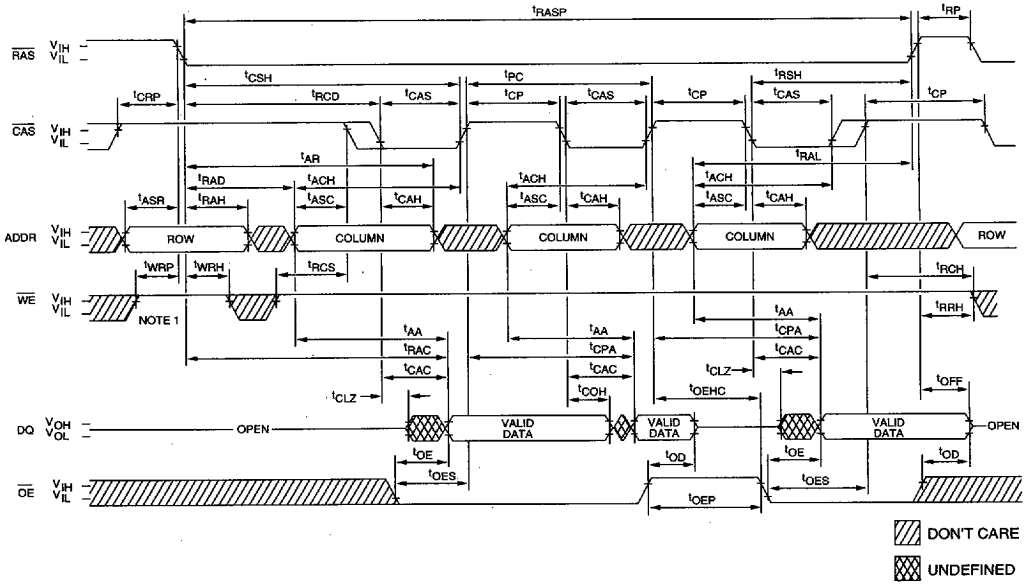

DRAM DIMM

## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 5 | | 5 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 40 | | 45 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOFF | 5 | 20 | 5 | 25 | ns |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRCH | 2 | | 2 | | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 20 | | 25 | | ns |

## EDO-PAGE-MODE READ CYCLE



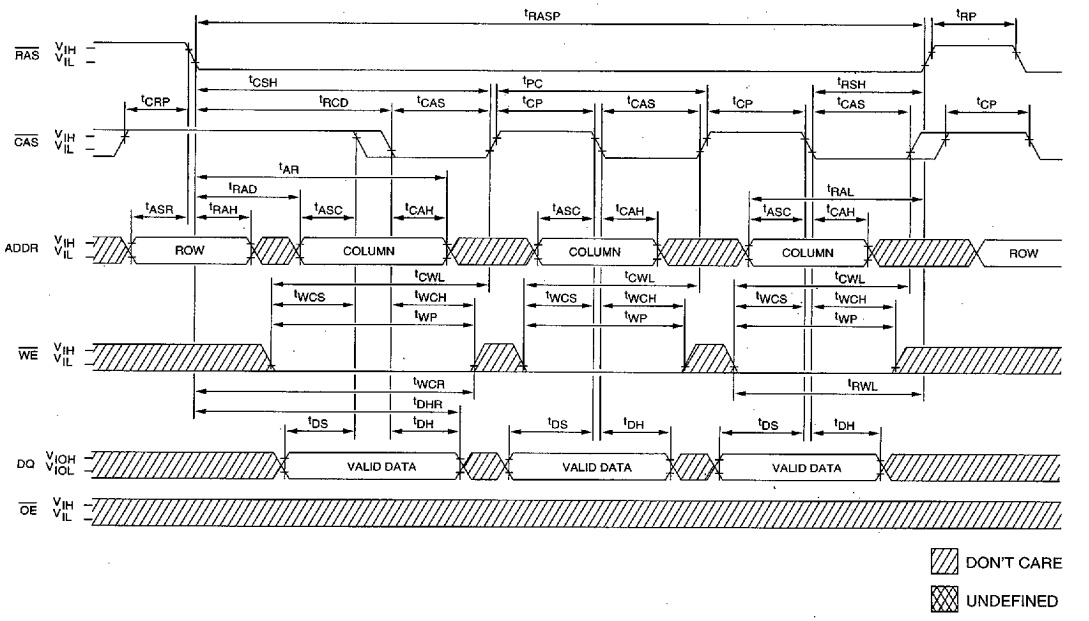

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 17 | | ns |
| tCAS | 12 | 10,000 | 12 | 10,000 | ns |
| tCLZ | 2 | | 2 | | ns |
| tCOH | 5 | | 5 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 40 | | 45 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 48 | | 53 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |
| tOE | | 15 | | 20 | ns |
| tOEHC | 10 | | 10 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOEP | 10 | | 10 | | ns |
| tOES | 5 | | 5 | | ns |
| tOFF | 5 | 20 | 5 | 20 | ns |
| tPC | 25 | | 30 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 12 | 40 | 12 | 45 | ns |
| tRCH | 2 | | 2 | | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 18 | | 20 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## FAST-PAGE-MODE EARLY-WRITE CYCLE

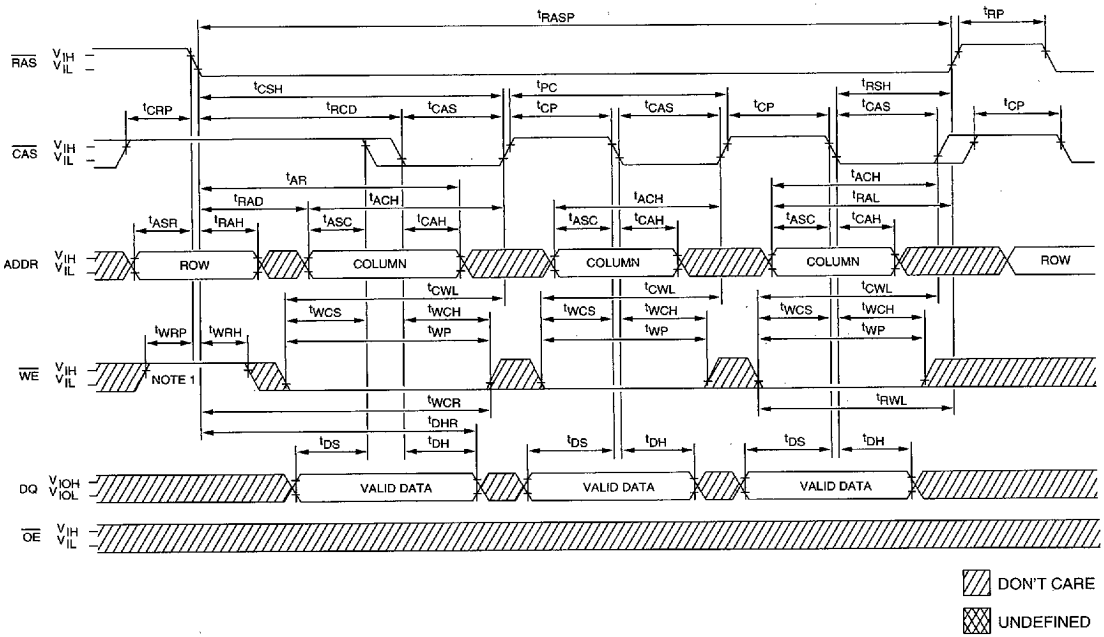



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 15 | | 20 | | ns |
| tDHR | 45 | | 55 | | ns |
| tDS | -2 | | -2 | | ns |
| tPC | 35 | | 40 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 20 | | 25 | | ns |
| tRWL | 20 | | 25 | | ns |
| tWCH | 15 | | 20 | | ns |
| tWCR | 43 | | 53 | | ns |
| tWCS | 2 | | 2 | | ns |
| tWP | 10 | | 15 | | ns |

## EDO-PAGE-MODE EARLY-WRITE CYCLE



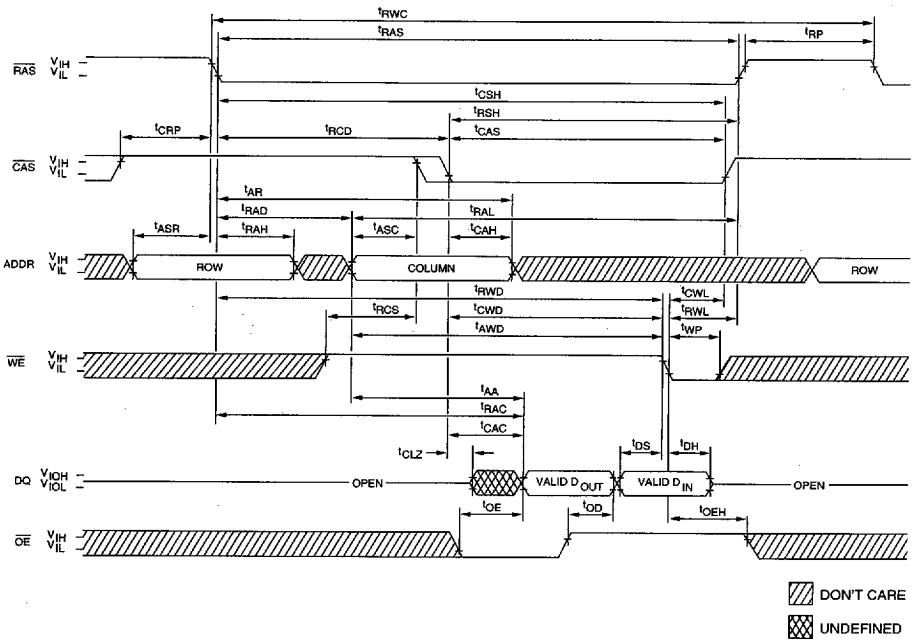

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for $^{t}$WRP and $^{t}$WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ACH | 15 | | 15 | | ns |
| $^{t}$AR | 43 | | 48 | | ns |
| $^{t}$ASC | 2 | | 2 | | ns |
| $^{t}$ASR | 5 | | 5 | | ns |
| $^{t}$CAH | 15 | | 17 | | ns |
| $^{t}$CAS | 12 | 10,000 | 12 | 10,000 | ns |
| $^{t}$CP | 10 | | 10 | | ns |
| $^{t}$CRP | 10 | | 10 | | ns |
| $^{t}$CSH | 48 | | 53 | | ns |
| $^{t}$CWL | 15 | | 15 | | ns |
| $^{t}$DH | 15 | | 17 | | ns |
| $^{t}$DHR | 45 | | 55 | | ns |
| $^{t}$DS | -2 | | -2 | | ns |
| $^{t}$PC | 25 | | 30 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$RAD | 10 | 25 | 10 | 30 | ns |
| $^{t}$RAH | 8 | | 8 | | ns |
| $^{t}$RAL | 35 | | 40 | | ns |
| $^{t}$RASP | 60 | 125,000 | 70 | 125,000 | ns |
| $^{t}$RCD | 12 | 40 | 12 | 45 | ns |
| $^{t}$RP | 40 | | 50 | | ns |
| $^{t}$RSH | 18 | | 20 | | ns |
| $^{t}$RWL | 20 | | 20 | | ns |
| $^{t}$WCH | 15 | | 17 | | ns |
| $^{t}$WCR | 43 | | 53 | | ns |
| $^{t}$WCS | 2 | | 2 | | ns |
| $^{t}$WP | 10 | | 12 | | ns |
| $^{t}$WRH | 8 | | 8 | | ns |
| $^{t}$WRP | 12 | | 12 | | ns |

## READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

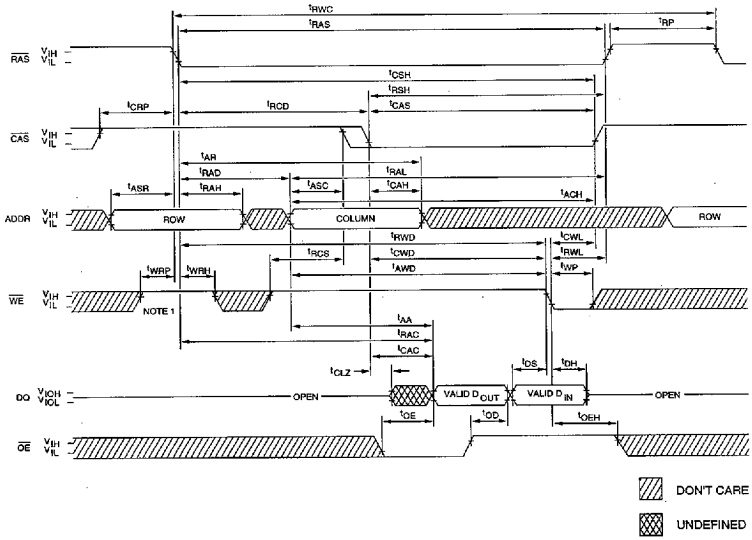



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tAWD | 57 | | 62 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 5 | | 5 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tCWD | 42 | | 47 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 15 | | 20 | | ns |
| tDS | -2 | | -2 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 13 | | 13 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 20 | | 25 | | ns |
| tRWC | 155 | | 185 | | ns |
| tRWD | 87 | | 97 | | ns |
| tRWL | 20 | | 25 | | ns |
| tWP | 10 | | 15 | | ns |

## READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



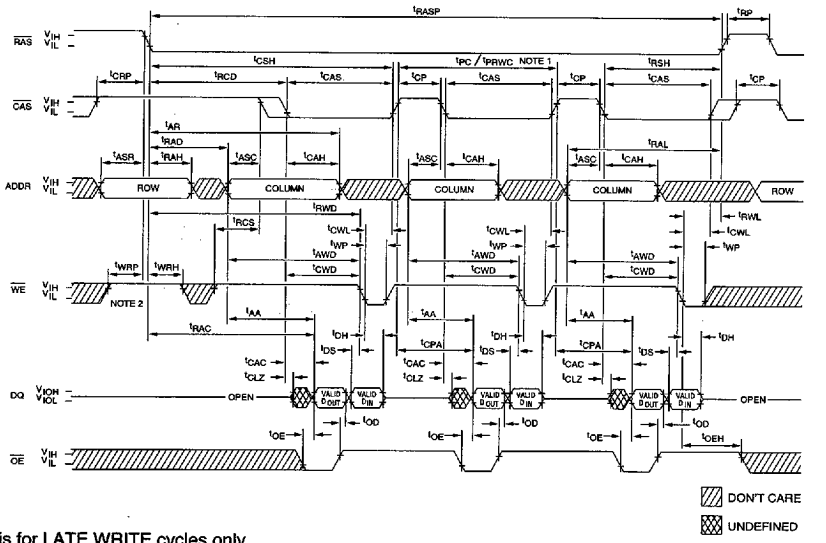

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tAWD | 57 | | 62 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 17 | | ns |
| tCAS | 12 | 10,000 | 12 | 10,000 | ns |
| tCLZ | 2 | | 2 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 48 | | 53 | | ns |
| tCWD | 37 | | 42 | | ns |
| tCWL | 15 | | 15 | | ns |
| tDH | 15 | | 17 | | ns |
| tDS | -2 | | -2 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 10 | | 10 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRCD | 12 | 40 | 12 | 45 | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 18 | | 20 | | ns |
| tRWC | 150 | | 175 | | ns |
| tRWD | 82 | | 92 | | ns |
| tRWL | 20 | | 20 | | ns |
| tWP | 10 | | 12 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



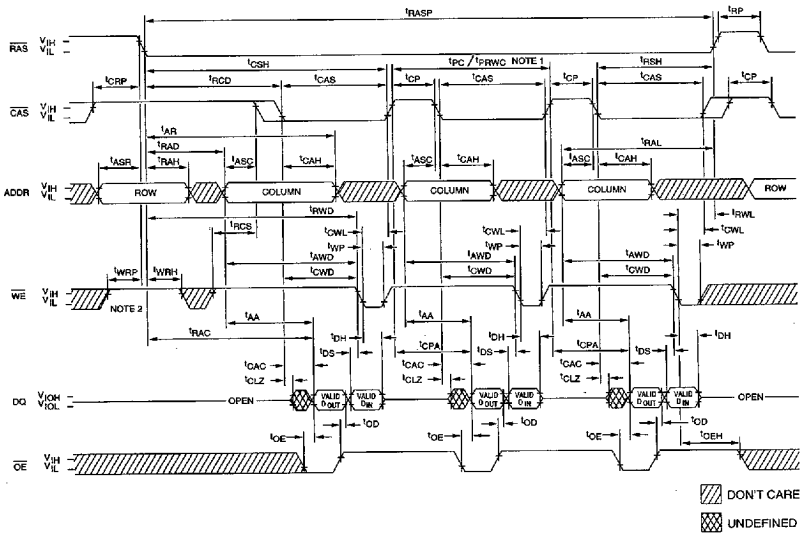

**NOTE:**
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tAWD | 57 | | 62 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 5 | | 5 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 40 | | 45 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tCWD | 42 | | 47 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 15 | | 20 | | ns |
| tDS | -2 | | -2 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 13 | | 13 | | ns |
| tPC | 35 | | 40 | | ns |
| tPRWC | 87 | | 97 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 20 | | 25 | | ns |
| tRWD | 87 | | 97 | | ns |
| tRWL | 20 | | 25 | | ns |
| tWP | 10 | | 15 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



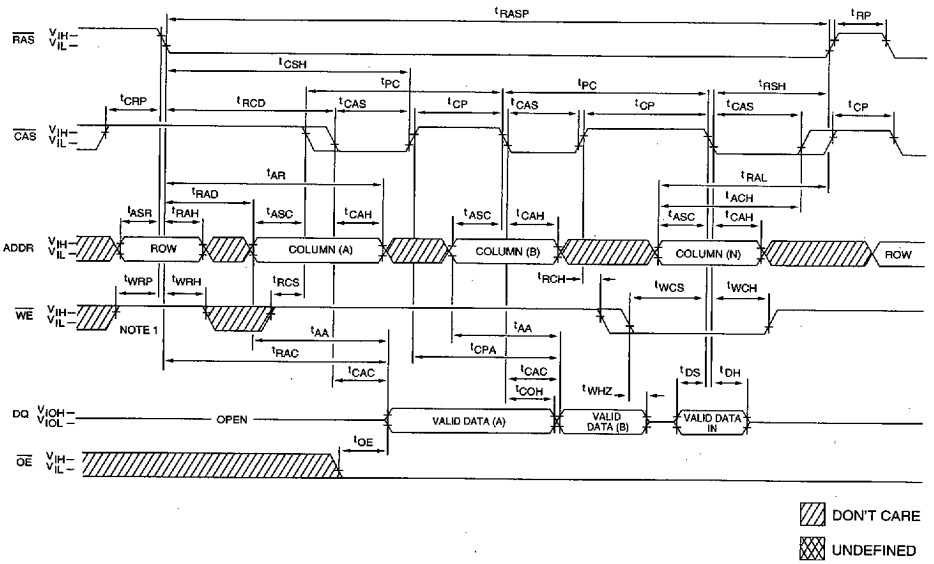

**NOTE:**
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tAWD | 57 | | 62 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 17 | | ns |
| tCAS | 12 | 10,000 | 12 | 10,000 | ns |
| tCLZ | 2 | | 2 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 40 | | 45 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 48 | | 53 | | ns |
| tCWD | 37 | | 42 | | ns |
| tCWL | 15 | | 15 | | ns |
| tDH | 15 | | 17 | | ns |
| tDS | -2 | | -2 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 10 | | 10 | | ns |
| tPC | 25 | | 30 | | ns |
| tPRWC | 77 | | 87 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 12 | 40 | 12 | 45 | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 18 | | 20 | | ns |
| tRWD | 82 | | 92 | | ns |
| tRWL | 20 | | 20 | | ns |
| tWP | 10 | | 12 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



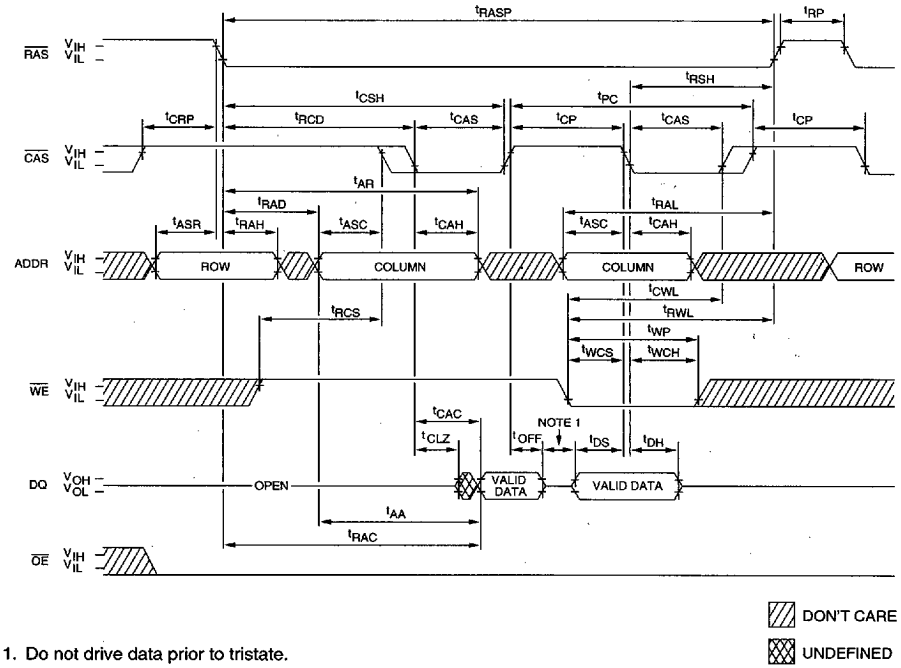

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 17 | | ns |
| tCAS | 12 | 10,000 | 12 | 10,000 | ns |
| tCOH | 5 | | 5 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 40 | | 45 | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 48 | | 53 | | ns |
| tDH | 15 | | 17 | | ns |
| tDS | -2 | | -2 | | ns |
| tOE | | 15 | | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tPC | 25 | | 30 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 12 | 40 | 12 | 45 | ns |
| tRCH | 2 | | 2 | | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 18 | | 20 | | ns |
| tWCH | 15 | | 17 | | ns |
| tWCS | 2 | | 2 | | ns |
| tWHZ | 2 | 18 | 2 | 20 | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



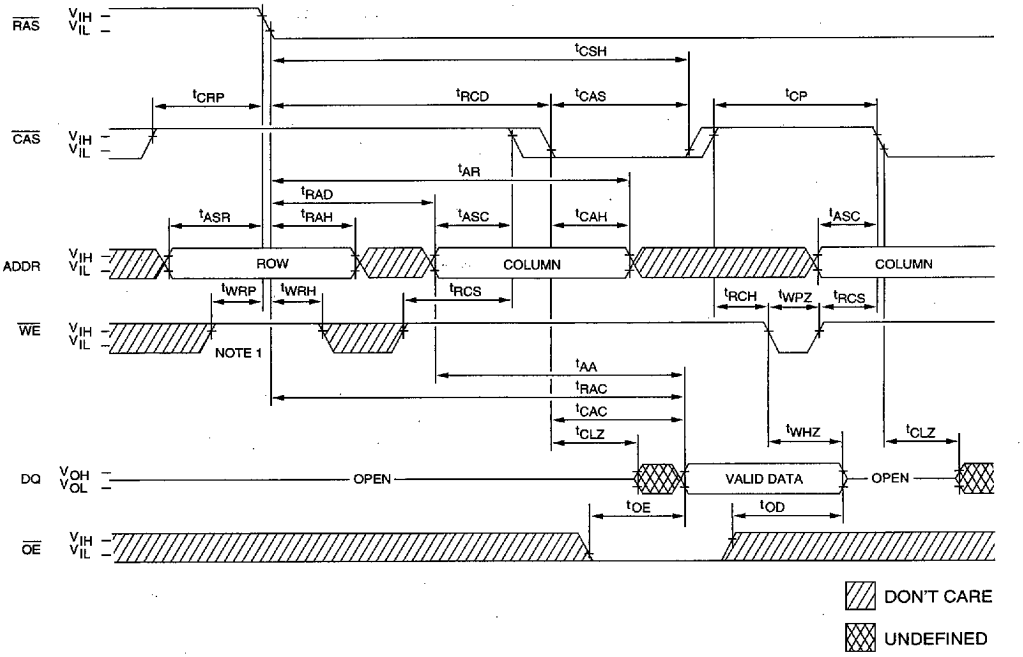

**NOTE:** 1. Do not drive data prior to tristate.

## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tAA | | 35 | | 40 | ns |
| tAR | 48 | | 53 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH | 15 | | 20 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 5 | | 5 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 10 | | 10 | | ns |
| tCSH | 58 | | 68 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 15 | | 20 | | ns |
| tDS | -2 | | -2 | | ns |
| tOFF | 5 | 20 | 5 | 25 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 13 | 25 | 13 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 18 | 40 | 18 | 45 | ns |
| tRCS | 2 | | 2 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 20 | | 25 | | ns |
| tRWL | 20 | | 25 | | ns |
| tWCH | 15 | | 20 | | ns |
| tWCS | 2 | | 2 | | ns |
| tWP | 10 | | 15 | | ns |

## EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



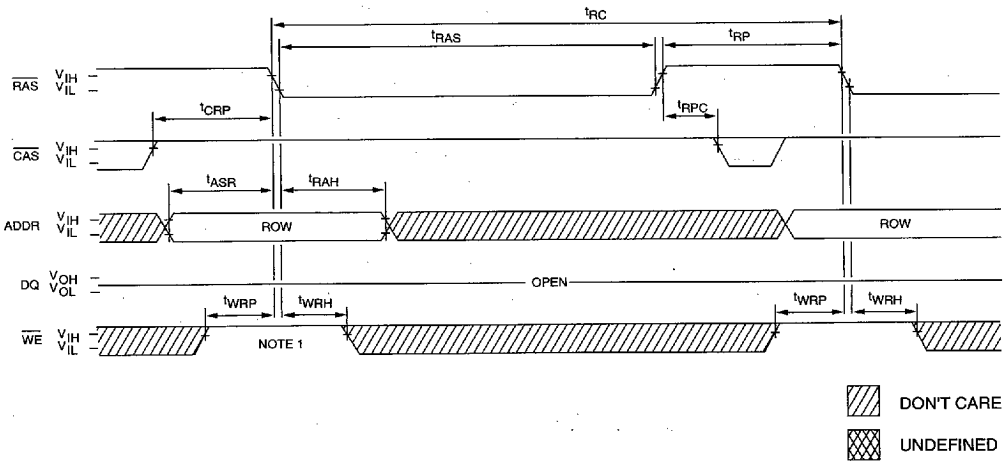

**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for $^{t}$WRP and $^{t}$WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AA | | 35 | | 40 | ns |
| $^{t}$AR | 43 | | 48 | | ns |
| $^{t}$ASC | 2 | | 2 | | ns |
| $^{t}$ASR | 5 | | 5 | | ns |
| $^{t}$CAC | | 20 | | 25 | ns |
| $^{t}$CAH | 15 | | 17 | | ns |
| $^{t}$CAS | 12 | 10,000 | 12 | 10,000 | ns |
| $^{t}$CLZ | 2 | | 2 | | ns |
| $^{t}$CP | 10 | | 10 | | ns |
| $^{t}$CRP | 10 | | 10 | | ns |
| $^{t}$CSH | 48 | | 53 | | ns |
| $^{t}$OD | 0 | 15 | 0 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$OE | | 15 | | 20 | ns |
| $^{t}$RAC | | 60 | | 70 | ns |
| $^{t}$RAD | 10 | 25 | 10 | 30 | ns |
| $^{t}$RAH | 8 | | 8 | | ns |
| $^{t}$RCD | 12 | 40 | 12 | 45 | ns |
| $^{t}$RCH | 2 | | 2 | | ns |
| $^{t}$RCS | 2 | | 2 | | ns |
| $^{t}$WHZ | 2 | 18 | 2 | 20 | ns |
| $^{t}$WPZ | 10 | | 12 | | ns |
| $^{t}$WRH | 8 | | 8 | | ns |
| $^{t}$WRP | 12 | | 12 | | ns |

## RAS-ONLY REFRESH CYCLE [34]




**NOTE:** 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

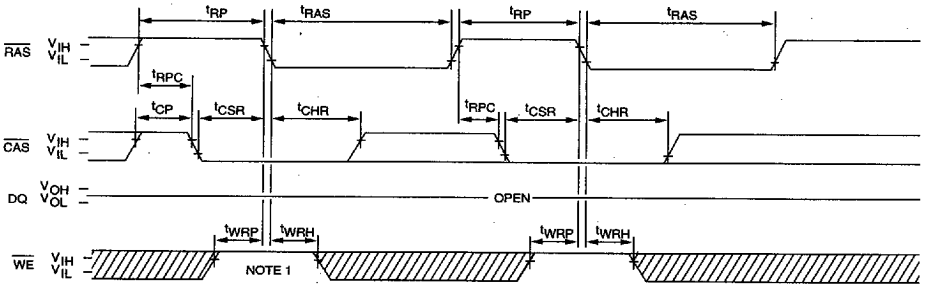
## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tASR | 5 | | 5 | | ns |
| tCRP | 10 | | 10 | | ns |
| tRAH | 8 | | 8 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC (FPM) | 110 | | 130 | | ns |
| tRC (EDO) | 105 | | 125 | | ns |

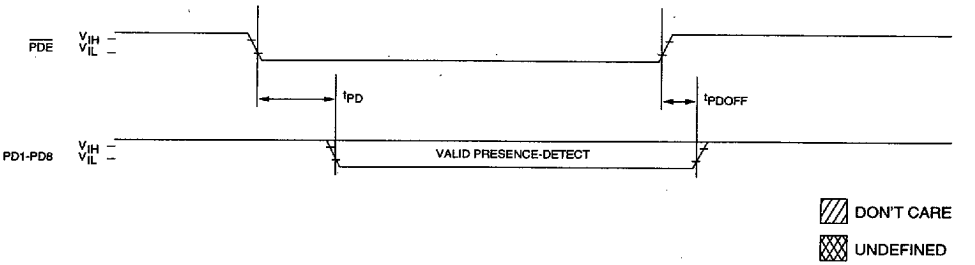
| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRP | 40 | | 50 | | ns |
| tRPC (FPM) | 0 | | 0 | | ns |
| tRPC (EDO) | 5 | | 5 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## CBR REFRESH CYCLE [34]

(Addresses, $\overline{OE}$ = DON'T CARE)




## PRESENCE-DETECT READ CYCLE [34]



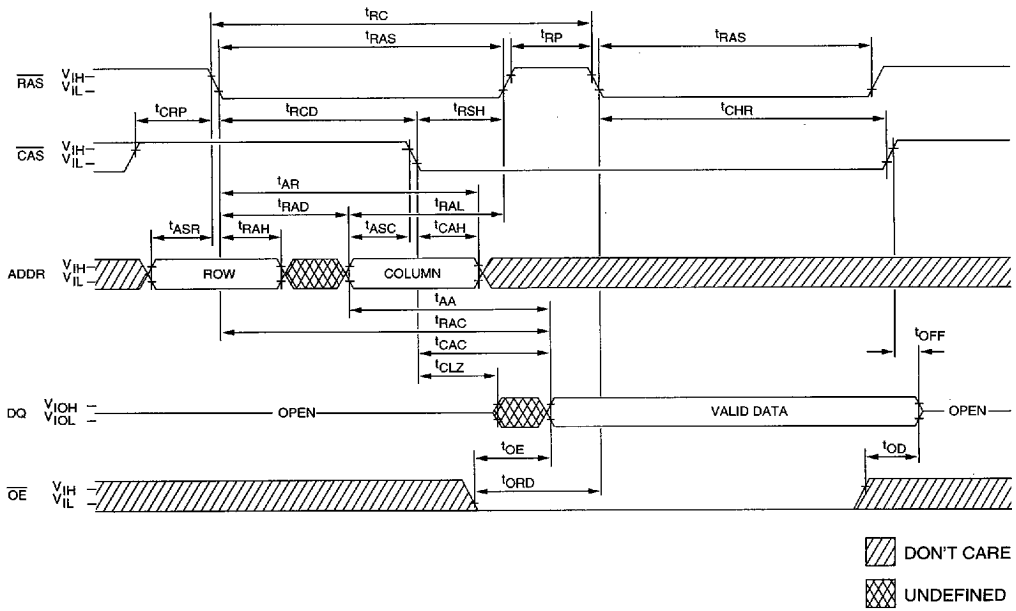

**NOTE:**
1. tWRP and tWRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.
2. PD pins must be pulled HIGH at next level.

## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tCHR (FPM) | 13 | | 13 | | ns |
| tCHR (EDO | 8 | | 10 | | ns |
| tCP | 10 | | 10 | | ns |
| tCSR | 7 | | 7 | | ns |
| tPD | | 10 | | 10 | ns |
| tPDOFF | 2 | | 2 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRP | 40 | | 50 | | ns |
| tRPC (FPM) | 0 | | 0 | | ns |
| tRPC (EDO) | 5 | | 5 | | ns |
| tWRH | 8 | | 8 | | ns |
| tWRP | 12 | | 12 | | ns |

## HIDDEN REFRESH CYCLE [20, 34]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)






## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 35 | | 40 | ns |
| tAR (FPM) | 48 | | 53 | | ns |
| tAR (EDO) | 43 | | 48 | | ns |
| tASC | 2 | | 2 | | ns |
| tASR | 5 | | 5 | | ns |
| tCAC | | 20 | | 25 | ns |
| tCAH (FPM) | 15 | | 20 | | ns |
| tCAH (EDO) | 15 | | 17 | | ns |
| tCHR (FPM) | 13 | | 13 | | ns |
| tCHR (EDO) | 8 | | 10 | | ns |
| tCLZ (FPM) | 5 | | 5 | | ns |
| tCLZ | 2 | | 2 | | ns |
| tCRP | 10 | | 10 | | ns |
| tOD (FPM) | 3 | 15 | 3 | 20 | ns |
| tOD (EDO) | 0 | 15 | 0 | 15 | ns |
| tOE | | 15 | | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOFF (FPM) | 5 | 20 | 5 | 25 | ns |
| tOFF (EDO) | 5 | 20 | 5 | 20 | ns |
| tORD | 0 | | 0 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD (FPM) | 13 | 25 | 13 | 30 | ns |
| tRAD (EDO) | 10 | 25 | 10 | 30 | ns |
| tRAH | 8 | | 8 | | ns |
| tRAL | 35 | | 40 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC (FPM) | 110 | | 130 | | ns |
| tRC (EDO) | 105 | | 125 | | ns |
| tRCD (FPM) | 18 | 40 | 18 | 45 | ns |
| tRCD (EDO) | 12 | 40 | 12 | 45 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH (FPM) | 20 | | 25 | | ns |
| tRSH (EDO) | 18 | | 20 | | ns |