Data Sheet January 2002

3.5A, 30V, 0.06 Ohm, Logic Level, Dual N-Channel LittleFET™ Power MOSFET

This Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA49088.

Ordering Information

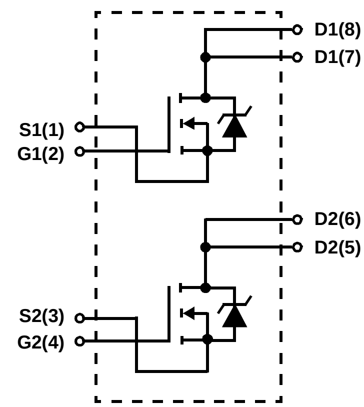
PART NUMBER	PACKAGE	BRAND
RF1K49088	MS-012AA	RF1K49088

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4908896.

Features

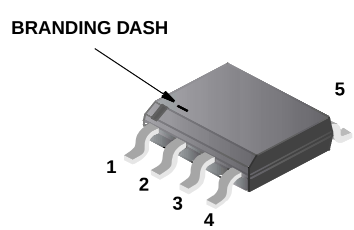
- 3.5A, 30V
- $r_{DS(ON)} = 0.060\Omega$
- Temperature Compensating PSPICE® Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC MS-012AA



Absolute Maximum Ratings $T_A = 25^oC$ Unless Otherwise Specified

		RF1K49088	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ, Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse Width = 5s)	I_D	3.5	A
Pulsed (Figure 5)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating (Figure 6)	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = 25^oC$	P_D	2	W
Derate Above 25^oC		0.016	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V, (Figure 13)		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA, (Figure 12)		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	$T_A = 25^oC$	-	-	1	μA
			$T_A = 150^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 3.5A, V_{GS} = 5V, (Figures 9, 11)		-	-	0.060	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D ≈ 3.5A, R_L = 4.29Ω, V_{GS} = 5V, R_{GS} = 25Ω (Figure 10)		-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$			-	18	-	ns
Rise Time	t_r			-	60	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	53	-	ns
Fall Time	t_f			-	47	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 24V, I_D = 3.5A, R_L = 6.86Ω (Figure 15)	-	24	30	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	13	17	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	0.8	1.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 14)		-	750	-	pF
Output Capacitance	C_{OSS}			-	275	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 3.5A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3.5A, dI_{SD}/dt = 100A/μs	-	-	50	ns

Typical Performance Curves

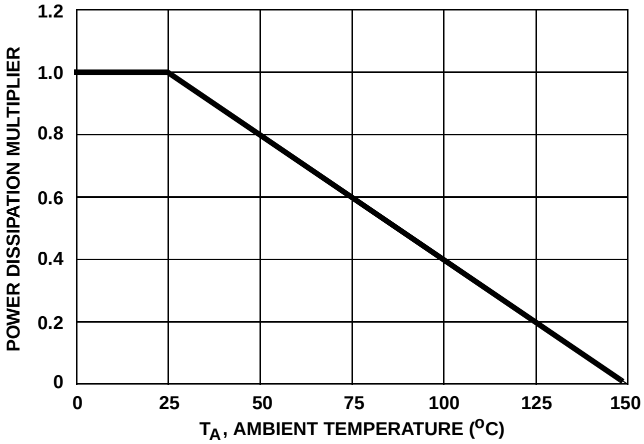


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

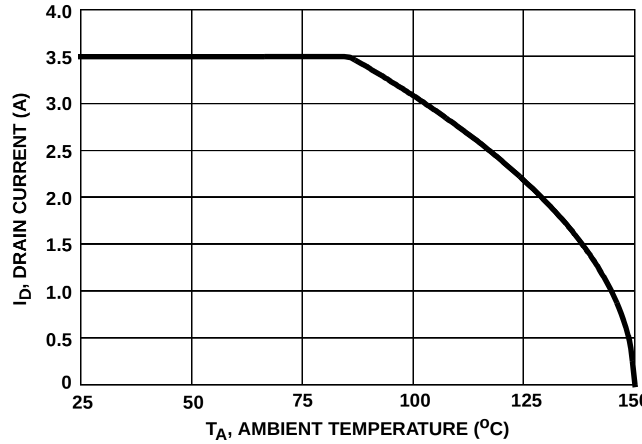


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

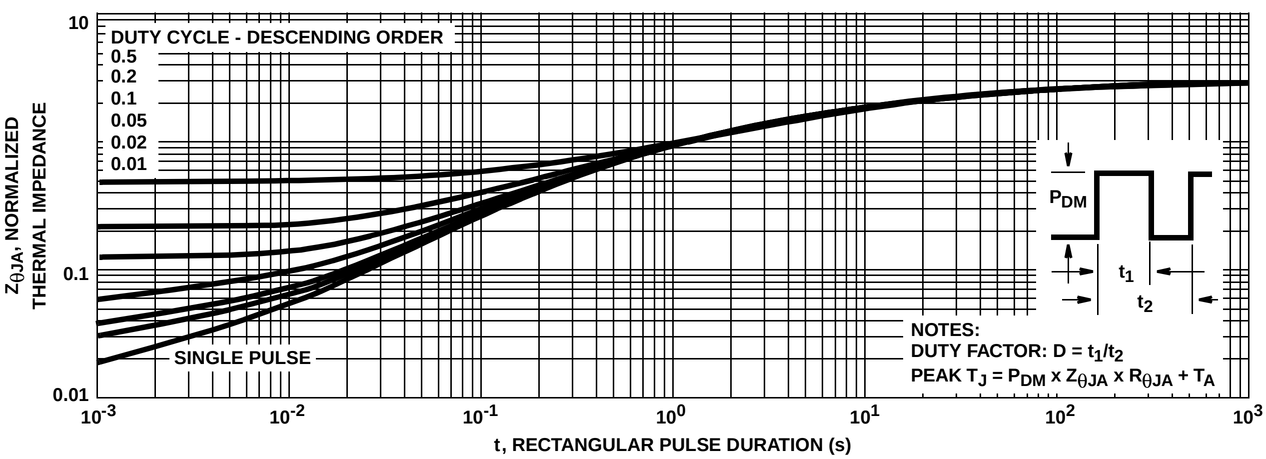


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

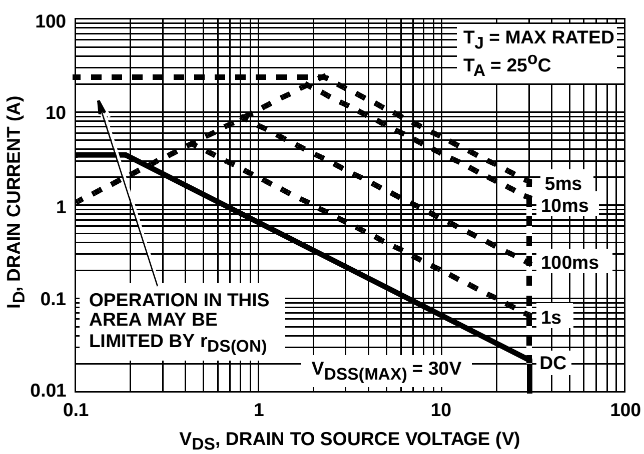


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

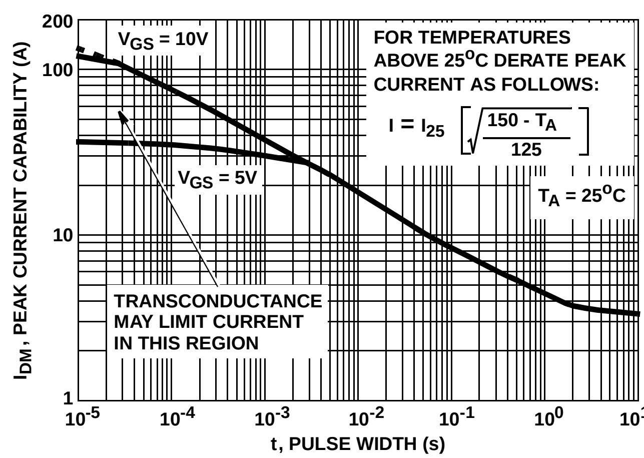
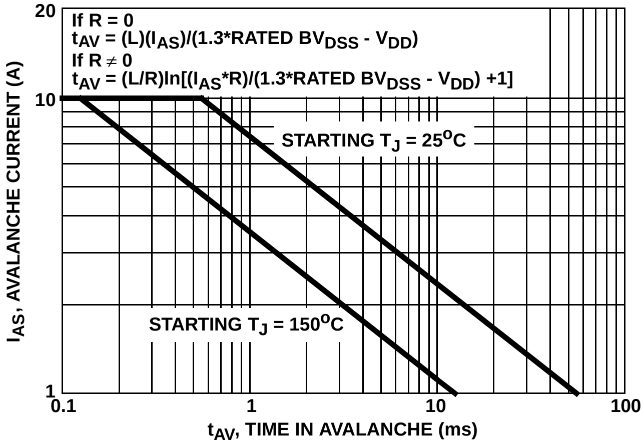


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

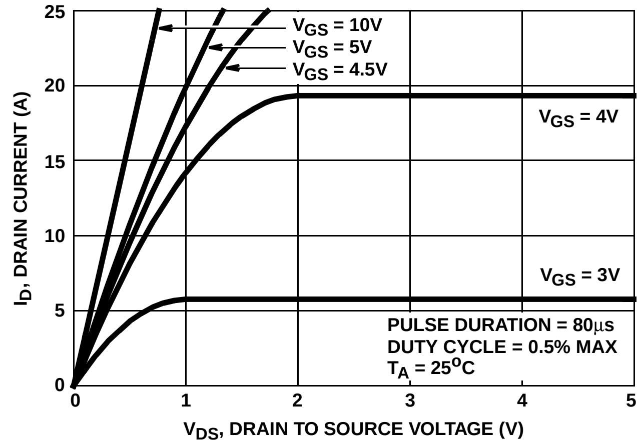


FIGURE 7. SATURATION CHARACTERISTICS

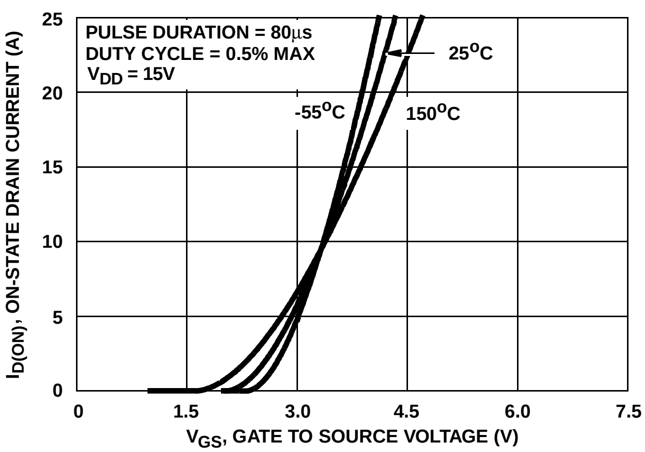


FIGURE 8. TRANSFER CHARACTERISTICS

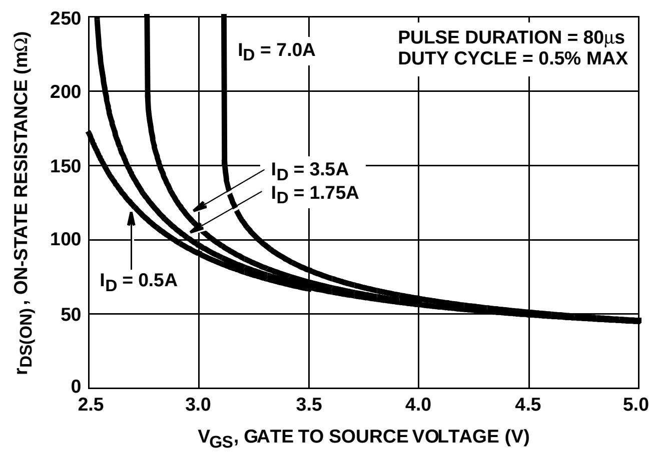


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

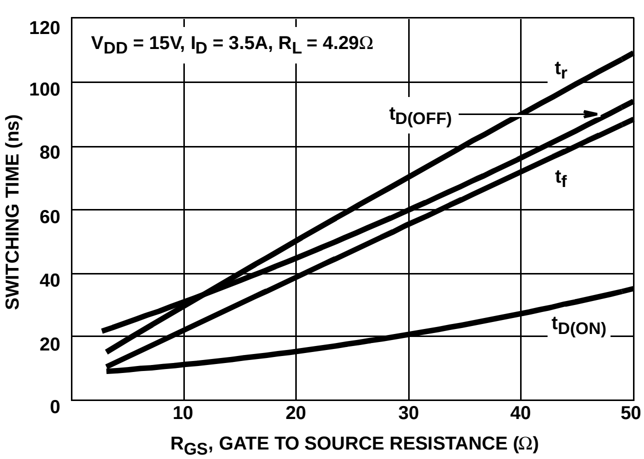


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

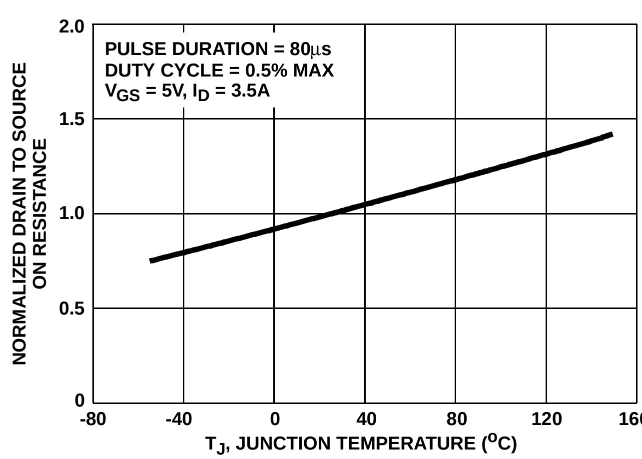


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

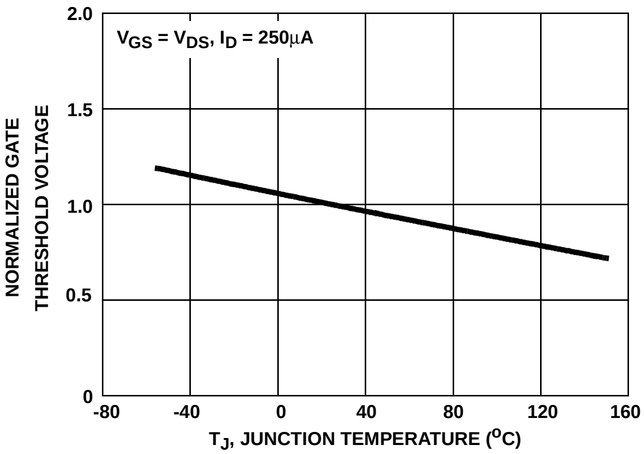


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

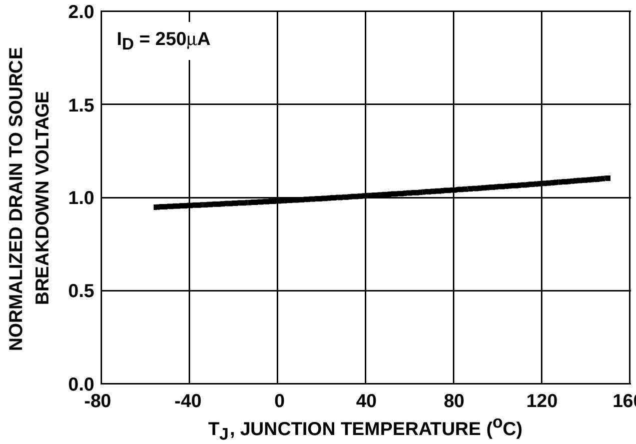


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

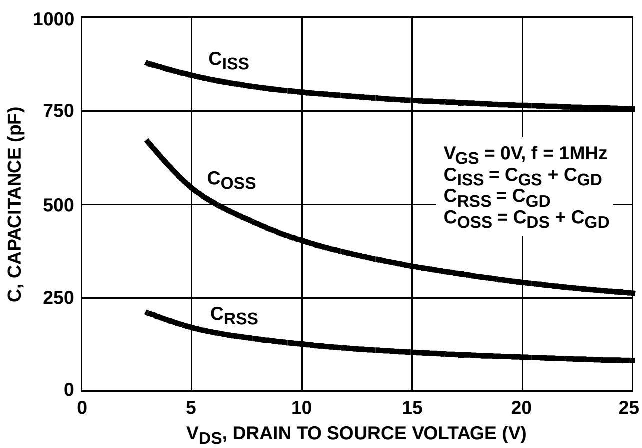
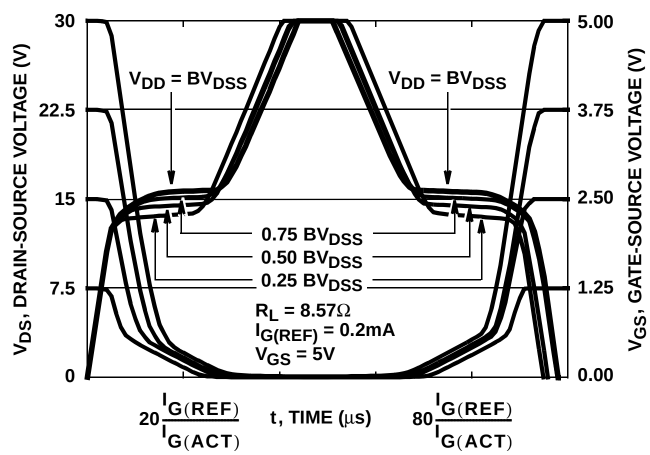


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

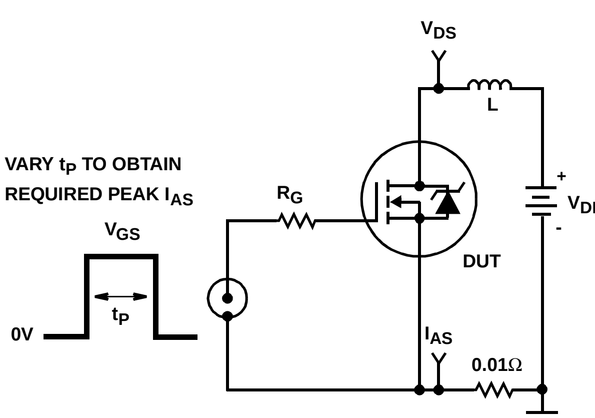


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

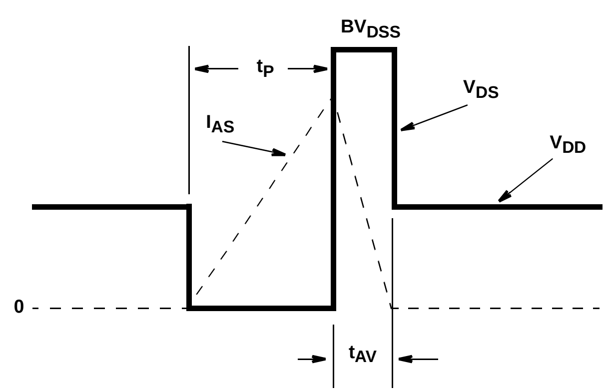


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

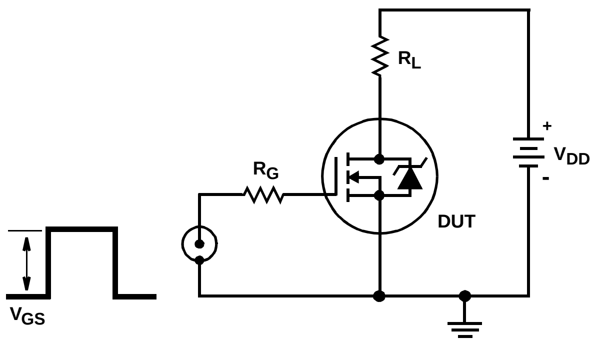


FIGURE 18. SWITCHING TIME TEST CIRCUIT

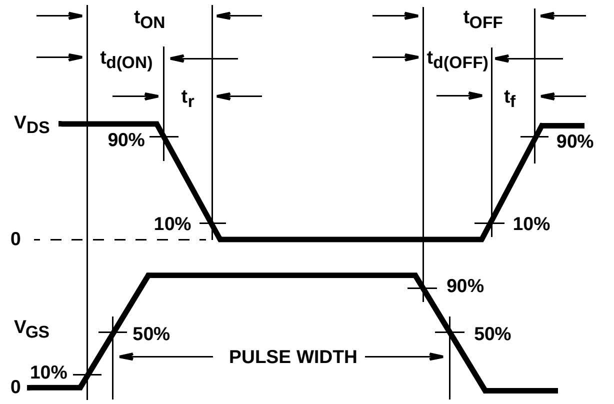


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

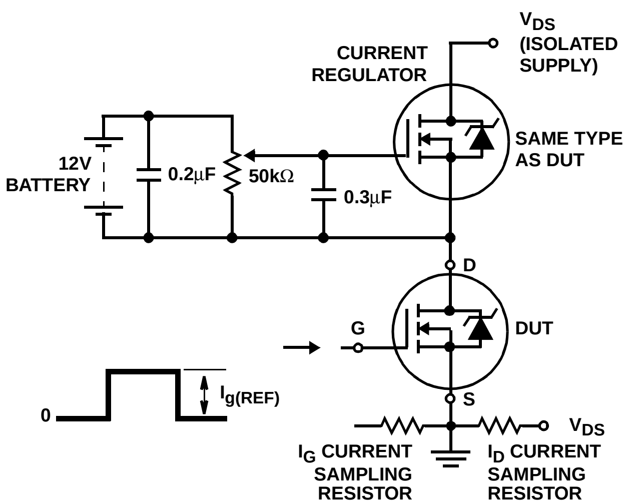


FIGURE 20. GATE CHARGE TEST CIRCUIT

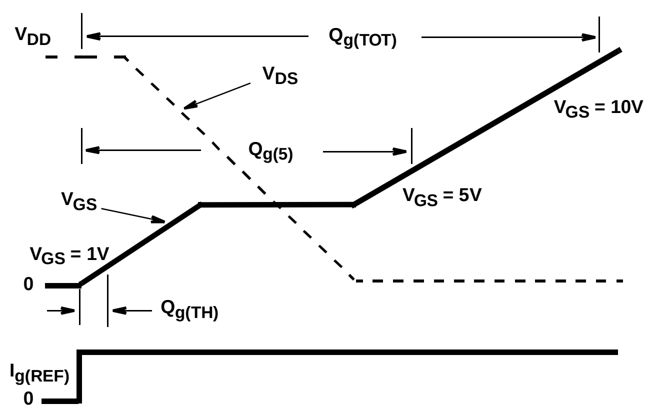


FIGURE 21. GATE CHARGE WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100^{o}C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5^{o}C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30^{o}C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260^{o}C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

PSPICE Electrical Model

SUBCKT RF1K49088 2 1 3;rev 7/21/94

CA 12 8 1.081e-9
CB 15 14 1.138e-9
CIN 6 8 0.673e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.1
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

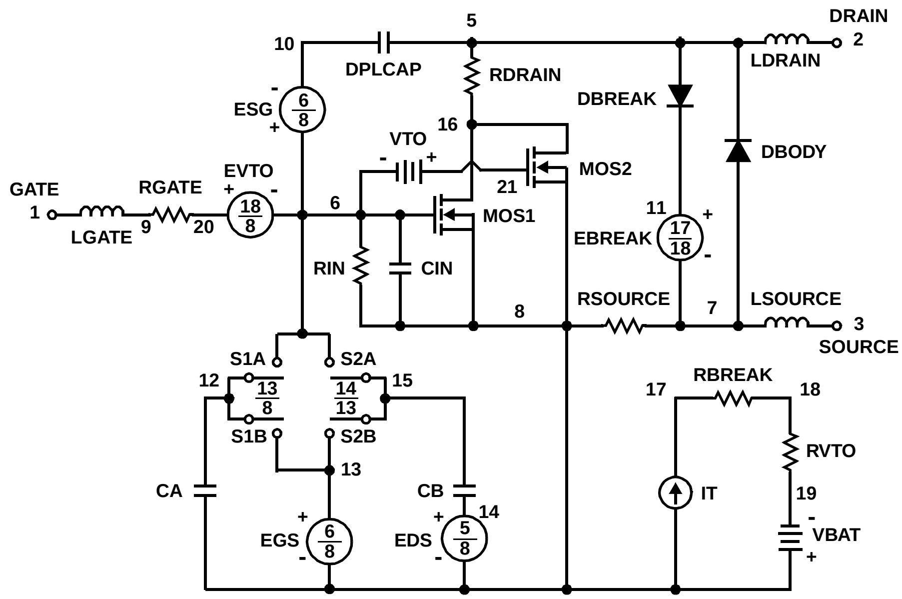
LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1.408e-3
RGATE 9 20 3.33
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 20e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.211



.MODEL DBDMOD D (IS = 2.82e-13 RS = 1.72e-2 TRS1 = 1.58e-3 TRS2 = 1.23e-7 CJO = 9.19e-10 TT = 2.03e-8)
.MODEL DBKMOD D (RS = 2.65e-1 TRS1 = 5.00e-3 TRS2 = 7.09e-5)
.MODEL DPLCAPMOD D (CJO = 0.42e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.0 1KP = 15.0 1IS = 1e-3 0N = 1 0TOX = 1L = 1 uW = 1u)
.MODEL RBKMOD RES (TC1 = 1.02e- 3TC2 = -1.98e-6)
.MODEL RDSMOD RES (TC1 = 3.50e-3 TC2 = 3.70e-6)
.MODEL RVTOMOD RES (TC1 = -2.53e- 3TC2 = 8.13e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF= -3.8)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.8 VOFF= -6.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.4 VOFF= 4.1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.1 VOFF= -1.4)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

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FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
ISOPLANAR™
LittleFET™
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MicroPak™
MICROWIRE™
OPTOLOGIC™
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PACMAN™
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Power247™
PowerTrench®
QFET™
QS™
QT Optoelectronics™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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