



Optimum power handling
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T143-500

Mean on-state current	I_{TAV}	500 A					
Repetitive peak off-state voltage	V_{DRM}	400 ÷ 1600 V					
Repetitive peak reverse voltage	V_{RRM}						
Turn-off time	t_q	160; 250; 500 μ s					
V_{DRM}, V_{RRM}, V	400	600	800	1000	1200	1400	1600
Voltage code	4	6	8	10	12	14	16
$T_j, ^\circ C$	– 60 ÷ 125						

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	500	$T_c=94\ ^\circ C$; 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	1160	$T_c=94\ ^\circ C$; Full cycle sine wave, 50 Hz
I_{TSM}	Surge on-state current	kA	11.0 12.0	$T_j=T_{j\ max}$ $T_j=25^\circ C$ 180° half-sine wave, 50 Hz, single pulse; $V_R=0\ V$;
I^2t	Circuit fusing considerations	$A^2s \cdot 10^3$	605 720	$T_j=T_{j\ max}$ $T_j=25^\circ C$ Gate pulse: 20 V, 5 Ω , 1 μ s rise time, 50 μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	400÷1600	$T_j=T_{j\ max}$; 180° half-sine wave, 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	450÷1800	$T_j= T_{j\ max}$; 180° half-sine wave, 50 Hz, single pulse Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75· V_{DRM} 0.75· V_{RRM}	$T_j=T_{j\ max}$; Gate open
TRIGGERING				
P_{GM}	Peak gate power dissipation	W	40	$T_j=T_{j\ max}$
$P_{G(AV)}$	Mean gate power dissipation	W	6	$T_j=T_{j\ max}$
V_{RGM}	Peak gate reverse voltage	V	5	$T_j=T_{j\ max}$
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current: non-repetitive repetitive	A/ μ s	200 100	$T_j=T_{j\ max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM} \leq 2I_{T(AV)}$; Gate pulse: 20 V, 5 Ω , 1 μ s rise time, 50 μ s
THERMAL				
T_{stg}	Storage temperature	$^\circ C$	– 60 ÷ 50	
T_j	Junction temperature	$^\circ C$	– 60 ÷ 125	

CHARACTERISTICS

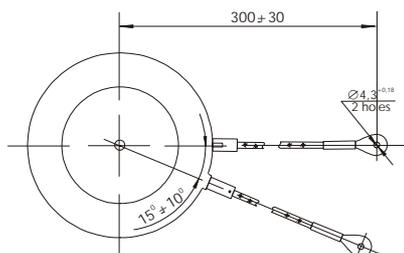
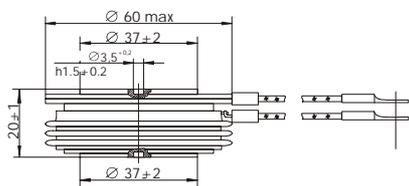
Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage	V	1.80	$T_j=25^\circ\text{C}; I_{TM}=3.14 \cdot I_{TAV}$
$V_{T(TO)}$	On-state threshold voltage	V	1.10	$T_j=T_{j\max}$
r_T	On-state slope resistance	m Ω	0.57	$T_j=T_{j\max}$
I_L	Latching current	mA	700	$T_j=25^\circ\text{C}; V_D=12\text{ V};$ Gate pulse: 20 V, 5 Ω , 1 μs rise time, 50 μs
I_H	Holding current	mA	300	$T_j=25^\circ\text{C}; V_D=12\text{ V};$ Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and repetitive peak reverse currents	mA	30	$T_j=T_{j\max};$ $V_D=V_{DRM}; V_R=V_{RRM}$
$(dV_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾	V/ μs	200 1600	$T_j=T_{j\max};$ $V_D=0.67 \cdot V_{DRM};$ Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage	V	3.50	$T_j=25^\circ\text{C}; V_D=12\text{ V};$
I_{GT}	Gate trigger direct current	A	0.25	Direct gate current
V_{GD}	Gate non-trigger direct voltage	V	0.5	$T_j=T_{j\max}; V_D=0.67 \cdot V_{DRM};$
I_{GD}	Gate non-trigger direct current	mA	10.0	Direct gate current
SWITCHING				
t_{gt}	Turn-on time	μs	25.0	$T_j=25^\circ\text{C}; V_D=100\text{ V}; I_{TM}=I_{TAV};$ Gate pulse: 20 V, 5 Ω , 1 μs rise time, 50 μs
t_{gd}	Delay time	μs	7.0	
t_q	Turn-off time ²⁾	μs	160 250 500	$T_j=T_{j\max};$ $I_{TM}=I_{TAV};$ $di_R/dt=5\text{ A}/\mu\text{s}; V_R=100\text{ V};$ $V_D=0.67 \cdot V_{DRM}; dV_D/dt=50\text{ V}/\mu\text{s}$
Q_{rr}	Recovered charge	μC	1500	$T_j=T_{j\max}; I_{TM}=I_{TAV};$
t_{rr}	Reverse recovery time	μs	30.0	$di_R/dt=5\text{ A}/\mu\text{s}; V_R=100\text{ V};$
THERMAL				
R_{thjc}	Thermal resistance junction to case	$^\circ\text{C}/\text{W}$	0.034	Direct current, double side cooled

Note:

¹⁾ Critical rate of rise of off-state voltage

Symbol of group	P2	K2	E2	A2	T1
$(dV_D/dt)_{crit}, \text{ V}/\mu\text{s}$	200	320	500	1000	1600

OVERALL DIMENSIONS



Weight: 260 grams

Mounting force: 13.5 ÷ 16.5 kN

Recommended heatsink: O143; O243; O343

²⁾ Turn-off time

Symbol of group	T2	M2	E2
$t_q, \mu\text{s}$	160	250	500

PART NUMBERING GUIDE

T	143	500	16	T1	T2	N
1	2	3	4	5	6	7

1. Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time
7. Ambient conditions: N – normal; T – tropical

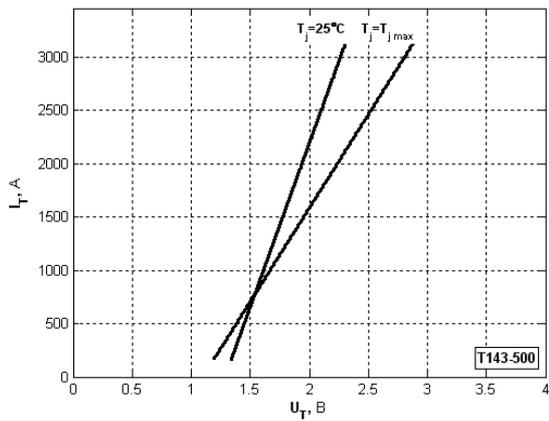


Fig 1 On-state characteristics

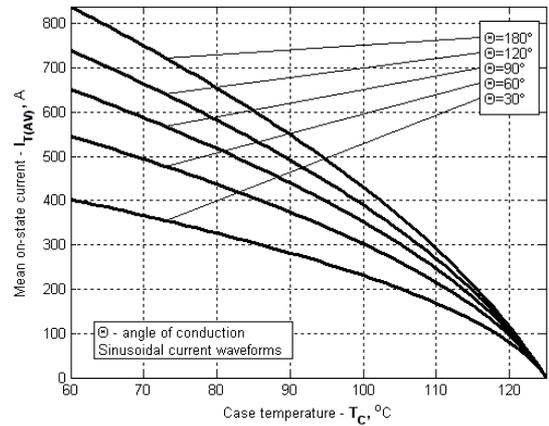


Fig 2 Maximum allowable mean on-state current I_{TAV} vs. case temperature T_c for sinusoidal current waveforms, $f=50$ Hz

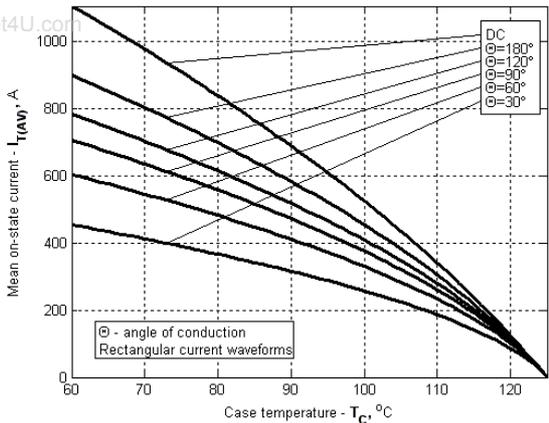


Fig 3 Maximum allowable mean on-state current I_{TAV} vs. case temperature T_c for rectangular current waveforms and for DC, $f=50$ Hz

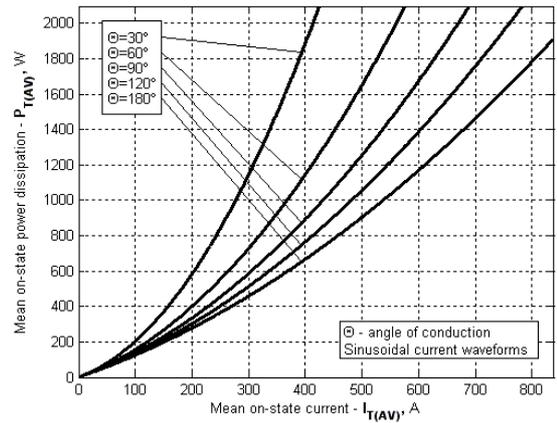


Fig 4 On-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles, $f=50$ Hz

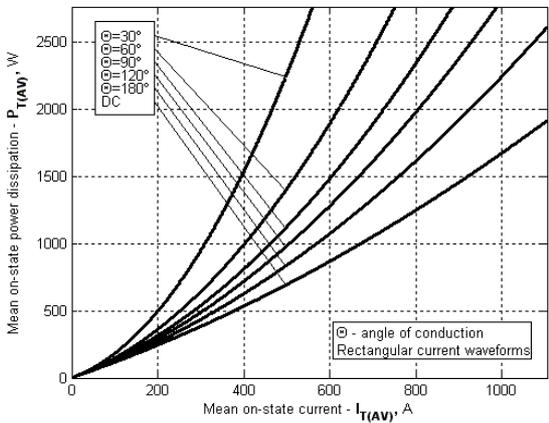


Fig 5 On-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms and for DC at different conduction angles, $f=50$ Hz

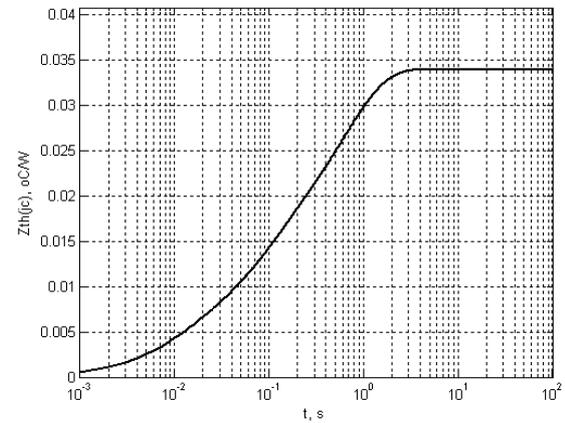


Fig 6 Transient thermal impedance junction to case $Z_{th(jc)}$

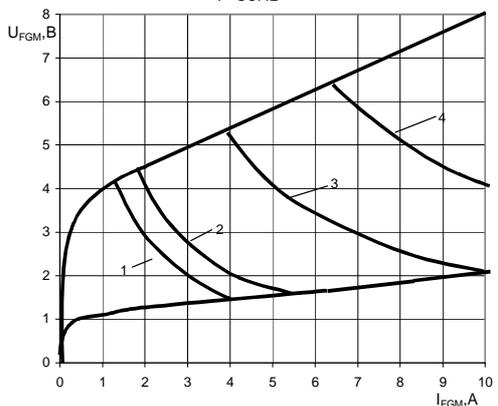


Fig 7 Max. peak gate power loss:

Position (See Fig. 7)	On-Off time ratio	Gate pulse length, ms	Gate Pulse Power, W
1	1	DC	6
2	2	10	8
3	20	1	20
4	40	0,5	40

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