UCS-5822H HERMETIC BiMOS II
8-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

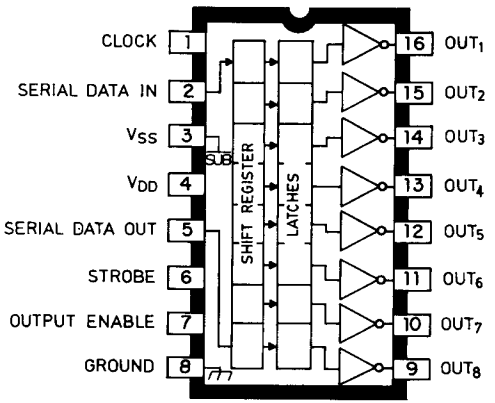
FEATURES

- 3.3 MHz Minimum Data Input Rate
- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Intended for military, aerospace, and related applications. The UCS-5822H 8-bit, serial-input, latched driver combines bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output alows cascading these devices for interface applications requiring additional drive lines.



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The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

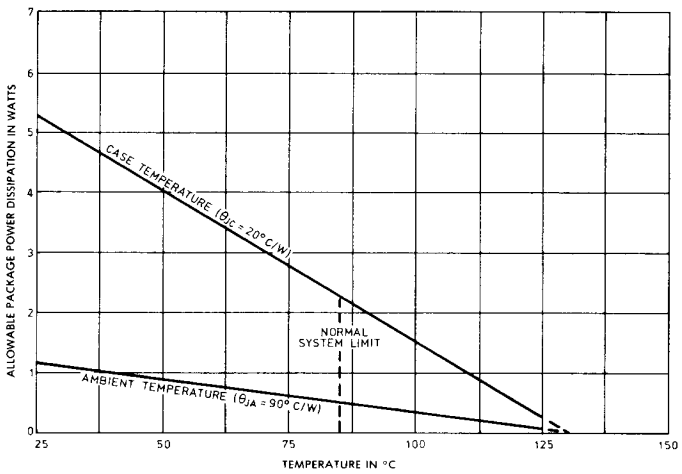
The UCS-5822H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, class B are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT}	80 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



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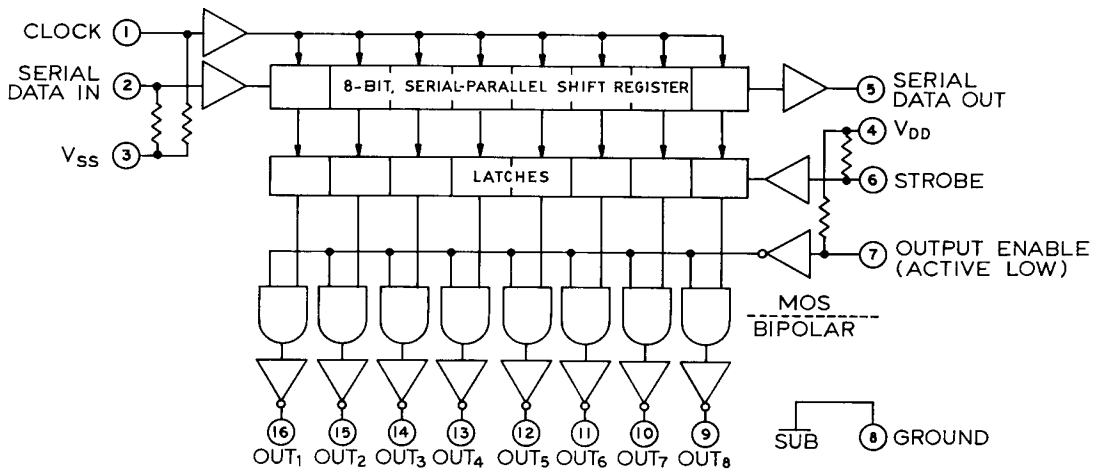
FUNCTIONAL BLOCK DIAGRAM



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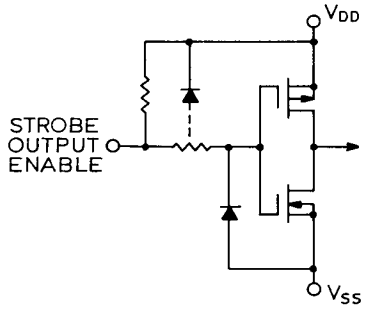
TYPICAL INPUT CIRCUITS



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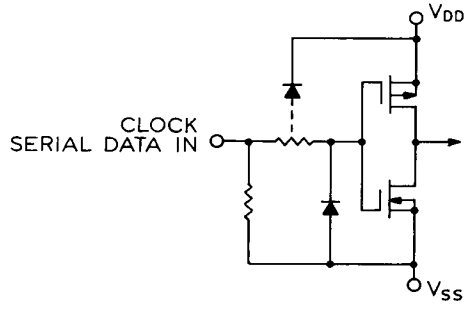

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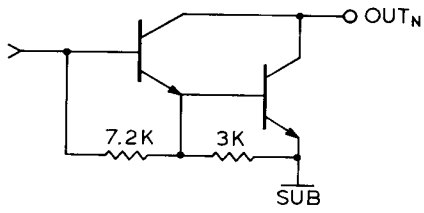
TYPICAL OUTPUT DRIVER



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ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\ V$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\ mA$	—	1.1	V
		$I_{OUT} = 200\ mA$	—	1.3	V
		$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	—	kΩ
		$V_{DD} = 10\ V$	50	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\ V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	3.9	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\ V$	—	2.9	mA

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

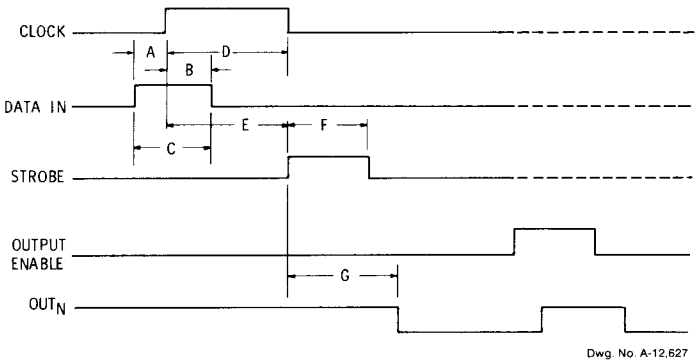
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\ V$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\ mA$	—	1.3	V
		$I_{OUT} = 200\ mA$	—	1.5	V
		$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	35	—	kΩ
		$V_{DD} = 10\ V$	35	—	kΩ
		$V_{DD} = 5.0\ V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\ V$	—	5.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	3.0	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	2.0	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\ V$	—	3.5	mA

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\ V$	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\ mA$*	—	1.3	V
		$I_{OUT} = 200\ mA$*	—	1.5	V
		$I_{OUT} = 350\ mA$*, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	—	kΩ
		$V_{DD} = 10\ V$	50	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\ V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	3.9	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\ V$	—	2.9	mA

*Pulsed test.
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

Number of Outputs ON ($I_{OUT} = 200\ mA$)	Max. Allowable Duty Cycle at $V_{DD} = 5\ V$ and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3	100%	100%	50%
2	100%	100%	75%
1	100%	100%	100%



Dwg. No. A-12,627

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

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UCS-5822H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H		H R_1 R_2 ..... R_7	R_7				
L		L R_1 R_2 ..... R_7	R_7				
X		R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State