

Description

The μPD71011 is a clock pulse generator/driver for the V20®/V30® microprocessors and their peripherals using NEC's high-speed CMOS technology.

Features

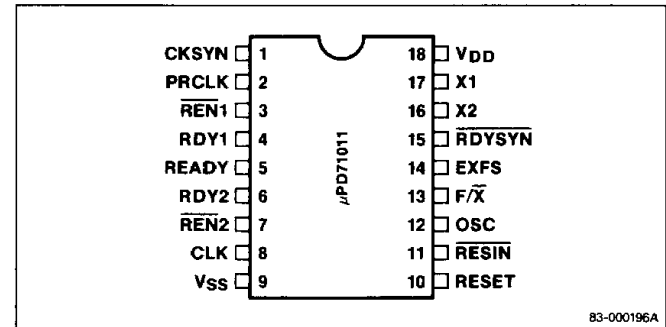
- CMOS technology
- Clock pulse generator/driver for μPD70108/70116 or other CMOS or NMOS CPUs and their peripherals
- 50% duty cycle
- Frequency source can be crystal or external clock input
- Reset signal with Schmitt-trigger circuit for CPU or peripherals
- Bus ready signal with two-bus system synchronization
- Clock synchronization with other μPD71011s
- Single +5-volt ±10% power supply
- Industrial temperature range: -40 to +85°C

Ordering Information

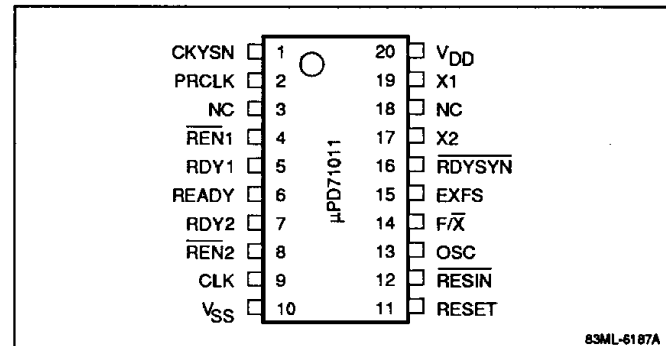
| Part Number | Maximum Clockout | | Package |
|-------------|------------------|--|--------------------|
| | Frequency | | |
| μPD71011C-8 | 8 MHz | | 18-pin plastic DIP |
| C-10 | 10 MHz | | |
| G-8 | 8 MHz | | 20-pin plastic SOP |

Pin Configurations

18-Pin Plastic DIP



20-Pin Plastic SOP



5a

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Pin Identification

| Symbol | Function |
|--------------------|--|
| CKSYN | Clock synchronization input |
| PRCLK | Peripheral clock output |
| $\overline{REN1}$ | Bus ready enable input 1 |
| RDY1 | Bus ready input 1 |
| READY | Ready output |
| RDY2 | Bus ready input 2 |
| $\overline{REN2}$ | Bus ready enable input 2 |
| CLK | Processor clock output |
| V_{SS} | Ground potential |
| RESET | Reset output |
| \overline{RESIN} | Reset input |
| OSC | Oscillator output |
| F/\overline{X} | External frequency source/crystal select input |
| EXFS | External frequency source input |
| RDYSYN | Ready synchronization select input |
| X2 | Crystal input |
| X1 | Crystal input |
| V_{DD} | +5-volt power supply |
| NC | No connection |

PIN FUNCTIONS

X1, X2 (Crystal)

When F/\overline{X} is low, a crystal connected to X1 and X2 will be the frequency source for a CPU and its peripherals. The crystal frequency should be two times the frequency of CLK.

EXFS (External Frequency Source)

EXFS input is the external frequency input in the external TTL-frequency source mode (F/\overline{X} high). A square TTL-level clock signal two times the frequency of CLK's output should be used for the source.

F/\overline{X} (Frequency/Crystal Select)

F/\overline{X} input selects whether an external TTL-type input or an external crystal input is the frequency source of the CLK output. When F/\overline{X} is low, CLK is generated from the crystal connected to X1 and X2. When F/\overline{X} is high, CLK is generated from an external TTL-level frequency input on the EXFS pin. At the same time, the internal oscillator circuit will go into stop mode and the OSC output will be high.

CLK (Processor Clock)

The CLK output supplies the CPU and its local bus peripherals' clocks. CLK is a 50-percent duty cycle clock of one-half the frequency of the external frequency source. The CLK output is +0.4 V higher than the other outputs.

PRCLK (Peripheral Clock)

The PRCLK output supplies a 50-percent duty cycle clock at one-half the frequency of CLK to drive peripheral devices.

OSC (Oscillator)

OSC outputs a signal at the same frequency as the crystal input. When EXFS is selected, the OSC output is powered down, and its output will be a high.

CKSYN (Clock Synchronization)

CKSYN synchronizes one μPD71011 to other μPD71011s. A high level at CKSYN resets the internal counter, and a low level enables it to count.

\overline{RESIN} (Reset)

This Schmitt-trigger input generates the RESET output. It is used as a power-on reset.

RESET (Reset)

This output is a reset signal for the CPU. Reset timing is provided by the \overline{RESIN} input to a Schmitt-trigger input gate and a flip-flop which will synchronize the reset timing to the falling edge of CLK. Power-on reset can be provided by a simple RC circuit on the \overline{RESIN} input.

RDY1, RDY2 (Bus Ready)

A peripheral device sends RDY1 or RDY2 to signal that the data on the system bus has been received or is ready to be sent. $\overline{REN1}$ and $\overline{REN2}$ enable the RDY1 or RDY2 signals.

$\overline{REN1}$, $\overline{REN2}$ (Bus Ready Enable)

$\overline{REN1}$ and $\overline{REN2}$ qualify their respective RDY inputs.

RDYSYN (Ready Synchronization Select)

RDYSYN selects the mode of READY signal synchronization. A low-level signal makes the synchronization a two-step process. This is used when RDY1 and RDY2 inputs are not synchronized to CLK. A high-level signal makes synchronization a one-step process. This is used when RDY1 and RDY2 are synchronized to CLK. See block diagram.

READY (Ready)

The READY signal to the processor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the RDY signal goes low and the guaranteed hold time of the processor has been met.

Crystal

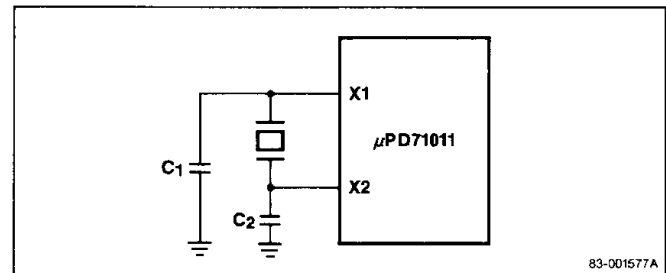
The oscillator circuit of the μPD71011 works with a parallel-resonant, fundamental mode, "AT cut" crystal connected to pins X1 and X2.

Figure 1 shows the recommended circuit configuration. Capacitors C1 and C2 are required for frequency stability. The values of C1 and C2 ($C_1 = C_2$) can be calculated from the load capacitance (C_L) specified by the crystal manufacturer.

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_S$$

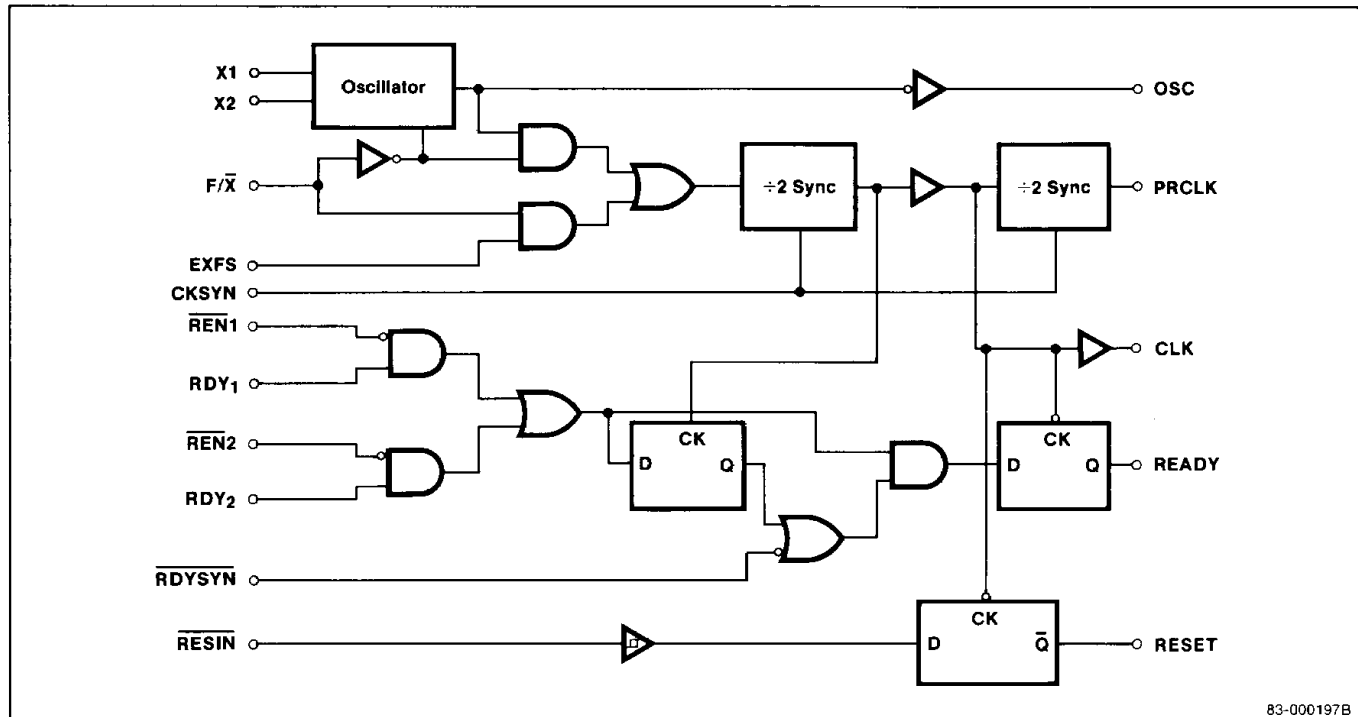
Where C_S is any stray capacitance in parallel with the crystal, such as the μPD71011 input capacitance C_{IN} .

Figure 1. Crystal Configuration Circuit



83-001577A

μPD71011 Block Diagram



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Absolute Maximum Ratings

T_A = 25°C; V_{SS} = 0 V

| | |
|--|------------------------------------|
| Power supply voltage, V _{DD} | - 0.5 to + 7.0 V |
| Input voltage, V _I | - 1.0 V to V _{DD} + 1.0 V |
| Output voltage, V _O | - 0.5 V to V _{DD} + 0.5 V |
| Operating temperature, T _{OPT} | - 40 to +85°C |
| Storage temperature, T _{STG} | - 65 to +150°C |
| Power dissipation, P _D (DIP) | 500 mW |
| Power dissipation, P _D (SO package) | 200 mW |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; V_{DD} = +5 V

| Parameter | Symbol | Min | Max | Unit | Conditions |
|-------------------|-----------------|-----|-----|------|------------------------|
| Input capacitance | C _{IN} | | 12 | pF | f _C = 1 MHz |

DC Characteristics

T_A = -40 to +85°C; V_{DD} = 5 V ±10%

| Parameter | Symbol | Min | Max | Unit | Conditions |
|--------------------------------|--------------------|-----------------------|------|------|-------------------------------------|
| Input voltage, high | V _{IH} | 2.2 | | V | |
| | | | 2.6 | V | RESIN input |
| Input voltage, low | V _{IL} | | 0.8 | V | |
| Output voltage, high | V _{OH} | V _{DD} - 0.4 | | V | CLK output, I _{OH} = -4 mA |
| | | V _{DD} - 0.8 | | V | I _{OH} = -4 mA |
| Output voltage, low | V _{OL} | | 0.45 | V | I _{OL} = 4 mA |
| Input leakage current | I _{IN} | -1.0 | 1.0 | μA | |
| | | -400 | 1.0 | μA | RDYSYN input |
| RESIN input hysteresis | | 0.20 | | V | |
| Power supply current (static) | I _{DD} | | 200 | μA | |
| Power supply current (dynamic) | I _{DDdyn} | | 30 | mA | f _{IN} = 20 MHz |

AC Characteristics

f_{OSC} = 10 MHz; T_A -40 to +85°C; V_{DD} = +5 V ±10%
 f_{OSC} = 16 MHz; T_A -10 to +70°C; V_{DD} = +5 V ±5%
 f_{OSC} = 20 MHz; T_A -10 to +70°C; V_{DD} = +5 V ±5%

| Parameter | Symbol | μPD71011 | | μPD71011-10 | | Unit | Conditions |
|------------------------|--------------------|--------------------|-----|--------------------|-----|------|---|
| | | Min | Max | Min | Max | | |
| Clock Timing | | | | | | | |
| EXFS input cycle time | t _{CYFS} | 50 | | 50 | | ns | |
| EXFS pulse width, high | t _{PWFH} | 20 | | 20 | | ns | 2.2 V measurement point |
| EXFS pulse width, low | t _{PWFL} | 20 | | 20 | | ns | 0.8 V measurement point |
| OSC cycle time | f _{OSC} | 8 | 20 | 8 | 20 | MHz | from EXFS |
| CKSYN pulse width | t _{PWCT} | 2t _{CYFS} | | 2t _{CYFS} | | ns | |
| CKSYN setup time | t _{HFSTK} | 20 | | 20 | | ns | |
| CKSYN hold time | t _{SCTFS} | 20 | | 20 | | ns | |
| CLK cycle time | t _{CYCK} | 125 | | 100 | | ns | |
| CLK pulse width, high | t _{PWCKH} | 80 | | 41 | | ns | 3.0 V, f _{OSC} = 10 MHz, f _{OSC} = 20 MHz |
| | | 50 | | | | ns | 3.0 V, f _{OSC} = 16 MHz |
| CLK pulse width, low | t _{PWCKL} | 90 | | 49 | | ns | 1.5 V, f _{OSC} = 10 MHz, f _{OSC} = 20 MHz |
| | | 60 | | | | ns | 1.5 V, f _{OSC} = 16 MHz |
| CLK rise time | t _{LHCK} | | 10 | | 5 | ns | 1.5 → 3.0 V, f _{OSC} = 10 MHz, f _{OSC} = 20 MHz |
| | | | 8 | | | ns | 1.5 → 3.0 V, f _{OSC} = 16 MHz |
| CLK fall time | t _{HLCK} | | 10 | | 5 | ns | 3.0 → 1.5 V, f _{OSC} = 10 MHz, f _{OSC} = 20 MHz |
| | | | 7 | | | ns | 3.0 → 1.5 V, f _{OSC} = 16 MHz |
| OSC to CLK ↑ delay | t _{DCK} | 2 | 30 | 2 | 30 | ns | CLK ↑ |
| OSC to CLK ↓ delay | t _{DCK} | -6 | 28 | -6 | 28 | ns | CLK ↓ |
| PRCLK cycle time | t _{CYPRK} | 250 | | 200 | | ns | |

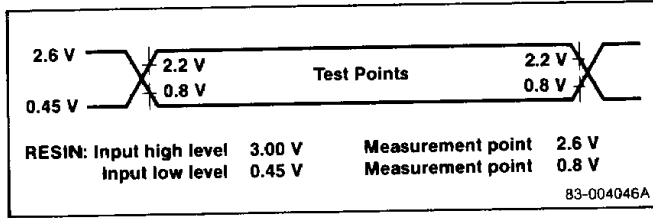
AC Characteristics (cont)

| Parameter | Symbol | μPD71011 | | μPD71011-10 | | Unit | Conditions |
|------------------------------------|---------------------|---------------------------|-----|---------------------------|-----|------|-------------|
| | | Min | Max | Min | Max | | |
| Clock Timing (cont) | | | | | | | |
| PRCLK pulse width, high | t _{PWPRKH} | t _{CYCK} - 20 | | t _{CYCK} - 20 | | ns | |
| PRCLK pulse width, low | t _{PWPRKL} | t _{CYCK} - 20 | | t _{CYCK} - 20 | | ns | |
| PRCLK ↑ delay from CLK ↓ | t _{DPRKH} | | 22 | | 22 | ns | |
| PRCLK ↓ delay from CLK ↓ | t _{DPRKL} | | 22 | | 22 | ns | |
| Reset Timing | | | | | | | |
| RESIN setup to CLK ↓ | t _{SRICK} | 65 | | 65 | | ns | |
| RESIN hold from CLK ↓ | t _{HCKRI} | 20 | | 20 | | ns | |
| RESET delay from CLK ↓ | t _{DCKRS} | | 40 | | 20 | ns | |
| Ready Timing (RDYSYN = 'H') | | | | | | | |
| REN1, 2 setup to RDY1, 2 | t _{SRERY} | 15 | | 15 | | ns | |
| REN1, 2 hold from CLK ↓ | t _{HCKRE} | 0 | | 0 | | ns | |
| RDY1, 2 setup to CLK ↓ | t _{SRYCK} | 35 | | 35 | | ns | RDYSYN high |
| RDY1, 2 hold from CLK ↓ | t _{HCKRY} | 0 | | 0 | | ns | |
| RDYSYN setup to CLK ↓ | t _{SRYSCK} | 50 | | 50 | | ns | |
| RDYSYN hold from | t _{HCKRYS} | 0 | | 0 | | ns | |
| READY output delay from CLK ↓ | t _{DCKRDY} | | 8 | | 8 | ns | READY ↑ |
| | | | 8 | | 8 | ns | READY ↓ |
| Ready Timing (RDYSYN = 'L') | | | | | | | |
| REN1, 2 setup to RDY1, 2 | t _{SRERY} | 15 | | 15 | | ns | |
| REN1, 2 hold from CLK ↓ | t _{HCKRE} | 0 | | 0 | | ns | |
| RDY1, 2 setup to CLK | t _{SRYCK} | 35 | | 35 | | ns | RDYSYN low |
| RDY1, 2 hold from CLK ↓ | t _{HCKRY} | 0 | | 0 | | ns | |
| RDYSYN setup to CLK ↓ | t _{SRYSCK} | 50 | | 50 | | ns | |
| RDYSYN hold from CLK ↓ | t _{HCKRYS} | 0 | | 0 | | ns | |
| READY output delay from CLK ↓ | t _{DCKRDY} | | 8 | | 8 | ns | READY ↑ |
| | | | 8 | | 8 | ns | READY ↓ |
| Output Pin Timing | | | | | | | |
| Rise time | t _{LH} | | 20 | | 20 | ns | 0.8 → 2.0 V |
| Fall time | t _{HL} | | 12 | | 12 | ns | 2.0 → 0.8 V |

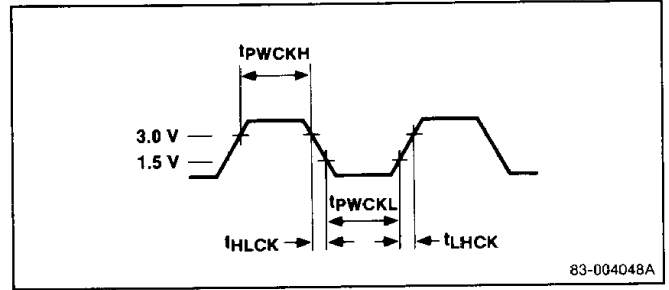
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Timing Waveforms

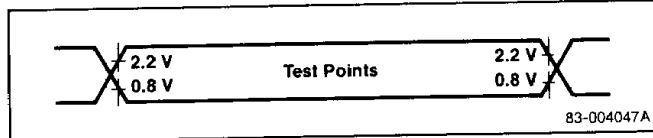
AC Test Input (except RESIN)



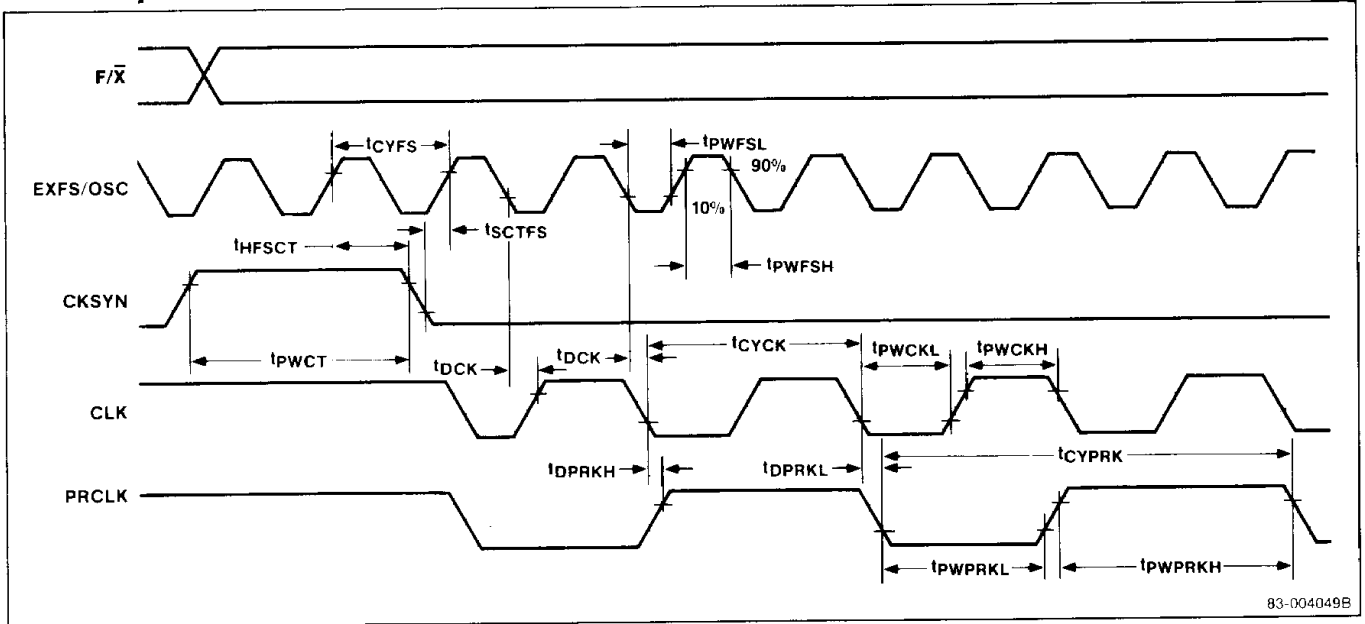
AC Test Output (CLK)



AC Test Output (except CLK)

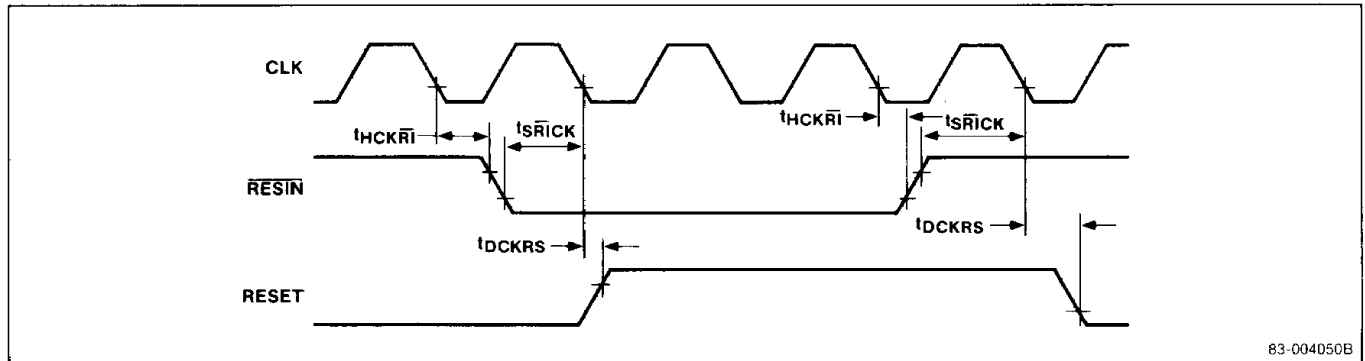


Clock Output

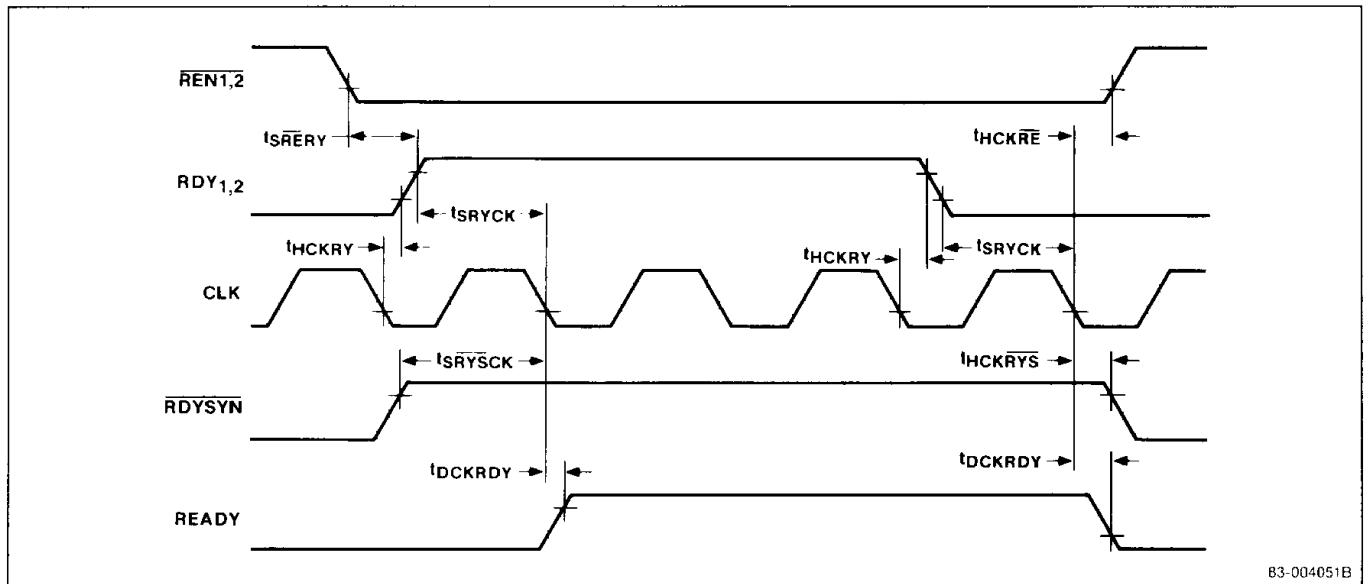


Timing Waveforms (cont)

RESET Pin



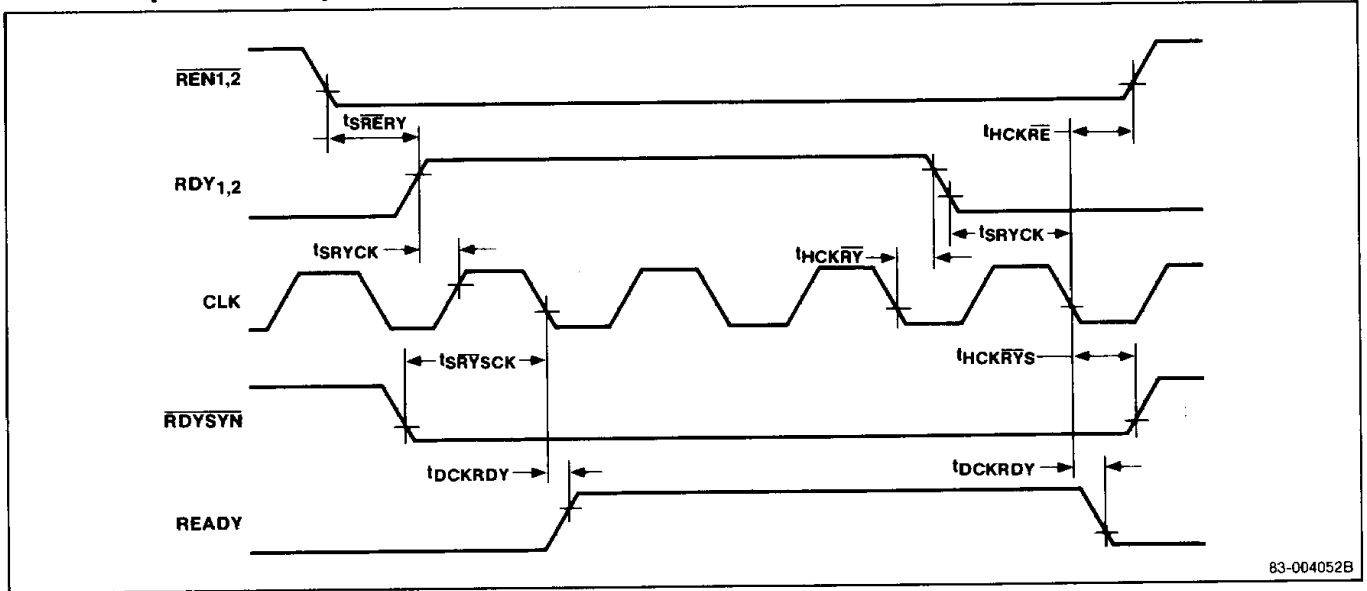
READY Pin ($\overline{RDYSYN} = 'H'$)



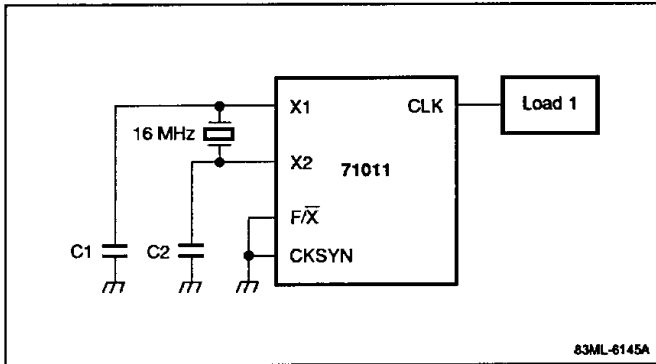
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Timing Waveforms (cont)

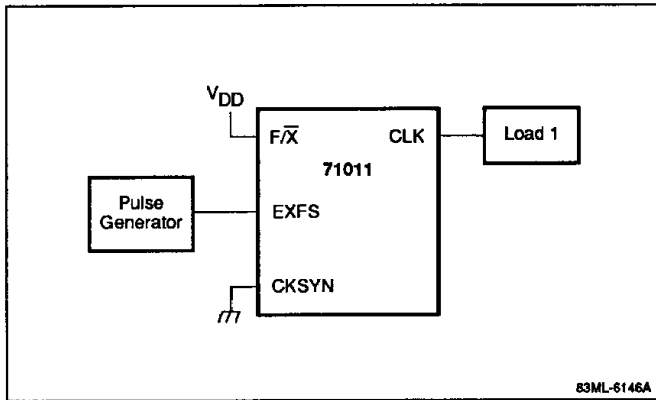
READY Pin ($\overline{RDYSYN} = 'L'$)



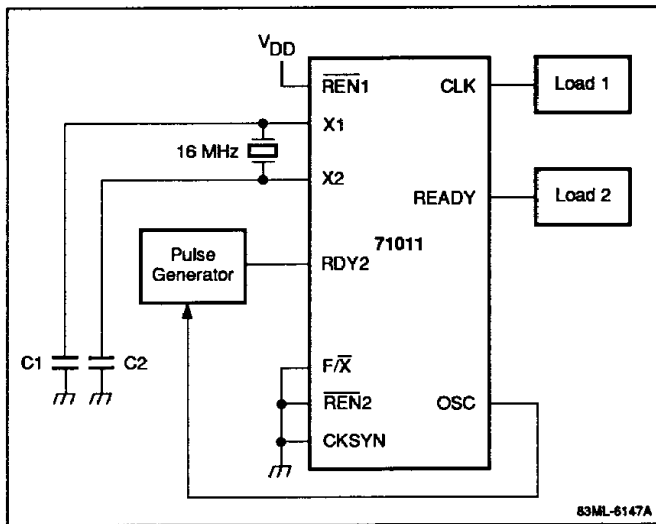
**Test Circuit for CLK High or Low Time
(in Crystal Oscillation Mode)**



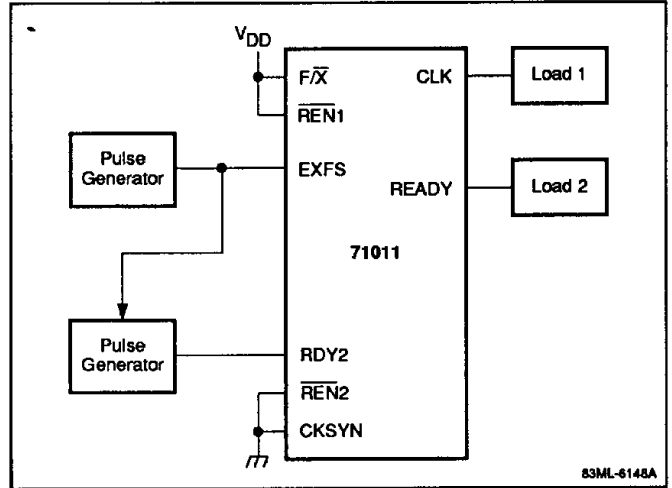
**Test Circuit for CLK High or Low Time
(in EXFS Oscillation Mode)**



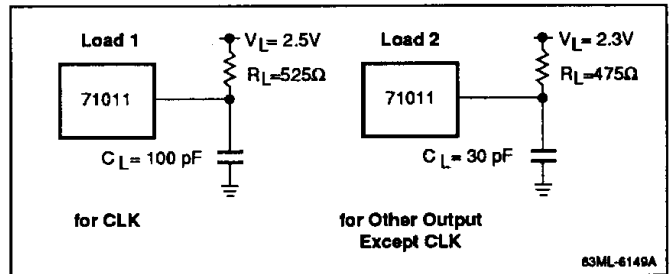
**Test Circuit for CLK to READY
(in Crystal Oscillation Mode)**



**Test Circuit for CLK to READY
(in EXFS Oscillation Mode)**



Loading Circuits



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