VMX1C1020

Datasheet *Rev 2.12*

Versa Mix 8051 Mixed-Signal MCU

Overview

The VMX51C1020 is a fully integrated mixed-signal microcontroller that provides a “one-chip solution” for a broad range of signal conditioning, data acquisition, processing, and control applications. The VMX51C1020 is based on a powerful single-cycle, RISC-based, 8051 microprocessor with an enhanced MULT/ACCU unit that can be used to perform complex mathematical operations.

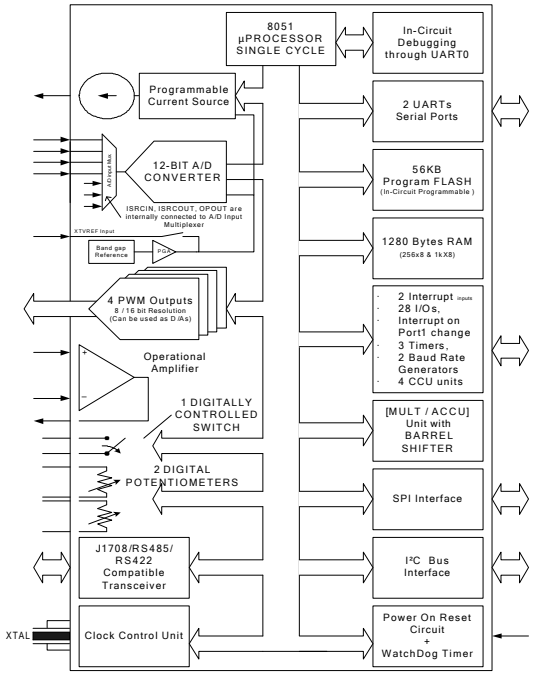
On-chip analog peripherals such as: an A/D converter, PWM outputs (that can be used as D/A converters), a voltage reference, a programmable current source, an uncommitted operational amplifier, digital potentiometers and an analog switch makes the VMX51C1020 ideal for analog data acquisition applications.

The inclusion of a full set of digital interfaces such as an enhanced fully configurable SPI, an I^2C interface, UARTs and a J1708/RS-485/RS-422 compatible differential transceiver, enables total system integration.

Applications

- Automotive Applications
- Industrial Controls / Instrumentation
- Consumer Products
- Intelligent Sensors
- Medical Devices

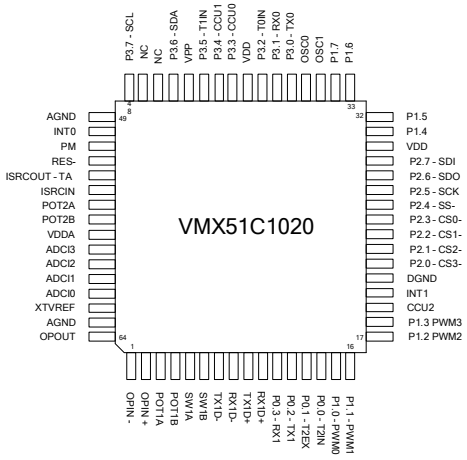
FIGURE 1: VMX51C1020 BLOCK DIAGRAM



Feature Set

- 8051 Compatible RISC performance Processor.
- Integrated Debugger
- 56KB Flash Program Memory
- 1280 Bytes of RAM
- MULT/ACCU unit including a Barrel Shifter
  - Provides DSP capabilities
- 2 UART Serial Ports
- 2 Baud Rate Generators for UARTs
- Differential Transceiver connected to UART1 J1708/RS-485/RS-422 compatible.
- Enhanced SPI interface (Master/Slave)
  - Fully Configurable
  - Controls up to 4 slave devices
- I2C interface
- 28 General Purpose I/Os
- 2 External Interrupt Inputs
- Interrupt on Port 1 pin change
- 3, 16-bit Timers/Counters
- 4 Compare & Capture Units with 3 Capture Inputs
- 4 PWM outputs, 8-bit / 16-bit resolution
- 4 ext. + 3 int. Channel 12-bit A/D Converter
  - Conversion rate up to 10kHz
  - 0-2.7 Volt Input range Continuous / One-Shot operation
  - Single or 4-channel automatic sequential conversions
- On-Chip Voltage Reference
- Programmable Current Source
- Operational Amplifier
- 2 Digital Potentiometers
- 1 Digitally Controlled Switch
- Power Saving Features + Clock Control
- Power-on Reset with Brown-Out Detect
- Watchdog Timer

FIGURE 2: VMX51C1020 QFP-64 PACKAGE PINOUT



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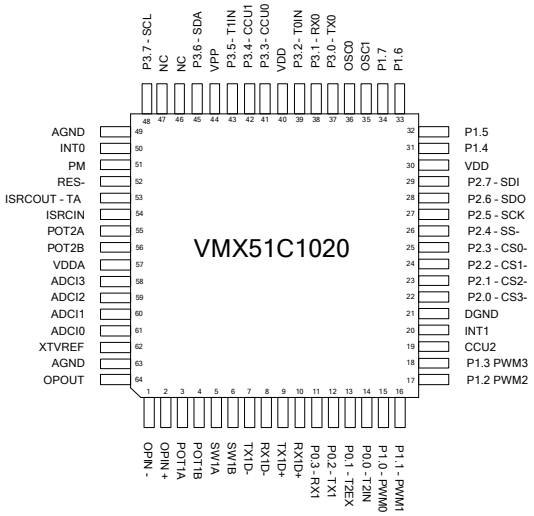
VMX51C1020 Pins Description

Table 1: Pin out description

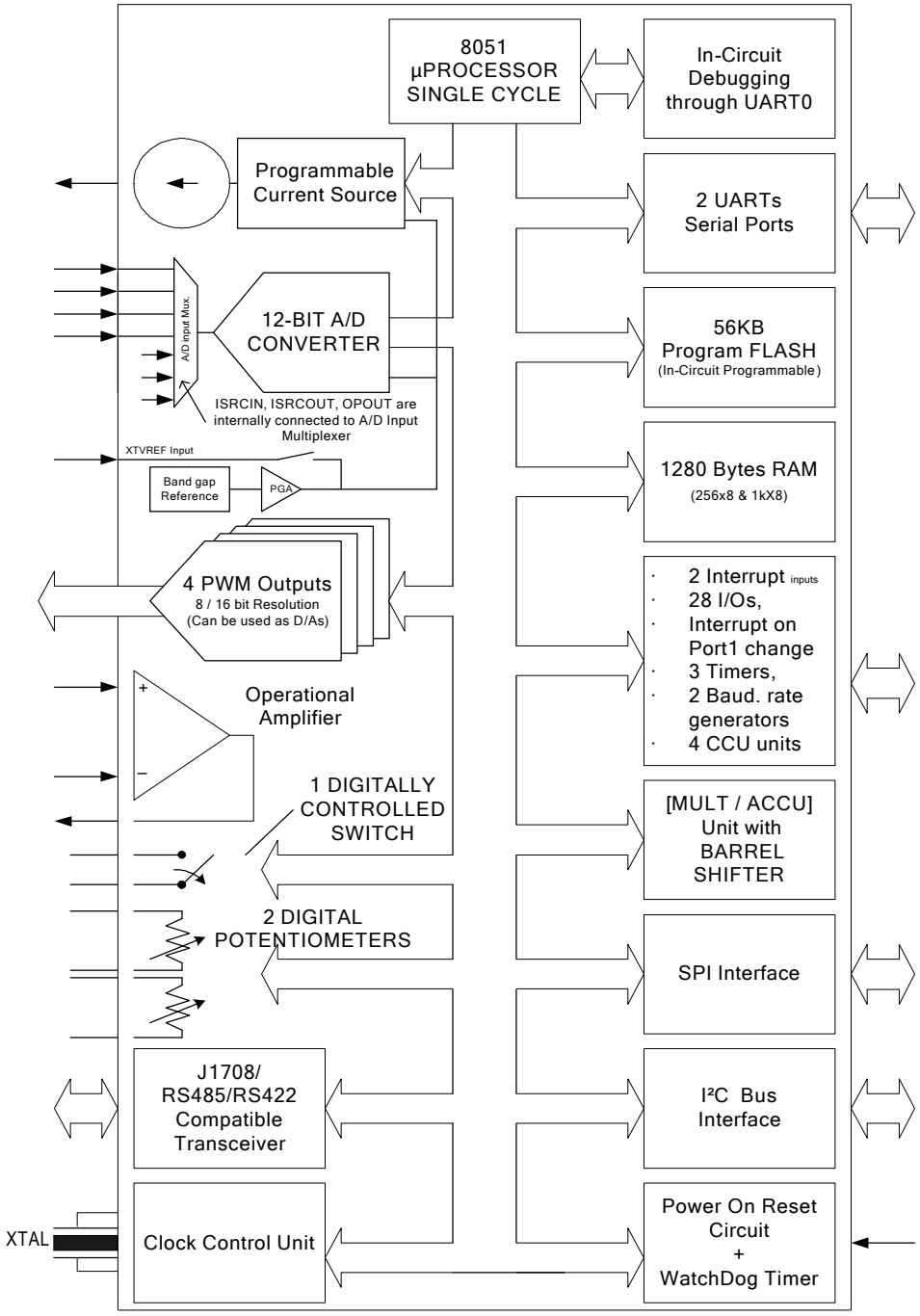
PIN	NAME	FUNCTION
1	OPIN-	Inverting Input of the Operational Amplifier
2	OPIN+	Non-inverting Input of the Operational Amplifier
3	POT1A	Digitally Controlled Potentiometer 1A
4	POT1B	Digitally Controlled Potentiometer 1B
5	SW1A	Digitally Controlled Switch 1A
6	SW1B	Digitally Controlled Switch 1B
7	TX1D-	RS-485/RS422 compatible differential Transmitter, Negative side
8	RX1D-	RS-485/RS422 compatible differential Receiver Negative side
9	TX1D+	RS-485/RS422 compatible differential Transmitter, Positive side
10	RX1D+	RS-485/RS422 compatible differential Receiver Positive side
11	P0.3-RX1	I/O - Asynchronous UART1 Receiver Input
12	P0.2-TX1	I/O - Asynchronous UART1 Transmitter Output
13	P0.1-T2EX	I/O -Timer/Counter 2 Input
14	P0.0-T2IN	I/O -Timer/Counter 2 Input
15	P1.0-PWM0	I/O - Pulse Width Modulator output 0
16	P1.1-PWM1	I/O - Pulse Width Modulator output 1
17	P1.2-PWM2	I/O - Pulse Width Modulator output 2
18	P1.3-PWM3	I/O - Pulse Width Modulator output 3
19	CCU2	Capture and Compare Unit 2 Input
20	INT1	Interrupt Input 1
21	DGND	Digital Ground
22	P2.0-CS3-	I/O - SPI Chip Enable Output (Master Mode)
23	P2.1-CS2-	I/O - SPI Chip Enable Output (Master Mode)
24	P2.2-CS1-	I/O - SPI Chip Enable Output (Master Mode)
25	P2.3-CS0-	I/O - SPI Chip Enable Output (Master Mode)
26	P2.4-SS-	I/O - SPI Chip Enable Output (Slave Mode)
27	P2.5-SCK	I/O - SPI Clock (Input in Slave Mode)
28	P2.6-SDO	I/O - SPI Data Output Bus
29	P2.7-SDI	I/O - SPI Data Input Bus
30	VDD	Digital Supply
31	P1.4	I/O
32	P1.5	I/O
33	P1.6	I/O
34	P1.7	I/O
35	OSC1	Oscillator Crystal Output
36	OSC0	Oscillator Crystal input/External Clock Source Input
37	P3.0-TX0	I/O - Asynchronous UART0 Transmitter Output
38	P3.1-RX0	I/O - Asynchronous UART0 Receiver Input
39	P3.2-T0IN	I/O - Timer/Counter 0 Input
40	VDD	5V Digital
41	P3.3-CCU0	I/O - Capture and Compare Unit 0 Input
42	P3.4-CCU1	I/O - Capture and Compare Unit 1 Input
43	P3.5-T1IN	I/O - Timer/Counter 1 Input
44	VPP	Flash Programming Voltage Input
45	P3.6-SDA	I/O - I2C / Prog. Interface Bi-Directional Data Bus
46	NC	Not Connected, leave floating
47	NC	Not Connected
48	P3.7-SCL	I/O - I2C / Prog. Interface Clock
49	AGND	Analog Ground
50	INT0	External interrupt Input (Negative Level or Edge Triggered)
51	PM	Mode Control Input
52	RES-	Hardware Reset Input (Active low)
53	ISRCOUT-TA	Programmable Current Source Analog Output
54	ISRCIN	Programmable Current Source Input
55	POT2A	Digitally Controlled Potentiometer 2A
56	POT2B	Digitally Controlled Potentiometer 2B
57	VDDA	Analog Supply
58	ADCI3	Analog to Digital Converter ext. Input 3
59	ADCI2	Analog to Digital Converter ext. Input 2
60	ADCI1	Analog to Digital Converter ext. Input 1
61	ADCI0	Analog to Digital Converter ext. Input 0
62	XTVREF	External Reference Voltage Input
63	AGND	Analog Ground
64	OPOUT	Output of the Operational Amplifier

FIGURE 3: VMX51C1020 PINOUT



VMX51C1020 Block Diagram

FIGURE 4: VMX51C1020 BLOCK DIAGRAM



Absolute Maximum Ratings

V_{DD} to DGND	–0.3V, +6V	Digital Output Voltage to DGND	–0.3V, V_{DD}+0.3V
V_{DDA} to DGND	-0.3V, +6V	V_{PP} to DGND	+13V
AGND to DGND	–0.3V, +0.3V	Power Dissipation	
V_{DD} to V_{DDA}	-0.3V, +0.3V	▪ To +70°C	1000mW
ADCI (0-3) to AGND	-0.3V, V_{DDA}+0.3V		
XTVREF to AGND	-0.3V, V_{DDA}+0.3V	Operating Temperature Range	0° to +70°C
Digital Input Voltage to DGND	-0.3V, V_{DD}+0.3V	Storage Temperature Range	–65°C to +110°C
RS422/485 Minimum and Maximum Voltages	-2V, +7V	Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

TABLE 2: ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS (V_{DD} = +5V, V_{DDA} = +5V, T_A = +25°C, 14.75MHz input clock, unless otherwise noted.)						
Power Supply Voltage	V_{DD}		4.75	5.0	5.5	V
	V_{DDA}		4.5	5.0	5.5	V
Power Supply Current	$I_{DD\ (14.75MHz)}$		5		45*	mA
	$I_{DD\ (1MHz)}$		0.6		6*	*Depends on clock speed and peripheral use and load
	I_{DDA}		0.1		5*	
Flash Programming Voltage	V_{PP}		11		13	V
DIGITAL INPUTS						
Minimum High-Level input	V_{IH}	V_{DD} = +5V		2.0		V
Maximum Low-Level input	V_{IL}	V_{DD} = +5V		0.8		V
Input Current	I_{IN}			±0.05		µA
Input Capacitance	C_{IN}			5	10	pF
DIGITAL OUTPUTS						
Minimum High-Level Output Voltage	V_{OH}	I_{SOURCE} = 4mA		4.2		V
Maximum Low-Level Output Voltage	V_{OL}	I_{SINK} = 4mA		0.2		V
Output Capacitance	C_{OUT}			10	15	Pf
Tri-state Output Leakage Current	I_{OZ}				0.25	µA

ANALOG INPUTS						
ADCI(0-3) Input Voltage Range	V_{ADCI}		0		2.7	V
ADCI(0-3) Input Resistance	R_{ADCI}			100		Mohms (design)
ADCI(0-3) Input Capacitance	C_{ADCI}			7		pF
ADCI(0-3) Input Leakage Current	I_{ADCI}			TBD		nA
Channel-to-Channel Crosstalk					-72 (12 bit)	dB (design)
ANALOG OUTPUT						
TA Output Drive Capabilities (Maximum Load Resistance)	$V_{TA}=V_{ADCI(0-3)}$		10			kOhms
	Others	Requires buffering		25M		
CURRENT SOURCE						
ISRC Current Drive $REF_{ISRC200}$	$I_{ISRC200}$			33	66	µA (design)
ISRC Current Drive $REF_{ISRC800}$	$I_{ISRC800}$			133	500	µA
ISRC Feedback voltage 200mV	$REF_{ISRC200}$		195		205	mV
ISRC Feedback voltage 800mV	$REF_{ISRC800}$		799		803	mV
ISRC Output Resistance	R_{ISRC}			50		MOhms
ISRC Output Capacitance	C_{ISRC}			25		pF
ISRCIN Input Reference Resistance	R_{RESIN}			100		Mohms
ISRCIN Input Reference Capacitance	C_{RESIN}			7		pF
ISRC stability	Drift				2.5	%
Allowable sensor capacitance between ISRCIN & ISRCOUT					1000	PF
Allowable capacitance between ISRCOUT & GND					100	pF
INTERNAL REFERENCE						
Bandgap Reference Voltage			1.18	1.23V	1.28	V
Bandgap Reference Tempco				100		ppm/°C
EXTERNAL REFERENCE						
Input Impedance	R_{XTVREF}			150		kOhms
PGA						
PGA Gain adjustment			2.11		2.29	
ANALOG TO DIGITAL CONVERTER **External Reference, TA=25C, Fosc = 14.75MHz**						
ADC Resolution				12		Bits
Differential Non linearity	DNL				±1.5	LSB
Integral Non linearity	INL		-1		+4	LSB
Full-Scale Error (Gain Error)		All channels, ADCI(0-3)		±4		LSB
Offset Error		All channels, ADCI(0-3)		±1		LSB
Channel-to-Channel Mismatch		All channels, ADCI(0-3)		±1		LSB
Sampling Rate		Single Channel	1		10k	Hz
		4 Channels	1		2.5k	
UART1 DIFFERENTIAL TRANSCEIVER COMPATIBLE TO J1708/ RS-485/RS-422						
Common mode Input Voltage	Vc_I		-2		+7	V
Input Impedance	Z_{IN}			1		MOhms
Output Drive Current				30		mA
Differential Input				100mV		mV

OPERATIONAL AMPLIFIER						
Output Impedance	Zout			20		mOhms
Input Resistance	Zin		36			GOhms
Voltage Gain	G_v			100		dB
Unit Gain Bandwidth	UGBW			5		MHz
Load Resistance to Ground					1	KOhms
Load Capacitance				40		pF
Slew rate	SR			7		V/µs (Design)
Input Offset Voltage	V_{IO}			+/- 2		mV
Input Voltage Range	$V_{I®}$		0		4	V (Design)
Common Mode Rejection Ratio	CMRRdc	DC	83		99	dB
	CMRR1kHz	Taken at 1kHz		75		dB Design)
Power Supply Rejection Ratio	PSRR	Taken at 1kHz (20dB/decade)	-75 (Vdd)		-94 (Vss)	dB (Design)
Output Voltage Swing (RL=10k)	$V_{O\ (P-P)}$		25mV		4.975	V
Short Circuit Current to ground	I_{IC}			86		mA (Design)
DIGITAL POTENTIOMETERS						
Number of Steps (8-bit binary weighted)				256		steps
Maximum Resistance			28k	30k	32k	Ohms
Minimum Resistance			485	510	535	Ohms
Step size			105	115	130	Ohms
Inter channel Matching				1		%
Temperature Coefficient				0.16		%/°C
Allowable current (DC)					5	mA
Inherent Capacitance				3		pF
DIGITAL SWITCH						
Switch on Resistance			50		100	Ohms (+/-10%)
Input capacitance				4		pF
Voltage range on Pin			0		5	V
Allowable current (DC)					5	mA
BROWN OUT / RESET CIRCUIT						
Brown-out circuit Threshold			3.7		4.0	V
RES- pin internal Pull-Up				20		KOhms

Detailed Description

The following sections will describe the VMX51C1020's architecture and peripherals.

FIGURE 5: INTERFACE DIAGRAM FOR THE VMX51C1020

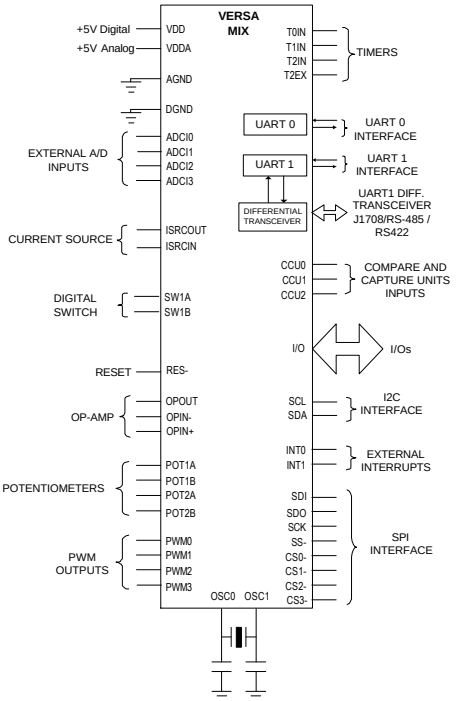
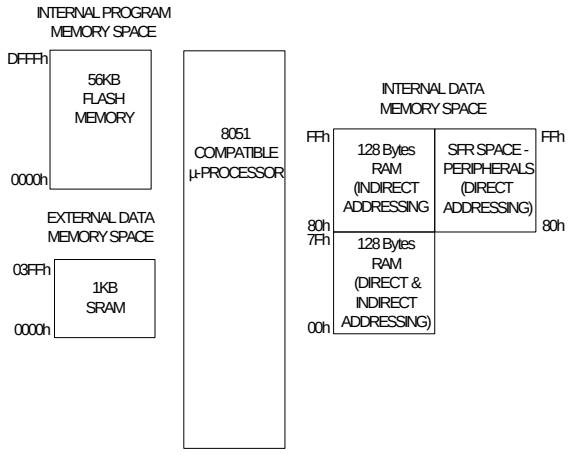


FIGURE 6: MEMORY ORGANIZATION OF THE VMX51C1020



Memory Organization

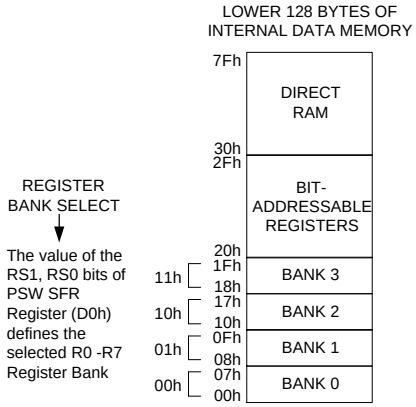
Figure 6 shows the memory organization of the VMX51C1020.

At power-up/reset, the code is executed from the 56Kx8 Flash memory mapped into the processor's internal Program space.

A 1KB block of RAM is also mapped into the external data memory of the VMX51C1020. This block can be used as general-purpose scratch pad or storage memory. A 256 byte block of RAM is mapped to the internal data memory space. This block of RAM is broken into 2 sub-blocks, with the upper block accessible via indirect addressing and the lower block accessible via both direct and indirect addressing.

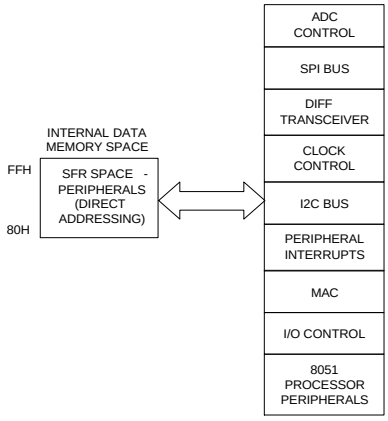
The following figure describes the access to the lower block of 128 bytes.

FIGURE 7: LOWER 128 BYTES BLOCK INTERNAL MEMORY MAP



The SFR (Special Function Register) space is also mapped into the upper 128 bytes of internal data memory space. This SFR space is only accessible using direct-access. The SFR space provides the interface to all the on-chip peripherals. This interfacing is illustrated in Figure 8.

FIGURE 8: SFR ORGANIZATION



Dual Data Pointers

The VMX51C1020 includes two data pointers.

The first data pointer (DPTR0) is mapped into SFR locations 82h and 83h and the second data pointer (DPTR1) mapped into SFR locations 84h and 85h. The SEL bit in the data pointer select register, DPS (SFR 86h), selects which data pointer is active. When SEL = 0, instructions that use the data pointer will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is located in bit 0 of the DPS (SFR location 86h - the remaining bits of SFR location 86h are un-used.

All DPTR-related instructions use the currently selected data pointer. In order to switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS).

The use of the two data pointers can significantly increase the speed of moving large blocks of data because only one instruction is needed to switch from a source address and destination address.

The SFR locations and register representations related to the dual data pointers are outlined as follows:

TABLE 3: (DPH0) DATA POINTER HIGH 0 - SFR 83H

15	14	13	12	11	10	9	8
DPH0 [7:0]							

TABLE 4: (DPL0) DATA POINTER LOW 0 - SFR 82H

7	6	5	4	3	2	1	0
DPL0 [7:0]							

Bit	Mnemonic	Function
15-8	DPH0	Data Pointer 0 MSB
7-0	DPL0	Data Pointer LSB.

TABLE 5: (DPH1) DATA POINTER HIGH 1 - SFR 85H

15	14	13	12	11	10	9	8
DPH1 [7:0]							

TABLE 6: (DPL1) DATA POINTER LOW 1 - SFR 84H

7	6	5	4	3	2	1	0
DPL1 [7:0]							

Bit	Mnemonic	Function
15-8	DPH1	Data Pointer 1 MSB.
7-0	DPL1	Data Pointer 1 LSB.

TABLE 7: (DPS) DATA POINTER SELECT REGISTER - SFR 86H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEL

Bit	Mnemonic	Function
7-1	0	Always zero
0	SEL	0 = DPTR0 is selected 1 = DPTR1 is selected Used to toggle between both data pointers

MPAGE Register

The MPAGE register controls the upper 8 bits of the targeted address when the MOVX instruction is used for external RAM data transfer. This allows access to the entire external RAM content without using the Data Pointer.

TABLE 8: (MPAGE) MEMORY PAGE - SFR CFH

7	6	5	4	3	2	1	0
MPAGE [7:0]							

User Flags

The VMX51C1020 provides an SFR register that gives the user the ability to define software flags. Each bit of this register is individually addressable. This register may also be used as a general-purpose storage location. Thus, the user flag feature allows the VMX51C1020 to better adapt to each specific application. This register is located at SFR address F8h

TABLE 9: (USERFLAGS) USER FLAG - SFR F8H

7	6	5	4	3	2	1	0
UF7	UF6	UF5	UF4	UF3	UF2	UF1	UF0

Instruction Set

All VMX51C1020 instructions are function and binary code compatible with the industry standard 8051. However, the timing of instructions may be different. The following two tables describe the instruction set of the VMX51C1020.

TABLE 10: LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 11: VMX51C1020 INSTRUCTION SET

Mnemonic	Description	Size (bytes)	Instr. Cycles
Arithmetic instructions			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add data memory to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add data memory to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract data mem from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	2
INC direct	Increment direct byte	2	3
INC @Ri	Increment data memory	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	2
DEC direct	Decrement direct byte	2	3
DEC @Ri	Decrement data memory	1	3
INC DPTR	Increment data pointer	1	1
MUL AB	Multiply A by B	1	5
DIV AB	Divide A by B	1	5
DA A	Decimal adjust A	1	1
Logical Instructions			
ANL A, Rn	AND register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND data memory to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	3
ANL direct, #data	AND immediate data to direct byte	3	4
ORL A, Rn	OR register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR data memory to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	3
ORL direct, #data	OR immediate data to direct byte	3	4
XRL A, Rn	Exclusive-OR register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR data memory to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	3
XRL direct, #data	Exclusive-OR immediate to direct byte	3	4
CLR A	Clear A	1	1
CPL A	Compliment A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer Instructions			
MOV A, Rn	Move register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move data memory to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to register	1	2
MOV Rn, direct	Move direct byte to register	2	4
MOV Rn, #data	Move immediate to register	2	2
MOV direct, A	Move A to direct byte	2	3
MOV direct, Rn	Move register to direct byte	2	3
MOV direct, direct	Move direct byte to direct byte	3	4
MOV direct, @Ri	Move data memory to direct byte	2	4
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to data memory	1	3
MOV @Ri, direct	Move direct byte to data memory	2	5
MOV @Ri, #data	Move immediate to data memory	2	3
MOV DPTR, #data16	Move immediate 16 bit to data pointer	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (A8) to A	1	3-10
MOVX A, @DPTR	Move external data (A16) to A	1	3-10
MOVX @Ri, A	Move A to external data (A8)	1	4-11
MOVX @DPTR, A	Move A to external data (A16)	1	4-11
PUSH direct	Push direct byte onto stack	2	4
POP direct	Pop direct byte from stack	2	3
XCH A, Rn	Exchange A and register	1	2
XCH A, direct	Exchange A and direct byte	2	3
XCH A, @Ri	Exchange A and data memory	1	3
XCHD A, @Ri	Exchange A and data memory nibble	1	3
Branching Instructions			
ACALL addr 11	Absolute call to subroutine	2	6
LCALL addr 16	Long call to subroutine	3	6
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr 11	Absolute jump unconditional	2	3
LJMP addr 16	Long jump unconditional	3	4
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JB bit, rel	Jump on direct bit = 1	3	4
JNB bit, rel	Jump on direct bit = 0	3	4
JBC bit, rel	Jump on direct bit = 1 and clear	3	4
JMP @A+DPTR	Jump indirect relative DPTR	1	2
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump when accumulator not equal to 0	2	3
CJNE A, direct, rel	Compare A, direct JNE relative	3	4
CJNE A, #data, rel	Compare A, immediate JNE relative	3	4
CJNE Rn, #data, rel	Compare reg, immediate JNE relative	3	4
CJNE @Ri, #data, rel	Compare ind, immediate JNE relative	3	4
DJNZ Rn, rel	Decrement register, JNZ relative	2	3
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4
Bit Operations			
CLR C	Clear carry flag	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry flag	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry Flag	1	1
CPL bit	Complement direct bit	2	3
ANL C,bit	Logical AND direct bit to carry flag	2	2
ANL C, /bit	Logical AND between /bit and carry flag	2	2
ORL C,bit	Logical OR bit to carry flag	2	2
ORL C, /bit	Logical OR /bit to carry flag	2	2
MOC c,bit	Copy direct bit location to carry flag	2	2
MOV bit,C	Copy carry flag to direct bit location	2	3
Miscellaneous Instruction			
NOP	No operation	1	1

Special Function Registers

The Special Function Registers (SFRs) control several features of the VMX51C1020. Many of the VMX51C1020 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control the VMX51C1020's specific peripheral features that are not available in the standard 8051.

TABLE 12: SPECIAL FUNCTION REGISTERS

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
P0	80h	-	-	-	-	-	-	-	-	1111 1111b
SP	81h	-	-	-	-	-	-	-	-	0000 0111b
DPL0	82h	-	-	-	-	-	-	-	-	0000 0000b
DPH0	83h	-	-	-	-	-	-	-	-	0000 0000b
DPL1	84h	-	-	-	-	-	-	-	-	0000 0000b
DPH1	85h	-	-	-	-	-	-	-	-	0000 0000b
DPS	86h	0	0	0	0	0	0	0	SEL	0000 0000b
PCON	87h	SMOD	-	-	-	GF1	GF0	STOP	IDLE	0000 0000b
TCON*	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000b
TMOD	89h	GATE1	CT1	M11	M01	GATE0	CT0	M10	M00	0000 0000b
TL0	8Ah	-	-	-	-	-	-	-	-	0000 0000b
TL1	8Bh	-	-	-	-	-	-	-	-	0000 0000b
TH0	8Ch	-	-	-	-	-	-	-	-	0000 0000b
TH1	8Dh	-	-	-	-	-	-	-	-	0000 0000b
Reserved	8Eh									0000 0000b
Reserved	8Fh									0000 0000b
P1*	90h	-	-	-	-	-	-	-	-	1111 1111b
IRCON	91h	T2EXIF	T2IF	ADCIF/ COMPINT3	MACIF/ COMPINT2	I2CIF/ COMPINT1	SPIRXIF/ COMPINT0	SPITXIF	Reserved	0000 0000b
ANALOGPWREN	92h	OPAMPEN	DIGPOTEN	ISRCSEL	ISRCEN	TAEN	ADCEN	PGAEN	BGAPEN	0000 0000b
DIGPWREN	93h	T2CLKEN	WDOGEN	MACEN	I2CEN	SPIEN	UART1DIFFEN	UART1EN	UART0EN	0000 0000b
CLKDIVCTRL	94h	SOFTRST	-	-	IRQNORMSPD	MCKDIV_3	MCKDIV_2	MCKDIV_1	MCKDIV_0	0000 0000b
ADCCLKDIV	95h	-	-	-	-	-	-	-	-	0000 1100b
S0RELL	96h	-	-	-	-	-	-	-	-	11011001b
S0RELH	97h	0	0	0	0	0	0	-	-	0000 0011b
S0CON*	98h	S0M0	S0M1	MPCE0	R0EN	T0B8	R0B8	T0I	R0I	0000 0000b
S0BUF	99h	-	-	-	-	-	-	-	-	0000 0000b
IEN2	9Ah	-	-	-	-	-	-	-	S1IE	0000 0000b
P0PINCFG	9Bh	P07IO	P06IO	P05IO	P04IO	P0.3/RX1INE	P0.2/TX1OE	P0.1/T2EXINE	P0.0/T2INE	0000 0000b
P1PINCFG	9Ch	P1.7	P1.6	P1.5	P1.4	P1.3/PWM3OE	P1.2/PWM2OE	P1.1/PWM1OE	P1.0/PWM0OE	0000 0000b
P2PINCFG	9Dh	P2.7/SDIEN	P2.6/SDOEN	P2.5/SCKEN	P2.4/SSEN	P2.3/CS0EN	P2.2/CS1EN	P2.1/CS2EN	P2.0/CS3EN	0000 0000b
P3PINCFG	9Eh	P3.7/MSCLEN	P3.6/MSDAEN	P3.5/T1INEN	P3.4/CCU1EN	P3.3/CCU0EN	P3.2/T0INEN	P3.1/RX0EN	P3.0/TX0EN	0000 0000b
PORTIRQEN	9Fh	P17IEN	P16IEN	P15IEN	P14IEN	P13IEN	P12IEN	P11IEN	P10IEN	0000 0000b
P2*	A0h	-	-	-	-	-	-	-	-	1111 1111b
PORTIRQSTAT	A1h	P17ISTAT	P16ISTAT	P15ISTAT	P14ISTAT	P13ISTAT	P12ISTAT	P11ISTAT	P10ISTAT	0000 0000b
ADCCTRL	A2h	ADCIRQCLR	XVREFCAP	1	ADCIRQ	ADCIE	ONECHAN	CONT	ONESHOT	0000 0000b
ADCCONVRLOW	A3h	-	-	-	-	-	-	-	-	0000 0000b
ADCCONVRMED	A4h	-	-	-	-	-	-	-	-	0000 0000b
ADCCONVRHIGH	A5h	-	-	-	-	-	-	-	-	0000 0000b
ADCD0LO	A6h	-	-	-	-	-	-	-	-	0000 0000b
ADCD0HI	A7h					ADCD0HI_3	ADCD0HI_2	ADCD0HI_1	ADCD0HI_0	0000 0000b
IEN0*	A8h	EA	WDT	T2IE	S0IE	T1IE	INT1IE	T0IE	INT0IE	0000 0000b
ADCD1LO	A9h	-	-	-	-	-	-	-	-	0000 0000b
ADCD1HI	AAh					ADCD1HI_3	ADCD1HI_2	ADCD1HI_1	ADCD1HI_0	0000 0000b
ADCD2LO	ABh	-	-	-	-	-	-	-	-	0000 0000b
ADCD2HI	ACh					ADCD2HI_3	ADCD2HI_2	ADCD2HI_1	ADCD2HI_0	0000 0000b
ADCD3LO	ADh	-	-	-	-	-	-	-	-	0000 0000b
ADCD3HI	AEh					ADCD3HI_3	ADCD3HI_2	ADCD3HI_1	ADCD3HI_0	0000 0000b
Reserved	AFh									0000 0000b
P3*	B0h	-	-	-	-	-	-	-	-	1111 1111b
Reserved	B1h									1101 0001b
Reserved	B2h									0000 0000b
BGAPCAL	B3h	-	-	-	-	-	-	-	-	Cal. Vector
PGACAL	B4h	-	-	-	-	-	-	-	-	Cal. Vector
INMUXCTRL	B5h	-	ADCINSEL_2	ADCINSEL_1	ADCINSEL_0	AINEN_3	AINEN_2	AINEN_1	AINEN_0	0000 0000b
OUTMUXCTRL	B6h	-	-	-	-	-	TAOUTSEL_2	TAOUTSEL_1	TAOUTSEL_0	0000 0000b
SWITCHCTRL	B7h	-	-	-	-	SWITCH1_3	SWITCH1_2	SWITCH1_1	SWITCH1_0	0000 0000b
IP0*	B8h	UF8	WDTSTAT	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	0000 0000b
IP1	B9h	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	0000 0000b
DIGPOT1	BAh	-	-	-	-	-	-	-	-	0000 0000b

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
DIGPOT2	BBh	-	-	-	-	-	-	-	-	0000 0000b
ISRCCAL1	BCh	PGACAL0	ISRCCAL1_6	ISRCCAL1_5	ISRCCAL1_4	ISRCCAL1_3	ISRCCAL1_2	ISRCCAL1_1	ISRCCAL1_0	Cal. Vector
ISRCCAL2	BDh	-	ISRCCAL2_6	ISRCCAL2_5	ISRCCAL2_4	ISRCCAL2_3	ISRCCAL2_2	ISRCCAL2_1	ISRCCAL2_0	Cal. Vector
S1RELL	BEh	-	-	-	-	-	-	-	-	0000 0000b
S1RELH	BFh	-	-	-	-	-	-	-	-	0000 0000b
S1CON*	C0h	S1M	reserved	MPCE1	R1EN	T1B8	R1B8	T1I	R1I	0000 0000b
S1BUF	C1h	-	-	-	-	-	-	-	-	0000 0000b
CCL1	C2h	-	-	-	-	-	-	-	-	0000 0000b
CCH1	C3h	-	-	-	-	-	-	-	-	0000 0000b
CCL2	C4h	-	-	-	-	-	-	-	-	0000 0000b
CCH2	C5h	-	-	-	-	-	-	-	-	0000 0000b
CCL3	C6h	-	-	-	-	-	-	-	-	0000 0000b
CCH3	C7h	-	-	-	-	-	-	-	-	0000 0000b
T2CON*	C8h	T2PS	T2PSM	T2SIZE	T2RM1	T2RM0	T2CM	T2IN1	T2IN0	0000 0000b
CCEN	C9h	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0	0000 0000b
CRCL	CAh	-	-	-	-	-	-	-	-	0000 0000b
CRCH	CBh	-	-	-	-	-	-	-	-	0000 0000b
TL2	CCh	-	-	-	-	-	-	-	-	0000 0000b
TH2	CDh	-	-	-	-	-	-	-	-	0000 0000b
Reserved	CEh									
MPAGE	CFh	-	-	-	-	-	-	-	-	0000 0000b
PSW*	D0h	CY	AC	F0	RS1	RS0	OV	reserved	P	0000 0001b
Reserved	D1h To D7									D1h-D4h =FFh D5h-D7h = 00h
U0BAUD	D8h	BAUDSRC	-	-	-	-	-	-	-	0000 0000b
WDTREL	D9h	PRES	WDTREL_6	WDTREL_5	WDTREL_4	WDTREL_3	WDTREL_2	WDTREL_1	WDTREL_0	0000 0000b
I2CCONFIG	DAh	I2CMASKID	I2CRXOVIE	I2CRXDAVIE	I2CTXEMPIE	I2CMANACK	I2CACKMODE	I2CMSTOP	I2CMASTER	0000 0010b
I2CCLKCTRL	DBh	-	-	-	-	-	-	-	-	0000 0000b
I2CCHIPID	DCh	I2CID_6	I2CID_5	I2CID_4	I2CID_3	I2CID_2	I2CID_1	I2CID_0	I2CWID	0100 0010b
I2CIRQSTAT	DDh	I2CGOTSTOP	I2CNOACK	I2CSDA	I2CDATACK	I2CIDLE	I2CRXOV	I2CRXAV	I2CTXEMP	0010 1001b
I2CRXTX	DEh	-	-	-	-	-	-	-	-	0000 0000b
Reserved	DFh									0000 0000b
ACC*	E0h	-	-	-	-	-	-	-	-	1110 0000b
SPIRX3TX0	E1h	-	-	-	-	-	-	-	-	0000 0000b
SPIRX2TX1	E2h	-	-	-	-	-	-	-	-	0000 0000b
SPIRX1TX2	E3h	-	-	-	-	-	-	-	-	0000 0000b
SPIRX0TX3	E4h	-	-	-	-	-	-	-	-	0000 0000b
SPICTRL	E5h	SPICK_2	SPICK_1	SPICK_0	SPICS_1	SPICS_0	SPICKPH	SPICKPOL	SPIMA_SL	0000 0001b
SPICONFIG	E6h	SPICSLO	-	FSONCS3	SPI LOAD	-	SPIRXOVIE	SPIRXAVIE	SPITXEMPIE	0000 0000b
SPISIZE	E7h	-								0000 0111b
IEN1*	E8h	T2EXIE	SWDT	ADCPCIE	MACOVIE	I2CIE	SPIRXOVIE	SPITEIE	reserved	0000 0000b
SPIIRQSTAT	E9h	-	-	SPITXEMPTO	SPISLAVESEL	SPISEL	SPIOV	SPIRXAV	SPITXEMP	00011001b
Reserved	EAh									0000 0000b
MACCTRL1	EBh	LOADPREV	PREVMODE	OVMODE	OVRDVAL	ADDSRC_1	ADDSRC_0	MULCMD_1	MULCMD_0	0000 0000b
MACC0	ECh	-	-	-	-	-	-	-	-	0000 0000b
MACC1	EDh	-	-	-	-	-	-	-	-	0000 0000b
MACC2	EEh	-	-	-	-	-	-	-	-	0000 0000b
MACC3	EFh	-	-	-	-	-	-	-	-	0000 0000b
B*	F0h	-	-	-	-	-	-	-	-	0000 0000b
MACCTRL2	F1h	MACCLR2_2	MACCLR2_1	MACCLR2_0	MACOV32IE	-	-	MACOV16	MACOV32	0000 0000b
MACA0	F2h	-	-	-	-	-	-	-	-	0000 0000b
MACA1	F3h	-	-	-	-	-	-	-	-	0000 0000b
MACRES0	F4h	-	-	-	-	-	-	-	-	0000 0000b
MACRES1	F5h	-	-	-	-	-	-	-	-	0000 0000b
MACRES2	F6h	-	-	-	-	-	-	-	-	0000 0000b
MACRES3	F7h	-	-	-	-	-	-	-	-	0000 0000b
USERFLAGS*	F8h	UF7	UF6	UF5	UF4	UF3	UF2	UF1	UF0	0000 0000b
MACB0	F9h	-	-	-	-	-	-	-	-	0000 0000b
MACB1	FAh	-	-	-	-	-	-	-	-	0000 0000b
MACSHIFTCTRL	FBh	SHIFTMODE	ALSHSTYLE	SHIFTAMPL_5	SHIFTAMPL_4	SHIFTAMPL_3	SHIFTAMPL_2	SHIFTAMPL_1	SHIFTAMPL_0	0000 0000b
MACPREV0	FCh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV1	FDh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV2	FEh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV3	FFh	-	-	-	-	-	-	-	-	0000 0000b

* Bit addressable

Peripheral Activation Control

Digital Peripheral Power Enable

In order to save power upon reset, many of the digital peripherals of the VMX51C1020 are not activated. The peripherals affected by this feature are:

- Timer 2 / Port1
- Watchdog Timer
- MULT/ACCU unit
- I²C interface
- SPI interface
- UART0
- UART1
- Differential Transceiver

Before using any of the above-listed peripherals, they must first be enabled by setting the corresponding bit of the DIGPWREN SFR register to 1.

The same rule applies when accessing a given peripheral's SFR register(s). The targeted peripheral must have been powered on (enabled) first, otherwise the SFR register content will be ignored

The following table shows the structure of the DIGPWREN register.

TABLE 13: (DIGPWREN) DIGITAL PERIPHERALS POWER ENABLE REGISTER - SFR 93H

7	6	5	4
T2CLKEN	WDOGEN	MACEN	I2CEN

3	2	1	0
SPIEN	UART1DIFFEN	UART1EN	UART0EN

Bit	Mnemonic	Function
7	T2CLKEN	Timer 2 / PWM Enable 0 = Timer 2 CLK stopped 1 = Timer 2 CLK Running
6	WDOGEN	Watchdog Enable 0 = Watchdog Disable 1 = Watchdog Enable
5	MACEN	1 = MULT/ACCU Unit Enable 0 = MULT/ACCU Unit Disable
4	I2CEN	1= I2C Interface Enable 0 = I2C Interface Disable This bit is merged with CLK STOP bit
3	SPIEN	1 = SPI interface is Enable 0 = SPI interface is Disable
2	UART1DIFFEN	UART1 Differential mode 0 = Disable 1 = Enable
1	UART1EN	0 = UART1 Disable 1 = UART1 Enable
0	UART0EN	0 = UART0 Disable 1 = UART0 Enable

Analog Peripheral Power Enable

The analog peripherals, specifically, the op-amp digital potentiometer, current source and analog to digital converter, have a shared dedicated register used for enabling and disabling these peripherals. By default, these peripherals are powered down when the device is reset.

TABLE 14: (ANALOGPWREN) ANALOG PERIPHERALS POWER ENABLE REGISTER - SFR 92H

7	6	5	4
OPAMPEN	DIGPOTEN	ISRCSEL	ISRCEN

3	2	1	0
TAEN	ADCEN	PGAEN	BGAPEN

Bit	Mnemonic	Function
7	OPAMPEN	1 = User Op-Amp Enable 0 = User Op-Amp Disable
6	DIGPOTEN	1 = Digital Potentiometer and Switch Enable 0 = Digital Potentiometer and Switch Disable
5	ISRCSEL	0 = ISRC with 200mV feedback 1 = ISRC with 200mV feedback
4	ISRCEN	1 = ISRC Output Enable 0 = ISRC Output Disable
3	TAEN	1 = TA Output Enable 0 = TA Output Disable
2	ADCEN	1 = ADC Enable 0 = ADC Disable
1	PGAEN	1 = PGA Enable 0 = PGA Disable
0	BGAPEN	1 = Bandgap Enable 0 = Bandgap Disable

Note: The SFR registers associated with all analog peripherals are activated when one or more analog peripherals are enabled.

General Purpose I/O

The VMX51C1020 provides 28 general-purpose I/O pins. The I/Os are shared with digital peripherals and can be configured individually.

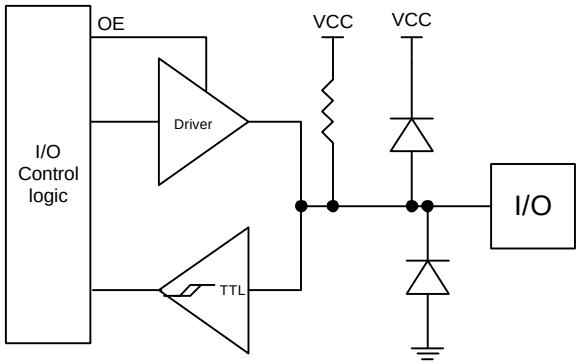
At Reset, all the VMX51C1020 I/O ports are configured as Inputs

The I/O Ports are bi-directional and the CPU can write or read data through any of these ports.

I/O Port Structure

The VMX51C1020 I/O port structure is shown in the following figure.

FIGURE 9 – I/O PORT STRUCTURE



Each I/O pin includes pull-up circuitry (represented by the internal pull-up resistor) and a pair of internal protection diodes connected to VCC and ground, providing ESD protection.

The I/O operational configuration is defined in the I/O control logic block.

I/O Port Drive Capability

Each I/O port pin, when configured as an output is able to source or sink up to 4mA. The following graphs show typical I/O output voltage vs. source and I/O output voltage versus sink current.

FIGURE 10: TYPICAL I/O VOUT VS. SOURCE CURRENT

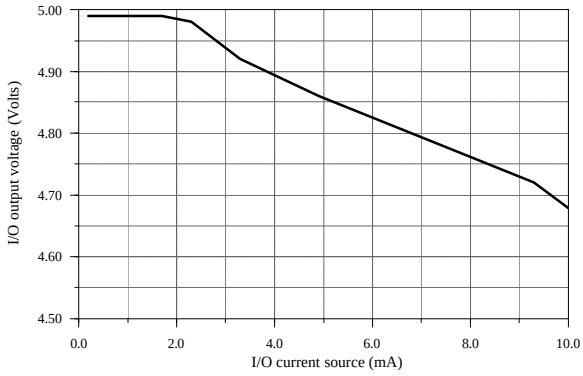
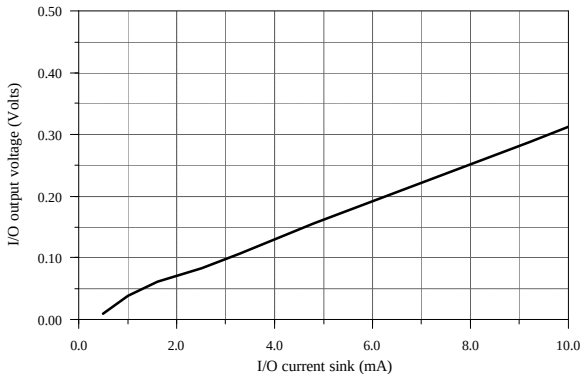


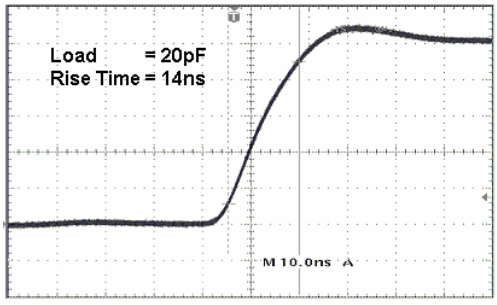
FIGURE 11: TYPICAL I/O VOUT VS. SINK CURRENT



The maximum recommended driving current of a single I/O on a given port is 10mA. The recommended limit when more than one I/O on a given port is driving current is 5mA on each I/O. The total current drive of all I/O ports should be limited to 40mA

The following figure shows typical I/O rise time when driving a 20pF capacitive load. In this case, rise time is about 14ns.

FIGURE 12: I/O RISE TIME WITH A 20PF LOAD



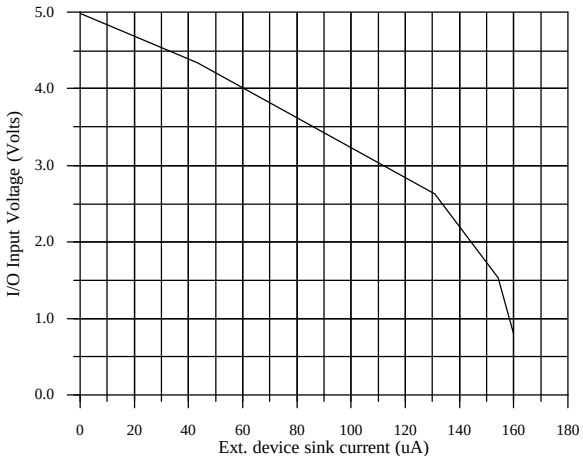
Input Voltage vs. Ext. device sink

The I/Os of the VMIX, when configured as Inputs, include an internal pull-up resistor made of a transistor that ensures the level present at the input is stable when the I/O pin is unconnected.

Due to the presence of the pull-up resistor on the digital inputs, the external device driving the I/O must be able to sink enough current to bring the I/O pin low.

The following figure shows the VMX51C1020 Input port voltage vs. external device sink current.

FIGURE 13: INPUT PORT VOLTAGE VS. EXT DEVICE SINK CURRENT



I/O Port Configuration Registers

The VMX51C1020's I/O port operation is controlled by two sets of four registers which are:

- The Port Pin Configuration registers
- The Port Access registers

The port pin configuration registers combined with specific peripheral configuration will define if a given pin acts as a general purpose I/O or if it provides alternate peripheral functionality.

Before using a peripheral that is shared with I/Os, the pin corresponding to the peripheral output must be configured as an output and the pins that are shared with the peripheral inputs must be configured as inputs.

The following registers are used to configure each of the ports as either general-purpose input, output or alternate peripheral function..

For example, when bit 5 of Port 2 is configured as an output, it will output the SCK signal if the SPI interface is enabled and working.

The only exception to this rule is the I^2C Clock and data bus signals. In these two cases, the VMX51C1020 configures the pins automatically as inputs or outputs.

The P0PINCFG register controls the I/O access to UART1, the Timer 2 input and output, as well as defines the direction of the P0 when used as general purpose I/O.

TABLE 15: (P0PINCFG) PORT 0 PORT CONFIGURATION REGISTER - SFR 9BH

7	6	5	4
P07IO	P06IO	P05IO	P04IO

3	2	1	0
P0.3/RX1INE	P0.2/TX1OE	P0.1/T2EXINE	P0.0/T2INE

Bit	Mnemonic	Function
7:4	P0xIO	Unavailable on VMX51C1020
3	P0.3/RX1INE	0: General purpose input or UART1 RX 1: General purpose output ***When using UART1 you must set this bit to 0.***
2	P0.2/TX1OE	0: General purpose input 1: General purpose output or UART1 TX ***When using UART1 you must set this bit to 1.***
1	P0.1/T2EXINE	0: General purpose input or Timer 2 EX 1: General purpose output ***When using Timer 2EX input you must set this bit to 0.***
0	P0.0/T2INE	0: General purpose input or Timer 2 IN 1: General purpose output ***When using Timer 2 input you must set this bit to 0.***

The P1PINCFG register controls the access from the PWM to the I/O pins as well as defines the direction of the P1 when the PWM's are not used.

TABLE 16: (P1PINCFG) PORT 1 PORT CONFIGURATION REGISTER - SFR 9CH

7	6	5	4
P1.7	P1.6	P1.5	P1.4

3	2	1	0
P1.3/PWM3OE	P1.2/PWM2OE	P1.1/PWM1OE	P1.0/PWM0OE

Bit	Mnemonic	Function
7	P1.7	0: General purpose input 1: General purpose output
6	P1.6	0: General purpose input 1: General purpose output
5	P1.5	0: General purpose input 1: General purpose output
4	P1.4	0: General purpose input 1: General purpose output
3	P1.3/PWM3OE	0: General purpose input 1: General purpose output or PWM bit 3 output ***When using PWM you must set this bit to 1.***
2	P1.2/PWM2OE	0: General purpose input 1: General purpose output or PWM bit 2 output ***When using PWM you must set this bit to 1***
1	P1.1/PWM1OE	0: General purpose input 1: General purpose output or PWM bit 1 output ***When using PWM you must set this bit to 1***
0	P1.0/PWM0OE	0: General purpose input 1: General purpose output or PWM bit 0 output ***When using PWM you must set this bit to 1***

The P2PINCFG register controls the I/O access to SPI interface and defines the direction of the P2 when used as general purpose I/O

TABLE 17: (P2PINCFG) PORT 2 PORT CONFIGURATION REGISTER - SFR 9DH

7	6	5	4
P2.7/SDIEN	P2.6/SDOEN	P2.5/SCKEN	P2.4/SSEN

3	2	1	0
P2.3/CS0EN	P2.2/CS1EN	P2.1/CS2EN	P2.0CS3EN

Bit	Mnemonic	Function
7	P2.7/SDIEN	0: General purpose input or SDI 1: General purpose output ***When using SPI you must set this bit to 0.***
6	P2.6/SDOEN	0: General purpose input 1: General purpose output or SDO ***When using SPI you must set this bit to 1.***
5	P2.5/SCKEN	0: General purpose input or SCK 1: General purpose output ***When using SPI you must set this bit to 0.***
4	P2.4/SSEN	0: General purpose input or Slave Select 1: General purpose output ***When using SPI SS you must set this bit to 0.***
3	P2.3/CS0EN	0: General purpose input 1: General purpose output or Chip Select bit 0 output ***When using SPI CS0 you must set this bit to 1.***
2	P2.2/CS1EN	0: General purpose input 1: General purpose output or Chip Select bit 1 output ***When using SPI CS1 you must set this bit to 1.***
1	P2.1/CS2EN	0: General purpose input 1: General purpose output or Chip Select bit 2 output ***When using SPI CS2 you must set this bit to 1.***
0	P2.0/CS3EN	0: General purpose input 1: General purpose output or Chip Select bit 3 output ***When using SPI CS3 you must set this bit to 1.***

The P3PINCFG register controls I/O access to UART0, the I2C interface, capture compare input0 and 1, Timer 0 and Timer 1 inputs as well as defines the direction of P3 when used as general purpose I/O

TABLE 18: (P3PINCFG) PORT 3 PORT CONFIGURATION REGISTER - SFR 9EH

7	6	5	4
P3.7/MSCLEN	P3.6/MSDAEN	P3.5/T1INEN	P3.4/CCU1EN

3	2	1	0
P3.3/CCU0EN	P3.2/T0INEN	P3.1/RX0EN	P3.0/TX0EN

Bit	Mnemonic	Function
7	P3.7/MSCLEN	0: General purpose input 1: General purpose output or Master I2C SCL output ***When using the I2C you must set this bit to 1.***
6	P3.6/MSDAEN	0: General purpose input 1: General purpose output or Master I2C SDA ***When using the I2C you must set this bit to 1.***
5	P3.5/T1INEN	0: General purpose input or Timer1 Input 1: General purpose output ***When using Timer 1 you must set this bit to 0.***
4	P3.4/CCU1EN	0: General purpose input or CCU1 Input 1: General purpose output ***When using the Compare and Capture unit you must set this bit to 0.***
3	P3.3/CCU0EN	0: General purpose input or CCU0 Input 1: General purpose output ***When using the Compare and Capture unit you must set this bit to 0.***
2	P3.2/T0INEN	0: General purpose input or Timer 0 Input 1: General purpose output ***When using Timer 0 you must set this bit to 0.***
1	P3.1/RX0EN	0: General purpose input or UART0 Rx 1: General purpose output ***When using UART0 you must set this bit to 0.***
0	P3.0/TX0EN	0: General purpose input 1: General purpose output or UART0 Tx ***When using UART0 you must set this bit to 1.***

Using General Purpose I/O Ports

The VMX51C1020's 28 I/Os are grouped into four ports. For each port an SFR register location is defined. Those registers are bit addressable providing the ability to control the I/O lines individually.

When the port pin configuration register value defines the pin as an output, the value written into the port register will be reflected at the pin level.

Reading the I/O pin configured as input is done by reading the contents of its associated port register.

TABLE 19:
PORT 0 - SFR 80H

7	6	5	4	3	2	1	0
P0 [7:0]							

PORT 1 - SFR 90H

7	6	5	4	3	2	1	0
P1 [7:0]							

PORT 2 - SFR A0H

7	6	5	4	3	2	1	0
P2 [7:0]							

PORT 3 - SFR B0H

7	6	5	4	3	2	1	0
P3 [7:0]							

Bit	Mnemonic	Function
7-0	P0, 1, 2, 3	When the Port is configured as an output, setting a port pin to 1 will make the corresponding pin to output logic high. When set to 0, the corresponding pin will set a logic low.

I/O usage example

The following example demonstrates the configuration of the VMX51C1020 I/Os.

```
//-------------------------------------------------------------------------
//This example continuously reads the P0 and writes its contents into //P1 and it toggle P2 and P3.
//-------------------------------------------------------------------------
#pragma TINY
#pragma UNSIGNEDCHAR

#include <VMIXReg.h>

at 0x0000 void main (void)
{
  DIGPWREN = 0x80;              // Enable Timer 2 to activate P1
                                //Output
  P1PINCFG = 0x00;              // Configure all P0 as Input
  P1PINCFG = 0xFF;              //Configure P1 as Output
  P2PINCFG = 0xFF;              //Configure P2 as Output
  P3PINCFG = 0xFF;              //Configure P3 as Output

  while(1)
   {
     P1 = P0;                   //Write P0 into P1
     P2 = ~P2;                  //Toggle P2 & P3
     P3 = ~P3;
   }
}//end of main() function
```

Using Port1.0-3 as General Purpose Output

Port1.0-P1.3 can be used as standard digital outputs. However, in order to do this, the Timer 2 clock must be enabled by setting the

T2CLKEN bit of the DIGPWREN register. In addition, the Timer 2 CCEN register must also have the reset value.

Interrupt on Port1 Change Feature

The VMX51C1020 includes an *Interrupt on Port1 change* feature. This feature can be used to monitor the activity on each I/O Port1 pin (individually) and trigger an interrupt when the state of the pin on which this feature has been activated changes. This is equivalent to having eight individual external interrupt inputs. The Interrupt on Port1 change shares the interrupt vector of the ADC peripheral at address 006Bh.

See the Interrupt section for more details on how to use this feature.

MULT/ACCU - Multiply Accumulator Unit

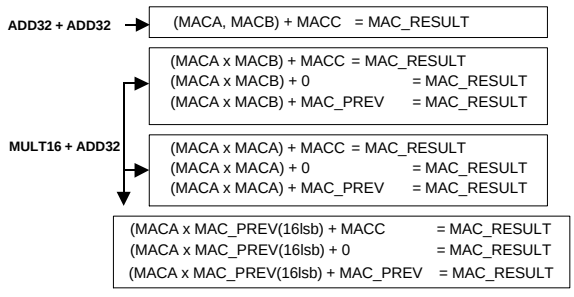
The VMX51C1020 includes a hardware based multiply-accumulator unit which provides the user the ability to perform fast and complex arithmetic operations.

MULT/ACCU Features:

- Hardware Calculation Engine
- Calculation result is ready as soon as the input registers are loaded
- Signed mathematical calculations
- Unsigned MATH operations are possible if the MUL engine operands are limited to 15-bits in size
- Auto/Manual reload of MAC_RES
- Enhanced VMX51C1020 MULT/ACCU Unit
- Easy implementation of complex MATH operations
- 16-bit and 32-bit Overflow Flag
- 32-bit Overflow can raise an interrupt
- MULT/ACCU operand registers can be cleared individually or all together
- Overflow flags can be configured to stay active until manually cleared
- Can store and use results from previous operations

The MULT/ACCU can be configured to perform the following operations:

FIGURE 13: VMX51C1020 MULT/ACCU OPERATION



Where MACA (multiplier), MACB (multiplicand), MACACC (accumulator) and MACRESULT (result) are 16, 16, 32 and 32 bits, respectively.

MULT/ACCU Control Registers

With the exception of the Barrel Shifter, the MULT/ACCU unit operation is controlled by two SFR registers:

- The MACCTRL1
- The MACCTRL2

The following two tables describe the details of these control registers.

TABLE 20: (MACCTRL1) MULT/ACCU UNIT CONTROL REGISTER - SFR EBH

7	6	5	4
LOADPREV	PREVMODE	OVMODE	OVRDVAL

3	2	1	0
ADDSRC [1:0]		MULCMD [1:0]	

Bit	Mnemonic	Function
7	LOADPREV	MACPREV manual Load control 1 = Manual load of the MACPREV register content if PREVMODE = 1
6	PREVMODE	Loading method of MACPREV register 0 = Automatic load when MACA0 is written. 1 = Manual Load when 1 is written into LOADPREV
5	OVMODE	0 = Once set by math operation, the OV16 and OV32 flag will remain set until the overflow condition is removed. 1= Once set by math operation, the OV16 and OV32 flag will stay set until it is cleared manually.
4	OVRDVAL	0 = The value on MACRES is the calculation result. 1 = the value on MACRES is the 32LSB of the MACRES when the OV32 overflow occurred
3:2	ADDSRC[1:0]	32-bit Addition source **B Input** 00 = 0 (No Add) 01 = C (std 32-bit reg) 10 = RES –1 11 = C (std 32-bit reg) **A Input** 00=Multiplication 01=Multiplication 10=Multiplication 11= Concatenation of {A, B} for 32-bit addition
1:0	MULCMD[1:0]	Multiplication Command 00 = MACA x MACB 01 = MACA x MACA 10 = MACA x MACPREV (16 LSB) 11 = MACA x MACB

TABLE 21: (MACCTRL2) MULT/ACCU UNIT CONTROL REGISTER 2 -SFR F1H

7	6	5	4
MACCLR2 [2:0]			MACOV32IE

3	2	1	0
-	-	MACOV16	MACOV32

Bit	Mnemonic	Function
7:5	MACCLR[2:0]	MULT/ACCU Register Clear 000 = No Clear 001 = Clear MACA 010 = Clear MACB 011 = Clear MACC 100 = Clear MACPREV 101 = Clear All MAC regs + Overflow Flags 110 = Clear Overflow Flags only
4	MACOV32IE	MULT/ACCU 32-bit Overflow IRQ Enable
3	-	-
2	-	-
1	MACOV16	16-bit Overflow Flag 0 = No 16 overflow 1 = 16-bit MULT/ACCU Overflow occurred
0	MACOV32	32-bit Overflow Flag 1 = 32-bit MULT/ACCU Overflow This automatically loads the MAC32OV register. The MACOV32 can generate a MULT/ACCU interrupt when enabled.

MULT/ACCU Unit Data Registers

The MULT/ACCU Data registers include operand and result registers that serve to store the numbers being manipulated in mathematical operations. Some of these registers are uniquely for addition (such as MACC) while others can be used for all operations. The MULT/ACCU operation registers are represented below.

MACA and MACB Multiplication (Addition) Input Registers

The MACA and MACB register serve as 16-bit input operands when performing multiplication.

When the MULT/ACCU is configured to perform 32-bit addition, the MACA and the MACB registers are concatenated to represent a 32-bit word. In that case the MACA register contains the upper 16-bit of the 32-bit operand and the MACB contains the lower 16-bit

TABLE 22: (MACA0) MULT/ACCU UNIT A OPERAND, LOW BYTE - SFR F2H

7	6	5	4	3	2	1	0
MACA0 [7:0]							

Bit	Mnemonic	Function
7:0	MACA0	Lower segment of the MACA operand

TABLE 23: (MACA1) MULT/ACCU UNIT A OPERAND, HIGH BYTE - SFR F3H

7	6	5	4	3	2	1	0
MACA1 [15:8]							

Bit	Mnemonic	Function
15:8	MACA1	Upper segment of the MACA operand

TABLE 24: (MACB0) MULT/ACCU UNIT B OPERAND, LOW BYTE - SFR F9H

7	6	5	4	3	2	1	0
MACB0 [7:0]							

Bit	Mnemonic	Function
7:0	MACB0	Lower segment of the MACB operand

TABLE 25: (MACB1) MULT/ACCU UNIT B OPERAND, HIGH BYTE - SFR FAH

7	6	5	4	3	2	1	0
MACB1 [7:0]							

Bit	Mnemonic	Function
7:0	MACB1	Upper segment of the MACB operand

MACC Input Register

The MACC register is a 32-bit register used to perform 32-bit addition.

It's possible to substitute the MACPREV Register for the MACC register or 0 in the 32-bit addition.

TABLE 26: (MACC0) MULT/ACCU UNIT C OPERAND, LOW BYTE - SFR ECH

7	6	5	4	3	2	1	0
MACC0 [7:0]							

Bit	Mnemonic	Function
7:0	MACC0	Lower segment of the 32-bit addition register

TABLE 27: (MACC1) MULT/ACCU UNIT C OPERAND, BYTE 1 - SFR EDH

7	6	5	4	3	2	1	0
MACC1 [15:8]							

Bit	Mnemonic	Function
15:8	MACC1	Lower middle segment of the 32-bit addition register

TABLE 28: (MACC2) MULT/ACCU UNIT C OPERAND, BYTE 2 - SFR EEH

7	6	5	4	3	2	1	0
MACC2 [23:16]							

Bit	Mnemonic	Function
23:16	MACC2	Upper middle segment of the 32-bit addition register

TABLE 29: (MACC3) MULT/ACCU UNIT C OPERAND, HIGH BYTE - SFR EFH

7	6	5	4	3	2	1	0
MACC3 [31:24]							

Bit	Mnemonic	Function
31:24	MACC3	Upper segment of the 32-bit addition register

MACRES Result Register

The MACRES register, which is 32-bits wide, contains the result of the MULT/ACCU operation. In fact, the MACRES register is the output of the Barrel Shifter.

TABLE 30: (MACRES0) MULT/ACCU UNIT RESULT, LOW BYTE - SFR F4H

7	6	5	4	3	2	1	0
MACRES0 [7:0]							

Bit	Mnemonic	Function
7:0	MACRES0	Lower segment of the 32-bit MULT/ACCU result register

TABLE 31: (MACRES1) MULT/ACCU UNIT RESULT, BYTE 1 - SFR F5H

7	6	5	4	3	2	1	0
MACRES1 [15:8]							

Bit	Mnemonic	Function
15:8	MACRES1	Lower middle segment of the 32-bit MULT/ACCU result register

TABLE 32: (MACRES2) MULT/ACCU UNIT RESULT, BYTE 2 - SFR F6H

7	6	5	4	3	2	1	0
MACRES2 [23:16]							

Bit	Mnemonic	Function
23:16	MACRES2	Upper middle segment of the 32-bit MULT/ACCU result register

TABLE 33: (MACRES3) MULT/ACCU UNIT RESULT, HIGH BYTE - SFR F7H

7	6	5	4	3	2	1	0
MACRES3 [31:24]							

Bit	Mnemonic	Function
31:24	MACRES3	Upper segment of the 32-bit MULT/ACCU result register

MACPREV Register

The MACPREV register provides the ability to automatically or manually save the contents of the MACRES register and re-inject it into the calculation. This feature is especially useful in applications where the result of a given operation serves as one of the operands of the next one.

As mentioned previously, there are two ways to load the MACPREV register controlled by the PREVMODE bit value:

PREVMODE = 0:
Auto MACPREV load, by writing into the MACA0 register. Selected when PREVMODE = 0.

PREVMODE = 1:
Manual load of MACPREV when the LOADPREV bit is set to 1

A good example using the auto loading of the MACPREV feature is the implementation of a FIR Filter. In that specific case, it is possible to save a total of 8 MOV operations per tap calculation.

TABLE 34: (MACPREV0) MULT/ACCU UNIT PREVIOUS OPERATION RESULT, LOW BYTE - SFR FCH

7	6	5	4	3	2	1	0
MACPREV0 [7:0]							

Bit	Mnemonic	Function
7:0	MACPREV0	Lower segment of 32-bit MULT/ACCU previous result register

TABLE 35: (MACPREV1) MULT/ACCU UNIT PREVIOUS OPERATION RESULT, BYTE 1 - SFR FDH

7	6	5	4	3	2	1	0
MACPREV1 [7:0]							

Bit	Mnemonic	Function
15:8	MACPREV1	Lower middle segment of 32-bit MULT/ACCU previous result register

TABLE 36: (MACPREV2) MULT/ACCU UNIT PREVIOUS OPERATION RESULT, BYTE 2 - SFR FEH

7	6	5	4	3	2	1	0
MACPREV2 [15:8]							

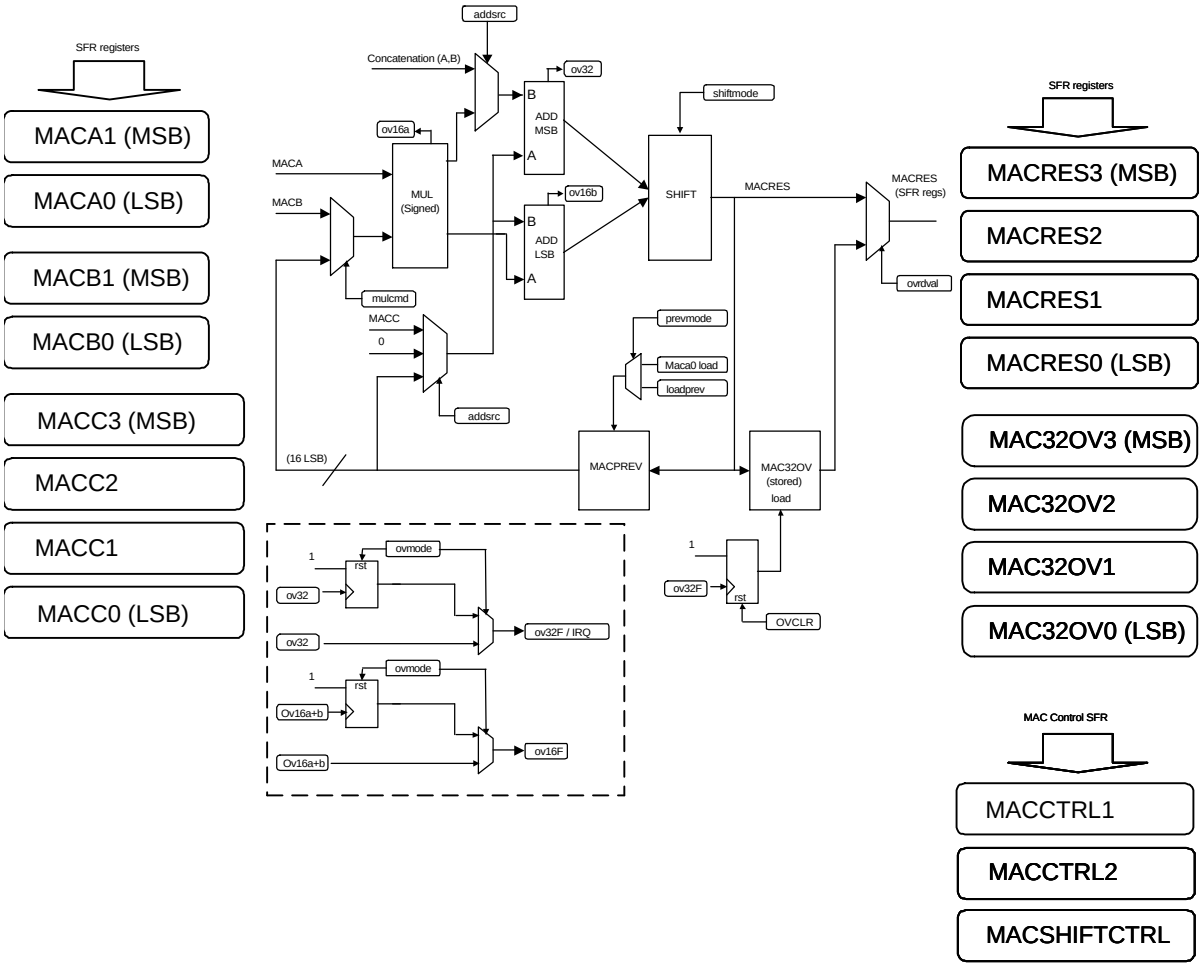
Bit	Mnemonic	Function
23:16	MACPREV2	Upper middle segment of 32-bit MULT/ACCU previous result register

TABLE 37: (MACPREV3) MULT/ACCU UNIT PREVIOUS OPERATION RESULT, HIGH BYTE - SFR FFH

7	6	5	4	3	2	1	0
MACPREV3 [7:0]							

Bit	Mnemonic	Function
31:24	MACPREV3	Upper segment of 32-bit MULT/ACCU previous result register

FIGURE 14: VMX51C1020 MULT/ACCU FUNCTIONAL DIAGRAM



The above block diagram shows the interaction between the registers and the other components that comprise the MULT/ACCU unit on the VMX51C1020.

MULT/ACCU Barrel Shifter

The MULT/ACCU includes a 32-bit Barrel Shifter at the output of the 32-bit addition unit. The Barrel Shifter can perform right/left shift operations in one cycle, which is useful for scaling the output result of the MULT/ACCU.
The shift range is adjustable from 0 to 16 in both directions. The "shifted" addition unit output can be routed to the:

- MACRES
- MACPREV
- MACOV32

The barrel shifter can perform both arithmetic and logical shifts: The shift left operation can be configured as an arithmetic or logical shift. In the later, the sign bit is discarded.

TABLE 38: (MACSHIFTCTRL) MULT/ACCU UNIT BARREL SHIFTER CONTROL REGISTER - SFR FBH

7	6	5	4	3	2	1	0
SHIFTMODE	ALSHSTYLE	SHIFTAMPL [5:0]					

Bit	Mnemonic	Function
7	SHIFTMODE	0 = Logical SHIFT 1 = Arithmetic SHIFT
6	ALSHSTYLE	Arithmetic Shift Left Style 0= Arithmetic Left Shift: Logical Left 1= Arithmetic Left Shift: Keep sign bit
5:0	SHIFTAMPL[5:0]	Shift Amplitude 0 to 16 (5 bits to provide 16 bits shift range) Neg. Number = Shift Right (2 complements) Pos. Number = Shift Left

MULT/ACCU Unit Setup and OV32 Interrupt Example

In order to use the MULT/ACCU unit, the user must first set up and configure the module. The following provides setup code examples. The first part of the code is the interrupt setup and module configuration, whereas the second part is the interrupt function itself.

Sample C code for MULT/ACCU Unit interrupt setup and module configuration:

```
//-------------------------------------------------------------------------
// Sample C code to setup the MULT/ACCU unit
//-------------------------------------------------------------------------

//--- Program initialisation omitted…
(…)
void main(void){
// MULT/ACCU setup
IEN0 |= 0x80;                   // Enable all interrupts
IEN1 |= 0x10;                   // Enable MULT/ACCU interrupt
DIGPWREN |= 0x20;               // Enable MULT/ACCU unit
MACCTRL1 = 0x0C;                // {A,B}+C
MACCTRL2 = 0x10;                // Enable INT overflow_32

// MULT/ACCU example use

MACA0 = 0xFF;
MACA1 = 0x7F;
MACB0 = 0xFF;
MACB1 = 0xFF;
MACC0 = 0xFF;
MACC1 = 0xFF;
MACC2 = 0xFF;
MACC3 = 0x7F;

//--- as soon as the MAC input registers are loaded the result is available in the MACRESx registers.
}//end of main

//-------------------------------------------------------------------------
// MAC 32 bit overflow Interrupt Function

void int_5_mac (void) interrupt 12
{
IEN0 &= 0x7F;                   // Disable all interrupts

//Put MAC 32 bit Overflow Interrupt code here.*/
//Note that when a 32bit overflow occurs, the 32 least significant bit of the current
//result are stored into the MAC32OVx registers and can be read at the location
of MACRESx by setting to 1 the OVRDVAL bit of the MACCTRL register

IRCON &= 0xEF;                  // Clear flag (IEX5)
IEN0 |= 0x80;                   // Enable all interrupts
}
//-------------------------------------------------------------------------
```

MULT/ACCU Application Example: FIR Filter Function

The following ASM code shows the implementation of a FIR filter computation function for one iteration, the data shifting operation and the definition of the FIR filter coefficient table. The FIR computation is simple to implement, however, it is quite demanding in terms of processing power. For each new data point, the multiplication with associated coefficients + addition operation must be performed N times (N=number of filter tapps).

Due to being hardware based and including features such as automatic reload of the result of the previous operation, the VMX51C1020 MULT/ACCU unit is very efficient for performing operations such as FIR filter computation.

In the code example below, the COMPUTEFIR loop forms the heart of the FIR computation and it is clear that use of the MULT/ACCU unit implies very few instructions being required for mathematical operations. The net result is a dramatic performance improvement when compared with manual calculations done solely via the standard 8051 instruction set.

VMX51C1020 FIR Filter Example

The example below shows how to use the MULT/ACCU unit of the VMX51C1020 to perform FIR filter computing. In order to minimize the example size, only the FIR computing function and the coefficient table are presented.

```
;-------------------------------------------------//
;** FIR Filter Computing Function        //
;-------------------------------------------------//
FIRCOMPUTE:    MOV    R0,#NPOINTSBASEADRS
                                          ;INPUT ADC RAW DATA
                                          ;AT Xn LOCATIONS...

;Saving acquired data from calling function into RAM for computation

               MOV        VARH,DATAH
               MOV        VARL,DATAL
               MOV        @R0,VARH          ;(MSB)
               INC        R0
               MOV        @R0,VARFL         ;(LSB)

;** Prepare to compute Yn...
;***Define Base ADRS of input values
               MOV        R0,#NPOINTSBASEADRS

;***Define Base Address of coefficients
               MOV        R1,#COEFBASEADRS
               MOV        R7,#NPOINTS       ;DEFINE COUNTER

;***Configure the MULT/ACCU unit as Follow:

               MOV        MACCTRL,#00001000B

               ;BIT7 LOADPREV = 0     No manual Previous result
               ;BIT6 PREVMODE = 0     Automatic Previous result save when
               ;                      MULT/ACCUA0 is loaded
               ;BIT5 OVMODE   = 0     Overflow flag remains ON until overflow
               ;                      condition exist
               ;BIT4 OVRDVAL  = 0     The value of MACRES is the calculation
               ;                      result
               ;BIT3:2 ADDSRC = 10    MACPREV is the Addition Source
               ;BIT1:0 MULCMD = 00    Mul Operation = MACAxMACB


;**Clear the MULT/ACCU registers content
               MOV                   MACCTRL2,#0A0H
;** COMPUTE Yn...

COMPUTEFIR:    MOVMACB1,@R1          ;Put a given Coefficient into
                                     ;MULT/ACCUB
               INC        R1
               MOV        MACB0,@R1
               INC        R1

               MOV        MACA1,@R0   ; Put a given Xn Input into
               INC        R0
               MOV         MACA0,@R0
               ;This last instruction load the MACPREV register for next Operation
               INC        R0
               DJNZ       R7,COMPUTEFIR  ;Do the Computation for N taps

;*** Second part
;-------------------------------------------------------------------------------------//
;** SHIFT PREVIOUS INPUT VALUES TO LET PLACE FOR NEXT ONE...
;-------------------------------------------------------------------------------------//
SHIFTPAST:
               MOV        R7,#(NPOINTS-1)*2     ;Define # of datashift
                                                ;To perform (N-1)*2
;***COMPUTE FIRST FETCH ADDRESS
               MOV        R0,#(NPOINTSBASEADRS - 1 + 2*(NPOINTS-1))

;***COMPUTE FIRST DESTINATION ADDRESS
               MOV        R1,#(NPOINTSBASEADRS + 1 + 2*(NPOINTS-1))
SHIFTLOOP:  MOV           A,@R0       ;Shift Given LSB input...
               MOV        @R1,A       ;To next location
               DEC        R0          ;Prepare pointer for moving LSB
               DEC        R1
               DJNZ       R7,SHIFTLOOP

;** PERFORM TRANSFORMATION OF Yn HERE AND PUT INTO BINH, BINL
;** IN THIS CASE THE COEFFICIENTS HAVE BEEN MULTIPLIED BY 65536
;** SO THE RESULT IS ON 32-BITS
;** DIVISING YN BY 65536 MEAN ONLY TAKING THE UPPER 16-BITS

               MOV        DATAH,MACRES3
               MOV        DATAL,MACRES2

               LCALL      SENDLTC1452
               MOV        P3,#00
               RET

;-------------------------------------------------
;* FIR Filter Coefficients Table         *
;-------------------------------------------------
;FSAMPLE 480HZ, N=16, LOW PASS 0.1HZ -78DB @ 60HZ

COEFTABLE:     DW     023DH
               DW     049DH
               DW     086AH
               DW     0D2DH
               DW     1263H
               DW     1752H
               DW     1B30H
               DW     1D51H
               DW     1D51H
               DW     1B30H
               DW     1752H
               DW     1263H
               DW     0D2DH
               DW     086AH
               DW     049DH
               DW     023DH

               DW     0FFFFH          ;END OF TABLE
```

VMX51C1020 Timers

The VMX51C1020 includes 3 general-purpose timer/counters

- Timer0
- Timer1
- Timer2

Timer0 and Timer1 are general purpose timers that can operate as a timer with a clock rate based on the system clock, or as an event counter that monitosr events occurring on an external timer input pin (T0IN for Timer 0 and T1IN for Timer 1).

Timers 0 and Timer 1 are similar to the standard 8051 timers.

Apart from also being capabile of operating as a timer based on a system clock or as an event counter, Timer2 is also the heart of the PWM counter outputs and the Compare and Capture Units.

Each of the VMX51C1020's timers has a dedicated interrupt vector which can be triggered when the Timers overflow.

Timer 0 and Timer 1

The VMX51C1020's Timer0 and Timer1 are very similar in their structure and operation. The main difference being that Timer1 serves as a baud rate generator for UART0 and it shares some of its resources when Timer0 is used in mode 3.

Timer0 and Timer1 each consist of a 16-bit register for which the content is accessible as two independent SFR registers: TLx and THx.

TABLE 39: (TL0) TIMER 0 LOW BYTE - SFR 8AH

7	6	5	4	3	2	1	0
TL0 [7:0]							

TABLE 40: (TH0) TIMER 0 HIGH BYTE - SFR 8CH

7	6	5	4	3	2	1	0
TH0 [7:0]							

TABLE 41: (TL1) TIMER 1 LOW BYTE - SFR 8BH

7	6	5	4	3	2	1	0
TL1 [7:0]							

TABLE 42: (TH1) TIMER 1 HIGH BYTE - SFR 8DH

7	6	5	4	3	2	1	0
TH1 [7:0]							

With the exception of their associated interrupts, the configuration and control of Timer0 and Timer1 is performed via the TMOD and TCON SFR registers.

The following table shows the TCON special function register of the VMX51C1020. This register contains the Timer 0/1 overflow flags, Timer 0/1 run control bits, interrupt 0/1 edge flags, and the interrupt 0/1 interrupt type control bits.

TABLE 43: (TCON) TIMER 0, TIMER 1 TIMER/COUNTER CONTROL - SFR 88H

7	6	5	4
TF1	TR1	TF0	TR0

3	2	1	0
IE1	IT1	IE0	IT0

Bit	Mnemonic	Function
7	TF1	Timer 1 overflow flag. Set by hardware when Timer 1 overflows. It is automatically cleared when the Timer 1 interrupt is serviced. This flag can also be cleared by software.
6	TR1	Timer 1 Run control bit. TR1 = 0, Stop Timer 1 TR1 = 1, Start Timer 1
5	TF0	Timer 0 overflow flag. Set by hardware when Timer 0 overflows. It is automatically cleared when the Timer 0 interrupt is serviced. This flag can also be cleared by software.
4	TR0	Timer 0 Run control bit. TR0 = 0, Stop Timer 0 TR0 = 1, Start Timer 0
3	IE1	Interrupt 1 edge flag. This flag is set by hardware when falling edge on external INT1 is observed. It is cleared when interrupt is processed.
2	IT1	INT1 interrupt event type control bit. IT1 = 0, interrupt will be caused by a Low Level on INT1 IT1 = 1, Interrupt will be caused by a High to Low transition on INT1.
1	IE0	INT0 edge flag configuration Set by hardware when falling edge on external pin INT0 is observed. It is cleared when interrupt is processed.
0	IT0	INT0 interrupt event type control bit. IT0 = 0, interrupt will be caused by a Low Level on INT0 IT0 = 1, Interrupt will be caused by a High to Low transition on INT0.

The TMOD register is mainly used to set the operating mode of the timers and it allows the user to enable the external gate control as well as select timer or counter operation.

TABLE 44: (TMOD) TIMER MODE CONTROL - SFR 89H

7	6	5	4
GATE1	CT1	M11	M01

3	2	1	0
GATE0	CT0	M10	M00

Bit	Mnemonic	Function
7	GATE1	GATE1 = 0, The level present on the INT1 pin has no effect on Timer1 operation. GATE1 = 1, The level of INT1 pin serves as a Gate control on to Timer/Counter operation provided the TR1 bit is set. Applying a Low Level on the INT1 pin makes the Timer stop.
	CT1	Selects TIMER1 Operation. CT1 = 0, Sets the Timer 1 as a Timer which value is incremented by SYSCLK events. CT1 = 1, The Timer 1 operates as a counter which counts the High to Low transition on that occurs on the T1IN input.
5	M11	Selects mode for Timer/Counter 1, as shown in the Table below.
4	M01	
3	GATE0	GATE0 = 0, The level present on the INT0 pin has no effect on Timer1 operation. GATE0 = 1, The level of INT0 pin serves as a Gate control on to Timer/Counter operation provided the TR0 bit is set. Applying a Low Level on the INT0 pin makes the Timer stop.
2	CT0	Selects Timer 0 Operation. CT1 = 0, Sets the Timer 0 as a Timer which value is incremented by SYSCLK events. CT1 = 1, The Timer 0 operates as a counter which counts the High to Low transition on that occurs on the T1IN input.
1	M10	Selects mode for Timer/Counter 0, as shown in the Table below.
0	M00	

Timer0/Timer1/Counter Operation

The CT0 and CT1 bits of the TMOD register control the Clock source for Timer0 and Timer1, respectively. When the CT bit is set to 0 (Timer mode) the Timer is sourced from the system clock divided by 12.

Setting the CTx bit to 1 sets the Timer to operate in event counter mode. In this mode, High to Low transitions on the TxIN pin of the VMX51C1020 increments the timer value.

Note that when Timer0 and Timer1 operate in Timer mode, they use the System Clock as their source. Therefore configuring the CLKDIVCTRL register will affect the Timer's operation.

Timer0 & Timer1 Gate Control

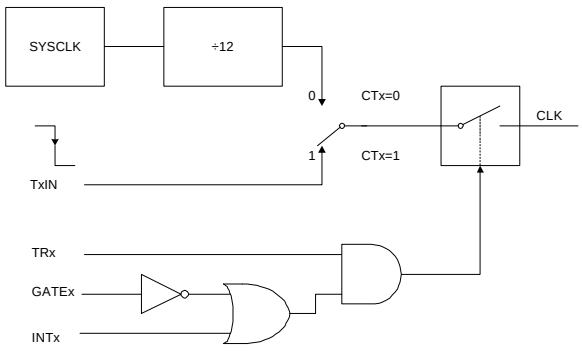
The Gate control makes it possible for an external device to control Timer0 and Timer1 operation through the interrupt (INTx) pins.

When the GATEx and TRx bits of the TMOD register are set to 1:

- INTx = Logic LOW, The Timer x Stops
- INTx = Logic High, The Timer x Runs

When the Gate bit equals 0, then the logic level present at the INTx pin have no effect on the Timer Operation.

FIGURE 15: TIMER 0, TIMER 1 CTX & GATE CONTROL



Timer0, Timer1 Operation Modes

The operating mode of Timer0 and Timer1 is determined by the M1x and M0x bits in the TMOD register. The following summarizes the four modes of operation for Timers0 and 1.

TABLE 45: TIMER/COUNTER MODE DESCRIPTION SUMMARY

M1	M0	Mode	Function
0	0	**Mode 0**	**13-bit Timer / Counter**, with 5 lower bits in TL0 or TL1 register and bits in TH0 or TH1 register (for timer 0 and timer 1, respectively). The 3 high order bits of TL0 and TL1 are held at 0.
0	1	**Mode 1**	**16-bit Timer / Counter**
1	0	**Mode 2**	**8-bit auto reload Timer / Counter**. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	**Mode 3**	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8-bit Timers / Counters.

Mode 0, 13-bit Timer/Counter

Mode 0 operation is the same for Timer0 and Timer1.

In Mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of the TLx register and all 8-bits of the THx register. The Timer Run bit (TRx) of the TCON SFR starts the timer. The value of the CTx bit defines if the Timer will operate as a Timer (CTx = 0), deriving its source from the System Clock, or count the High to Low Transitions (CTx = 1) that occurs on the External Timer input pin (TxIN). When the 13-bit count increments from 1FFFh (all ones) to all zeros, the TF0 (or TF1) bit will be set in the TCON SFR.

The state of the upper 3-bits of the TLx register is indeterminate in Mode 0 and must be masked when the software evaluates the register's contents.

Timer 0, Timer 1: Mode 0 - Overflow Rate (Hz)
CTx = 0
Timer overflow rate (Hz) = $\frac{f_{SYSCLK}}{12 \times [8192-(THx, TLx)]}$
CTx = 1
Timer overflow rate (Hz) = $\frac{f_{TxIN}}{[8192-(THx,TLx)]}$

Mode 1 (16-bit)

Mode 1 operation is the same for Timer0 and Timer1. In Mode 1, the timer is configured as a 16-bit counter. Other than rollover at FFFFh, Mode 1 operation is the same as Mode 0.

FIGURE 16 : TIMER 0 MODE 0 & MODE 1

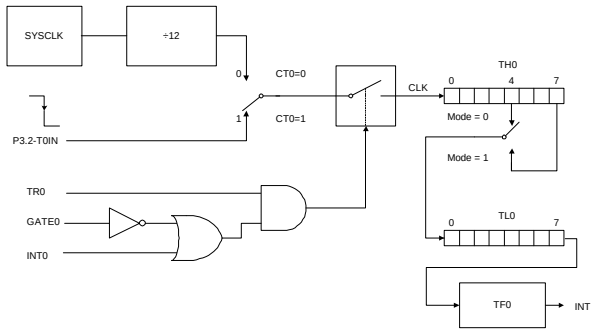
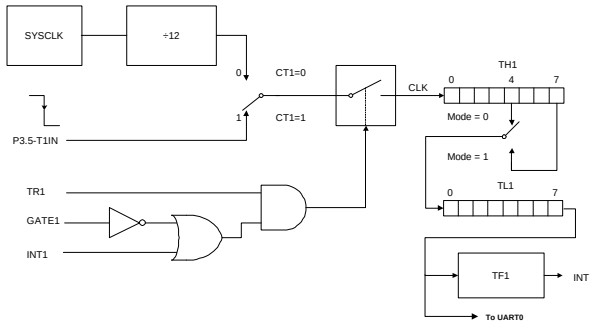


FIGURE 17: TIMER 1 MODE 0 & MODE 1



The Timer0 and Timer1 overflow rate in mode 1 can be calculated using the following equations:

Timer 0, Timer 1: Mode 1 - Overflow Rate (Hz)
CTx = 0
Timer overflow rate (Hz) = $\frac{f_{SYSCLK}}{12 \times [65536-(THx, TLx)]}$
CTx = 1
Timer overflow rate (Hz) = $\frac{f_{TxIN}}{[65536-(THx, TLx)]}$

Mode 2 (8-bit)

The operation of Mode2 is the same for Timer0 and Timer1. In Mode 2, the timer is configured

as an 8-bit counter, with automatic reload of the start value. The LSB of the Timer register, TLx, is the counter itself and the MSB portion of the Timer, THx, stores the timer reload value.

Mode 2's counter control is the same as for Mode 0 and Mode 1. However, in Mode 2, when TLx rolls over from FFh, the value stored in THx is reloaded into TLx.

FIGURE 18 : TIMER 0 MODE 2

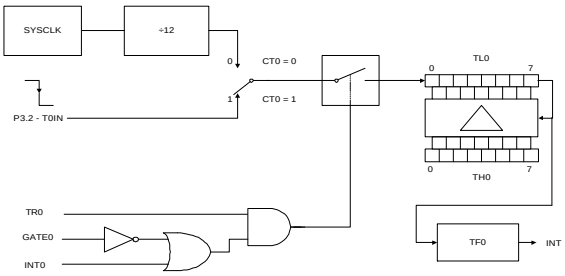
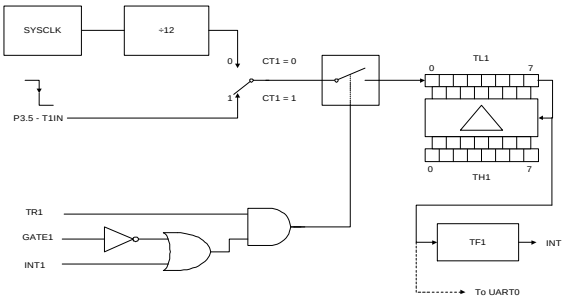


FIGURE 19: TIMER 1 MODE 2



The Timer0 and Timer1 overflow rate in Mode 2 can be calculated using the following equations:

Timer 0, Timer 1: Mode 2 - Overflow Rate (Hz)
CTx = 0
Timer overflow rate (Hz) = $\frac{f_{SYSCLK}}{12 \times [256-(THx)]}$
CTx = 1
Timer overflow rate (Hz) = $\frac{f_{TxIN}}{[256--(THx)]}$

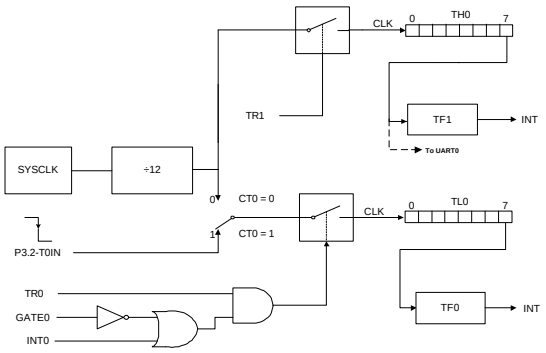
Using Timer1 as Baud Rate generator

Using Timer1 in mode 2 is recommended as the best approach when using Timer1 as the UART0 baud rate generator.

Mode 3 (2 x 8-bit)

In Mode 3, Timer0 operates as two 8-bit counters and Timer1 stops counting and holds its value.

FIGURE 20: TIMER0, TIMER 1 STRUCTURE IN MODE 3



The Timer0 overflow rate in Mode 3 can be calculated by using following equations:

Timer 0, Timer 1: Mode 3 - Overflow Rate (Hz)
TH0, CTx = 0 or 1
Timer overflow rate (Hz) = $\frac{f_{SYSCLK}}{12 \times 256}$
TL0, CTx = 0
Timer overflow rate (Hz) = $\frac{f_{SYSCLK}}{12 \times 256}$
TL0, CTx = 1
Timer overflow rate (Hz) = $\frac{f_{TxIN}}{256}$

In Mode 3, the values present in the TH1 and TL1 registers, as well as the value of the GATE1 and CT1 control bits, have no impact on the Timer operation.

Timer0 & Timer1 Interrupts

Timer0 and Timer1 have a dedicated interrupt vectors located at:

- **000Bh** for the **Timer 0**
- **001Bh** for the **Timer 1**

The natural priority of Timer0 is higher than that of Timer1.

The following table provides a summary of the Interrupt control and Flag bits associated with the Timer0 and Timer1 interrupts.

Bit Name	Location	Description
EA	IEN0.7	General interrupt control bit 0, Interrupt Disabled 1, Enabled Interrupt active
T0IE	IEN0.1	Timer 0 Overflow Interrupt 1 = Enable 0 = Disable
T1IE	IEN0.3	Timer 1 Overflow Interrupt 1 = Enable 0 = Disable
TF0	TCON.5	TF0 Flag is set when Timer 0 Overflow occurs. Automatically cleared when Timer 0 interrupt is serviced. This flag can also be cleared by software
TF1	TCON.7	TF1 Flag is set when Timer 1 Overflow occurs. Automatically cleared when Timer 1 interrupt is serviced. This flag can also be cleared by software

Setting Up Timer0 Example

In order to use Timer0, the first step is to setup the interrupt and then configure the module and this is described in the following code example.

Sample C code to set up Timer 0:

```
//-------------------------------------------------------------------------
// Sample C code to setup Timer 0
//-------------------------------------------------------------------------
//  (…) PROGRAM INITIALIZATION OMITTED

AT 0X0100 VOID MAIN(VOID){

// INTERRUPT + TIMER 0 SETUP
IEN0 |= 0x80;                   // ENABLE ALL INTERRUPTS
IEN0 |= 0x02;                   // ENABLE INTERRUPT TIMER 0
TMOD = 0x02;                    // TIMER 0 MODE 2
TCON = 0x10;                    // START TIMER 0

DO{}WHILE(1);           //WAIT FOR TIMER 0 INTERRUPT

}//END OF MAIN()

//-------------------------------------------------------------------------
// INTERRUPT FUNCTION

VOID INT_TIMER_0 (VOID) INTERRUPT 1
        {
IEN0 &= 0x7F;                   // DISABLE ALL INTERRUPTS
        /*-----------------------*/
        /*Put Interrupt code here*/
        /*-----------------------*/
IEN0 |= 0x80;                   // Enable all interrupts
}
//-------------------------------------------------------------------------
```

Setting Up Timer1 Example

The following code provides an example of how to configure Timer1 (first part of the code is the interrupt setup and module configuration whereas the second part is the interrupt function).

Example1: Delay function

```
//-------------------------------------------------------------------------
// Sample C code using the Timer 1: Delay function
//-------------------------------------------------------------------------
VOID DELAY1MS(UNSIGNED CHAR DLAIS) {
        IDATA UNSIGNED CHAR X=0;
        TMOD = 0x10;
        TL1 = 0x33;
        TH1 = 0xFB;
        ;//TIMER1 RELOAD VALUE FOR
        TCON = 0x40;

        WHILE (DLAIS > 0)
        {
  DO{
  X=TCON;
  X= X&0x80;
  }WHILE(X==0);

        TCON = TCON&0x7F;
        TL1 = 0x33;
        TH1 = 0xFB;
        ;//TIMER1 RELOAD VALUE FOR

        DLAIS = DLAIS-1;
        }
}//END OF DELAY 1MS
```

Example 2: Timer1 interrupt example

```
//-------------------------------------------------------------------------
// Sample C code using the Timer 1:  Interrupt
//-------------------------------------------------------------------------
//  (…) PROGRAM INITIALIZATION OMITTED
at 0xo100 void main(void){

// TIMER 1 setup

IEN0 |= 0x80;                   // Enable all interrupts
IEN0 |= 0x08;                   // Enable interrupt Timer1
TMOD = 0x20;                    // Timer 1 mode 2
TCON = 0x40;                    // Start Timer 1
TL1 = 0xFC;                     // Timer1 offset

do {
        }while(1);              //Wait Timer 1 interrupt

}//end of main() function
//----------------------------------------
// Timer 1 Interrupt function
//----------------------------------------
void int_timer_1 (void) interrupt 3
{
IEN0 &= 0x7F;                   // Disable all interrupts

/* Put Interrupt code here*/

IEN0 |= 0x80;                   // Enable all interrupts
}
```

Timer2

The VMX51C1020 Timer2 and associated peripherals include the following capabilities:

- 16-Bit Timer
- 16-Bit Auto-Reload Timer
- Compare and Capture units
- 8 / 16 PWM outputs

TABLE 46: (TL2) TIMER 2, LOW BYTE - SFR CCH

7	6	5	4	3	2	1	0
TL2 [7:0]							

TABLE 47: (TH2) TIMER 2, HIGH BYTE - SFR CDH

7	6	5	4	3	2	1	0
TH2 [7:0]							

Figure 21 shows the Timer2 Compare/Capture unit block diagram. The following paragraphs will describe describe how these blocks work.

Timer2 Registers

Timer2 constists of a 16-bit register, whose upper and lower bytes are accessible via two independent SFR registers (TL2, TH2).

TABLE 48: (TL2) TIMER 2 LOW BYTE - SFR CCH

7	6	5	4	3	2	1	0
TL2 [7:0]							

TABLE 49: (TH2) TIMER 2 HIGH BYTE - SFR CDH

7	6	5	4	3	2	1	0
TH2 [7:0]							

Timer2 Control Register

Most of Timer2's control is accomplished via the T2CON register located at SFR address C8h.

The T2CON register controls:

- T2 clock source Prescaler
- T2 count size (8/16-bits)
- T2 reload mode
- T2 Input selection

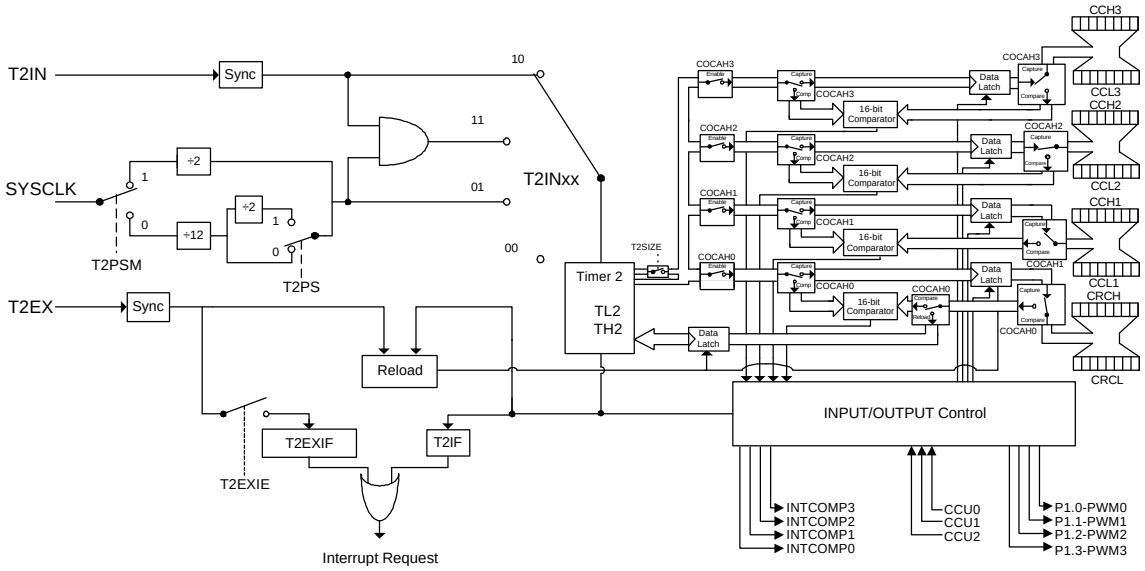
TABLE 50: (T2CON) TIMER 2 CONTROL REGISTER -SFR C8H

7	6	5	4
T2PS	T2PSM	T2SIZE	T2RM1

3	2	1	0
T2RM0	T2CM	T2IN1	T2IN0

Bit	Mnemonic	Function
7	T2PS	Prescaler select bit: 0 = Timer 2 is clocked with 1/12 of the oscillatory frequency 1 = Timer 2 is clocked with 1/24 of the oscillatory frequency
6	T2PSM	0 = Prescaler 1 = clock/2
5	T2SIZE	Timer 2 Size 0 = 16-bit 1 = 8-bit
4	T2RM1	Timer 2 reload mode selection 0X = Reload disabled 10 = Mode 0 11 = Mode 1
3	T2RM0	
2	T2CM	Timer 2 compare mode selection 0 = Mode 0 1 = Mode 1
1	T2IN1	Timer 2 input selection 00 = Timer 2 stops 01 = Input frequency f/2, f/12 or f/24 10 = Timer 2 is incremented by external signal at pin T2IN 11 = Internal clock is gated to the T2IN input.
0	T2IN0	

FIGURE 21: TIMER 2 AND COMPARE/CAPTURE UNIT



Timer2 Clock Sources

As previously stated, Timer2 can operate in Timer mode, in which case it derives its source from the System Clock (SYSCLK) or it can be configured as an event counter where the High to Low transition on the T2IN input makes the Timer 2 to increment.

The T2IN0 and T2IN1 bits of the T2CON register serve to define the selected Timer2 input and the operating mode of Timer2 (see following table).

TIMER 2 CLOCK SOURCE

T2IN1	T2IN0	Selected Timer 2 input
0	0	Timer 2 Stop
0	1	Standard Timer mode using internal clock with or without prescaler
1	0	External T2IN pin clock Timer2
1	1	Internal Clock is gated by the T2IN input When T2IN = 0, the Timer2 stop

When in Timer mode, Timer2 derives its source from the System Clock and the CLKDIVCTRL register will affect Timer 2's operation.

Timer 2 Stop

When both T2IN1 and T2IN0 bit are set to 0, Timer2 is in STOP mode.

Timer2 Operating Modes

When the T2IN1 bit is set to 0 and the T2IN0 bit is set to 1, Timer2 derives its source from the internal pre-scaled clock or not, depending on the T2PSM bit value.

Event Counter Mode

When operating in the Event Counter Mode, the timer is incremented as soon as the external signal T2IN transitions from a 1 to a 0. A sample of the T2IN input is taken at every machine cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected.

Gated Timer Mode

In the Gated Timer Mode, the internal clock, which serves as the Timer2 clock source, is gated by the external signal T2IN. In other words, when T2IN is high, the internal clock is allowed to pass through the AND gate. A low value of T2IN will diable the clock pulse. This provides the ability for an external device to control Timer2's operation or to use Timer2 to monitor the duration of an event.

Timer2 Clock Prescaler

When Timer2 is configured so that it derives its clock source from the System Clock, the Clock prescaling value can be controlled by software using the T2PSM and the T2PS bit of the T2CON register.

The different system clock prescaling values are shown in the following table:

T2PSM	T2PS	Timer 2 input clock
1	X	SYSCLK / 2
0	0	SYSCLK / 12
0	1	SYSCLK / 24

Timer2 Count Size

Timer2 can be configured to operate in 8-bit or 16-bit formats. The T2SIZE bit of the T2CON register selects the Timer2 count size.

- If T2SIZE = 0, Timer2 size is 16-bits
- If T2SIZE = 1, Timer2 size is 8-bits

Timer2 Reload Modes

The Timer2 reload mode is selected by the T2RM1 and T2RM0 bits of the T2CON register. The following figure shows the reload operation.

Timer2 must be configured as a 16-bit Timer/Counter for the reload modes to be operational by clearing the T2SIZE bit.

Timer 2 Mode 0

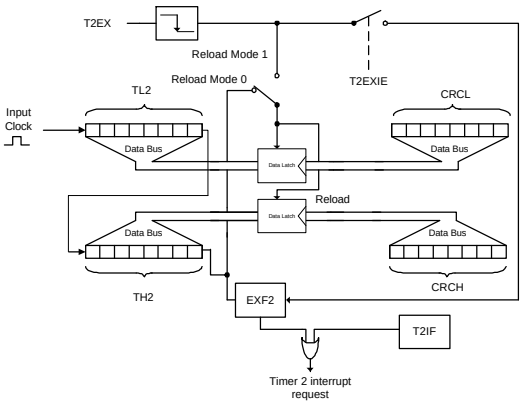
When the timer overflows, the T2IF overflow flag is set. Concurrently, this overflow causes Timer2 to be reloaded with the 16-bit value contained in the CRCx register, (which has been preset by software). This reload operation will occur during the same clock cycle in which T2IF was set.

Timer2 Mode 1

In Mode 1, a 16-bit reload from the CRCx register on the falling edge of T2EX occurs. This transition will set T2EXIF if T2EXIE is set. This action will cause an interrupt (providing that the Timer2 interrupt is enabled) and the T2IF flag value will not be affected.

The value of the T2SIZE does not affect the Reload in Mode 1. Also, the reload operation is performed independently of the state of the T2EXIE bit.

FIGURE 22: TIMER 2 RELOAD MODE



Timer2 Overflows and Interrupts

Timer2's interrupt is enabled when the Timer2 counter, the T2IF flag is set, and a Timer 2 interrupt occurs.

A Timer2 interrupt may also be raised from T2EX if the T2EXIE bit of the IEN1 register is set.

Finding the exact source of a Timer2 interrupt can be verified by checking the value of the T2IF and the T2EXIF bits of the IRCON register.

Timer2's interrupt vector is located at address 002Bh

Timer2 Setup Example

In order to use Timer2, one must first set up and configure the module (see following code example).

```
//---------------------------------------------------------------------------

// Sample C code to setup Timer 2
//---------------------------------------------------------------------------
// (…) PROGRAM INITIALIZATION OMITTED

at 0x100 void main(void){

// TIMER 2 & Interrupt setup
DIGPWREN = 0x80;                    // Enable Timer2,
T2CON = 0x01;                       // Set timer 2 to OSC/12
TL2 = 0xE0;
TH2 = 0xFF;

IEN0 |= 0x80;                       // Enable all interrupts
IEN0 |= 0x20;                       // Enable interrupt Timer 2

        do{                         //wait for Timer 2 interrupt
        }while(1);

}//end of main()

//---------------------------------------------------------------------------
// Timer 2 Interrupt Function
//---------------------------------------------------------------------------
void int_timer_2 (void) interrupt 5
{
IEN0 &= 0x7F;                       // Disable all interrupts

        /*-------------------------*/
        /*Interrupt code here*/
        /*-------------------------*/

IEN0 |= 0x80;                       // Enable all interrupts
}
```

Timer2 Special Modes

For general timing/counting operations, the VMX51C1020's Timer2 includes 4 Compare and Capture units that can be used to monitor specific events and serve to drive PWM outputs. Each Compare and Capture unit provides three specific operating modes that are controlled by the CCEN register. These 3 modes are:

- Compare Modes Enable.
- Capture on write into CRCL/CCLx registers.
- Capture on transitions at CCU input pins level.

TABLE 51: (CCEN) COMPARE/CAPTURE ENABLE REGISTER -SFR C9H

7	6	5	4
COCAH3	COCAL3	COCAH2	COCAL2

3	2	1	0
COCAH1	COCAL1	COCAH0	COCAL0

The CCEN register bits are grouped in pairs of COCAHx/COCALx bits. Each pair corresponds to one Compare and Capture Unit. The Compare and Compare unit operating mode vs. the configuration bit is described in the following table.

Bit		
Mnemonic	Mnemonic	Function
COCAH0	**COCAL0**	Compare and Capture mode for CRC register
0	0	Compare/capture disabled
0	1	Capture on a falling edge at pin CCU0 (1 cycle)
1	0	Compare enabled (PWM0)
1	1	Capture on write operation into register CRC1
COCAH1	**COCAL1**	Compare/capture mode for CC register 1
0	0	Compare/capture disabled
0	1	Capture on a rising edge at pin CCU1 (2 cycles)
1	0	Compare enabled (PWM1)
1	1	Capture on write operation into register CCL1
COCAH2	**COCAL2**	Compare/capture mode for CC register 2
0	0	Compare/Capture disabled
0	1	Capture on a rising edge at pin CCU2 (2 cycles)
1	0	Compare enabled (PWM2)
1	1	Capture on write operation into register CCL2
COCAH3	**COCAL3**	Compare/Capture mode for CC register 3
0	0	Compare/capture disabled
0	1	N/A - CCU3 not pinned out
1	0	Compare enabled (PWM)
1	1	Capture on write operation into register CCL3

This allows individual configuration and operation of each Compare and Capture Unit.

Compare/Capture & Reload Registers

Each Compare and Capture Unit has a specific 16-bit register accessible via two SFR addresses.

Note that the CRCHx/CRCLx registers associated with Compare/Capture Unit 0 are the only ones that can be used to perform a reload of Timer2 operation.

The following tables describe the different registers that may be captured or compared to the value of Timer2.

TABLE 52: (CRCL) COMPARE/RELOAD/CAPTURE REGISTER, LOW BYTE - SFR CAH

7	6	5	4	3	2	1	0
CRCL [7:0]							

TABLE 53: (CRCH) COMPARE/RELOAD/CAPTURE REGISTER, HIGH BYTE - SFR CBH

7	6	5	4	3	2	1	0
CRCH [7:0]							

TABLE 54: (CCL1) COMPARE/CAPTURE REGISTER 1, LOW BYTE - SFR C2H

7	6	5	4	3	2	1	0
CCL1 [7:0]							

TABLE 55: (CCH1) COMPARE/CAPTURE REGISTER 1, HIGH BYTE - SFR C3H

7	6	5	4	3	2	1	0
CCH1 [7:0]							

TABLE 56: (CCL2) COMPARE/CAPTURE REGISTER 2, LOW BYTE - SFR C4H

7	6	5	4	3	2	1	0
CCL2 [7:0]							

TABLE 57: (CCH2) COMPARE/CAPTURE REGISTER 2, HIGH BYTE - SFR C5H

7	6	5	4	3	2	1	0
CCH2 [7:0]							

TABLE 58: (CCL3) COMPARE/CAPTURE REGISTER 3, LOW BYTE - SFR C6H

7	6	5	4	3	2	1	0
CCL3 [7:0]							

TABLE 59: (CCH3) COMPARE/CAPTURE REGISTER 3, HIGH BYTE - SFR C7H

7	6	5	4	3	2	1	0
CCH3 [7:0]							

Compare/Capture Data Line Width

The VMX51C1020 is capable of comparing and capturing data using data lines up to 16 bits wide. When comparing 2 registers or capturing 1 register, it is required to set the T2SIZE bit of the T2CON register to 1. This adjusts the line width to 8-bits.

When comparing two pairs of registers, for example, CCH1 and CCL1 to TH2 and TL2, the T2SIZE bit must be set to 0. This adjusts the line width to 16 bits.

Timer2 Capture Modes

The Timer2 Capture Modes allow acquiring and storing the 16-bit contents of Timer2 into a Capture/Compare register following a MOV SFR operation or the occurrence of an external event on one of the CCU pins (described in the following table).

Capture input	Timer 2 Capture triggering event
CCU0	High to Low Transition on CCU0
CCU1	Low to High Transition on CCU1
CCU2	Low to High Transition on CCU2

Timer2 capture is done without affecting Timer2 operation.

Each individual Compare and Capture Unit can be configured for Capture Mode by configuring the appropriate bit pair of the CCEN register.
The two Capture modes are Mode 0 and Mode 1.

Capture Mode 0

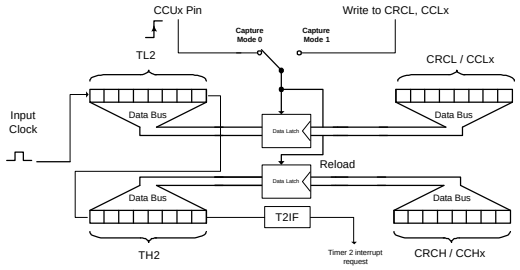
In Capture Mode 0, a transition on a given CCU pin triggers the latching of Timer2 data into the associated Compare/Capture register.

Capture Mode 1

In Capture Mode 1, a capture of the Timer2 value will occur upon writing to the Low Byte of the chosen capture register.

Note: On the VMX51C1020, the CCU3 input is NOT pinned out.

FIGURE 23: TIMER 2 CAPTURE MODE 0 FOR CRCL AND CRCH BLOCK DIAGRAM



The Capture modes can be especially useful for external event duration calculation with the ability to latch the timer value at a given time (computation can then be performed at a later time).

When operating in Capture Modes, the Compare and Capture units don't affect the VMX51C1020 Interrupts.

Timer2 Compare Modes

In Compare Mode, a Timer2 count value is compared to a value that is stored in the CCHxx/CCLx or CRCHx/CRCLx registers. If the values compared match (i.e. when the pulse changes state), a Compare/Capture interrupt is generated, if enabled. Varying the value of the CCHx/CCLx or CRCHx/CRCLx allows a variation of the rectangular pulse generated at the output. This variation can be used to perform pulse width modulation. See PWM in the following section.

In order to activate the Compare Mode on one of the four Compare Capture Units, the associated COCAHx and COCALx bits must be set to 1 and 0, respectively

When the Compare Mode is enabled, the corresponding output pin value is under the control of the internal timer circuitry.

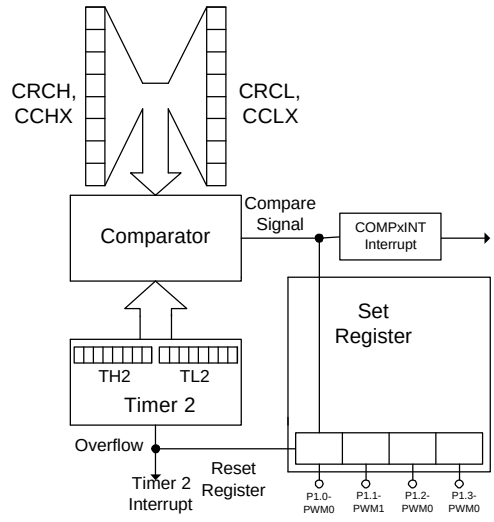
On the VMX51C1020, two Compare Modes are possible. In both modes, the new value arrives at port pin 1 in the same clock cycle as the internal compare signal is activated. The T2CM of the T2CON register defines the Compare Mode and is described in the following paragraphs.

Compare Mode 0

A functional diagram of Compare Mode 0 is shown below. A comparison is made between the 16-bit value of the Compare/Capture registers and the TH2, TL2 registers. When the Timer2 value exceeds the value stored in the CRCH, CRCL / CCHx, CCLx registers, a high compare signal is generated and a Compare/Capture interrupt is activated if enabled. If T2SIZE = 1, the comparison is made between the TL2 and CRCL/CCLx register.

This compare signal is then propagated to the pin corresponding P1.x Pin(s) and to the associated COMPINTx interrupt (if enabled). The corresponding P1.x pin is reset when a Timer2 overflow occurs.

FIGURE 24: TIMER 2 COMPARE MODE 0 BLOCK DIAGRAM

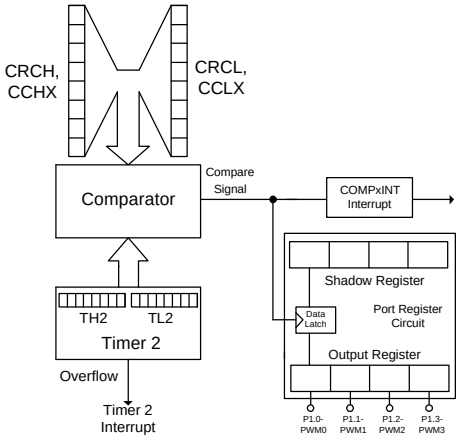


Compare Mode 1

When a given Compare Capture unit is operating in Mode 1, any write operations to the corresponding output register of the port P1.x (x=0 to3) will not appear on the physical port pin until the next compare match occurs.
As is the case in Compare Mode 0, the Compare signal in Mode 1 can also generate an interrupt (if enabled).

The figure below shows the operating structure of a given Capture Compare unit operating in Compare Mode 1.

FIGURE 25: TIMER 2 COMPARE MODE 1 BLOCK DIAGRAM

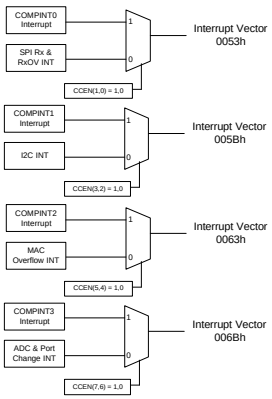


Timer 2 Compare Mode Interrupt

Configuration of the Compare and Capture Units for the “Compare Mode” through the CCEN register has an impact on the Interrupt structure of the VMX51C1020. In that specific mode each Compare Capture Unit takes control of one interrupt line.

When using the PWM output device, some care must be excercised to avoid other peripheral interrupts from being blocked by this mechanism.

FIGURE 26: COMPARE AND CAPTURE UNIT INTERRUPT CONTROL



Using Timer 2 for PWM Outputs

Configuring the Compare and Capture Units in Compare Mode 0 allows PWM output generation on the Port1 I/O pins. This mode can be used for PWM applications such as:

- o D/A conversion
- o Motor control
- o Light control
- o Etc.

When one specific Compare and Capture unit is configured for this mode, its associated I/O pin is reserved for this operation only and any write operation to the associated I/O pin of the P1 register will have no effect on it.

The following table shows the association between the Compare and Capture Units, associated registers and I/O pin

TABLE 60: COMPARE AND CAPTURE UNIT PWM ASSOCIATION

Compare Capture Unit	Registers	I/O pin
0	CRCH / CRCL	P1.0
1	CCH1 / CCL1	P1.1
2	CCH2 / CCL2	P1.2
3	CCH3 / CCL3	P1.3

PWM signal generation is derived from the comparison result between the values stored into the capture compare registers and the Timer2 value.
When a digital value is written into one of the Compare and Capture registers, a comparison is performed between this register and the Timer2 value (providing that Timer2 is in Compare Mode). As long as the value present in the Compare and Capture register is greater than the Timer2 value, the Compare unit will output a logic low.

When the value of Timer2 equals the value of the Compare and Capture register, the Compare unit will change from a logic Low to a logic High.

The clock source for the PWM is derived from Timer2; which is incremented at every signal pulse of the appropriate source. The source is selected by the T2IN1 and T2IN0 bits of the T2CON register
The T2SIZE bit of the T2CON register allows configuring the PWM output for 8 or 16-bit operation. The Timer2 Size affects all the PWM outputs.

When the Timer2 Size is 8-bits, the comparison is performed between Timer2 and the LSB of the Compare and Capture Unit register. The resulting PWM resolution is 8-bit.

When the Timer2 Size is configured for 16-bit operation, the comparison is performed between Timer2 and the contents of the whole Compare and Capture Unit register. The resulting PWM resolution is 16-bits but the PWM frequency is consequently low.

When the System clock is used as the Timer2 clock source, the PWM output frequency equals the Timer2 overflow rate. Note that the CLKDIVCTRL register contents affects Timer2 operation and thus, PWM output frequency.

Fosc	T2CON T2PSM	T2CON T2PS	T2CON T2SIZE	Freq PWM
14.74MHz	1	X	0	112.5Hz
	1	x	1	28.8KHz
	0	0-12	1-8	4.8KHz
	0	0-12	0-16	18.8Hz
	0	1-24	1-8	2.4KHz
	0	1-24	0-16	9.38Hz

The duty cycle of the PWM output is proportional to the ratio of the Compare and Capture Unit register's content versus the Maximum Timer2 number of cycles before overflow: 256 or 65536, depending on the T2SIZE bit value

PWM Duty Cycle Calculation: 8-bit
PWM duty cycle CCU0 (%) = 100% x (256-CRCL) / 256
PWM duty cycle CCU1-3 (%) = 100% x (256-CCLx) / 256

PWM Duty Cycle Calculation: 16-bit
PWM duty cycle CCU0 (%) = 100% x 65536–(CRCH, CRCL) / (CRCH, CRCL)
PWM duty cycle CCU1-3 (%) = 100% x 65536–(CRCH, CRCL) / (CRCH, CRCL)

PWM Configuration Example

The following example shows how to configure the Timer2 based PWM in 8-bit mode.

```
(…)
DIGPWREN = 0x80;                    //ENABLE TIMER 2 MODULE
T2CON = 0x61;                       //BIT 7 - Select 0=1/12, 1=1/24 of Fosc
                                    //BIT 6 - T2 clk source:  0 = Presc,
                                    1=clk/2
                                    //BIT 5 - T2 size: 0=16-bit, 1=8-bit
                                    //BIT 4,3 - T2 Reload mode:
                                    //BIT 2   - T2 Compare mode
                                    //BIT 1,0 - T2 input select: 01= input
                                    derived from osc.

//WHEN THE PWM IS CONFIGURED IN 16-BIT FORMAT, THE PWM OUTPUT
FREQUENCY IS GIVEN BY //THE FOLLOWING EXPRESSION:
// PWM Freq = [(FOSC/2)] / 65536
// WITH A 14.7456MHZ CRYSTAL PWM FREQUENCY = 112.5HZ

//When the PWM is configured in 8-bit its output freq  = [(Fosc/2)] / 256
//USING A 14.7456MHZ CRYSTAL PWM FREQUENCY = 28.8KHZ

CCEN = 0x0AA;                       //Enable Compare on 4 PWM outputs

// In 16-bit PWM resolution both LSB and MSB of compare unit are used

//In 8-bit PWM Resolution, only the LSB of compare units are used
// and MSB is kept to 00h

CRCL = 0x0E6;                       //PWM0 duty = [(256-CRCL)/256]
x100%
CRCH = 0x000;                       //E6h => 10.1%
CCL1 = 0x0C0;                       //PWM1 duty  = [(256-CCL1)/256]
x100%
CCH1 = 0x000;                       //C0h => 25%
CCL2 = 0x080;                       //PWM2 duty = [(256-CCL2)/256] x100%
CCH2 = 0x000;                       //80h => 50%
CCL3 = 0x033;                       //PWM3 duty = [(256-CCL3)/256] x100%
CCH3 = 0x000;                       //33h => 80%
P1PINCFG = 0x0F;                    //Configure P1 LSQ as output to enable
                                    PWM

(…)
```

Using the PWM as a D/A Converter

One of the popular uses of the PWM is to perform D/A conversion by low pass filtering its' modulated square wave output. The greater the duty cycle of the square wave, the greater the DC value is at the output of the low pass filter and vice versa.

Variations in the duty cycle of the PWM when filtered can therefore generate arbitrary waveforms.

Serial UART Interfaces

The VMX51C1020 includes two serial UART interface ports (UART0 and UART1). Each serial port has a 10-bit timer devoted to baud rate generation.

Both serial ports can operate in full duplex mode. The VMX51C1020 also includes a double buffer, enabling the UART to accept an incoming word before the software has read the previous value.

UART0 Serial Interface

The operation of UART0 of the VMX51C1020 is similar to the standard 8051 UART.

UART0 can derive its clock source from a 10-bit dedicated baud rate generator or from the Timer1 overflow.

UART0's Transmit and Receive buffers are accessed through a unique SFR register named S0BUF.

The UART0 S0BUF has a double buffering feature on reception which allows accepting an incoming word before the software has read the previous value from the S0BUF.

TABLE 61: (S0BUF) SERIAL PORT 0, DATA BUFFER - SFR 99H

7	6	5	4	3	2	1	0
S0BUF [7:0]							

UART0 Control Register

UART0 configuration is performed mostly via the S0CON SFR register located at address 98h.

TABLE 62: (S0CON) SERIAL PORT 0, CONTROL REGISTER - SFR 98H

7	6	5	4
S0M0	S0M1	MPCE0	R0EN

3	2	1	0
T0B8	R0B8	T0I	R0I

Bit	Mnemonic	Function
7	S0M0	Sets Serial Port Operating Mode See Table
6	S0M1	
5	MPCE	1 = Enables the multiprocessor communication feature.
4	R0EN	1 = Enables serial reception. Cleared by software to disable reception.
3	T0B8	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication etc.)
2	R0B8	In Modes 2 and 3, it is the 9th data bit received. In Mode 1, if sm20 is 0, RB80 is the stop bit. In Mode 0, this bit is not used. Must be cleared by software.
1	T0I	Transmit interrupt flag set by hardware after completion of a serial reception. Must be cleared by software.
0	R0I	Receive interrupt flag set by hardware after completion of a serial reception. Must be cleared by software.

UART0 Operating Modes

UART0 can operate in four distinct modes, which are defined by the SM0 and SM1 bits of the S0CON register (see following table).

TABLE 63: SERIAL PORT 0 MODES

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fclk/32 or /64
1	1	3	9-bit UART	Variable

**Note that the speed in mode 2 depends on SMOD bit in the Special Function Register PCON when SMOD = 1 fclk/32

UART0 - Mode 0

In this Mode, pin RX0 is used as an input and an output, while TX0 is used only to output the shift clock. For an operation in this mode, 8 bits are transmitted with the LSB as the first bit. Additionally, the baud rate is fixed at 1/12 of the crystal oscillator frequency. In order to initialize reception in this mode, the user must set bits R0I and R0EN in the S0CON register to 0 and 1, respectively. Note that in other Modes, when R0EN=1, the interface begins to receive data.

UART0 - Mode 1

In this Mode, the RX0 pin serves as an input and the TX0 pin as a serial output and no external shift clock is used. In Mode 0, 10-bits are transmitted:

- Start bit (logic low);
- 8-bits of data (LSB first);
- A stop bit (logic high).

The start bit synchronizes data reception, with the 8-bits of received data then being available in the S0BUF register. Reception is completed once the stop bit sets the R0B8 flag in the S0CON register.

UART0 - Mode 2

In this Mode the RX0 pin is used as an input and an output while TX0 is used to output the shift clock. In Mode 2, 11 bits are transmitted/received. hese 11-bits consist of:

- Start bit (logic low)
- 8 bits of data (LSB first),
- One programmable 9th bit,
- Stop bit (logic high).

The 9th bit is used for parity. In the data transmission case, bit TB80 of the S0CON is output as the 9th bit. For reception, the 9th bit will be stored captured in the RB80 bit of the S0CON register.

UART0 - Mode 3

Mode 3 is essentially identical to Mode 2, with the difference being that the internal baud rate generator or Timer1 can be used to set the baud rate.

UART0 - Baud Rate Generator Source

As mentioned previously, the UART0 baud rate clock can be sourced from either Timer 1 or the dedicated 10-bit baud rate generator.

Selection between these sources is enabled via the BAUDSRC bit of the U0BAUD register (see following table).

TABLE 64: (U0BAUD) UART0 BAUD RATE SOURCE SELECT - SFR D8H

7	6	5	4	3	2	1	0
BAUDSRC	-	-	-	-	-	-	-

7	BAUDSRC	Baud rate generator clock source 0 = Timer 1 1 = Use UART0 dedicated Baud rate generator
6:0	-	-

Using the UART0 dedicated baud rate generator, frees up Timer 1 for other uses.

The S0RELH and S0REL registers are used to store the 10-bit reload value of the UART0 baud rate generator.

TABLE 65: (S0RELL) SERIAL PORT 0, RELOAD REGISTER, LOW BYTE - SFR 96H

7	6	5	4	3	2	1	0
S0RELL [7:0]							

TABLE 66: (S0RELH) SERIAL PORT 0, RELOAD REGISTER, HIGH BYTE - SFR 97H

7	6	5	4	3	2	1	0
S0RELH [15:8]							

The following equations should be used to calculate the reload value for the SOREL register (examples follow).

Mode 3: For BAUDSRC=1
$SOREL = 1024 - \frac{2^{SMOD} \times f_{clk}}{64 \times \text{Baud Rate}}$
$\text{Baud Rate} = \frac{2^{SMOD} \times f_{clk}}{64 \times (1024 - SOREL)}$

TABLE 67: SERIAL 0 BAUD RATE SAMPLE VALUES BAUDSRC = 1, SMOD = 1

Desired Baud Rate	**S0REL @ f_{clk}= 11.059 MHz**	**S0REL @ f_{clk}= 14.75 MHz**
500.0 kbps	-	-
460.8 kbps	-	3FFh
230.4 kbps	-	3FEh
115.2 kbps	3FDh	3FCh
57.6 kbps	3FAh	3F8h
19.2 kbps	3EEh	3E8h
9.6 kbps	3DCh	3D0h
2.4 kbps	370h	340h
1.2 kbps	2E0h	280h
300 bps	-	-

TABLE 68: SERIAL 0 BAUD RATE SAMPLE VALUES BAUDSRC =1, SMOD = 0

Desired Baud Rate	**S0REL @ f_{clk}= 11.059 MHz**	**S0REL @ f_{clk}= 14.75 MHz**
115.2 kbps	-	3FEh
57.6 kbps	3FDh	3FCh
19.2 kbps	3F7h	3F4h
9.6 kbps	3EEh	3E8h
2.4 kbps	3B8h	3A0h
1.2 kbps	370h	340h
300 bps	1C0h	100

Timer1 can also be used as the baud rate generator for the UART0. Set BAUDSRC to 0 and assign Timer1's output to UART0.

When the baud rate clock source is derived from Timer1, the baud rate and timer reload values can be calculated using the following formulas (examples follow).

TABLE 69: EQUATION TO CALCULATE BAUD RATE FOR SERIAL 0

Serial 0: mode 1 and 3
Mode 1: ForU0BAUD.7=0 (standard mode)
$\text{Baud Rate} = \frac{2^{SMOD} \times f_{clk}}{32 \times 12 \times (256 - TH1)}$
$TH1 = 256 - \frac{2^{SMOD} \times f_{clk}}{32 \times 12 \times \text{Baud Rate}}$

TABLE 70: UART 0 BAUD RATE SAMPLE VALUES BAUDSRC =0, SMOD = 1

Desired Baud Rate	**TH1 @ f_{clk}= 11.059 MHz**	**TH1 @ f_{clk}= 14.75 MHz**
115.2 kbps	-	-
57.6 kbps	FFh	-
19.2 kbps	FDh	FCh
9.6 kbps	FAh	F8h
2.4 kbps	E8h	E0h
1.2 kbps	D0h	C0h
300 bps	40h	-

TABLE 71:UART 0 BAUD RATE SAMPLE VALUES BAUDSRC =0, SMOD = 0

Desired Baud Rate	**TH1 @ f_{clk}= 11.059 MHz**	**TH1 @ f_{clk}= 14.75 MHz**
115.2 kbps	-	-
57.6 kbps	-	-
19.2 kbps	-	FEh
9.6 kbps	FDh	FCh
2.4 kbps	F4h	F0h
1.2 kbps	E8h	E0h
300 bps	A0h	80h

Example of UART0 Setup and Use

In order to use UART0, the following operations must be performed:

- Enable the UART0 Interface
- Set I/O Pad direction TX= output, RX=Input
- Enable Reception (if required)
- Configure the Uart0 controller S0CON

The following are configuration and transmission code examples for UART0.

```
//-------------------------------------------------------------------------------------//
// UART0 CONFIG with S0REL
//
// Configure the UART0 to operate in RS232 mode at 19200bps
// with a crystal of 14.7456MHz
//
//-------------------------------------------------------------------------------------//
void uart0ws0relcfg()
        {
        P3PINCFG |= 0x01;               // pads for uart 0
        DIGPWREN |= 0x01;               // enable uart0/timer1
        S0RELL = 0xF4;                  //com speed = 19200bps
        S0RELH = 0x03;
        S0CON = 0x50;           // Uart0 in mode1, 8 bit, var. baud rate
        U0BAUD = 0x80;          //Set S0REL is source for UART0
                                //Baud rate clock

        }//end of uart0ws0relcfg() function

//-------------------------------------------------------------------------------------//
// UART0 CONFIG with Timer 1
//
// Configure the UART0 to operate in RS232 mode at 19200bps
// with a crystal of 14.7456MHz
//
//-------------------------------------------------------------------------------------//
void uart0wTimer1cfg()
        {
        P3PINCFG |= 0x01;               // pads for uart0
        DIGPWREN |= 0x01;               // enable uart0/timer1
        TMOD &= 0x0F;
        TMOD =0x20;             //Set Timer 1, Gate 0, Mode 2
        TH1 = 0xFE;                     //Com Speed = 19200bps
        TCON &= 0x0F;
        TCON =0x40;                     //Start Timer 1
        U0BAUD = 0x00;                  //Set Timer 1 Baud rate
                                        //generator for UART0

        PCON = 0x00;                    //Set SMOD = 0
        S0CON = 0x50;                   // Config Uart0 in mode 1,
                                        //8 bit, variable baud rate
        }//end of uart1Config() function

//-------------------------------------------------------------------------------------//
// Txmit0()
//
// One Byte transmission on UART0
//-------------------------------------------------------------------------------------//

// - Constants definition
sbit UART_TX_EMPTY = USERFLAGS^1;

void txmit0( unsigned char charact){
        S0BUF = charact;
        USERFLAGS = S0CON;
        //Wait TX EMPTY flag to be raised
        while (!UART_TX_EMPTY) {USERFLAGS = S0CON;}S0CON =

        //clear both R0I & T0I bits
        S0CON & 0xFD;
        }//end of txmit0() function
```

See the Interrupt section for example of setup of UART0 interrupts

UART1 Serial Interface

The UART1 serial interface is based on a subset of UART0. It provides two operating modes and its clock source is derived exclusively from a dedicated 10-bit baud rate generator.

The UART1 Transmit and Receive buffers are accessed via SFR register S1BUF.

TABLE 72: (S1BUF) SERIAL PORT 1, DATA BUFFER - SFR C1H

7	6	5	4	3	2	1	0
S1BUF [7:0]							

As is the case with UART0, UART1 includes a double buffering feature in order to avoid overwriting of the receive register.

UART1 Control Register

UART1 is controlled by the S1CON register. The following table provides a description of the UART1 Control Register.

TABLE 73: (S1CON) SERIAL PORT 1, CONTROL REGISTER - SFR C0H

7	6	5	4
S1M	Reserved	MPCE1	R1EN

3	2	1	0
T1B8	R1B8	T1I	R1I

Bit	Mnemonic	Function
7	S1M	Operation mode Select
6	Reserved	-
5	MPCE1	1 = Enables multiprocessor communication feature.
4	R1EN	If set, enables serial reception. Cleared by software to disable reception.
3	T1B8	The 9th transmitted data bit in mode A. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication, etc.)
2	R1B8	In Mode A, it is the 9th data bit received. In Mode B, if SM21 is 0, RB81 is the stop bit. Must be cleared by software.
1	T1I	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software
0	R1I	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software

UART1: Operating Modes

The VMX51C1020 UART1 has two operating Modes, A and B, which provide 9 or 8-bit operation, respectively (see following table).

TABLE 74: UART1 MODES

SM	MODE	DESCRIPTION	BAUD RATE
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

UART1 - Mode A

In this Mode, 11 bits are transmitted or received. These 11 bits are composed of:

- A start bit (logic low),
- 8 bits of data (LSB first),
- A programmable 9th bit,
- Stop bit (logic high).

As in Mode 2 and 3 of UART0, the 9th bit is used for parity. For data transmission, the TB81 bit of the S1CON register holds the 9th bit. In the case of reception, the 9th bit will be captured into the R1B8 bit of the S1CON register.

UART1 - Mode B

In this Mode, 10 bits are transmitted and consist of:

- A start bit (logic low)
- 8 bits of data (LSB first);
- A stop bit (logic high).

Received data (8-bit) is read via the S1BUF register. Reception is completed once the stop bit sets the R1B8 flag in the S1CON register.

UART1 - Baud Rate Generator

As previously mentioned, UART1's clock source is derived from a dedicated 10-bit baud rate generator module.

The S1REL registers are used to adjust the baud rate of UART1.

TABLE 75: (S1RELL) UART1, RELOAD REGISTER, LOW BYTE - SFR BEH

7	6	5	4	3	2	1	0
S1RELL [7:0]							

TABLE 76: (S1RELH) UART 1, RELOAD REGISTER, HIGH BYTE - SFR BFH

7	6	5	4	3	2	1	0
S1RELH [7:0]							

The following formulas are used to calculate the baud Rate, S1RELL and S1RELH values.

Serial 1
$\text{Baud Rate} = \frac{f_{clk}}{32 \times (1024 - \text{S1REL})}$ Note: S1REL.9-0 = S1RELH.1-0 + S1RELL.7-0
$\text{S1REL} = 1024 - \frac{f_{clk}}{32 \times \text{Baud Rate}}$

TABLE 77: SERIAL 1 BAUD RATE SAMPLE VALUES

Desired Baud Rate	S1REL @ f_{clk}= 11.0592 MHz	S1REL @ f_{clk}= 14.746 MHz
500.0 kbps	-	-
460.8 kbps	-	3FFh
230.4 kbps	-	3FEh
115.2 kbps	3FDh	3FCh
57.6 kbps	3FAh	3F8h
19.2 kbps	3EEh	3E8h
9.6 kbps	3DCh	3D0h
2.4 kbps	370h	34Fh
1.2 kbps	2E0h	280h

Setting Up and Using UART1

In order to use UART1, the following operations must be performed:

- Enable the UART1 Interface
- Set I/O Pad direction TX= output, RX=Input
- Enable Reception (if required)
- Configure the UART1 controller S1CON

Example of UART1 Setup and Use

The following are C code examples of UART1 configuration, serial byte transmission and interrupt usage.

```
//-------------------------------------------------------------------------------//
// UART1 CONFIG
//
// Configure the UART1 to operate in RS232 mode at 115200bps
// with a crystal of 14.7456MHz
//-------------------------------------------------------------------------------//
void uart1Config(void)
        {
        P0PINCFG |= 0x04;       // pads for uart 1
        DIGPWREN |= 0x02;       // enable uart1
        S1RELL = 0xFC;          // Set com speed = 115200bps
        S1RELH = 0x03;
        S1CON = 0x90;           // Mode B, receive enable
        }//end of uart1Config() function


//-------------------------------------------------------------------------------//
// TXMIT1  -- Transmit one byte on the UART1
//-------------------------------------------------------------------------------//
void txmit1( unsigned char charact){
        S1BUF = charact;
        USERFLAGS = S1CON;
        while (!UART_TX_EMPTY) {USERFLAGS = S1CON;}
                                        //Wait TX EMPTY flag
        S1CON = S1CON & 0xFD;           //clear both R1I & T1I bits
        }//end of txmit1() function


//-------------------------------------------------------------------------------//
// Interrupt configuration
//-------------------------------------------------------------------------------//

IEN0 |= 0x80;                   // Enable all interrupts
IEN2 |= 0x01;                   // Enable interrupt UART 1


//-------------------------------------------------------------------------------//
// Interrupt function
//-------------------------------------------------------------------------------//

void int_serial_1 (void) interrupt 16
{
IEN0 &= 0x7F;                   // Disable all interrupts

        /*-----------------------*/
        /*Interrupt code here*/
        /*-----------------------*/

if (S1CON&0x01==0x01)
        {
        S1CON &= 0xFE;          // Clear RI (it comes
                                // before T1I)
        }
        else
        {
        S1CON &= 0xFD;          // Clear T1I
        }
        IEN0 |= 0x80;}          // Enable all interrupts
        }
}
/-------------------------------------------------------------------
```

UART1 Driven Differential Transceiver

The VMX51C1020 includes a differential transceiver compatible with the J1708/RS-485/RS-422 standards. These are driven by UART1.

The Transceiver's signals are differential which provide high electrical noise immunity. The differential interface is capable of transferring/recieving data over hundreds of feet of twisted pair wire.

A number of devices can be connected in parallel to the differential bus in order to implement a multi-drop network. The number of devices that can be networked depends on the bus length and configuration.

The admissible common mode voltage range of the differential interface is –2.0 V to +7.0 V. When implementing this type of transmission network over long distances in noisy environments, appropriate protection is recommended in order to prevent the common mode voltage from causing any damage to the VMX51C1020.

FIGURE 27: DIFFERENTIAL INTERFACE (J1708 CONFIG)

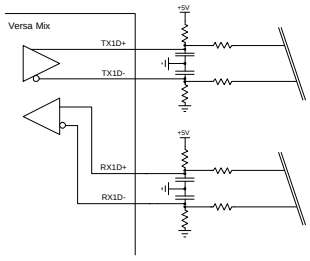
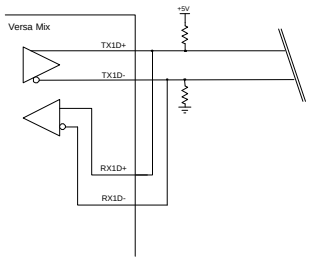


FIGURE 28: DIFFERENTIAL INTERFACE (RS485 CONFIG)



From the software point of view, the differential transceiver is viewed as differential UART.

The differential transceiver I/Os are connected to UART1 of the VMX51C1020, therefore communication parameters such as the data length, speed, etc are managed by the UART1 peripheral interface/registers.

Using the UART1 Differential Transceiver

In order to use the Differential Transceiver interface, one must perform the following operations:

- Enable UART1 and the differential interface by setting bits 1 and 2 of the DIGPWREN register.
- Configure UART1's operating mode via the S1CON register.
- Set the baud rate via the S1RELH and S1RELL registers.
- Enable UART1's interrupt, if required

Use UART1's S1BUF register to transmit and receive data through the differential transceiver. If the P0.2 pin is configured as an output, the signal corresponding to the TX1 signal of UART1 will appear on this pin (note that the P0.3-RX1 pin can be used as regular digital output).

When the transceiver is connected in Half-Duplex mode (RX1D+ connected to TX1D+ and RX1D- connected to TX1D-) and UART1's interrupts are enabled, careful management of the UART1 interrupts will be required as every byte transmitted will generate a local Rx interrupt.

Differential Interface Use Example

The following code provides and an example of configuration and use of the VMX51C1020 Differential Interface.

```
#pragma SMALL
#pragma UNSIGNEDCHAR
#include <vmixreg.h>

// --- function prototypes
void txmit1( unsigned char charact);
void uart1differential(void);

// - global variables

// - Constants definition
sbit UART_TX_EMPTY = USERFLAGS^1;

code char irq0msg[]="Ramtron inc";

//-------------------------------------------------------------------------------------//
//                              MAIN FUNCTION
//-------------------------------------------------------------------------------------//

 at 0x0100 void main (void) {

// Enable and configure the UART1
        uart1differential();        //Config UART1 diff interface

// Warning:  The Clock Control circuit does affect the dedicated baud rate
//           generator S0REL, S1REL and Timer1 operation


//*** Configure the interrupts
        IEN0 |= 0x81;               //Enable interrupts + Ext. 0 interrupt
        IEN2 |= 0x01;               //Enable UART1 Interrupt

        Txmit1("A");                //Transmit one character on UART1

        do
        {

        }while(1);                  //Wait for UART1 Rx interrupt

}// End of main()...


//-------------------------------------------------------------------------------------//
// UART1 Differential interface interrupt
//
// In this example, the source of UART1 interrupt would be caused
// by bytes reception on the differential interface
//-------------------------------------------------------------------------------------//
void int_uart1 (void) interrupt 16 {
        unsigned char charact;

        IEN0 &= 0x7F;

        // -- Put you code here…

        S1CON = S1CON & 0xFC;           //clear both R1I & T1I bits
        IEN0 |= 0x80;                   // enable all interrupts

}// end of uart1 INTERRUPT

//-------------------------------------------------------------------------------------//
// EXT INT0 interrupt
//
//
// when the External interrupt 0 is triggered A Message string  is sent over the
// the serial UART1
//-------------------------------------------------------------------------------------//
void int_ext_0 (void) interrupt 0 {

        int x=0;
        idata unsigned char     cptr=0x01;

        IEN0 &= 0x7F;
                                //disable ext0 interrupt

        cptr = cptr-1;
        while( irq0msg[cptr] != '\n')
        //Send a text string over the differential interface
                {
                txmit1( irq0msg[cptr]);
                cptr = cptr +1;
                }

        IEN0 = 0x81;
                                //Enable all interrupts + int_0

//-------------------------------------------------------------------------------------//
//------------------------------ Individual Functions ---------------------------------//
//-------------------------------------------------------------------------------------//

//-------------------------------------------------------------------------------------//
// UART1 DIFFERENTIAL CONFIG
//
// Configure the UART1 differential interface to operate in
// RS232 mode at 115200bps with a crystal of 14.7456MHz
//
//-------------------------------------------------------------------------------------//
void uart1differential(void)
        {
        DIGPWREN |= 0x06;       // enable uart1 & differential transceiver
        P0PINCFG |= 0x04;       // pads for uart1
        P0PINCFG = 0x00;

        S1RELL = 0xFC;          // Set com speed = 115200bps
        S1RELH = 0x03;
        S1CON = 0x90;           // Mode B, receive enable
        }//end of uart1differential()  function

//-------------------------------------------------------------------------------------//
// TXMIT1
//
// Transmit one byte on the UART1 Differential interface
//
//-------------------------------------------------------------------------------------//
void txmit1( unsigned char charact){
        S1BUF = charact;
        USERFLAGS = S1CON;

        //Wait TX EMPTY flag to be raised

        while (!UART_TX_EMPTY) {USERFLAGS = S1CON;}

        S1CON = S1CON & 0xFD;           //clear both R1I & T1I bits
        }//end of txmit1() function
```

SPI Interface

The VMX51C1020's SPI peripheral is a highly configurable and powerful interface enabling high speed serial data exchange with external devices such as A/Ds, D/Aa, EEPROMs, etc.

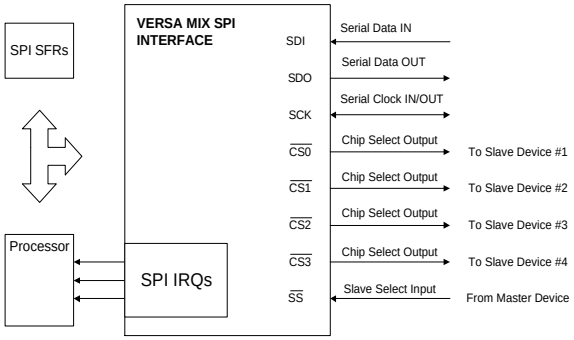
The SPI interface can operate as either a master or a slave device. In master mode, it can control up to 4 slave devices connected to the SPI bus.

The following lists a number of the VMX51C1020's SPI features.

- Allows synchronous serial data transfers
- Transaction size is configurable from 1-32-bits and more.
- Full duplex support
- SPI Modes 0, 1, 2, 3 and 4 supported (Full clock polarity and phase control)
- Up to four slave devices can be connected to the SPI bus when it is configured in master mode
- Slave mode operation
- Data transmission speed is configurable
- Double 32-bit buffers in transmission and reception
- 3 dedicated interrupt flags
  - TX-Empty
  - RX Data Available
  - RX Overrun
- Automatic/Manual control of the chip selects lines.
- SPI operation is not affected by the clock control unit

The following provides a block diagram view of the SPI Interface.

FIGURE 29: SPI INTERFACE BLOCK DIAGRAM



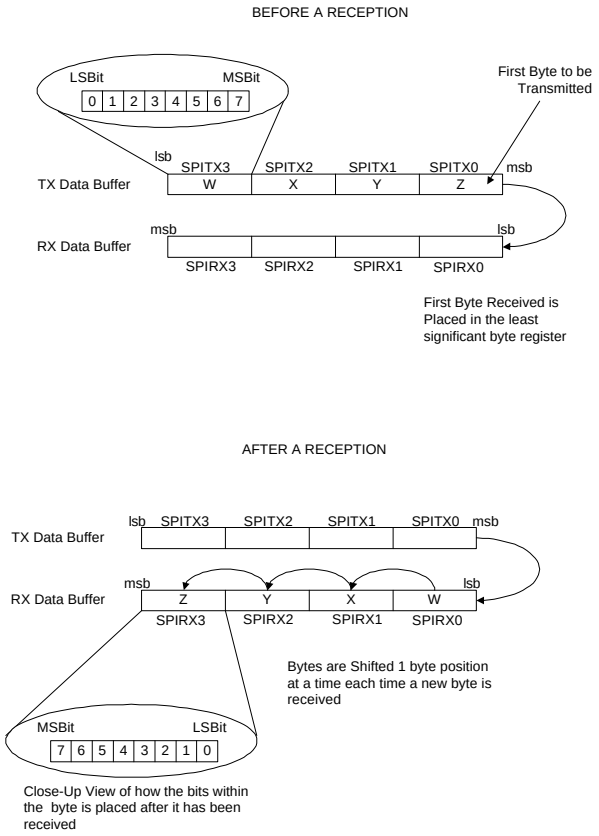
SPI Transmit/Receive Buffer Structure

When receiving data, the first byte received is stored in the SPIRX0 Buffer. As bits continue to arrive, the data already present in the buffer is shifted towards the least significant byte end of the receive registers (see following figure).

For example (see following figure), assume the SPI is about to receive 4 consecutive bytes of data: W, X, Y and Z, where the first byte received is byte W, The first received byte (W) will be placed in the SPIRX0 register. Upon reception of the next byte (X), the contents of SPIRX0 will be shifted into SFR register SPIRX1 and byte X will be placed in the SPIRX0 registers. Following this same procedure, we bytes W, X, Y and Z will end up in RX data buffer registers SPIRX0, SPIRX1, SPIRX2 and SPIRX3, respectively.

The case where the SDO and SDI pins are shorted together is represented in the following diagram.

FIGURE 30 : SPI INTERFACE RECEIVE TRANSMIT SCHEMATIC



When using the SPI Interface, it is important to keep in mind that a transmission is started when the SPIRX3TX0 register is written to.

From an SFR point of view, the transmission and reception buffers of the SPI interface occupy the following addresses.

TABLE 78: (SPIRX3TX0) SPI DATA BUFFER, LOW BYTE - SFR E1H

7	6	5	4	3	2	1	0
SPIRX3TX0 [7:0]							

Bit	Mnemonic	Function
7-0	SPITX0	SPI Transmit Data Bits 7:0
	SPIRX3	SPI Receive Data Bits 31:24

TABLE 79: (SPIRX2TX1) SPI DATA BUFFER, BYTE 1 - SFR E2H

7	6	5	4	3	2	1	0
SPIRX2TX1 [15:8]							

Bit	Mnemonic	Function
15:8	SPITX1	SPI 1 Transmit Data Bits 15:8
	SPIRX2	SPI Receive 1 Data Bits 23:16

TABLE 80: (SPIRX1TX2) SPI DATA BUFFER, BYTE 2 - SFR E3H

7	6	5	4	3	2	1	0
SPIRX1TX2 [23:16]							

Bit	Mnemonic	Function
22:16	SPITX2	SPI Transmit Data Bits 23:16
	SPIRX1	SPI Receive Data Bits 15:8

TABLE 81: (SPIRX0TX3) SPI DATA BUFFER, HIGH BYTE - SFR E4H

7	6	5	4	3	2	1	0
SPIRX0TX3 [31:24]							

Bit	Mnemonic	Function
31:24	SPITX3	SPI Transmit Data Bits 31:24
	SPIRX0	SPI Receive Data Bits 7:0

SPI Control Registers

The SPI Control registers are used to define:

- SPI operating speed (Master mode)
- Active Chip Select output (Master mode)
- SPI clock Phase (Master/Slave modes).
- SPI clock Polarity (Master/Slave modes).

TABLE 82: (SPICTRL) SPI CONTROL REGISTER - SFR E5H

7	6	5	4
SPICK [2:0]			SPICS_1

3	2	1	0
SPICS_0	SPICKPH	SPICKPOL	SPIMA_SL

Bit	Mnemonic	Function
7:5	SPICK[2:0]	SPI Clock control 000 = OSC Ck Div 2 001 = OSC Ck Div 4 010 = OSC Ck Div 8 011 = OSC Ck Div 16 100 = OSC Ck Div 32 101 = OSC Ck Div 64 110 = OSC Ck Div 128 111 = OSC Ck Div 256
4:3	SPICS[1:0]	Active CS line in Master Mode 00 = CS0- Active 01 = CS1- Active 10 = CS2- Active 11 = CS3- Active
2	SPICKPH	SPI Clock Phase
1	SPICKPOL	SPI Clock Polarity 0 – CK Polarity is Low 1 – CK Polarity is High
0	SPIMA_SL	Master / -Slave 1 = Master 0 = Slave

SPI Operating Speed

Three bit in the SPICTRL register serve to adjust the communication speed of the SPI interface.

SPICK[2:0] Div Ratio	Fosc = 14.74MHz	Fosc = 11.059MHz
Clk Div 2	7.37 MHz	5.53 MHz
Clk Div 4	3.68 MHz	2.76 MHz
Clk Div 8	1.84 MHz	1.38 MHz
Clk Div 16	922 kHz	691 kHz
Clk Div 32	461 kHz	346 kHz
Clk Div 64	230 kHz	173 kHz
Clk Div 128	115 kHz	86 kHz
Clk Div 256	57.6 kHz	43.2 kHz

SPI Master Chip Select Control

When the SPI is configured in Master mode, the value of the SPICS[1:0] bits will define which Chip select pins will be active during the transaction.

The following sections will describe how the SPI Clock Polarity and Phase affects the read and write operations of the SPI interface.

SPI Operating Modes

The SPI interface can operate in four distinct modes defined by the SPICKPH and SPICKPOL bits of the SPICTRL register.

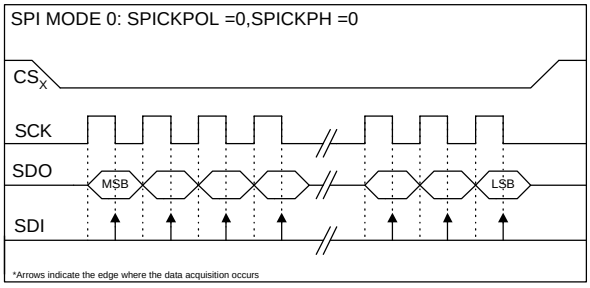
SPICKPH defines the SPI clock phase and SPICKPOL defines the Clock polarity for data exchange.

SPICKPOL bit value	SPICKPH bit value	SPI Operating Mode
0	0	SPI Mode 0
0	1	SPI Mode 1
1	0	SPI Mode 2
1	1	SPI Mode 3

SPI Mode 0

- Data is placed on the SDO pin at the rising edge of the clock.
- Data is sampled on the SDI pin at the falling edge of the clock.

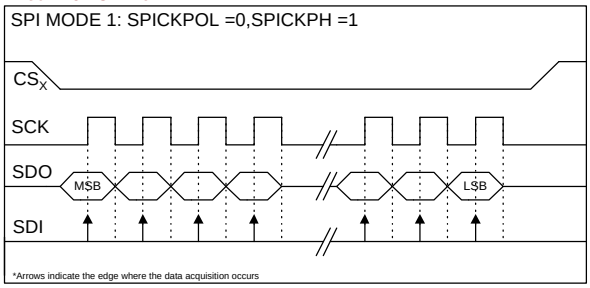
FIGURE 31 : SPI MODE 0



SPI Mode 1

- Data is placed on the SDO pin at the falling edge of the clock.
- Data is sampled on the SDI pin at the rising edge of the clock.

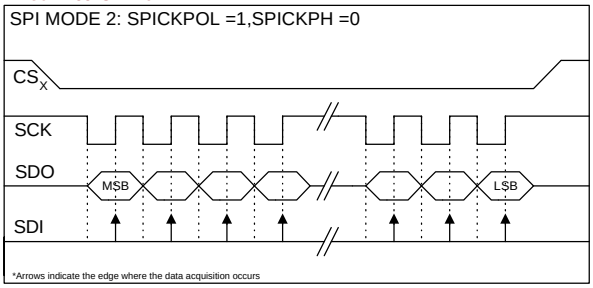
FIGURE 32: SPI MODE 1



SPI Mode 2

- Data is placed on the SDO pin at the falling edge of the clock.
- Data is sampled on the SDI pin at the rising edge of the clock.

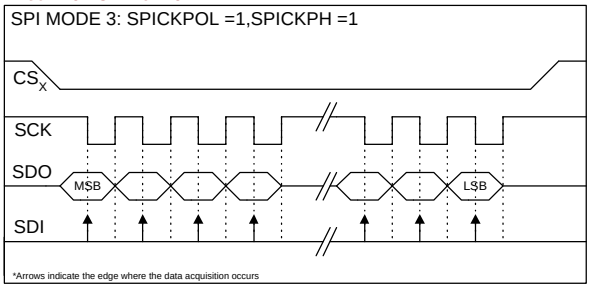
FIGURE 33: SPI MODE 2



SPI Mode 3

- Data is placed on the SDO pin at the rising edge of the clock.
- Data is sampled on the SDI pin at the falling edge of the clock.

FIGURE 34: SPI MODE 3



SPI Transaction Size

Many SPI based microcontrollers only allow a fixed SPI transaction size of 8-bits. However, most devices requiring SPI control require transactions of more than 8-bits, giving way to alternate inefficient means of dealing with SPI transactions.

The VMX51C1020 SPI interface includes a transaction size control register, SPISIZE that enables different sized transaction to be performed. The SPI interface also automatically controls the Chip select line.

The following table describes the SPISIZE register.

TABLE 83: (SPISIZE) SPI SIZE CONTROL REGISTER - SFR E7H

7	6	5	4	3	2	1	0
SPISIZE[7:0]							

Bit	Mnemonic	Function
7:0	SPISIZE[7:0]	Value of the SPI packet size

The following formula is used to calculate the transaction size.

For SPISIZE from 0 to 31:

SPI Transaction Size = [SPISIZE + 1]

For SPISIZE from 32 to 255*:

SPI Transaction Size = [SPISIZE*8 - 216]

An SPI transaction size greater than 32 bits is possible when using the VMX51C1020 SPI interface, however, large data packets of this size require careful management of the associated interrupts in order to avoid buffer overwrites.

SPI Interrupts

The SPI interface has three associated interrupts.

- SPI RX Overrun
- SPI RX Data Available
- SPI TX Empty

The SPIRXOVIE, SPIRXAVIE and SPITXEMPIE bits of the SPICONFIG register allow individual enabling of the above interrupt sources at the SPI interface level.

At the processor level, two interrupt vectors are dedicated to the SPI interface:

- SPI RX data available and Overrun interrupt
- SPI TX empty interrupt

In order to have the processor jump to the associated interrupt routine, you must also enable one or both of these interrupts in the IEN1 register as well as set the EA bit of the IEN0 register (see interrupt section).

TABLE 84: (SPICONFIG) SPI CONFIG REGISTER - SFR E6H

7	6	5	4
SPICSLO	-	FSONCS3	SPILOAD

3	2	1	0
-	SPIRXOVIE	SPIRXAVIE	SPITXEMPIE

Bit	Mnemonic	Function
7	SPICSLO	Manual CS up (Master mode) 0 = The CSx goes low when transmission begins and returns to high when it ends. 1 = The CSx stays low after transmission ends. The user must clear this bit for the CSx line to return high.
6	-	-
5	FSONCS3	This bit sends the frame select pulse on CS3.
4	SPILOAD	This bit sends load pulse on CS3.
3	-	-
2	SPIRXOVIE	SPI Receiver overrun interrupt enable.
1	SPIRXAVIE	SPI Receiver available interrupt enable.
0	SPITXEMPIE	SPI Transmitter empty interrupt enable.

The SPIIRQSTAT register contains the interrupts flags associated with the SPI interface.

Monitoring these bits allows polling the control of the SPI interface.

TABLE 85: (SPIIRQSTAT) SPI INTERRUPT STATUS REGISTER - SFR E9H

7	6	5	4
-	-	SPITXEMPTO	SPISLAVESEL

3	2	1	0
SPISEL	SPIOV	SPIRXAV	SPITXEMP

Bit	Mnemonic	Function
7:6	-	-
5	SPITXEMPTO	Flag that indicates that we have not reloaded the transmit buffer fast enough (only used for packets greater than 32 bits.).
4	SPISLAVESEL	Slave Select “NOT” (SSN)
3	SPISEL	This bit is the result of the logical AND operation between CS0, CS1, CS2 and CS3. (Indicates if one chip is selected.)
2	SPIOV	SPI Receiver overrun
1	SPIRXAV	SPI Receiver available
0	SPITXEMP	SPI Transmit buffer is ready to receive mode data. It does not flag that the transmission is completed.

SPI Manual Chip Select Control

In some applications, manual control of the active select line can be useful. Setting the SPICSLO bit of the SPICONFIG register forces the active chip select line to stay low when the SPI transaction is completed in Master mode. When the SPICSLO bit is cleared, the Chip select line returns to its inactive state.

SPI Manual Load Control

The SPI can generate a LOAD pulse on the CS3 pin when the SPILOAD bit is set. This is useful for some D/A converters and avoids having to use a separate I/O pin for this purpose.

SPI Frame Select Control

It's also possible to generate a positive pulse on the CS3 pin of the SPI interface by setting the FSONCS3 bit of the SPICONFIG register. This feature can be used to generate a Frame Select signal required by some DSP compatible devices without requiring the use of a separate I/O pin.

Note that when both the SPILOAD and FSONCS3 are selected, the internal logic give priority to the Frame Select pulse.

SPI Interface to 16-bit D/A Example

The following is a code example for doing 16-bit transfers over the the SPI interface.

```
//-----------------------------------------------//
// VMIX_SPI_to_dac_interface. c    //
//-----------------------------------------------//
//
//  This demonstration program show the how to interface a 16-bit D/A
//  to the VMX51C1020 SPI interface.
//
#pragma SMALL
#include <vmixreg.h>

// --- function prototypes

//Function Prototype:  Send Data to the 16 bit D/A

void send16bitdac( unsigned char valhigh, unsigned char vallow);

// Bit definition
sbit SPI_TX_EMPTY = USERFLAGS^0;

//-------------------------------------------------------------------------//
//                          MAIN FUNCTION                                  //
//-------------------------------------------------------------------------//
 at 0x0100 main (void) {

                unsigned char dacvall=0;                //LSB of current DAC value
                unsigned char dacvalh=0;                //MSB of current DAC value
                DIGPWREN |= 0x08;                       //ENABLE SPI INTERFACE

                //*** Initialise the SPI interface ****
                P2PINCFG |= 0x68;                       // config I/O port to allow the SPI
                                                        //interface to access the pins
// In this application we only need to configure the 5 upper bit of P2PINCFG
                        // P2PINCFG bit 7 - SDIEN  = 0 -> INPUT (NOT USED)
                        // P2PINCFG bit 6 - SDOEN  = 1 -> OUTPUT TO DAC SDI PIN
                        // P2PINCFG bit 5 - SCKEN  = 1 -> OUTPUT TO DAC SCK PIN
                        // P2PINCFG bit 4 - SSEN   = 0 -> INPUT (NOT USED)
                        // P2PINCFG bit 3 - CS0EN  = 1 -> OUTPUT TO DAC CS PIN
                        // P2PINCFG bit 2 - CS1EN  = 0 -> INPUT (NOT USED)
                        // P2PINCFG bit 1 - CS2EN  = 0 -> INPUT (NOT USED)
                        // P2PINCFG bit 0 - CS3EN  = 0 -> INPUT (NOT USED)


                SPICTRL = 0x25;
                        // SPI ctrl: OSC/16, CS0, phase=0, pol=0, master
                        // SPICK    BIT 7:5  = 001 -> SPI CLK SPEED = OSC/2
                        // SPICS    BIT 4:3  = 00  -> CS0 LINE IS ACTIVE
                        // SPICKPH  BIT 2    = 1 SPI CLK PHASE
                        // SPICKPOL BIT 1    = 0 SPI CLOCK POLARITY
                        // SPIMA_SL BIT 0    = 1 -> SET SPI IN MASTER MODE

                SPICONFIG = 0x00;
                        // SPI CONFIG: auto CSLO, no FS, NO Load, clear IRQ flags
                        // SPICSLO    BIT 7 = 0 AUTOMATIC CHIP SELECT CONTROL
                        // UNSUSED    BIT 6 = 0
                        // FSONCS3  BIT 5 = 0 Do not send FrameSelect Signal on CS3
                        // SPILOAD    BIT 4 = 0 do not Sen the Low pulse on CS3
                        // UNUSED     BIT 3 = 0
                        // SPIRXOVIE  BIT 2 = 0 Dont enable SPI RX Overrun IRQ
                        // SPIRXAVIE  BIT 1 = 0 Dont enable SPI RX AVAILLABLE IRQ
                        // SPITXEMPIE BIT 0 = 0 Dont Enable  SPI TX EMPTY IRQ

                SPISIZE = 0x0F;                 // SPI SIZE:  16-bits

                // GENERATE A TRIANGLE WAVE ON THE DAC OUTPUT

                while(1){

                        do{
                        dacvall = dacvall + 1;
                        if( dacvall==0xff)
                                        {
                                        dacvalh = dacvalh +1;
                                        dacvall = 0x00;
                                        }

                        send16-bitdac( dacvalh, dacvall);
                        }while( (dacvall != 0xff) && (dacvalh != 0xff) );

                        do{
                        dacvall = dacvall - 1;
                        if( dacvall==0x00)
                                        {
                                        dacvalh = dacvalh - 1;
                                        dacvall = 0xff;
                                        }
                        send16-bitdac( dacvalh, dacvall);
                        }while( (dacvall != 0x00) && (dacvalh != 0x00) );
                        };

}// End of main()...

//-------------------------------------------------------------------------//
//  Send16-bitdac - Send data to 16 bit D/A Converter    //
//-------------------------------------------------------------------------//
void send16-bitdac( unsigned char valhigh, unsigned char vallow){

//              USERFLAGS = 0x00;
//              while(!SPI_TX_EMPTY){USERFLAGS = SPIIRQSTAT;}

                SPIRX2TX1 = vallow;     //Put LSB of value in SPI transmit buffer
                                        //-> trigger transmission
                SPIRX3TX0 = valhigh;    //Put MSB of value in SPI transmit buffer
                                        //-> trigger transmission

                do{             //Wait SPI TX empty flag to be activated
                                USERFLAGS = P2;
                                USERFLAGS &= 0x08;
                                }while( USERFLAGS == 0);
}//end of send16-bitdac
```

SPI Interrupt Example

The following provides an example of basic SPI configuration and Interrupt handling.

```
//-------------------------------------------------------------------------------//
// Sample C code for SPI RX & TX interrupt set-up
//-------------------------------------------------------------------------------//
//
#pragma SMALL
#include <vmixreg.h>

at 0x0100 main (void) {


DIGPWREN = 0x08;                    // Enable SPI
P2PINCFG = 0x4F;                    // Set pads direction
SPICONFIG = 0x03;                   // Enable Rx_avail + TX_empty
SPISIZE = 0x07;                     // SPI SIZE:  8 bits


IEN0 |= 0x80;               // Enable all interrupts
IEN1 |= 0x06;               // Enable SPI Txempty + RXavail interrupt

SPIRX3TX0 = valhigh;        //Put MSB of value in SPI transmit buffer
                            //-> trigger transmission

            Do{
                            }while(1)

}//end of main()


//-------------------------------------------------------------------------------//
// SPI TX Empty Interrupt function
//-------------------------------------------------------------------------------//

void int_2_spi_tx (void) interrupt 9
{
IEN0 &= 0x7F;                       // Disable all interrupts

            /*-------------------------*/
            /* Interrupt code here*/
            /*-------------------------*/

IRCON &= 0xFD;                      // Clear flag SPITXIF
IEN0 |= 0x80;                       // Enable all interrupts
}

//-------------------------------------------------------------------------------//
// SPI RX availlable function
//-------------------------------------------------------------------------------//

void int_2_spi_rx (void) interrupt 10
{
IEN0 &= 0x7F;                       // Disable all interrupts

            /*-------------------------*/
            /* Interrupt code here*/
            /*-------------------------*/

IRCON &= 0xFB;                      // Clear flag SPIRXIF
IEN0 |= 0x80;                       // Enable all interrupts
}


//-------------------------------------------------------------------------------//
```

Due to the double buffering of the SPI interface, an SPI TX empty interrupt will be activated as soon as the data to be transmitted is written into the SPI interface transmit buffer. If data is subsequently written into the SPI transmit buffer before the original data has been transmitted, the TX empty interrupt will only be activated when the original data has been fully transmitted.

The SPI also includes double buffering for data reception. Once a data reception is completed, the RX interrupt is activated and the data is transferred into the SPI RX buffer. At this point, the SPI interface can receive more data. However, the processor must have retrieved the first data stream before the second data stream reception is complete, otherwise a data overrun will occur and the SPI RX overrun interrupt will be activated, if enabled.

I²C Interface

The VMX51C1020 includes an I²C compatible communication interface that can be configured in Master mode or in Slave mode.

I²C Control Registers

The I2CRXTX SFR register is used to retrieve and transmit data on the I²C interface.

TABLE86: (I2CRXTX) I2C DATA BUFFER - SFR DEH

7	6	5	4	3	2	1	0
I2CRXTX [7:0]							

Bit	Mnemonic	Function
7:0	I2CRXTX[7:0]	I2C Data Receiver / Transmitter buffer

The I2CCONFIG register serves to configure the operation of the VMX51C1020 I²C interface. The following table describes the I2CCONFIG register bits.

TABLE 87: (I2CCONFIG) I2C CONFIGURATION - SFR DAH

7	6	5	4
I2CMASKID	I2CRXOVIE	I2CRXDAVIE	I2CTXEMPIE

3	2	1	0
I2CMANACK	I2CACKMODE	I2CMSTOP	I2CMASTER

Bit	Mnemonic	Function
7	I2CMASKID	This is used to mask the chip ID when you have only two devices. Therefore in a transaction, rather that receiving the chip ID first, you will receive the first packet of data.
6	I2CRXOVIE	I2C Receiver overrun interrupt enable
5	I2CRXDAVIE	I2C Receiver available interrupt enable
4	I2CTXEMPIE	I2C Transmitter empty interrupt enable
3	I2CMANACK	1= Manual acknowledge line goes to 0 0= Manual acknowledge line goes to 1
2	I2CACKMODE	Used only with Master Rx, Master Tx, and Slave Rx. 1= Manual Acknowledge on 0= Manual Acknowledge off
1	I2CMSTOP	I2C Master receiver stops at next acknowledge phase. (read during data phase)
0	I2CMASTER	I2C Master mode enable 1= I2C interface is Master 0= I2C interface is Slave

The I2CIRQSTAT register provides the status of the I²C interface operation and monitors the I²C bus status.

TABLE 88: (I2CIRQSTAT) I2C INTERRUPT STATUS - SFR DDH

7	6	5	4
I2CGOTSTOP	I2CNOACK	I2CSDA	I2CDATACK

3	2	1	0
I2CIDLE	I2CRXOV	I2CRXAV	I2CTXEMP

Bit	Mnemonic	Function
7	I2CSGOTSTOP	This means that the slave has received a stop (this bit is read only). Reset only when the master begins a new transmission.
6	I2CNOACK	Flag that indicates that no acknowledge has been received. Is reset at the start of the next transaction
5	I2CSDA	Value of SDA line.
4	I2CDATACK	Data acknowledge phase.
3	I2CIDLE	Indicates that I2C is idle
2	I2CRXOV	I2C Receiver overrun
1	I2CRXAV	I2C Receiver available
0	I2CTXEMP	I2C Transmitter empty

The I2CCHIPID register holds the VMX51C1020 I²C interface ID as well as the status bit that indicates if the last byte monitored on the I²C interface was destined for the VMX51C1020 or not.

The reset value of this register is 0x42, corresponding to an I²C Chip ID of 0x21. The chip ID value of the VMX51C1020 can be dynamically changed by writing the desired ID into the I2CCHIPID register (see following table).

TABLE 89: (I2CCHIPID) I2C CHIP ID - SFR DCH

7	6	5	4	3	2	1	0
I2CID [6:0]							I2CWID

Bit	Mnemonic	Function
7:1	I2CID[6:0]	The value of this chip's ID
0	I2WID	Read Only and is used only in slave mode. 0:The .ID received corresponds to the I2CID 1: The ID received do not correspond to the I2CID

The I2WID bit is "read only" and used only in Slave mode and is an indicator of whether the transaction is targeted to the VMX1020 device.

If the device ID sent by the Master device corresponds to the I2CID value stored in the I2CCHIPID, the I2WID bit will be cleared to 0 by the I2C module. If the transaction was destined for another I2C slave device, the I2WID bit will be set to 1.

The I2WID value is valid at the moment the device ID transmission from the master device on the I²C bus has completee.

In the case where the I²C RX available interrupt is activated, once the device ID is received, an I²C RX available interrupt will be triggered. The interrupt service routine should then monitor the I2WID bit in order to establish if the transaction is destined for this VMX1020 device.

If the I2WID bit is set to 1, the I²C interrupt service routine can be terminated and there won't be another I²C Rx available interrupt until the next I²C transaction.

If the I2WID bit is cleared, the RX Available interrupt, if enabled, will be triggered for each data byte received.

I²C Clock Speed

The VMX51C1020's I²C communication speed is fully configurable.

Control of the I²C communication speed enabled via the I2CCLKCTRL register. The following formula is used to calculate the I²C clock frequency in Master mode.

$$I^2C\ Clk = \frac{f_{osc}}{[8 \times (I2CCLKCTRL)]}$$

The following table provides examples of I²C clock (on SCL pin) speeds for various setting of the I2CCLKCTRL register when using a 14.75MHz oscillator to drive the VMX51C1020.

I2CCLKCTRL Value	I2C Clock (SCL Value)
01h	920kHz
03h	461KHz
07h	230KHz
13h	92KHz
27h	46KHz
C7h	9.2KHz

When the I²C interface is configured for slave modethe I2CCLKCTRL is not used

TABLE 90: (I2CCLKCTRL) I2C CLOCK CONTROL - SFR DBH

7	6	5	4	3	2	1	0
I2CCLKCTRL [7:0]							

Bit	Mnemonic	Function
7:0	I2CCLKCTRL	I2C Clock speed control

I²C Interface Interrupts

The I²C interface has a dedicated interrupt vector located at address 0x5B. Three flags (see below) share the I²C interrupt vector and can be used to monitor the I²C interface status making it possible to activate the I²C interrupt.

I2CTXEMP:	Is set to 1 when the transmit buffer is empty
I2CRXAV:	Is set to 1 when data byte reception completes.
I2CRXOV:	Is set to 1 if a new byte reception completes before the previous data in the reception buffer is read, resulting in a data collision.

These flags can all trigger the I²C interrupt if their corresponding bit in the I2CCONFIG register is set to one.

In the case where more than one of these flags can activate an I²C interrupt, the interrupt service routine is left to figure out which condition generated the interrupt.

Note that the I2CRXAV, I2CTXEMP and I2CRXOV flags can still be polled if their corresponding interrupt enable flag is cleared. Therefore they can still be used to monitor status.

Master I²C Operation

In Master mode, the VMX51C1020 I²C interface controls the I²C bus transfers. In order to configure the I²C interface as a Master, the I2CMASTER bit of the I2CCONFIG register must be set to one.

Once the I²C interface is configured, sending data to a Slave device connected to the bus is done by writing the data into the I2CRXTX register.

Before sending data to a Slave device, a byte containing the target device's chip ID and Read/Write bit must be sent to it.

A master mode data read is triggered by reading the I2CRXAV (bit 1) of the I2CIRQSTAT register. The data is present on the I2CRXTX register when the I2CRXAV bit is set.

Reading the value of the I2CRXTX register resets the I2CRXAV bit. Once started, the I²C byte read process will continue until the Master generates a STOP condition.

When the I²C interface is configured as a Master, setting the I2CMSTOP bit of the I2CCONFIG register to a 1 will result in the I²C interface generating a STOP condition after the reception of the next byte.

In Master Mode, it's possible to manually control the operation of the acknowledged timing when receiving data. To do this, you must first set the I2CMANACK bit of the I2CCONFIG register to 1. Then, once you have received a byte, you can manually control the acknowledge level by clearing or setting the I2CMANACK bit.

Note: The VMX51C1020 I²C Interface is not compatible with the I²C multi-master mode.

Slave I²C Operation

The VMX51C1020 I²C interface can be configured as a Slave by clearing the I2CMASTER bit of the I2CCONFIG register.

In Slave mode, the VMX51C1020 has no control over the rate or timing of the data exchange that occurs on the I²C bus. Therefore, in Slave mode, it is preferable to manage the transactions using the I²C interrupts.

The I2CMASKID bit, when set, will configure the Slave device to mask the received ID byte and receive the data directly. This is useful when only two devices are present on the I²C bus.

Note: When the VMX51C1020 starts transmitting data in Slave mode, it will continually transmit the value present in the I²C transmit register as long as the Master provides the clock signal or until the Master device generates a STOP condition

Errata:

The VMX1020 I²C Interface has a critical timing issue when the device is configured as a Slave and transmits multiple data bytes. Single byte transmission in slave mode is not effected.

The condition arises if the Master device releases the SDA line at the same time it brings the SCL line low for the Acknowledge phase.

In order for the VMX1020 I²C Slave transmission to work properly for multiple bytes, the Master device MUST release the SDA line AFTER the SCL negative edge.

For this reason it is not possible to have a VMX1020 device configured as an I²C Master and VMX1020 devices configured as I²C Slaves on the same I²C bus. Unless data transmitted from VMX1020 I²C Slaves to the I²C Master is done one byte at a time.

I²C EEPROM Interface Example Program

The following provides an example program using the VMX51C1020 I²C interface for performing read and write operations to an externally connected EEPROM device.

```
#pragma SMALL
#include <vmixreg.h>

// --- Function prototypes
unsigned char eeread(idata unsigned char, idata unsigned char);
void eewrite(idata unsigned char, idata unsigned char, unsigned char);

// - Global variables
idata unsigned char          irqcptr=0x00;

sbit  I2C_TX_EMPTY = USERFLAGS^0;
sbit  I2C_RX_AVAIL = USERFLAGS^1;
sbit  I2C_IS_IDLE = USERFLAGS^3;
sbit   I2C_NO_ACK = USERFLAGS^6;


//-------------------------------------------------------------------------//
//                      MAIN FUNCTION                                      //
//-------------------------------------------------------------------------//
void main (void){

                unsigned char x=0;

                DIGPWREN = 0x13;        //Enable the I2C peripheral

                //*** configure I2C Speed.
                I2CCLKCTRL = 0x013;     //…To about 100KHZ...

                //*** Configure the interrupts
                IEN0 |= 0x81;           //Enable Ext INT0 interrupt + main

    //*** infinite loop waiting for ext IRQ
                while(1){
                };

}// End of main()...

//-------------------------------------------------------------------------//
// EXT INT0 interrupt
//
// When the External interrupt 0 is triggered read and write
// operations are performed on the EEPROM
//-------------------------------------------------------------------------//
void int_ext_0 (void) interrupt 0 {

// Local variables declaration
                idata unsigned char eedata;
                idata unsigned char adrsh =0;
                idata unsigned char adrsl =0;
                idata int adrs =0;

//              IEN0 &= 0x7F;           //disable ext0 interrupt
                                        //(Masked for debugger compatibility)

                //Write irqcptr into the EEPROM at adrs 0x0100
                eewrite( 0x01,0x00,irqcptr);

                irqcptr = irqcptr + 1;  //Increment the Interrupt counter

                //Perform an EEPROM read at address 0x100
                eedata = eeread(0x01, 0x00);

                delay1ms(100);           //Debo delay for the switch on INT0
//              IEN0 = 0x81;            // enable all interrupts + int_0 (Removed
                                        //for debugger compatibility)

}// end of EXT INT 0

//-------------------------------------------------------------------------//
//        INDIVIDUALS FUNCTIONS                                            //
//-------------------------------------------------------------------------//
//-------------------------------------------------------------//
//   EEREAD - EEPROM Random Read  //
//-------------------------------------------------------------//
 unsigned char eeread(idata unsigned char adrsh, idata unsigned char adrsl)
                {
                idata unsigned char x=0;
                idata unsigned char readvalue=0;
```

```
		I2CCONFIG = 0x03;
			//I2C MASTER MODE NO INTERRUPT

		I2CRXTX = 0xA8;
			//SEND 24LC64 ADRS + write COMMAND
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}

		I2CRXTX = adrsh;
			//SEND 24LC64 ADRSH
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}

		I2CRXTX = adrsl;
			//SEND 24LC64 ADRSL
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}
		USERFLAGS = 0x00;

		//wait for I2C interface to be idle
		while(!I2C_IS_IDLE){USERFLAGS = I2CIRQSTAT;}

		I2CCONFIG &= 0xFD;	//set Master Rx Stop, only 1 byte to receive

		I2CCONFIG |= 0x02;

		I2CRXTX = 0xA9;		// Chip ID read

		USERFLAGS = 0x00;
		while(!I2C_RX_AVAIL){USERFLAGS = I2CIRQSTAT;}

		readvalue = I2CRXTX;

		USERFLAGS = 0x00;
		while(!I2C_IS_IDLE){USERFLAGS = I2CIRQSTAT;}
		//Wait for I2C IDLE
		return		readvalue;

		}//End of EEREAD

//-------------------------------------------------------------------//
//  EEWRITE - EEPROM Random WRITE //
//-------------------------------------------------------------------//
void eewrite(idata unsigned char adrsh, idata unsigned char adrsl, unsigned char
eedata)
		{
		idata unsigned char x;
		I2CCONFIG = 0x01;	//I2C MASTER MODE NO INTERRUPT
		I2CRXTX = 0xA8;		//SEND EEPROM ADRS + READ
					//COMMAND
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}

		I2CRXTX = adrsh;	//SEND ADRSH
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}

		I2CRXTX = adrsl;	//SEND ADRSL
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}

		I2CRXTX = eedata;	//SEND 24LC64 DATA and wait
					//for I2C bus IDLE
		USERFLAGS = 0x00;
		while(!I2C_IS_IDLE){USERFLAGS = I2CIRQSTAT;}
		///--Wait Write operation to end

		I2CCONFIG = 0x01;	//I2C Master Mode no Interrupt

		do{
		I2CRXTX = 0xA8;		//Send 24LC64 Adrs +read Command
		USERFLAGS = 0x00;
		while(!I2C_TX_EMPTY){USERFLAGS = I2CIRQSTAT;}
		USERFLAGS = I2CIRQSTAT;
			}while(I2C_NO_ACK);
		delay1ms(5);		//5ms delay for EEPROM write
		}// End of EEPROM Write
```

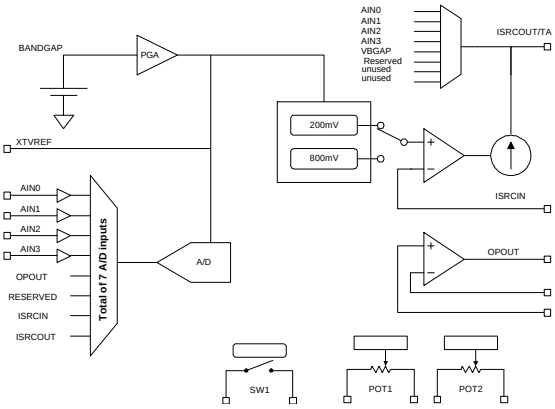
Analog Signal Path

The VMX51C1020 implements a complete single chip acquisition system by integrating the following analog peripherals:

- 12-bit A/D converter having 4 external inputs as well as 3 internal connections to the Operational amplifier and Current source input and output for a ***total of 7 inputs***. The ADC conversion rate is programmable up to 10KHz
- Internal Bandgap reference and PGA
- 1 Programmable current source
- 2 Digital potentiometers
- 1 Digital switch

The following figure provides a block diagram of the VMX51C1020's analog peripherals and their connection.

FIGURE 35: ANALOG SIGNAL PATH OF THE VMX51C1020



The on-chip calibrated bandgap or the external reference provides the basis for all derived on-chip voltages. These signals serve as reference for the ADC and the current source.

Analog Peripheral Power Control

Selection of the internal/ external reference, the multiplexer's current source drive, ADC control, and the respective power downs for these peripherals are controlled via the ANALOGPWREN SFR registers.

Internal Reference and PGA

The VMX51C1020 provides a temperature calibrated internal bandgap reference coupled with a programmable gain amplifier.

The programmable gain amplifier's role is to amplify the bandgap output to 2.7 volts and provide the drive required for the ADC reference input and current source.

Both the bandgap and the PGA are calibrated during production and their associated calibration registers are automatically loaded with the appropriate calibration vectors when the device is reset.

The bandgap and PGA calibration vectors are stored into the BGAPCAL and PGACAL SFR registers when a reset occurs. It is possible for the user program to overwrite the contents of those registers.

TABLE 91: (BGAPCAL) BAND-GAP CALIBRATION VECTOR REGISTER - SFR B3H

7	6	5	4	3	2	1	0
BGAPCAL [7:0]							

Bit	Mnemonic	Function
7:0	BGAPCAL	Band-gap data calibration

TABLE 92: (PGACAL) PGA CALIBRATION VECTOR REGISTER - SFR B4H

7	6	5	4	3	2	1	0
PGACAL [7:0]							

Bit	Mnemonic	Function
7:0	PGACAL	8 MSBs of PGA Calibration Vector (LSBit is on ISRCCAL1)

Using the VMX51C1020 Internal Reference

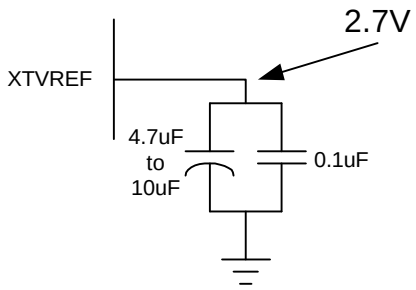
The configuration and setup up of the VMX51C1020's internal reference is done by setting bits 0 and 1 of the ANALOGPWREN register to 1. This powers on the bandgap and the PGA, respectively.

Use of the internal reference requires the addition of two external tank capacitors on the XTVREF pin.

These capacitors consist of one 4.7uF to 10uF Tantalum capacitor in parallel with one 0.1uF Ceramic capacitor.

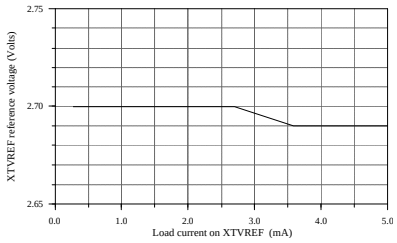
The following shows the connection of the tank capacitors to the XTVREF pin

FIGURE 36: TANK CAPACITORS CONNECTION TO THE XTVREF PIN



The VMX51C1020 internal reference can also be used as an external reference provided that the load on the XTVREF pin is kept to a minimum. The following table shows the typical effect of loading on the XTVREF voltage.

FIGURE 37: TANK CAPACITORS CONNECTION TO THE XTVREF PIN



It is recommended that the external load on the XTVREF pin be less than 1mA.

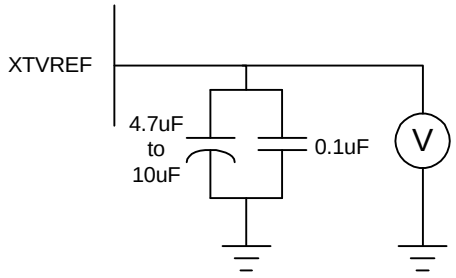
Note: A stabilization delay of more than 1ms should be provided between the activation of the bandgap, the PGA and the first A/D conversion or measurement made on the programmable current source.

Using an External Reference

An external reference can be used to drive the VMX51C1020 ADC and the programmable current source instead of the internal reference.

The external reference voltage source can be set from 0.5 to 3.5 volts and must provide sufficient drive to operate the ADC load.

FIGURE 38: EXTERNAL REFERENCE CONNECTION TO THE XTVREF PIN



Warning:

When an external reference source is applied to the XTVREF pin, it is mandatory not to power-on the PGA. The internal bandgap reference should also be kept de-activated.

Reference Impact on the Programmable Current Source

The Programmable Current Source uses the same reference as the ADC for its operation, therefore, using an external reference will have a direct impact on the current source output.

The 200/800mV current source reference voltage, calibrated at 2.7V will change in a linear fashion according to the voltage present on the XTVREF pin.

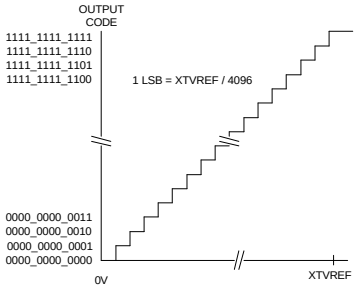
For example, in the case where the reference voltage applied to the XTVREF pin is 3V, the current source reference voltage will be scaled up by a factor of [VXTVREF/2.7V] to 222mV and 889mV respectively.

A/D Converter

The VMX51C1020 includes a feature rich, highly configurable on-chip 12-bit A/D converter.

The A/D conversion data is output as unsigned 12-bit binary, with 1 LSB = Full Scale/4096. The following figure describes the ideal transfer function for the ADC.

FIGURE 39: IDEAL A/D CONVERTER TRANSFER FUNCTION



The A/D converter includes a system that provides the ability to trigger automatic periodic conversions of up to 10kHz without processor intervention.

Once the conversion is complete, the A/D system can activate an interrupt that can wake-up the processor (assuming it has been put into idle mode) or automatically throttle the processor clock to full speed.

The VMX51C1020 A/D converter can also be configured to perform the conversion on one specific channel or on four consecutive channels (in round-robin fashion).

These features make the A/D adaptable for many applications.

The following paragraphs describe the VMX51C1020's A/D converter register features.

ADC Data Registers

The ADC data registers hold the ADC conversion results. The ADCDxLO register(s) hold the 8 Least Significant Bits (LSBs) of the conversion results while the ADCDxHI register(s) hold the 4 Most Significant Bits (MSB) of the conversion results.

TABLE 93: (ADCD0LO) ADC CHANNEL 0 DATA REGISTER, LOW BYTE - SFR A6H

Bit	Mnemonic	Function
7:0	ADCD0LO	ADC channel 0 low

TABLE 94: (ADCD0HI) ADC CHANNEL 0 DATA REGISTER, HIGH BYTE - SFR A7H

Bit	Mnemonic	Function
3:0	ADCD0HI	ADC channel 0 high

TABLE 95: (ADCD1LO) ADC CHANNEL 1 DATA REGISTER, LOW BYTE - SFR A9H

7	6	5	4	3	2	1	0
ADCD1LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD1LO	ADC channel 1 low

TABLE 96: (ADCD1HI) ADC CHANNEL 1 DATA REGISTER, HIGH BYTE - SFR AAH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD1HI [3:0]			

Bit	Mnemonic	Function
3:0	ADCD1HI	ADC channel 1 high

TABLE 97: (ADCD2LO) ADC CHANNEL 2 DATA REGISTER, LOW BYTE - SFR ABH

7	6	5	4	3	2	1	0
ADCD2LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD2LO	ADC channel 2 low

TABLE 98: (ADCD2HI) ADC CHANNEL 2 DATA REGISTER, HIGH BYTE - SFR ACH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD2HI [3:0]			

Bit	Mnemonic	Function
7:4	-	-
3:0	ADCD2HI	ADC channel 2 high

TABLE 99: (ADCD3LO) ADC CHANNEL 3 DATA REGISTER, LOW BYTE - SFR ADH

7	6	5	4	3	2	1	0
ADCD3LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD3LO	ADC channel 3 low

TABLE 100: (ADCD3HI) ADC CHANNEL 3 DATA REGISTER, HIGH BYTE - SFR AEH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD3HI [3:0]			

Bit	Mnemonic	Function
7:4	-	-
3:0	ADCD3HI	ADC channel 3 high

ADC Input Selection

A/D conversions can be performed on a single channel, sequentially on the four lower channels, or sequentially on the four upper channels of the ADC input multiplexer.

An input buffer is present on each of the four external ADC inputs (ADIN0 to AIN3)

These buffers must be enabled before a conversion can take place on the ADC AIN0-

AIN3 inputs. These buffers are enabling by setting the corresponding bits of the lower nibble (AIEN [3:0]) of the INMUXCTRL register to 1.

TABLE 101: (INMUXCTRL) ANALOG INPUT MULTIPLEXER CONTROL REGISTER - SFR B5H

7	6	5	4	3	2	1	0
-	ADCINSEL [2:0]			AINEN [3:0]			

Bit	Mnemonic	Function
7	-	-
6:4	ADCINSEL[2:0]	ADC Input Select 000 - AIN0 001 - AIN1 010 - AIN2 011 - AIN3 100 - OPOUT 101 - VSR 110 - ISRCIN 111 - ISRCOUT
3:0	AINEN[3:0]	Analog Input Enable

The upper four bits of the INMUXCTRL register are used to define the channel on which the conversion will take place when the ADC is set to perform the conversion on one specific channel.

ADC Control Register

The ADCCTRL register is the main register used for control and operation of the ADC.

TABLE 102: (ADCCTRL) ADC CONTROL REGISTER - SFR A2H

7	6	5	4
ADCIRQCLR	XVREFCAP	1	ADCIRQ

3	2	1	0
ADCIE	ONECHAN	CONT	ONESHOT

Bit	Mnemonic	Function
7	ADCIRQCLR	ADC interrupt clear Writing 1 Clears interrupt
6	XVREFCAP	Always keep this bit at 1
5	Reserved = 1	Keep this bit = 1
4	ADCIRQ	Read ADC Interrupt Flag Write 1 generate ADC IRQ
3	ADCIE	ADC interrupt enable
2	ONECHAN	1 = Conversion is performed on one channel Specified ADCINSEL 0 = Conversion is performed on 4 ADC channels
1	CONT	1 = Enable ADC continuous conversion
0	ONESHOT	1 = Force a single conversion on 1 or 4 channels

ADC Continuous/One Shot Conversion

The CONT bit sets the ADC conversion mode. When the CONT bit is set to 1, the ADC will implement continuous conversions at a rate defined by the Conversion Rate register.

When the CONT bit is set to 0, the A/D operates in “One Shot” mode, initiating a conversion when the ONESHOT bit of the ADCCONTRL register is set.

ADC One Channel/ Four Channel Conversion

The VMX51C1020’s ADC includes a feature that renders it possible to perform a conversion on one specific channel or on four consecutive channels.

This feature minimizes the load on the processor when reading more than one ADC input is required.

The ONECHAN bit of the ADCCTRL register controls this feature. When the ONECHAN is set to 1, the conversion will take place on the channel selected by the INMUXCTRL register. Once the conversion is completed, the result will be put into the ADCD0LO and ADCD0HI registers

When the ONECHAN bit is set to 0, the conversion, once triggered, will be done sequentially on four channels and the conversion results will be placed into the ADCDxLO and ADCDxHI registers.

Bit 6 of the INMUXCTRL register controls whether the conversion will take place on the four upper channels of the input multiplexer or the 4 lower channels.

ADC Clock Source Configuration

A/D converter derives its clock source from the main VMX51C1020 clock. The frequency of the ADC clock should be set between 250kHz to 1.25MHz

Configuration of the ADC clock source frequency is done by adjusting the value of the ADCCLKDIV register. The following equation is used to calculate the ADC reference clock value.

ADC Clock Reference Equation:

$$\text{ADC Clk ref} = \frac{f_{OSC}}{4x\ (ADCCDIV + 1)}$$

The ADC conversion requires 111 ADC clock cycles to perform the conversion on one channel.

The following table provides recommended ADCCLKDIV register values versus conversion rate. The numbers given are conservative figures and derived from a 14.74MHz clock

ADCCLKDIV	Maximum Conv. Rate*
0x02	10500 Hz
0x03	8000 Hz
0x05	5000 Hz
0x07	4000 Hz
0x08	3500 Hz
0x09	3200 Hz
0x0B	2500 Hz
0x0D, 0x0E, 0x0F	2200 Hz

* The maximum conversion rate is for the single channel condition. If the conversion is performed on 4 channels, divide the maximum conversion rate by 4. For example to perform the conversion at 2.5KHz on four channels, the ADCCLKDIV register should be set to 0x02 (4x 2500Hz =10KHz)

TABLE 103: (ADCCLKDIV) ADC CLOCK DIVISION CONTROL REGISTER - SFR 95H

7	6	5	4	3	2	1	0
ADCCLKDIV [7:0]							

Bit	Mnemonic	Function
7:0	ADCCLKDIV[7:0]	ADC clock divider

ADC Conversion Rate Configuration

The VMX51C1020's ADC conversion rate, when configured in continuous mode is defined by the 24-bit A/D Conversion Rate register that serves as the time base for triggering the ADC conversion process.

The following equation is used to calculate the value of the conversion rate.

Conversion Rate Equation:

$$\text{Conversion rate registers value (24-bit)} = \frac{f_{OSC}}{Conv\_Rate}$$

The conversion rate register is accessible using three SFR registers as follows:

TABLE 104: (ADCCONVRLOW) ADC CONVERSION RATE REGISTER LOW BYTE - SFR A3H

Bit	Mnemonic	Function
7:0	ADCCONVRLOW	Conversion rate low byte

TABLE 105: (ADCCONVRMED) ADC CONVERSION RATE REGISTER MED BYTE - SFR A4H

Bit	Mnemonic	Function
7:0	ADCCONVRMED	Conversion rate medium byte

TABLE 106: (ADCCONVRHIGH) ADC CONVERSION RATE REGISTER HIGH BYTE - SFR A5H

Bit	Mnemonic	Function
7:0	ADCCONVRHIGH	Conversion rate high byte

The following table provides examples of typical values versus conversion rate.

Conversion Rate	**ADC conv. rate register value. Fosc= 14.74MHz**
1Hz	E10000h
10Hz	168000h
100Hz	024000h
1kHz	003999h
2.5kHz	00170Ah
5kHz	000B85h
8kHz	000733h
10kHz	0005C2h

ADC Status Register

The ADC shares interrupt vector 0x6B with the Interrupt on Port 1 Change and the Compare and Capture Unit 3. To enable the ADC interrupt, the ADCIE bit of the ADCCTRL register must be set. Before or at the same time this bit is set, the ADCIRQCLR and the ADCIRQ bits must be cleared. The ADCPCIE bit of the IEN1 register must also be set, as well as the EA bit of the IEN0 register.

Once the ADC interrupt occurs, ADC Interrupt must be cleared by writing a '1' into the ADCINTCLR bit of the ADCCTRL register. The ADCIF flag in the IRCON register must also be cleared.

A/D Converter Example

The following provides example code for the A/D converter. The first section of the code covers interrupt setup/module configuration whereas the second section is the interrupt function itself.

Sample C code to setup the A/D converter:

```
//-------------------------------------------------------------------//
//                        MAIN FUNCTION
//-------------------------------------------------------------------//

(…)
at 0x0100 void main (void) {

//*** Initialize the Analog Peripherals ***

ANALOGPWREN = 0x07;          //Enable the following analog
                             //peripherals: ISRC, ADC, PGA,
                             // BGAP.  TA = OFF (mandatory)

//Configure the ADC and Start it
ADCCLKDIV=0x0F;              //SET ADC CLOCK SOURCE
ADCCONVRLOW =0x00;           //CONFIGURE CONVERSION RATE
ADCCONVRMED=0x40;            //= 100Hz @ 14.74 MHz
ADCCONVRHIGH =0x02;

INMUXCTRL=0x0F;              //Enable All ADC External inputs
                             //buffers and select ADCI0
ADCCTRL=0xEA;                //Configure the ADC as follow:
                             //bit 7: =1 ADCIRQ Clear
                             //Bit 6: =1 XVREFCAP (always)
                             //Bit 5: =1 (always)
                             //Bit 4: =0 = ADCIRQ (don't care)
                             //Bit 3: =1 = ADC IRQ enable
                             //Bit 2: =0 conversion on 4
                             //channels
                             //Bit 1: =1 Continuous conversion
                             //Bit 0: =0 No single shot mode

//*** Configure the interrupts
IEN0 |= 0x80;                //enable main interrupt
IEN1 |= 0x020;               //Enable ADC Interrupt
while(1);                    //Infinite loop waiting ADC interrupts
}// End of main()...

//-------------------------------------------------------------------//
//                    ADC INTERRUPT ROUTINE
//-------------------------------------------------------------------//
void int_adc (void) interrupt 13 {
idata int value = 0;

IEN0 &= 0x7F;                //disable ext0 interrupts
ADCCTRL |=0x80;              //Clear ADC interrupt

// Read ADC channel 0
value = ADCD0HI;
value = valeur*256;
value = valeur + ADCD0LO;
(…)
// Read ADC channel 3
value = ADCD3HI;
value = valeur*256;
value = valeur + ADCD3LO;
(…)
IRCON &= 0xDF;               //Clear adc irq flag
ADCCTRL |=0xFA;              //prepare adc for next acquisition
IEN0 |= 0x80;                // enable all interrupts

}// End of ADC IRQ

(…)
```

Warning:

When using the ADC, make sure the output multiplexer controlled by the TAEN bit of the ANALOGPWREN register (92h) is powered down at all times, otherwise, the signal present on the ISRCOUT can be routed back to the selected ADC input, causing conversion errors.

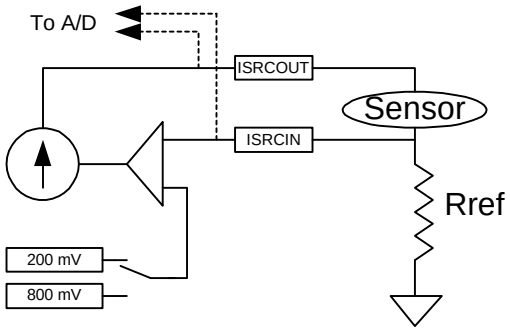
Programmable Current Source

The VMX51C1020 includes a programmable current source used to drive external devices such as resistive sensors connected between the ISRCOUT and ISRCIN pins

To ensure current output stability, the current source provides a feedback input, ISRCIN. The feedback is voltage controlled and can be dynamically set to either 200mV or 800mV. Placing a resistor between the ISRC pin and the ground defines the output current of the current source.

The VMX51C1020 current Source can drive currents up to 500µA when the reference is set to 800mV.

FIGURE 40: PROGRAMMABLE CURRENT SOURCE TO EXCITE SENSOR



As shown above, a resistive device (sensor) must be connected between the ISRCOUT and the ISRCIN.

In order to perform A/D conversion of the voltage present at the terminal of the current source, there is an internal link between each of the ISRCOUT and ISRCIN pins as well as the Input multiplexer of the A/D converter.

TABLE 107: (ISRCCAL1) CURRENT SOURCE CALIBRATION VECTOR FOR 200MV FEEDBACK VALUE - SFR BCH

7	6	5	4	3	2	1	0
PGACAL0	ISRCCAL1 [6:0]						

Bit	Mnemonic	Function
7	PGACAL0	Bit 0 of PGACAL
6:0	ISRCCAL1[6:0]	Calibration Value for ISRC feedback of 200mV

TABLE 108: (ISRCCAL2) CURRENT SOURCE CALIBRATION VECTOR FOR 800MV FEEDBACK VALUE - SFR BDH

7	6	5	4	3	2	1	0
-	ISRCCAL2 [6:0]						

Bit	Mnemonic	Function
7	-	-
6:0	ISRCCAL2[6:0]	Calibration Value for ISRC feedback of 800mV

Current Source Setup Example

The following provides setup examples for the current source.

Enabling the Current Source using the 200mV reference:

```
MOV     ANALOGPWREN,#00110011B

        ;Enable Analog peripherals
        ;Bit 7: OPAMPEN = 0 Op-Amp OFF
        ;Bit 6: DIGPOTEN= 0 Dig Pot OFF
        ;Bit 5: ISRCSEL = 1 ISRC 800mV
        ;Bit 4: ISRCEN  = 1 ISRC ON
        ;Bit 3: TAEN    = 0 TA output OFF
        ;Bit 2: ADCEN   = 0 ADC OFF
        ;Bit 1: PGAEN = 1 PGA ON
        ;Bit 0: BGAPEN  = 1 BandGap ON
```

Enabling the Current Source using the 200mV reference:

```
;MOV     ANALOGPWREN,#00010011B

        ;Enable Analog peripherals
        ;Bit 7: OPAMPEN = 0 Op-Amp OFF
        ;Bit 6: DIGPOTEN= 0 Dig Pot OFF
        ;Bit 5: ISRCSEL = 0 ISRC 200mV
        ;Bit 4: ISRCEN  = 1 ISRC ON
        ;Bit 3: TAEN    = 0 TA output OFF
        ;Bit 2: ADCEN   = 0 ADC OFF
        ;Bit 1: PGAEN = 1 PGA ON
        ;Bit 0: BGAPEN  = 1 BandGap ON
```

Digital Potentiometers

The VMX51C1020 has two digital potentiometers that are controlled by DIGPOTx registers (DIGPOT1, DIGPOT2) that can be used in applications such as:

- Gain control
- Offset adjustment
- A/D input attenuation
- Digitally controlled filter

FIGURE 41: DIGITAL POTENTIOMETER FUNCTIONAL DIAGRAM

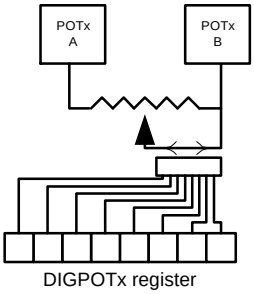


TABLE 109: (DIGPOT1) DIG. POTENTIOMETER 1 CONTROL REGISTER - SFR BAH

7	6	5	4	3	2	1	0
DIGPOT1 [7:0]							

Bit	Mnemonic	Function
7-0	DIGPOT1	Potentiometer 1 Value

TABLE 110: (DIGPOT2) DIG. POTENTIOMETER 2 CONTROL REGISTER - SFR BBH

7	6	5	4	3	2	1	0
DIGPOT2 [7:0]							

Bit	Mnemonic	Function
7-0	DIGPOT2	Potentiometer 2 Value

The digital potentiometers are floating devices, meaning that there are no restrictions on the voltage present on their terminals as long as they are kept within the nominal operating range of the VMX51C1020.

The current flow through the potentiometers should be limited to 5mA max.

The digital potentiometer maximum nominal resistance is 30k +/- 2Kohms from device to device. On a given device the two digital potentiometer values usually match within 1%.

Before using the digital potentiometers, they must first be enabled by setting bit 6 of the ANALOGPWREN register (92h) to 1. The potentiometer value is governed by the following equation.

$$R_{potentiometer\ *} = \frac{[\ 256 - DIGPOTx[7:0]\ ]}{256} \times 30k$$

*Potentiometer value

Digital Potentiometer Setup Example

Only two instructions are required to enable and configure the digital Potentiometers of the VMX51C1020:

```
MOV     ANALOGPWREN,#01000000B
MOV     DIGPOT1,#0C0h       ;SET POT1 to 25% of Max Pot value
MOV     DIGPOT2,#040h       ;SET POT2 to 75% of Max Pot value
```

Operational Amplifier

The VMX51C1020 is equipped with an operational amplifier. This op-amp can be used for a wide array of analog applications such as:

- Gain control
- Offset Control
- Reference buffering
- Integrator
- Other standard op amp applications

The op-amp on the VMX51C1020 has an open-loop gain of 100dB; a unity gain bandwidth of 5MHz and it is able to drive a 1kO and 40pf load. The slew rate of the Op-Amp is 7V/µs and the output voltage can swing between 25mV and 4.975 Volts (10kO load).

To activate the Operational Amplifier, the OPAMPEN bit (bit 7) of the ANALOGPWREN register (SFR 92h) must be set to 1.

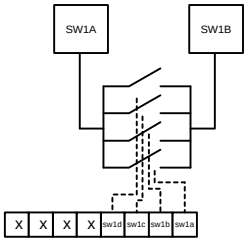
Warning:

If the VMX51C1020 Op-Amp inputs are left floating, it should be kept in power down to prevent risk of oscillation.

Digitally Controlled Switches

The VMX51C1020 include a digital switch composed of 4 sub-switches connected in parallel. These sub-switches can be individually controlled by writing to the SFR register at B7h.

FIGURE 42: SWITCH FUNCTIONAL DIAGRAM



SWITCHCTRL register

The switch "ON" resistance is between 50 and 100 Ohms depending on the number of sub-switches being used. If, for example, one sub-switch is closed, the switch resistance will be about 100 Ohms, and if all 4 switches are closed, the switch resistance will go down to about 50 Ohms.

TABLE 111: (SWITCHCTRL) USER SWITCHES CONTROL REGISTERS - SFR B7H

7	6	5	4	3	2	1	0
Not Used but implemented				SWTCH1 [3:0]			

Bit	Mnemonic	Function
7:4	User Flags	Not used but implemented bits Can be used as general purpose storage
3:0	SWITCH1[3:0]	Switch 1 control (composed of 4 individual switches each bit controlled)

The upper 4 bits of the SWITCHCTRL register can be used as general purpose flags.

Analog Output Multiplexer

The VMX51C1020's analog output multiplexer is used for production test purposes and provides access to internal test points of the analog signal path.. It can however, be used in applications, but due to its high intrinsic impedance, care must be taken with respect to loading.

The analog output multiplexer shares its output with the current source output and therefore must be disabled when the current source or the ADC is used.

Inversely, when the analog output multiplexer is used, the current source must be powered down.

The following table summarizes the analog output multiplexer select line settings.

TABLE 112: (OUTMUXCTRL) ANALOG OUTPUT MULTIPLEXER CONTROL REGISTER - SFR B6H

7	6	5	4	3	2	1	0
-	-	-	-	-	TAOUTSEL [2:0]		

Bit	Mnemonic	Function
7:3	Unused	Unused
2:0	TAOUTSEL[2:0]	Signal output on TA 000 – AIN0 001 – AIN1 010 – AIN2 011 – AIN3 100 – VBGAP 101 – reserved 110 – unused 111 – unused

VMX51C1020 Interrupts

The VMX51C1020 is a highly integrated device incorporating a vast number of peripherals for which a comprehensive set of 29 interrupt sources sharing 12 interrupt vectors is available. Most of the VMX51C1020 peripherals can generate an interrupt, providing feedback to the MCU core that an event has occurred or a task has been completed.

The following features are key VMX51C1020 interrupt features.

- Each digital peripheral on the VMX51C1020 has an interrupt channel.
- The SPI, UARTs and I²C all have event specific flag bits.
- When the processor is in IDLE mode, an interrupt may be used to wake it up.
- The processor can run at full speed during interrupt routines.

The following table summarizes the interrupt sources, natural priority and the associated interrupt vector addresses of the VMX51C1020.

TABLE 113: INTERRUPT SOURCES AND NATURAL PRIORITY

Interrupt	Interrupt Vector
Reserved	0E43h
INT0	0003h
UART1	0083h
TIMER 0	000Bh
SPI Tx	004Bh
INT1	0013h
SPI RX & SPI RX OVERRUN / COMPINT0	0053h
TIMER 1	001Bh
I2C (Tx, Rx, Rx Overrun) / COMPINT1	005Bh
UART0	0023h
MULT/ACCU 32bit Overflow / COMPINT2	0063h
TIMER 2: T2 Overflow, T2EX	002Bh
ADC and interrupt on Port 1 change (8 int.) / COMPINT3	006Bh

It is also possible to program the interrupts to wake-up the processor from an IDLE condition or force its clock to throttle up to full speed when an interrupt condition occurs.

Interrupt Enable Registers

The following tables describe the interrupt enable registers their associated bit functions:

TABLE 114: (IEN0) INTERRUPT ENABLE REGISTER 0 - SFR A8H

7	6	5	4
EA	WDT	T2IE	S0IE

3	2	1	0
T1IE	INT1IE	T0IE	INT0IE

Bit	Mnemonic	Function
7	EA	General Interrupt control 0 = Disable all Enabled interrupts 1 = Authorize all Enabled interrupts
6	WDT	Watchdog timer refresh flag. This bit is used to initiate a refresh of the watchdog timer. In order to prevent an unintentional reset, the watchdog timer the user must set this bit directly before SWDT.
5	T2IE	Timer 2 Overflow / external Reload interrupt 0 = Disable 1 = Enable
4	S0IE	Uart0 interrupt. 0 = Disable 1 = Enable
3	T1IE	Timer 1 overflow interrupt 0 = Disable 1 = Enable
2	INT1IE	External Interrupt 1 0 = Disable 1 = Enable
1	T0IE	Timer 0 overflow interrupt 0 = Disable 1 = Enable
0	INT0IE	External Interrupt 0 0 = Disable 1 = Enable

TABLE 115: (IEN1) INTERRUPT ENABLE 1 REGISTER -SFR E8H

7	6	5	4
T2EXIE	SWDT	ADCPCIE	MACOVIE

3	2	1	0
I2CIE	SPIRXOVIE	SPITEIE	reserved

Bit	Mnemonic	Function
7	T2EXIE	T2EX interrupt Enable 0 = Disable 1 = Enable
6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset.
5	ADCPCIE	ADC and Port change interrupt 0 = Disable 1 = Enable
4	MACOVIE	MULT/ACCU Overflow 32 bits interrupt 0 = Disable 1 = Enable
3	I2CIE	I2C Interrupt 0 = Disable 1 = Enable
2	SPIRXOVIE	SPI Rx avail + Overrun 0 = Disable 1 = Enable
1	SPITEIE	SPI Tx Empty interrupt 0 = Disable 1 = Enable
0	reserved	

TABLE 116: (IEN2) INTERRUPT ENABLE 2 REGISTER - SFR 9AH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	S1IE

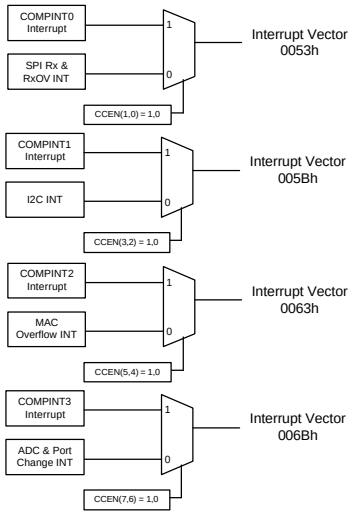
Bit	Mnemonic	Function
7-1	-	-
0	S1IE	UART 1 Interrupt 0 = Disable UART 1 Interrupt 1 = Enable UART 1 Interrupt

Timer2 Compare Mode Impact on Interrupts

The SPI RX (and RXOV), I^2C, MULT/ACCU and ADC Interrupts are shared with the four Timer2 Compare and Capture Unit interrupts.

When the Compare and Capture Units of Timer2 are configured in Compare Mode via CCEN register, the Compare and Capture unit takes control of one interrupt vector as shown below.

FIGURE 43: COMPARE CAPTURE INTERRUPT STRUCUTRE



The impact of this is that the corresponding peripheral interrupt, if enabled, will be blocked. The output signal from the comparison module will be routed to the Interrupt system and the control lines will be dedicated to the Compare and Capture unit.

This interrupt control “take over” is specific to each individual Compare and Capture unit. For example if Compare and Capture Unit number 2 is configured to generate a PWM signal on P1.2, the MULT/ACCU overflow interrupt, if enabled, will be dedicated to the Compare and Capture Unit number 2 and the SPI, I^2C and ADC interrupts won’t be affected.

Interrupt Status Flags

The IRCON register is used to identify the source of an interrupt. Before exitingthe interrupt service routine, the IRCON register bit that corresponds with the serviced interrupt should be cleared.

TABLE 117: (IRCON) INTERRUPT REQUEST CONTROL REGISTER - SFR 91H

7	6	5	4
T2EXIF	T2IF	ADCIF	MACIF

3	2	1	0
I2CIF	SPIRXIF	SPITXIF	Reserved

Bit	Mnemonic	Function
7	T2EXIF	Timer 2 external reload flag This bit informs the user whether an interrupt has been generated from T2EX, if the T2EXIE is enabled.
6	T2IF	Timer 2 interrupt flag
5	ADCIF / COMPINT3	A/D converter interrupt request flag/ port 0 change. / COMPINT3
4	MACIF / COMPINT2	MULT/ACCU unit interrupt request flag / COMPINT2
3	I2CIF / COMPINT1	I^2C interrupt request flag / COMPINT1
2	SPIRXIF / COMPINT0	RX available flag SPI + RX Overrun / / COMPINT0
1	SPITXIF	TX empty flag SPI
0	Reserved	Reserved

Interrupt Priority Register

All of the VMX51C1020's interrupt sources are combined into groups with four levels of priority.

These groups can be programmed individually to one of the four priority levels: from Level0 to Level3 with Level3 being the highest priority.

The IP0 and IP1 registers serve to define the specific priority of each of the interrupt groups. By default, when the IP0 and IP1 registers are at reset state 00h, the natural priority order of the interrupts shown previously are in force.

TABLE 118: (IP0) INTERRUPT PRIORITY REGISTER 0 - SFR B8H

7	6	5	4	3	2	1	0
UF8	WDTSTAT	IP0 [5:0]					

Bit	Mnemonic	Function		
7	UF8	User Flag bit		
6	WDTSTAT	Watchdog timer status flag. Set to 1 by hardware when the watchdog timer overflows. Must be cleared manually		
5	IP0.5	Timer 2	Port1 Change	ADC
4	IP0.4	UART0	-	MULT/ACCU
3	IP0.3	Timer 1	-	I2C
2	IP0.2	External INT1	-	SPI RX available
1	IP0.1	Timer 0 Interrupt	-	SPI TX Empty
0	IP0.0	External INT0	UART1	External INT 0

Table 119: (IP1) Interrupt Priority Register 1 - SFR B9h

7	6	5	4	3	2	1	0
-	-	IP1 [5:0]					

Bit	Mnemonic	Function		
7	-	-		
6	-	-		
5	IP1.5	Timer 2	Port1 Change	ADC
4	IP1.4	UART0	-	MULT/ACCU
3	IP1.3	Timer 1	-	I2C
2	IP1.2	External INT1	-	SPI RX available
1	IP1.1	Timer 0 Interrupt	-	SPI TX Empty
0	IP1.0	External INT0	UART1	External INT 0

Configuring the IP0 and IP1 registers makes it possible to change the priority order of the peripheral interrupts in order give higher priority to a given interrupt that belongs to a given group.

TABLE 120: INTERRUPT GROUPS

Bit	**Interrupt Group**		
IP1.5, IP0.5	Timer 2	Port1 Change	ADC
IP1.4, IP0.4	UART0	-	MULT/ACCU
IP1.3, IP0.3	Timer 1	-	I2C
IP1.2, IP0.2	External INT1	-	SPI RX available
IP1.1, IP0.1	Timer 0 Interrupt	-	SPI TX Empty
IP1.0, IP0.0	External INT0	UART1	External INT 0

The respective values of the IP1.x and IP0.x bits define the priority level of the interrupt group vs. the other interrupt groups as follows.

TABLE 121: INTERRUPT PRIORITY LEVEL

IP1.x	IP0.x	Priority Level
0	0	Level 0 (Low)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (High)

The WDTSTAT bit of the IP0 register is the Watchdog status flag and is set to 1 by the hardware whenever a Watchdog Timer overflow occurs. This bit must be cleared manually.

Finally, bit 7 of the IP0 register can be used as a general purpose user flag.

Setting up INT0 and INT1 Interrupts

The IT0 and IT1 bits of the TCON register define whether external interrupts 0 and 1 will be edge or level triggered.

When an interrupt condition occurs on INT0 or INT1, the associated interrupt flag IE0 or IE1 will be set. The interrupt flag is automatically cleared when the interrupt is serviced.

TABLE 122: (TCON) TIMER 0, TIMER 1 TIMER/COUNTER CONTROL - SFR 88H

7	6	5	4
TF1	TR1	TF0	TR0

3	2	1	0
IE1	IT1	IE0	IT0

Bit	Mnemonic	Function
7	TF1	Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
6	TR1	Timer 1 Run control bit. If cleared Timer 1 stops.
5	TF0	Timer 0 overflows flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
4	TR0	Timer 0 Run control bit. If cleared timer 0 stops.
3	IE1	Interrupt 1 edge flag. Set by hardware when falling edge on external INT1 is observed. Cleared when interrupt is processed.
2	IT1	Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
1	IE0	Interrupt 0 edge flag. Set by hardware when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.
0	IT0	Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

INT0 example

The following provides example code for interrupt setup and module configuration.

```
//-------------------------------------------------------------------------
// Sample C code to setup INT0
//-------------------------------------------------------------------------
#pragma TINY
#include <vmixreg.h>

at 0x0100 void main (void) {

// INT0 Config

        TCON |= 0x01;   //Interrupt on INT0 will be caused by a High->Low
                        //edge on the pin
// Enable INT0 interrupts
        IEN0 |= 0x80;           // Enable all interrupts
        IEN0 |= 0x01;           // Enable interrupt INT0

// Wait for INT0…
        do
        {
        }while(1);      //Wait for INT0 interrupts

}//end of main function

//-------------------------------------------------------------------------
// Interrupt Function

void int_ext_0 (void) interrupt 0
{
IEN0 &= 0x7F;                   // Disable all interrupts

/* Put the Interrupt code here*/

IEN0 |= 0x80;                   // Enable all interrupts
}
//-------------------------------------------------------------------------
```

INT1 example

The following code example shows the INT1 interrupt setup and module configuration:

```
//-------------------------------------------------------------------------
// Sample C code to setup INT1
//-------------------------------------------------------------------------
#pragma TINY
#include <vmixreg.h>

at 0x0100 void main (void) {

// INT1 Config

        TCON |= 0x04;   //Interrupt on INT1 will be caused by a High->Low
                        //edge on the pin

// Enable INT1 interrupts

        IEN0 |= 0x80;                   // Enable all interrupts
        IEN0 |= 0x04;                   // Enable interrupt INT1

// Wait for INT1…
        do
        {
        }while(1);      //Wait for INT1 interrupts


// Interrupt function

void int_ext_1 (void) interrupt 2
{
IEN0 &= 0x7F;                   // Disable all interrupts

/* Put the Interrupt code here*/

IEN0 |= 0x80;                   // Enable all interrupts
}
```

UART0 and UART1 Interrupt Example

The following program examples demonstrate how to initialization the UART0 and UART1 interrupts.

```
//-------------------------------------------------------------------------
// Sample C code for UART0 and UART1 interrupt example
//-------------------------------------------------------------------------
#pragma TINY
#include <vmixreg.h>

// --- function prototypes
void txmit0( unsigned char charact);
void txmit1( unsigned char charact);
void uart1Config(void);
void uart0ws0relcfg(void);

// - Constants definition
sbit UART_TX_EMPTY = USERFLAGS^1;

//-------------------------------------------------------------------------
//                      MAIN FUNCTION
//-------------------------------------------------------------------------
 at 0x0100 void main (void) {

        // Enable and configure the UART0  & UART1
        uart0ws0relcfg();       //Configure UART0
        uart1Config();          //Configure UART1


//*** Configure the interrupts
        IEN0 |= 0x91;           //Enable UART0 Int + enable all int
        IEN2 |= 0x01;           //Enable UART1 Interrupt
        do
                {
                }while(1);      //Wait for UARTs interrupts
        // End of main()...

//-------------------------------------------------------------------------
//              INTERRUPT ROUTINES
//-------------------------------------------------------------------------

//-------------------------------------------------------------------------
// UART0 interrupt
//
// Retrieve character received in S0BUF and transmit it
// back on UART0
// //-----------------------------------------------------------------------
void int_uart0 (void) interrupt 4 {

        IEN0 &= 0x7F;                   //disable All interrupts

//--- The only UART0 interrupt source is Rx...
        txmit0(S0BUF);                  // Return the character
                                        //received on UART0

        S0CON = S0CON & 0xFC;           //clear R0I & T0I bits
        IEN0 |= 0x80;                   // enable all interrupts
        }// end of UART0 interrupt

//-------------------------------------------------------------------------
// UART1 interrupt
//
// Retrieve character received in S1BUF and transmit it
// back on UART1
// //-----------------------------------------------------------------------
void int_uart1 (void) interrupt 16 {

        IEN0 &= 0x7F;                   //disable All interrupts

//--- The only UART1 interrupt source is Rx...
        txmit1(S1BUF);                  // Return the character
                                        // received on UART1
        S1CON = S1CON & 0xFC;           // clear both R1I & T1I bits
        IEN0 |= 0x80;                   // enable all interrupts

}// end of UART1 interrupt
```

Note: See UART0 / UART1 section for configuration examples and TXMITx functions

Interrupt on P1 Change

The VMX51C1020 includes an Interrupt on Port change feature, which is available on the Port1 pins of the VMX51C1020.

This feature is like having eight extra external interrupt inputs sharing the ADC interrupt vector at address 006Bh and can be very useful for applications such as switches, keypads, etc.

To activate this interrupt, the bits corresponding to the pins being monitored must be set in the PORTIRQEN register. The ADCPCIE bit in the IEN1 register must be set as well as the EA bit of the IEN0 register.

TABLE 123: (PORTIRQEN) PORT CHANGE IRQ CONFIGURATION - SFR 9FH

7	6	5	4
P17IEN	P16IEN	P15IEN	P4IEN

3	2	1	0
P13IEN	P12IEN	P11IEN	P10IEN

Bit	Mnemonic	Function
7	P17IEN	Port 1.7 IRQ on change enable 0 = Disable 1 = Enable
6	P16IEN	Port 1.6 IRQ on change enable 0 = Disable 1 = Enable
5	P15IEN	Port 1.5 IRQ on change enable 0 = Disable 1 = Enable
4	P14IEN	Port 1.4 IRQ on change enable 0 = Disable 1 = Enable
3	P13IEN	Port 1.3 IRQ on change enable 0 = Disable 1 = Enable
2	P12IEN	Port 1.2 IRQ on change enable 0 = Disable 1 = Enable
1	P11IEN	Port 1.1 IRQ on change enable 0 = Disable 1 = Enable
0	P10IEN	Port 1.0 IRQ on change enable 0 = Disable 1 = Enable

The PORTIRQSTAT register monitors the occurrence of the Interrupt on port change. This register serves to define which P1 pin has changed when an interrupt occurs.

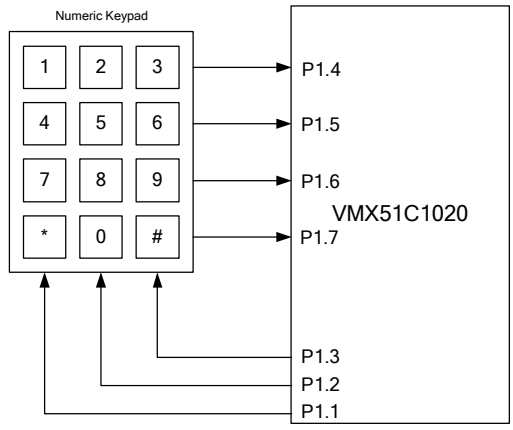
TABLE 124: (PORTIRQSTAT) PORT CHANGE IRQ STATUS - SFR A1H

7	6	5	4
P17ISTAT	P16ISTAT	P15ISTAT	P14ISTAT

3	2	1	0
P13ISTAT	P12ISTAT	P11ISTAT	P10ISTAT

Bit	Mnemonic	Function
7	P17ISTAT	Port 1.7 changed 0 = No 1 = Yes
6	P16ISTAT	Port 1.6 changed 0 = No 1 = Yes
5	P15ISTAT	Port 1.5 changed 0 = No 1 = Yes
4	P14ISTAT	Port 1.4 changed 0 = No 1 = Yes
3	P13ISTAT	Port 1.3 changed 0 = No 1 = Yes
2	P12ISTAT	Port 1.2 changed 0 = No 1 = Yes
1	P11ISTAT	Port 1.1 changed 0 = No 1 = Yes
0	P10ISTAT	Port 1.0 changed 0 = No 1 = Yes

FIGURE 44: APPLICATION EXAMPLE OF PORT CHANGE INTERRUPT



The following provides an assembler example for configuration of the Interrupt on Port1 pin change and how it is shared with the ADC interrupt.

```
include VMIXreg.INC
;*** INTERRUPT VECTORS JUMP TABLE  *
ORG 0000H               ;BOOT ORIGIN VECTOR
            LJMP        START
ORG 006BH               ;INT ADC and P1 change interrupt
            LJMP        INT_ADC_P1

;*** MAIN PROGRAM
ORG    0100h

START:      MOV         DIGPWREN,#01H       ;ENABLE TIMER 2
            MOV         P2PINCFG,#0FFH

;*** Initialise Port change interrupt on P1.0 - P1.7
            MOV         PORTIRQSTAT,#00H
            MOV         PORTIRQEN,#11111111B

;*** Initialise the ADC, BGAP, PGA Operation
            MOV         ANALOGPWREN,#07h

;Select CH0 as ADC input + Enable input buffer + Adc clk
            MOV         INMUXCTRL,#0Fh
            MOV         ADCCLKDIV,#0Fh
            MOV         ADCCONVRLOW,#000h

;*** configure ADC Conversion Rate
            MOV         ADCCONVRMED,#080h
            MOV         ADCCONVRHIGH,#016h
            MOV         ADCCTRL,#11111010b

;***Activate All interrupts + (serial port for debugger support)
            MOV         IEN0,#090H
;*** Enable ADC interrupt
            MOV         IEN1,#020H

;***Wait IRQ…
WAITIRQ:    LJMP        WAITIRQ

ORG    0200h
;*************************************************************************
;* IRQ ROUTINE:       IRQADC + P1Change
;*************************************************************************
INT_ADC_P1:
            ;MOV         IEN0,#00h    ;DISABLE ALL INTERRUPT

;***Check if IRQ was caused by Port Change
;***If PORTIRQSTAT = 00h -> IRQ comes from ADC
            MOV         A,PORTIRQSTAT
            JZ          CASE_ADC

;*** If interrupt was caused by Port 1, change
CASE_P0CHG:
            MOV         PORTIRQSTAT,#00H
;*** Perform other instructions related to Port1 change IRQ
            ;(...)

;*** Jump to Interrupt end
            AJMP        ENDADCP1INT

;*** If interrupt was caused by ADC
CASE_ADC:
            ANL         ADCCTRL,#11110011b
;***Reset ADC interrupt flags & Reset ADC for next acquisition
            ORL         ADCCTRL,#080h
            ORL         ADCCTRL,#11111010b
;*** Perform other instructions related to Port1 change IRQ
;(...)

;** End of ADC and Port 1 Change interrupt
ENDADCP0INT:
            ANL         IRCON,#11011111b

;***Enable All interrupts before exiting
            ; MOV       IEN0,#080H
            RETI
END
```

The Clock Control Circuit

The VMX51C1020's clock control circuit allows dynamic adjustment of the clock from which the processor and the peripherals derive their clock source. This allows reduction of overall power consumption by modulating the operating frequency according to processing requirements or peripheral use.

A typical application for this can be portable acquisition systems in which significant power savings can be achieved by lowering the operating frequency between A/D conversions and automatically throttling it back to full speed when an A/D interrupt is generated. Note that A/D converter operation is not affected by the Clock Control Unit.

The clock control circuit allows adjusting the System clock from [Fosc/1] (full speed) down to [Fosc/512]. The clock division control is done via the CLKDIVCTRL register located at address 94h of the SFR register area.

TABLE 125: (CLKDIVCTRL) CLOCK DIVISION CONTROL REGISTER -SFR 94H

7	6	5	4
SOFTRST	-	-	IRQNORMSPD

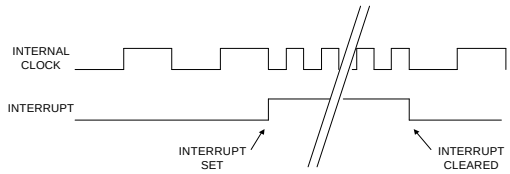
3	2	1	0
MCKDIV [3:0]			

Bit	Mnemonic	Function
7	SOFTRST	Writing 1 into this bit location provokes a reset. Read as a 0
6:5	-	-
4	IRQNORMSPD	0 = Full Speed in IRQ 1 = Selected speed during IRQs
3:0	MCKDIV [3:0]	Master Clock Divisor 0000 – Sys CLK 0001 = SYS /2 0010 = SYS /4 0011 = SYS /8 0100 = SYS /16 0101 = SYS /32 0110 = SYS /64 0111 = SYS /128 1000 = SYS /256 1001 = SYS /512 (…) 1111 = SYS /512

The value written into the lower nibble of the CLKDIVCTRL register, MCKDIV[3:0], defines the clock division ratio.

When the IRQNORMSPD bit is cleared, the VMX51C1020 will run at the maximum operating speed when an interrupt occurs (see following figure).

FIGURE 45: CLOCK TIMING WHEN AN INTERRUPT OCCURS



Once the interrupt is cleared, the VMX51C1020 returns to the selected operating speed as defined by the MCKDIV [3:0] bits of the CLKDIVCTRL register.

When the IRQNORMSPD bit is set, the VMX51C1020 will continue to operate at the selected speed as defined by the MCKDIV [3:0] bits of the CLKDIVCTRL register.

Note: With the exception of the A/D converter and analog only peripherals such as the current source, potentiometers and op-amp, all the peripheral operating speeds are affected by the Clock Control circuit

Software Reset

Software reset can be generated by setting the SOFTRST bit of the CLKDIVCTRL register to 1.

Power-on/Brown-Out Reset

The VMX51C1020 includes a Power-On-Reset/Brown-Out detector circuit that ensures the VMX51C1020 enters and stays in the reset state as long as the supply voltage is below the reset threshold voltage (order of 3.7 – 4.0 Volts).

In most applications, the VMX51C1020 requires no external components to perform a Power-on Reset when the device is powered on.

The VMX51C1020 includes a RESET input for applications in which external Reset control is required. The reset pin includes an internal pull-up resistor. When a Power-on reset occurs, all SFR locations return to their default values and peripherals are disabled.

Errata Note:

The VMX51C1020 may fail to exit the reset state if the supply voltage drops below the reset threshold, but not below 3V. For applications where this condition can occur, use an external supply monitoring circuit to reset the device.

Processor Power Control

The processor power management unit has two modes of operation: IDLE and STOP mode.

IDLE Mode

When the VMX51C1020 is in IDLE mode, the processor clock is halted. However, the internal clock and peripherals continue to run. The power consumption drops because the CPU is not active. As soon as an interrupt or reset occurs, the CPU exits the IDLE mode.

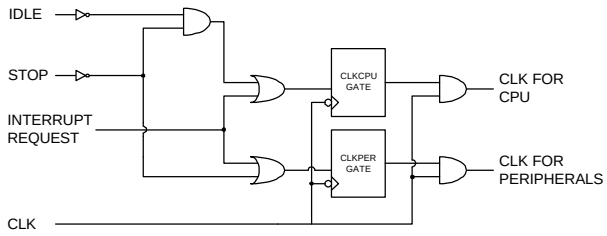
In order to enter IDLE mode, the user must set the IDLE bit of the PCON register. Any enabled interrupts will force the processor to exit IDLE mode

STOP Mode

In this mode, in contrast to IDLE mode, all internal clocking shuts down. In order to enter STOP mode, the user must set the STOP bit of the PCON register. The CPU will exit this state only when a non-clocked external interrupt or reset occurs (internal interrupts are not possible because they require clocking activity).

The following interrupts can restart the processor from STOP mode: Reset, INT0, INT1, SPI Rx/Rx Overrun, and the I^2C interface.

FIGURE 46: POWER MANAGEMENT ON THE VMX51C1020



The following table describes the power control register of the VMX51C1020.

TABLE 126: (PCON) POWER CONTROL (CPU) - SFR 87H

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	STOP	IDLE

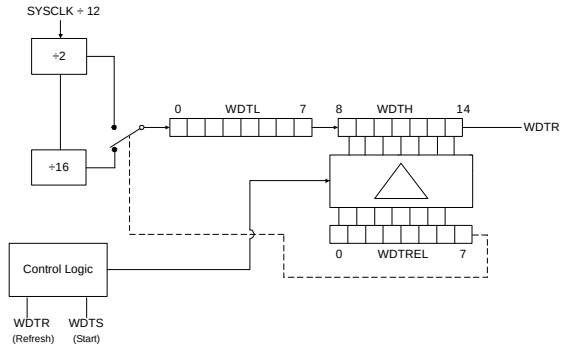
Bit	Mnemonic	Function
7	SMOD	The speed in Mode 2 of Serial Port 0 is controlled by this bit. When SMOD= 1, f_{clk} /32. This bit is also significant in Mode 1 and 3, as it adds a factor of 2 to the baud rate.
6	-	-
5	-	-
4	-	-
3	GF1	Not used for power management
2	GF0	Not used for power management
1	STOP	Stop mode control bit. Setting this bit turns on the STOP Mode. STOP bit is always read as 0.
0	IDLE	IDLE mode control bit. Setting this bit turns on the IDLE mode. IDLE bit is always read as 0.

Watchdog Timer

The VMX51C1020's Watchdog Timer is used to monitor program operation and reset the processor in the case where the program code would not be able to refresh the Watchdog before its timeout period has lapsed. This can come about from an event that results in the Program Counter executing faulty or incorrect code and inhibiting the device from doing its intended job.

The Watchdog Timer consists of a 15-bit counter composed of two registers (WDTL and WDTH) and a reload register (WDTREL). See following figure.

FIGURE 47: WATCH DOG TIMER



The WDTL and WDTH registers are not accessible from the SFR register. However the WDTREL register makes it possible to load the upper 6 bits of the WDTH register.

The PRES bit of the WDTREL register selects the Clock prescaler that is fed into the Watchdog Timer.

When PRES = 0, the clock prescaler = 24
When PRES = 1, the clock prescaler = 384

TABLE 127: (WDTREL) WATCHDOG TIMER RELOAD REGISTER - SFR D9H

7	6	5	4	3	2	1	0
PRES	WDTREL [6:0]						

Bit	Mnemonic	Function
7	PRES	Pre-scaler select bit. When set, the Watchdog is clocked through an additional divide-by-16 pre-scaler.
6-0	WDTREL	7-bit reload value for the high-byte of the Watchdog timer. This value is loaded into the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

TABLE 128: (IP0) INTERRUPT PRIORITY REGISTER 0 - SFR B8H

7	6	5	4	3	2	1	0
UF8	WDTSTAT	IP0 [5:0]					

Bit	Mnemonic	Function		
7	UF8	User Flag bit		
6	WDTSTAT	Watchdog timer status flag. Set to 1 by hardware when the watchdog timer overflows. Must be cleared manually		
5	IP0.5	Timer 2	Port1 Change	ADC
4	IP0.4	UART0	-	MULT/ACCU
3	IP0.3	Timer 1	-	I2C
2	IP0.2	External INT1	-	SPI RX availlable
1	IP0.1	Timer 0 Interrupt	-	SPI TX Empty
0	IP0.0	External INT0	UART1	External INT 0

The WDTSTAT bit of the IP0 register is the Watchdog status flag. This bit is set to 1 by the hardware whenever a Watchdog Timer overflow occurs. This bit must be cleared manually.

Setting-up the Watchdog Timer

Control of the Watchdog Timer's is enabled by the following bits:

Bit	Location	Role
WDOGEN	DIGPWREN.6	Watchdog timer Enable
WDTR	IEN0.6	Watchdog timer refresh flag
WDTS	IEN1.6	Watchdog Timer Start bit

In order for the Watchdog to begin counting, the user must set the WDOGEN bit (bit 6) of DIGPWREN register, as follows:

```
MOV     DIGPWREN,#x1xxxxxxB     ;x=0 or 1 depending
                                ;of other peripherals
                                ;to enable
```

The value written into the WDTREL register defines the Delay Time of the Watchdog Timer asfollows:

WDT delay when the WDTREL bit 7 is cleared
WDT Delay = $\frac{24*[32768-(WDTREL(6:0) \times 256)]}{Fosc}$

WDT delay when the WDTREL bit 7 is set
WDT Delay = $\frac{384*[32768-(WDTREL(6:0) \times 256)]}{Fosc}$

The following table provides WDT reload values and their corresponding delay times

Fosc	WDTREL	WDT Delay
14.74MHz	00h	53.3ms
14.74MHz	4Fh	20.4ms
14.74MHz	CCh	347ms

Note: The value present in the CLKDIVCTRL Register affects the Watchdog Timer Delay time. The above equations and examples assume that the CLKDIVCTRL register content is 00h

Starting the Watchdog Timer

To start the Watchdog timer using the hardware automatic start procedure, the WDTS (IEN1) and WDTR (IEN0) bits must be set. The Watchdog will begin to run with default settings, i.e. all registers will be set to zero.

```
;*** Do a Watchdog Timer Refresh / Start sequence

SETB    IEN0.6          ;Set the WDTR bit first
SETB    IEN1.6          ;Then without delay set the
;WDTS bit
```

When the WDT registers enter the state 7FFFh, the asynchronous signal, WDTS will become active. This signal will set bit 6 in the IP0 register and trigger a reset.

To prevent the Watchdog Timer from resetting the VMX51C1020, you must reset it periodically by clearing the WDTR and, immediately afterwards, clear the WDTS bit.

As a security feature to prevent inadvertent clearing of the Watchdog timer, no delay (instruction) is allowed between the clearing of the WDTR and the WDTS bits.

a) Watchdog Timer refresh example 1:

```
*** The Simple way ***

MOV     IEN0,#x1xxxxxxB     ;DIRECT WRITE THAT SET BIT
                            ;WDTR (x = 0 or 1)
MOV     IEN1,#x1xxxxxxB     ;DIRECT WRITE THAT SET BIT
                            ;WDTS (x = 0 or 1)
```

In the case where the program makes use of the interrupts, it is recommended to deactivate interrupts before the Watch Dog refresh is performed and reactivate them afterwards.

b) Watch Dog Timer refresh example 2:

```
*** If Interrupts are used: ***

CLR     IEN0.7              ;Deactivate the interrupt
MOV     A,IEN0              ;Retrieve IEN0 content
ORL     A,#01000000B        ;set the bit 6 (WDTR)
XCH     A,R1                ;Store IENO New Value
MOV     A,IEN1              ;Retrieve IEN1 content
ORL     A,#01000000B        ;Set bit 6, (WDTS)
MOV     IEN0,R1             ; Set WDTR BIT
MOV     IEN1,A              ;Set WDTS BIT
SETB    IEN0.7              ;Reactivate the Interrupts
```

Watchdog Timer Reset

To determine whether the Reset condition was caused by the Watchdog Timer, the state of the WDTSTAT bit of the IP0 register should be monitored. On a standard power on reset condition, this bit is cleared.

WDT Initialization and Use Example Program

```
ORG 0000H                ;RESET & WD IRQ VECTOR
LJMP      START

;****************************************
;* MAIN PROGRAM BEGINNING  *
;****************************************

ORG    0100h
;*** Initialize WDT and other peripherals***
MOV       DIGPWREN,#40H       ;ENABLE WDT OPERATION

;*** INITIALIZE WATCHDOG TIMER RELOAD VALUE
MOV       WDTREL,#04FH        ;The WDTREL register is used to
                              ;define the Delay Time WDT.
                              ;Bit 7 of WDTREL define clock
                              ;prescalng value
                              ;Bit 6:0 of WDTREL defines the
                              ;upper 7 bits reload value of the
                              ;watchdog Timer 15-bit timer

;*** PERFORM A WDT REFRESH/START SEQUENCE
SETB      IEN0.6              ;Set the WDTR bit first
SETB      IEN1.6              ;Then without delay (instruction)
                              ;set the WDTS bit right after.
                              ;No Delays are permitted between
                              ;setting of the WDTR bit and
                              ;setting of the WDTS bit.
                              ;This is a security feature to
                              ;prevent inadvertent reset/start of
                              ;the WDT

                              ;IF other interrupt are enabled,
                              ;It is recommended to disable
                              ;interrupts before refreshing the
                              ;WDT and reactivate them after

;*** Wait WDT Interrupt

WAITWDT:             NOP

;*** If the two following code lines below are  put "in-comment", the ;***WDT will
trigger a reset, and the program will restart.

;*** PERFORM A WATCHDOG TIMER REFRESH/START SEQUENCE
;SETB      IEN0.6              ;Set the WDTR bit first
;SETB      IEN1.6              ;Then without delay (instruction)
LJMP      WAITWDT             ;set the WDTS bit right after.
                              ;No Delays are permitted between
                              ;setting of the WDTR bit and
                              ;setting of WDTS bit.
                              ;This is a security feature to
                              ;prevent inadvertent reset/start of
                              ;the WDT
                              ;It is recommended to disable
                              ;interrupts before refreshing the ;WDT
                              and reactivate them after
```

VMX51C1020 Programming

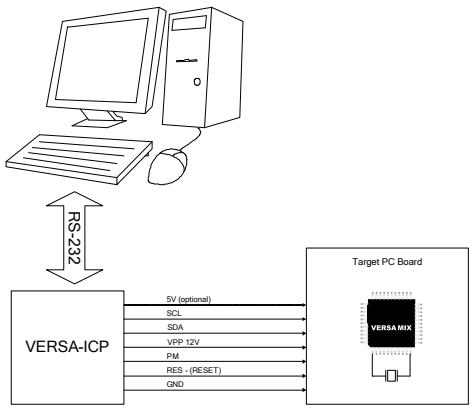
When the PM pin is set to 1, the I²C interface becomes the programming interface for the VMX51C1020's Flash memory.

An In-circuit programming interface is easy to implement at the board level. See VMIX APP-Note001.

Erasing and programming the VMX51C1020's Flash memory requires an external programming voltage of 12V. This programming voltage is supplied/controlled by the programming hardware/tools.

The VMX51C1020 can be programmed using the Ramtron In-Circuit Programmer.

FIGURE 48: VMX51C1020 PROGRAMMING



VMX51C1020 Debugger

The VMX51C1020 includes hardware Debugging features that speed-up embedded software development time.

Debugger Features

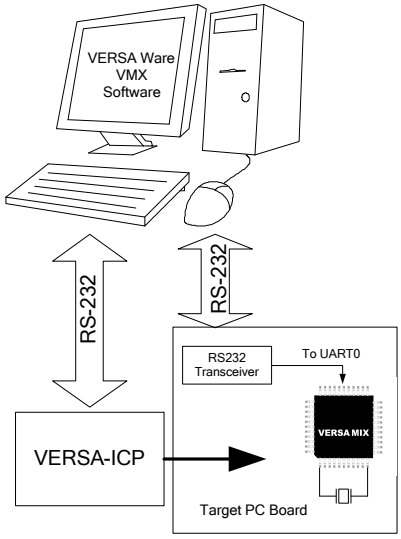
The VMX51C1020 Debugger supports breakpoints and single-stepping of the user program. It supports retrieval and editing of the contents of the SFR Registers and RAM memory contents when a breakpoint is reached or when the device operates in single-step mode. Unlike ROM monitor programs that execute user program instruction at a much lower speed, the VMX51C1020 Debugger does not affect program operating speed when in "Run Mode" before encountering a breakpoint.

Debugger Hardware Interface

The VMX51C1020's Development System provides the ideal platform for running the Debugger. Interfacing to the VMX51C1020's Debugger is done via the UART0 serial interface.

It is possible to run the VMX51C1020 Debugger on the end user PCB provided that access to the VMX51C1020's UART0 is available. However, a connection to a stand alone In-Circuit Programmer (ICP) will be required to perform Flash programming, control of the Reset line, and to activate the Debugger on the target VMX51C1020 device.

FIGURE 49: VMX51C1020 DEBUGGER HARDWARE INTERFACE



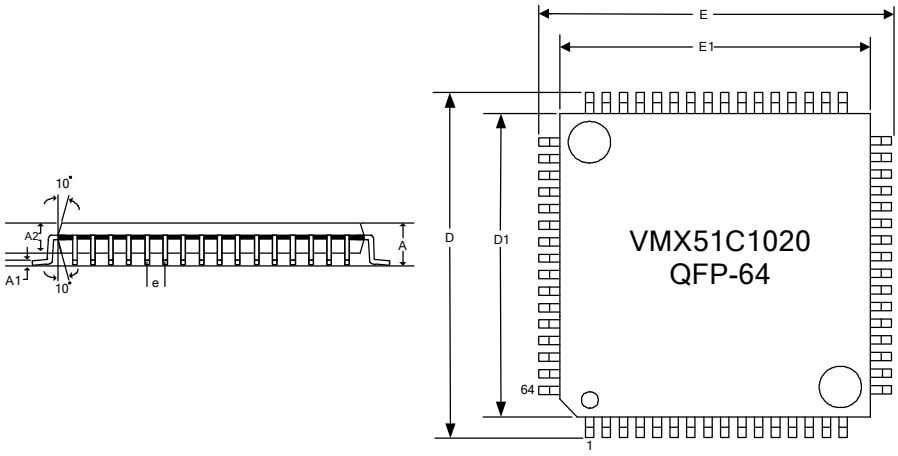
Debugger Software Interface

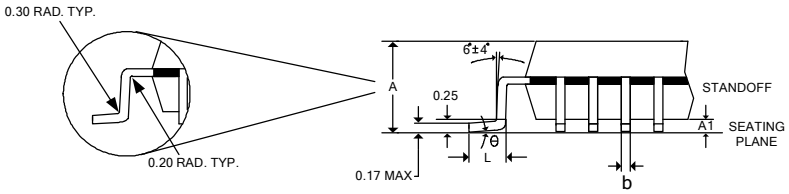
The VERSA WARE VMX51C1020 / VERSA1 Windows™ software provides an easy to use user interface for In-Circuit Debugging

For more details on the VMX51C1020 Debugger, see the *"VERSA WARE VMX51C1020 - V1 Software User Guide.pdf"*

All documents are accessible on the Ramtron Inc. website at www.ramtron.com

VMX51C1020 64 pin Quad Flat Package





		BODY +3.20mm Footprint
PACKAGE THICKNESS		2.00
Dims.	LEADS / TOLS	64L
A	MAX.	2.35
A1		0.25MAX
A2	+.10/-.05	2.00
D	±.25	17.20
D1	±.10	14.00
E	±.25	17.20
E1	±.10	14.00
L	+.15/-.10	.88
e	BASIC	.80
b	±.05	.35
θ		0º-7º

NOTES:

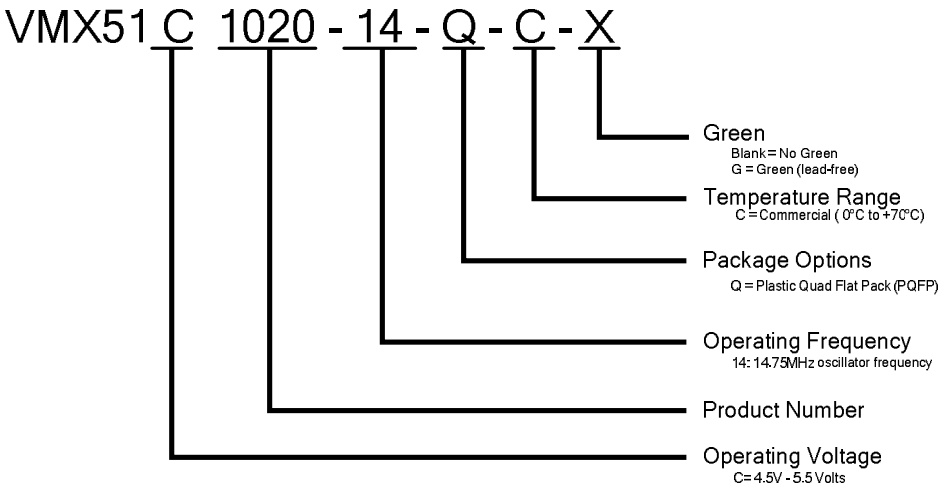
1) ALL DIMENSIONS ARE IN MILLIMETERS

2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.

3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE SEATING PLANE

Ordering Information

Device Number Structure



VMX51C1020 Ordering Options

Device Number	Package Option	Operating Voltage	Temperature	Frequency
VMX51C1020-14-QC	QFP-64	4.75V to 5.5V	0°C to +70°C	14.75MHz
VMX51C1020-14-QCG	QFP-64	4.75V to 5.5V	0°C to +70°C	14.75MHz

*See Errata information below

VMX51C1020 Errata

The VMX51C1020 operating frequency and temperature range have been revised with more conservative values.
The maximum operating frequency specifications of the VMX51C1020 has been revised to 14.75MHz and its operating temperature range to 0ºC to 70ºC.
These new specifications affect all the VMX51C1020 devices with the markings of VMX51C1020-QAI16.
In order to reflect the specification updates of the VMX51C1020, the new VMX51C1020 devices that have the same silicon version, features and performances as the VMX51C1020-QAI16 will now be marked VMX51C1020-QAC14.

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