HEWLETT PACKARD

T-41-91

1300 nm FDDI Transmitter and Receiver

Technical Data

Transmitter HFBR-1125
Receiver HFBR-2125

Features

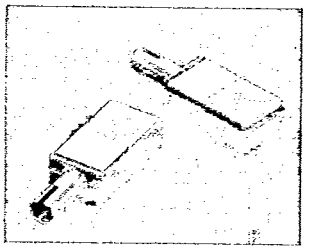
- Full Compliance with FDDI PMD Standard Performance Requirements
- Single +5 V Power Supply
- Shifted ECL Logic Interface Directly Compatible with FDDI PHY Integrated Circuits
- Directly Compatible with TAXIchip™* Encode/ Decode Circuits
- High Reliability
- ST®** Style Fiber Optic Connector
- High Immunity to EMI/RFI and ESD

Applications

- FDDI Single or Dual Attachment Stations
- FDDI Bridges, Routers and Concentrators
- FDDI Backbone Servers
- FDDI Workstations
- FDDI Stations With Internal Optical Bypass Switches to Minimize Board Space
- FDDI Stations With Packaging That Does Not Allow The Use of The FDDI Media Interface Connector (MIC)
- Non-FDDI Proprietary Data Links

Description

The FDDI† transmitter and receiver described in this data sheet are members of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. These FDDI transmitter and receiver products supply the performance necessary for the system designer who seeks to develop equipment with fully compliant FDDI interfaces per the FDDI Physical Layer Medium Dependent (PMD) standard. The performance of both the transmitter and receiver are guaranteed over the operating temperature and power supply voltage ranges found in most commercial equipment with sufficient margin over the FDDI PMD requirements to allow for substantial equipment mission-life and configuration flexibility.



Hewlett-Packard is a vertically integrated supplier. The 1300 nm LED and PIN devices along with the three custom bipolar integrated circuits (ICs) used in these products have been developed and manufactured by Hewlett-Packard. The assembly and testing of the transmitter and receiver products is performed in facilities wholly owned and operated by Hewlett-Packard.

*TAXIchip™ is a trademark of Advanced Micro Devices, Inc.
**ST® is a registered trademark of AT&T for Lightguide Cable Connectors.
†FDDI represents Fiber Distributed Data Interface. The FDDI Physical Layer Medium Dependent (PMD) document has been approved as International Standard for Organization (ISO) Developmental International Standard (DIS) 9314-3.

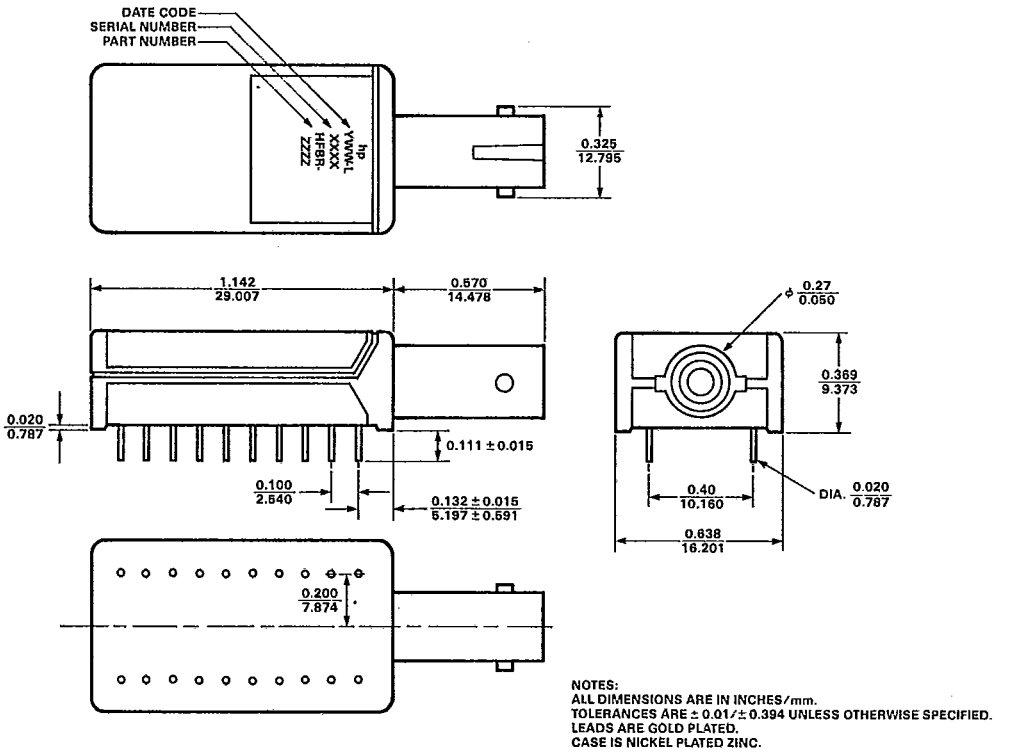


Figure 1. Outline Drawing.

Transmitter - HFBR-1125
The HFBR-1125 transmitter uses a 1300 nm InGaAsP LED and a single, custom silicon bipolar LED driver integrated circuit. The LED is an advanced planar device with an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0s" are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to the transmitter is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply.

Receiver - HFBR-2125
The HFBR-2125 receiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. This assures performance with the clock recovery circuit when any possible FDDI input optical signal condition exists. The second IC, a quantizer, provides the final pulse shaping for the logic output and the Signal Detect function. Both the data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply.

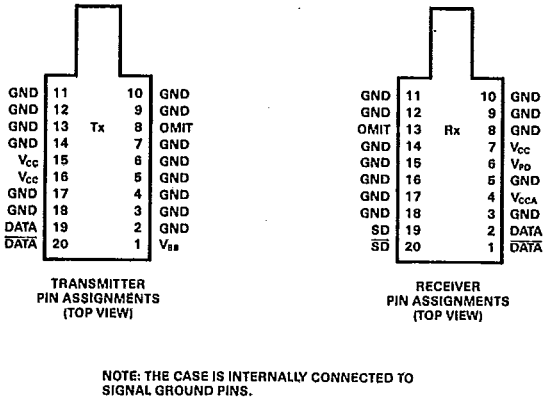


Figure 2. Pin Assignments.

Package

The overall package concept for the Hewlett-Packard FDDI transmitter and receiver consists of three basic elements: the optical subassembly, the electrical subassembly and the overall housing and connector port. The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission-lifetimes.

The optical subassembly contains either the 1300 nm LED or the 1300 nm PIN and preamplifier devices in a hermetic enclosure which is actively aligned to a GRIN rod optical element in the precision stainless steel ferrule-bore. This active alignment provides optimal optical performance for both the transmitter and receiver. The precision stainless steel bore assures that the ST® connector ferrule tip containing the fiber will be precisely positioned relative to the focal point of the optics.

The electrical subassembly is a multilayer, ceramic substrate containing the driver or quantizer integrated circuits along with various surface-mounted passive components. This multilayer substrate provides optimum electrical performance with good noise immunity and noise emission suppression.

The housing and connector port are die-cast zinc with nickel plating. Zinc is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at the lowest levels possible for high reliability and long mission-life. The optical subassembly with its precision stainless steel connector ferrule bore fits into the ST® style bayonet connector port. The electrical and optical subassembly signal grounds are connected to the zinc housing for maximum shielding. The electrical and optical subassemblies are mounted into the zinc housing and epoxy sealed for environmental protection. The optical port is protected with an easily removable, high temperature, vinyl cap for protection from contamination during assembly onto circuit boards and shipment to the end-user site.

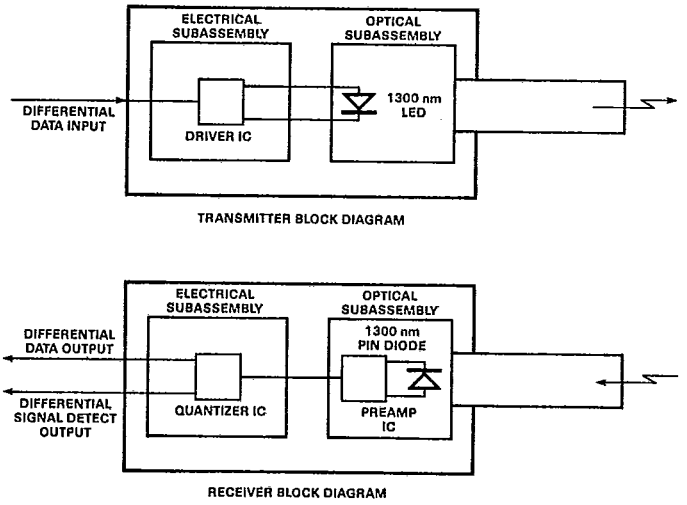


Figure 3. Block Diagrams.

Application Assistance

The Applications Engineering group in the Hewlett Packard Optical Communication Division is available to assist with the analysis of the performance of these products within a given circuit design. The effects of various data-encoding schemes and cable plants can be analyzed to predict the system performance for a particular data link. Assistance is also available to obtain the best performance from these parts with appropriate board layout techniques for these high signaling rates. Figure 10 provides a good example of a decoupling scheme that works well with these products. Contact your local Hewlett–Packard sales representative to obtain this assistance.

Product Reliability Data

Various environmental and life tests have been performed on these products and these tests are ongoing. Contact your local Hewlett-Packard sales representative to obtain copies of the summaries of these test results as they become available.

FDDI Transmitter and Receiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage – High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data Input Current – Low	I_{IL}	-350			µA	
Data Input Current – High	I_{IH}			350	µA	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate	f_S	10		125	MBd	Note 6 Figures 4, 5

FDDI Transmitter

FDDI Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		220	270	mA	Note 7
Power Dissipation	P_{DISS}		1.1	1.4	W	
Threshold Voltage	V_{BB} - V_{CC}	-1.420		-1.240	V	Note 8

FDDI Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	-18.5	-16	-14	dBm avg	Note 9
50/125 µm, NA = 0.20 Fiber	P_O		-20		dBm avg	Note 9, 10
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/°C	
Optical Extinction Ratio			.01 -40	10 -10	% dB	Note 11
Center Wavelength	λ_C	1270	1300	1380	nm	Note 12 Figure 6
Spectral Width – FWHM	$\Delta\lambda$		130	170	nm	Note 13 Figure 6
Optical Rise Time	t_r	0.6	2.1	3.5	ns	Note 14 Figures 6, 7
Optical Fall Time	t_f	0.6	2.7	3.5	ns	Note 14 Figures 6, 7
Duty Cycle Distortion	DCD		0.07	0.6	ns pk-to-pk	Note 15
Data Dependent Jitter	DDJ		0.20	0.6	ns pk-to-pk	Note 16
Random Jitter	RJ		0.01	0.69	ns pk-to-pk	Note 17

FDDI Receiver

FDDI Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power						
Minimum at Window Edge	$P_{IN\ Min}$ (W)		-35.3	-32.1	dBm avg	Note 18 Figure 8
Minimum at Center	$P_{IN\ Min}$ (C)		-37.5	-34	dBm avg	Note 19 Figure 8
Maximum	$P_{IN\ Max}$	-14	-13		dBm avg	Note 19
Operating Wavelength	λ	1270		1380	nm	
Signal Detect						
Asserted	P_A	P_D +1.5 dB	-36.2	-33.5	dBm avg	Note 20, 31 Figure 9
Deasserted	P_D	-45	-38.5		dBm avg	Note 21, 32 Figure 9
Hysteresis	$P_A - P_D$	1.5	2.3		dB	Figure 9

FDDI Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	100	mA	Note 22
Supply Current	I_{CCA}		30	40	mA	Note 22
Supply Current – PIN Diode	I_{PD}		35	500	µA	Note 23
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 24
Data Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 25
Data Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 25
Data Output Rise Time	t_r	0.35	0.7	1.3	ns	Note 26
Data Output Fall Time	t_f	0.35	0.7	1.3	ns	Note 26
Duty Cycle Distortion	DCD		0.08	0.4	ns pk-to-pk	Note 27
Data Dependent Jitter	DDJ		0.40	1.0	ns pk-to-pk	Note 28
Random Jitter	RJ			2.14	ns pk-to-pk	Note 29
Signal Detect						
Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 25
Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 25
Output Rise Time	t_r	0.35	1.0	1.6	ns	Note 30
Output Fall Time	t_f	0.35	1.0	1.6	ns	Note 30
Assert Time (off to on)	AS_Max	0	75	100	µs	Note 20, 31 Figure 9
Deassert Time (on to off)	ANS_Max	0	190	350	µs	Note 21, 32 Figure 9

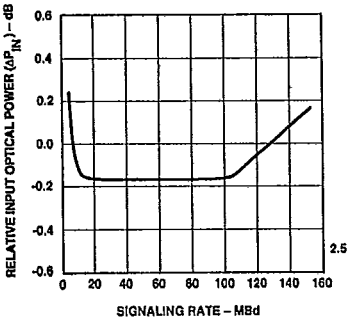
Notes:

1. This maximum rating applies to still air environments around the transmitter and receiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with 50 ohms connected to V_{CC} - 2 V.
6. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5 x 10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd operation. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, f_s, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load R_L = 10 kohms.
9. These optical power values are measured with the following conditions;
   - At the Beginning Of Life (BOL).
   - Over the specified operating voltage and temperature ranges.
   - With HALT Line State, (12.5 MHz) square-wave, input signal.
   - At the end of one meter of noted optical fiber with cladding modes removed.

   The average power value can be converted to a peak power value by adding 3 dB.

   Higher output optical power transmitters are available on special request.
10. This transmitter is available on special request with coupled optical power guaranteed into 50/125 µm fiber cables. The value will depend on the specific NA of the 50/125 µm fiber used.
11. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) the optical signal is detected with a receiver that linearly converts optical power to voltage, the extinction ratio is the ratio of the voltage of the "0" level compared to the voltage at the "1" level expressed as a percentage.
12. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. The temperature coefficient of the center wavelength is typically +0.37 nm/°C.
13. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. The temperature coefficient of the spectral width is typically +0.25 nm/°C.
14. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. This parameter also complies with the optical pulse envelope shown in Figure 7. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State logic input signal.
15. Duty Cycle Distortion is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz) square-wave, input signal.
16. Data Dependent Jitter is specified with the FDDI test pattern described in FDDI PMD Appendix A.5.
17. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz) square-wave, input signal.
18. The Input Optical Power dynamic range, from the maximum value of "$P_{IN\ Min}$ (W)" to the minimum value of "$P_{IN\ Max}$", is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 2.5 x 10^{-10}. The BER will be better than or equal to 1 x 10^{-12} at input optical power levels greater than the maximum "$P_{IN\ Min}$ (W)" plus approximately 0.8 dB with this Hewlett-Packard receiver. This is 1.2 dB better than required by the FDDI PMD. The measurement conditions are stated below.
   - At the Beginning of Life (BOL)
   - Over the specified operating temperature and voltage ranges
   - Input symbol pattern is the FDDI test pattern defined in FDDI PMD Appendix A.5 with 4B/5B NRZI encoded data that contains a baseline wander effect of 50 kHz. Baseline wander is the alternation of data that contains a low frequency variation in the data pattern.
   - Input optical rise and fall times are approximately 1 ns and 2 ns respectively.
   - Sampled over the range from the center of the symbol ±2.3 ns. This is because a window time-width of 4.6 ns is the worst case allowed between the FDDI PMD Active Input Interface and the FDDI PHY PM_Data.indication input per the example in FDDI PMD Appendix E. This window time-width value is based upon a nearly ideal input optical signal presented to the receiver, i.e., no DCD, insignificant DDJ and RJ and fast optical rise and fall times. Per the Appendix E example the receiver is allowed to contribute a peak-to-peak jitter of DCD(0.4ns) + DDJ(1.0ns) + RJ(2.14ns pk-pk) = 3.54ns. The valid data window time-width then becomes 8.0ns - 3.54ns = 4.46ns, or conservatively 4.6ns.
19. All conditions of Note 18 apply except that the measurement is made at the center of the symbol with no window time-width.
20. This value is measured during the transition from low to high levels of input optical power.
21. This value is measured during the transition from high to low levels of input optical power. The minimum value will be either -45 dBm average or when the input optical power yields a BER of 10^{-3} or less which ever power is higher.

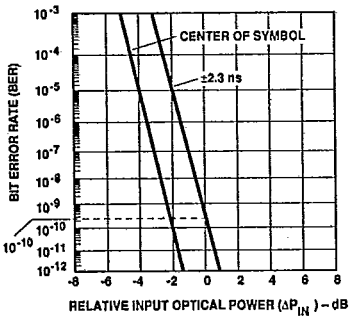
22. These values are measured with the outputs terminated into 50 ohms connected to V_{CC} - 2 V.
23. Measured at P_{IN} = -14 dBm average.
24. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
25. These values are measured with respect to V_{CC} with the output terminated into 50 ohms connected to V_{CC} - 2 V. The minimum values are corrected for +5.25 V operation for 100K ECL values that are usually specified at -4.8 V operation.
26. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 ohms.
27. Duty Cycle Distortion is measured at a 50% threshold using an IDLE pattern, 125 MBd (62.5 MHz) square-wave, input signal. The input optical power level is -20 dBm average.
28. Data Dependent Jitter is specified with the FDDI test pattern described in PMD Appendix A.5. The input optical power level is -20 dBm average.
29. Random Jitter is specified with an IDLE Line State pattern, 125 MBd (62.5 MHz) square-wave, input signal. The input optical power level is at maximum "$P_{IN\ Min}$ (W)".
30. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 ohms.
31. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, ≤ -45 dBm, into the range between greater than P_A and -14 dBm. The BER of the receiver output will be less than 10^{-2} from 15 µs (LS_Max) after Signal Detect has been asserted. See Figure 9 for more information.
32. Signal detect output shall be deasserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of; -31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or less for a period of 12 µs or until signal detect is deasserted. The input data stream is Quiet symbols. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades below 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 9 for more information.



CONDITIONS:

1. P_{IN} NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (C) AT 125 MBd AT CENTER OF SYMBOL.
2. ΔP_{IN} = P_{IN} @ MBd - P_{IN} @ 125 MBd
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
4. BER = 2.5 X 10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

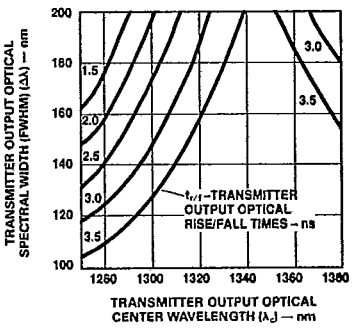
Figure 4. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS:

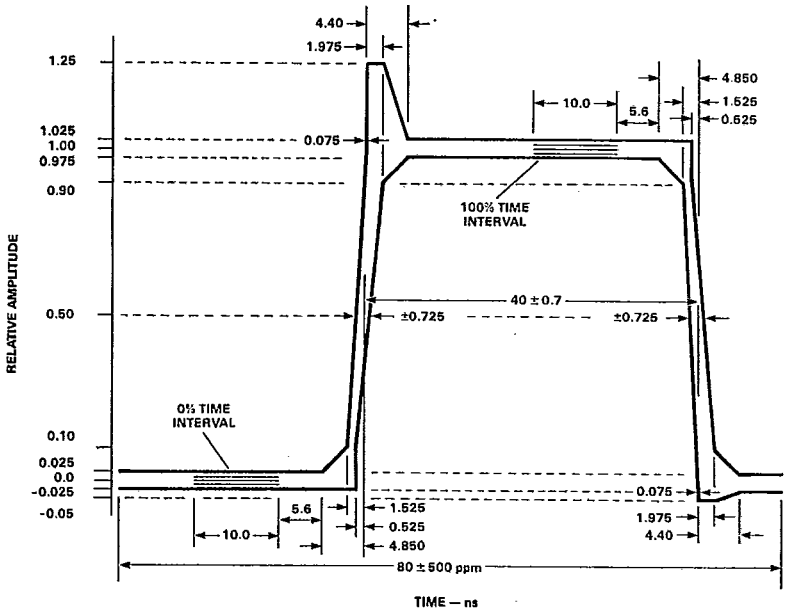
1. P_{IN} IS NORMALIZED (ΔP_{IN} = 0 dB) AT $P_{IN\ Min}$ (W) WITH BER = 2.6 x 10^{-10} AND WINDOW TIME-WIDTH OF ±2.3 ns EITHER SIDE OF SYMBOL CENTER.
2. ΔP_{IN} = P_{IN} @ BER - P_{IN} @ 2.5 x 10^{-10} BER
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. T_A = 25°C
5. V_{CC} = 5.0 Vdc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

Figure 5. Typical Bit Error Rate vs. Relative Input Optical Power.



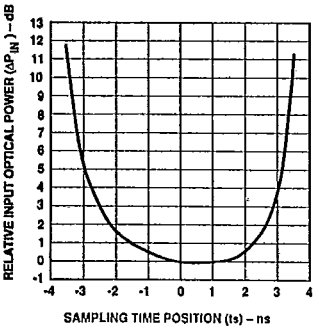
HEWLETT PACKARD FDDI TRANSMITTER TEST RESULTS OF λ_C, $\Delta\lambda$ AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES. REFERENCE FIGURE 5-1 OF FDDI PMD.

Figure 6. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength.



THE OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE. FOR RISE AND FALL TIME MEASUREMENTS, THE MAXIMUM POSITIVE AND MINIMUM NEGATIVE WAVEFORM EXCURSIONS IN THE ZERO AND 100% TIME INTERVALS SHALL BE CENTERED AROUND THE 0.0 AND 1.00 LEVELS, RESPECTIVELY. A MINIMUM BANDWIDTH RANGE OF 100 kHz TO 750 MHz IS REQUIRED FOR THE MEASUREMENT EQUIPMENT USED TO EVALUATE THE PULSE ENVELOPE.

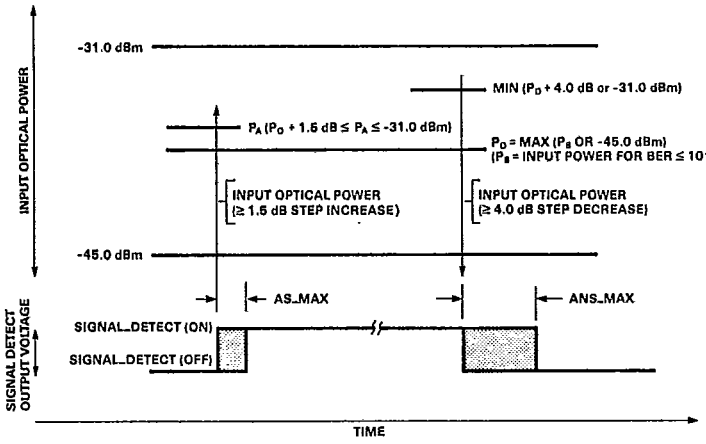
Figure 7. Output Optical Pulse Envelope.



CONDITIONS:

1. P_{IN} IS NORMALIZED TO $P_{IN\ Min}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN} @ t_s - P_{IN} @ t_{center}$
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. BER = 2.5×10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

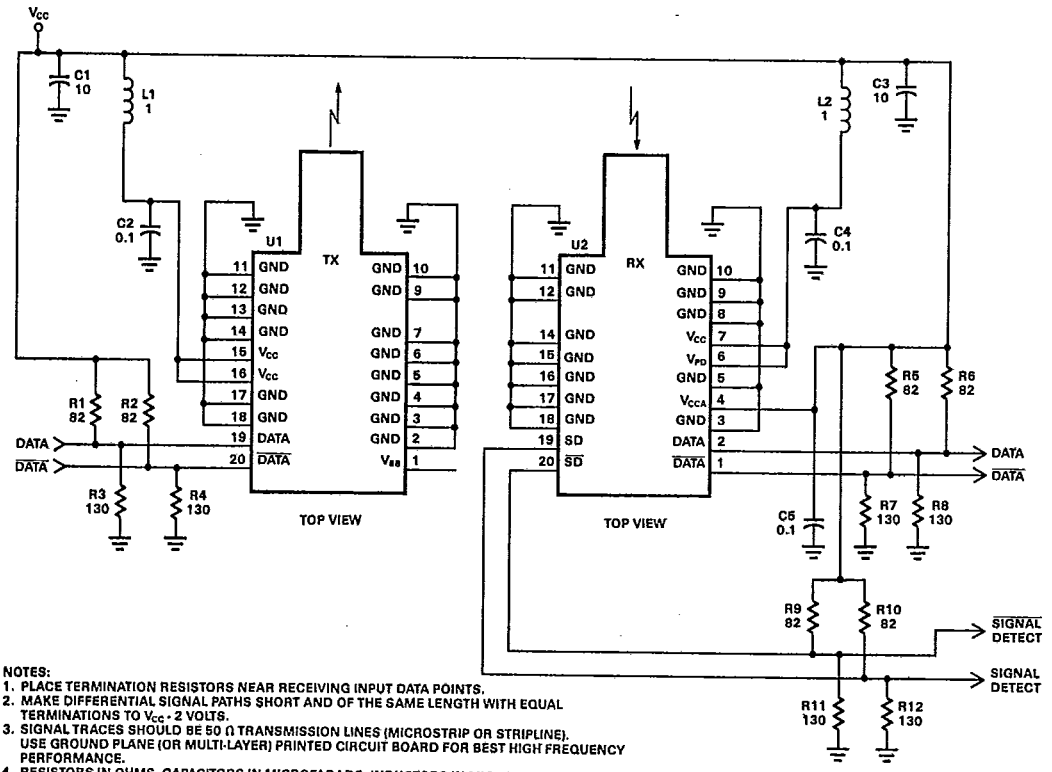
Figure 8. Relative Input Optical Power vs. Sampling Time Position.



AS_MAX—MAXIMUM ACQUISITION TIME (SIGNAL).
AS_MAX IS THE MAXIMUM SIGNAL_DETECT ASSERTION TIME FOR THE STATION.
AS_MAX SHALL NOT EXCEED 100.0 μs. THE DEFAULT VALUE OF AS_MAX IS 100.0 μs.

ANS_MAX—MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS_MAX IS THE MAXIMUM SIGNAL_DETECT DEASSERTION TIME FOR A STATION.
ANS_MAX SHALL NOT EXCEED 350 μs. THE DEFAULT VALUE OF ANS_MAX IS 350 μs.

Figure 9. Signal Detect Thresholds and Timing.



NOTES:
1. PLACE TERMINATION RESISTORS NEAR RECEIVING INPUT DATA POINTS.
2. MAKE DIFFERENTIAL SIGNAL PATHS SHORT AND OF THE SAME LENGTH WITH EQUAL TERMINATIONS TO V_{CC} - 2 VOLTS.
3. SIGNAL TRACES SHOULD BE 50 Ω TRANSMISSION LINES (MICROSTRIP OR STRIPLINE). USE GROUND PLANE (OR MULTI-LAYER) PRINTED CIRCUIT BOARD FOR BEST HIGH FREQUENCY PERFORMANCE.
4. RESISTORS IN OHMS. CAPACITORS IN MICROFARADS. INDUCTORS IN MICROHENRIES.
5. USE HIGH-FREQUENCY MONOLITHIC CERAMIC BYPASS CAPACITORS AND LOW SERIES dc RESISTANCE INDUCTORS. FERRITE INDUCTORS CAN BE USED. LOCATE POWER SUPPLY FILTER, COMPONENTS CLOSE TO FIBER OPTIC DEVICES.
6. CAUTION: DO NOT DIRECTLY CONNECT FIBER OPTIC MODULE ECL OUTPUTS (DATA, $\overline{\text{DATA}}$, SIGNAL DETECT, $\overline{\text{SIGNAL DETECT}}$) TO GROUND WITHOUT PROPER CURRENT LIMITING IMPEDANCE.
7. ALL POWER SUPPLY VOLTAGES FOR THE FIBER OPTIC RECEIVER OR TRANSMITTER SHOULD BE APPLIED SIMULTANEOUSLY TO PREVENT POSSIBLE DAMAGE TO THE DEVICE.
8. DEVICE GROUND PINS SHOULD BE DIRECTLY AND INDIVIDUALLY CONNECTED TO GROUND.

Figure 10. Recommended Decoupling Circuit Diagram.