HYS64D64300HU-[5/6/7]-B
HYS72D64300HU-[5/6/7F]-B
HYS64D128320HU-[5/6/7]-B
HYS72D128320HU-[5/6/7F]-B

184-Pin Unbuffered Dual-In-Line Memory Modules
UDIMM
DDR SDRAM

Memory Products

Infineon technologies

Never stop thinking.

Edition 2003-09

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Page	Subjects (major changes since last revision)
all	new data sheet template

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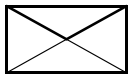


Table of Contents

1 Overview

1.1 Features

- 184-Pin Unbuffered Dual-In-Line Memory Modules (ECC and non-parity) for PC and Workstation main memory applications
- One rank 64M x 64, 64M ×72 and two ranks 128M × 64, 128M ×72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single +2.5V (±0.2V) power supply
- Built with 512 Mbit **DDR SDRAM** in P-TSOPII-66-1 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts
- DDR400 speed grade supported
- Lead-free

Table 1 Performance

Part Number Speed Code			**–5**	**–6**	**–7**	**–7F**	**Unit**
Speed Grade	Component		DDR400B	DDR333B	DDR266A	DDR266	—
	Module		PC3200 –3033	PC2700 –2533	PC2100 –2033	PC2100 –2022	—
max. Clock Frequency	@ CL = 3	f_{CK3}	200	166	—	—	MHz
	@ CL = 2.5	$f_{CK2.5}$	166	166	143	143	MHz
	@ CL = 2	f_{CK2}	133	133	133	133	MHz

1.2 Description

The HYS64D64300HU-[5/6/7]-B, HYS72D64300HU-[5/6/7F]-B, HYS64D128320HU-[5/6/7]-B, and HYS72D128320HU-[5/6/7F]-B are industry standard 184-Pin Unbuffered Dual-In-Line Memory Modules (UDIMM) organized as 64M ×64, 128M ×64 for non-parity and 64M ×72,128M ×72 for ECC main memory applications. The memory array is designed with 512Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer

Table 2 Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL=3)			
HYS64D64300HU-5-B	PC3200U-30330-A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU-5-B	PC3200U-30330-A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU-5-B	PC3200U-30330-B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU-5-B	PC3200U-30330-B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D64300HU-6-B	PC2700U-25330-A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU-6-B	PC2700U-25330-A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU-6-B	PC2700U-25330-B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU-6-B	PC2700U-25330-B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2100 (CL=2)			
HYS64D64300HU-7-B	PC2100U-20330-A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU-7F-B	PC2100U-20220-A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU-7-B	PC2700U-20330-B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU-7F-B	PC2100U-20220-B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)

Note: All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D64300HU-6-B, indicating rev. B dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, RCD[1)] latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.

1) RCD: Row-Column-Delay

2 Pin Configuration

Table 3 Pin Definitions and Functions

Symbol	Type	Function
A0 – A11, A12	Input	Address Inputs (A12 for 256 MB & 512 MB based modules)
BA0, BA1	Input	Bank Selects
DQ0 – DQ63	Input/Output	Data Input/Output
CB0 – CB7	Input/Output	Check Bits (×72 organization only)
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Input
CKE0, CKE1	Input	Clock Enable
DQS0 – DQS8	Input/Output	SDRAM low data strobes
CK0, $\overline{CK0}$	Input	Differential Clock Input
DM0 – DM8	Input	SDRAM low data mask
DQS9 – DQS17	Input/Output	high data strobes
$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects
V_{DD}	Supply	Power (+2.5 V)
V_{SS}	Supply	Ground
V_{DDQ}	Supply	I/O Driver power supply
V_{DDID}	Output	V_{DD} Indentification flag
V_{DDSPD}	Supply	EEPROM power supply
V_{REF}	Supply	I/O reference supply
SCL	Input	Serial bus clock
SDA	Output	Serial bus data line
SA0 – SA2	Input	slave address select
NC	Input	no connect
DU	Input	don’t use
$\overline{RESET}$	Input	Reset pin (forces register inputs low) *)

*) for detailed description of the Power Up and Power Management on DDR Registered DIMMs see the Application Note at the end of this datasheet

Table 4 Pin Configuration

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
1	V_{REF}	48	A0	94	DQ4	141	A10
2	DQ0	49	CB2	95	DQ5	142	CB6
3	V_{SS}	50	V_{SS}	96	V_{DDQ}	143	V_{DDQ}
4	DQ1	51	CB3	97	DM0/DQS9	144	CB7
5	DQ0	52	BA1	98	DQ6	**KEY**	
6	DQ2	**KEY**		99	DQ7	145	V_{SS}
7	V_{DD}	53	DQ32	100	V_{SS}	146	DQ36
8	DQ3	54	V_{DDQ}	101	NC	147	DQ37
9	NC	55	DQ33	102	NC	148	V_{DD}
10	$\overline{\text{RESET}}$	56	DQS4	103	NC	149	DM4/DQS13
11	V_{SS}	57	DQ34	104	V_{DDQ}	150	DQ38
12	DQ8	58	VSS	105	DQ12	151	DQ39
13	DQ9	59	BA0	106	DQ13	152	V_{SS}
14	DQS1	60	DQ35	107	DM1/DQS10	153	DQ44
15	V_{DDQ}	61	DQ40	108	V_{DD}	154	RAS
16	DU	62	V_{DDQ}	109	DQ14	155	DQ45
17	DU	63	WE	110	DQ15	156	V_{DDQ}
18	V_{SS}	64	DQ41	111	CKE1	157	CS0
19	DQ10	65	CAS	112	V_{DDQ}	158	CS1
20	DQ11	66	V_{SS}	113	NC	159	DM5/DQS14
21	DKE0	67	DQS5	114	DQ20	160	V_{SS}
22	V_{DDQ}	68	DQ42	115	NC / A12	161	DQ46
23	DQ16	69	DQ43	116	V_{SS}	162	DQ47
24	DQ17	70	VDD	117	DQ21	163	NC
25	DQS2	71	NC	118	A11	164	V_{DDQ}
26	V_{SS}	72	DQ48	119	DM2/DQS11	165	DQ52
27	A9	73	DQ49	120	V_{DD}	166	DQ53
28	DQ18	74	VSS	121	DQ22	167	NC
29	A7	75	DU	122	A8	168	V_{DD}
30	V_{DDQ}	76	DU	123	DQ23	169	DM6/DQS15
31	DQ19	77	V_{DDQ}	124	V_{SS}	170	DQ54
32	A5	78	DQS6	125	A6	171	DQ55
33	DQ24	79	DQ50	126	DQ28	172	V_{DDQ}
34	V_{SS}	80	DQ51	127	DQ29	173	NC
35	DQ25	81	V_{SS}	128	V_{DDQ}	174	DQ60
36	DQS3	82	V_{DDID}	129	DM3/DQS12	175	DQ61
37	A4	83	DQ56	130	A3	176	V_{SS}
38	V_{DD}	84	DQ57	131	DQ30	177	DM7/DQS16
39	DQ26	85	V_{DD}	132	V_{SS}	178	DQ62
40	DQ27	86	DQS7	133	DQ31	179	DQ63

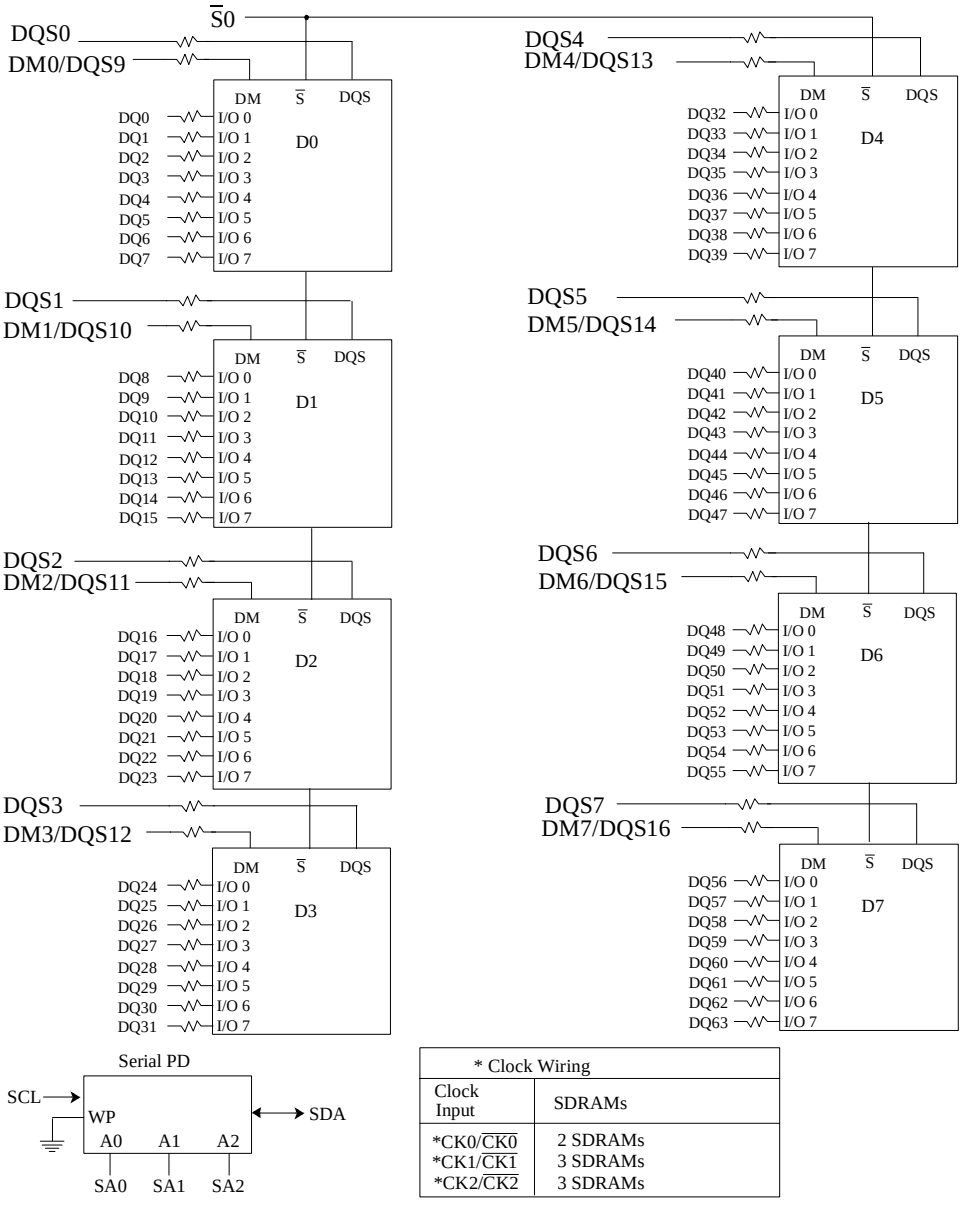
Table 4 Pin Configuration (cont'd)

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
41	A2	87	DQ58	134	CB4	180	V_{DDQ}
42	V_{SS}	88	DQ59	135	CB5	181	SA0
43	A1	89	V_{SS}	136	V_{DDQ}	182	SA1
44	CB0	90	NC	137	CK0	183	SA2
45	CB1	91	SDA	138	CK0	184	V_{DDSPD}
46	V_{DD}	92	SCL	139	V_{SS}	–	–
47	DQS8	93	V_{SS}	140	DM8/DQS17	–	–

Note: A12 is used for 256Mbit and 512Mbit based modules only

Table 5 Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
512 MB	64M × 64	1	64M × 8	8	13/2/11	8K	64 ms	7.8 µs
512 MB	64M × 72	1	64M × 8	8	13/2/11	8K	64 ms	7.8 µs
1 GB	128M × 64	2	64M × 8	16	13/2/12	8K	64 ms	7.8 µs
1 GB	128M × 72	2	64M × 8	16	13/2/12	8K	64 ms	7.8 µs



* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	2 SDRAMs
*CK1/CK1	3 SDRAMs
*CK2/CK2	3 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, RAS, CAS, WE resistors: 5.1 ohms ±5%

Figure 1 Block Diagram - One Rank 64M × 64 DDR SDRAM DIMM HYS64D64300HU-[5/6/7]-B

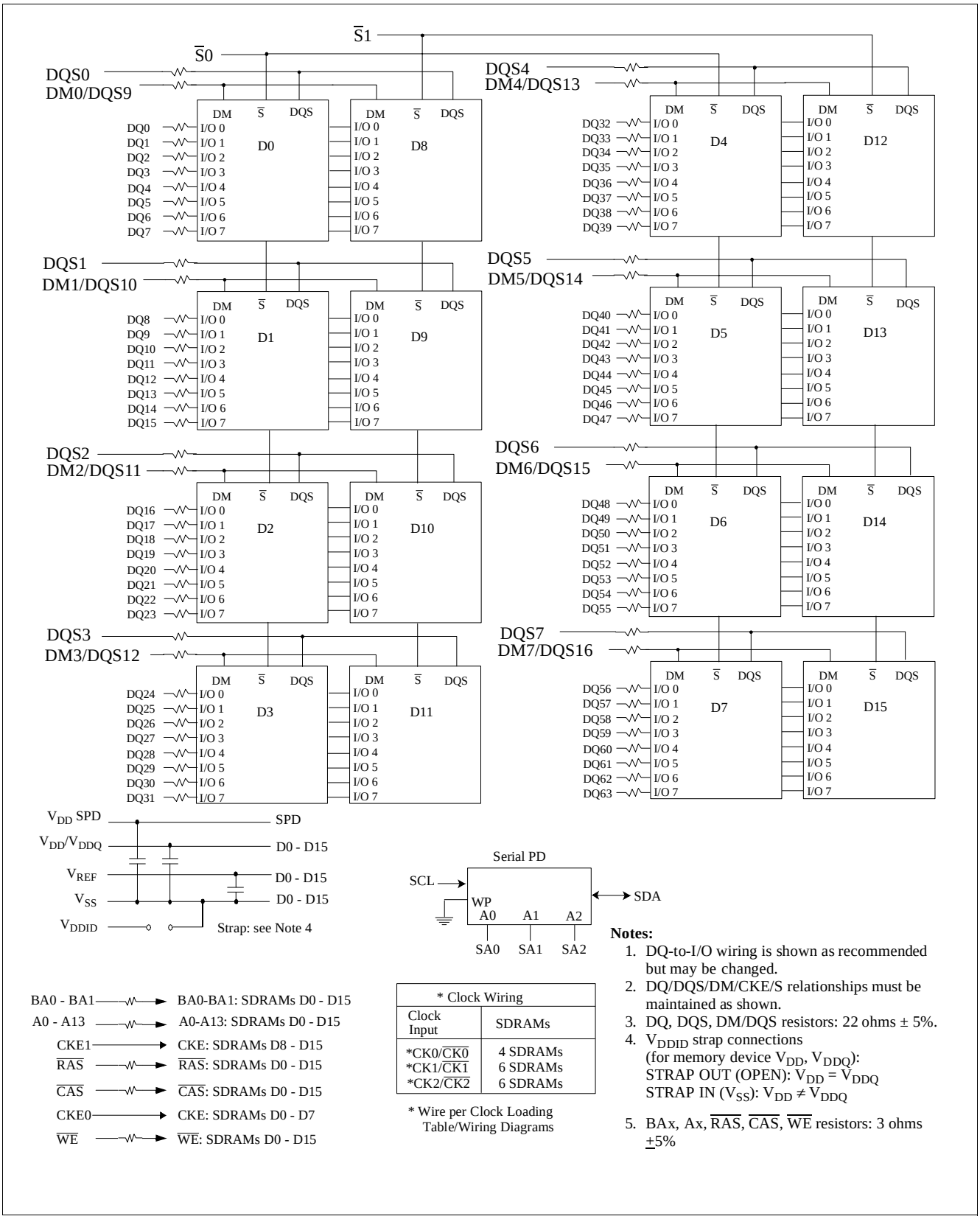


Figure 2 Block Diagram - Two Rank 128M × 64 DDR SDRAM DIMM HYS64D128320HU-[5/6/7]-B

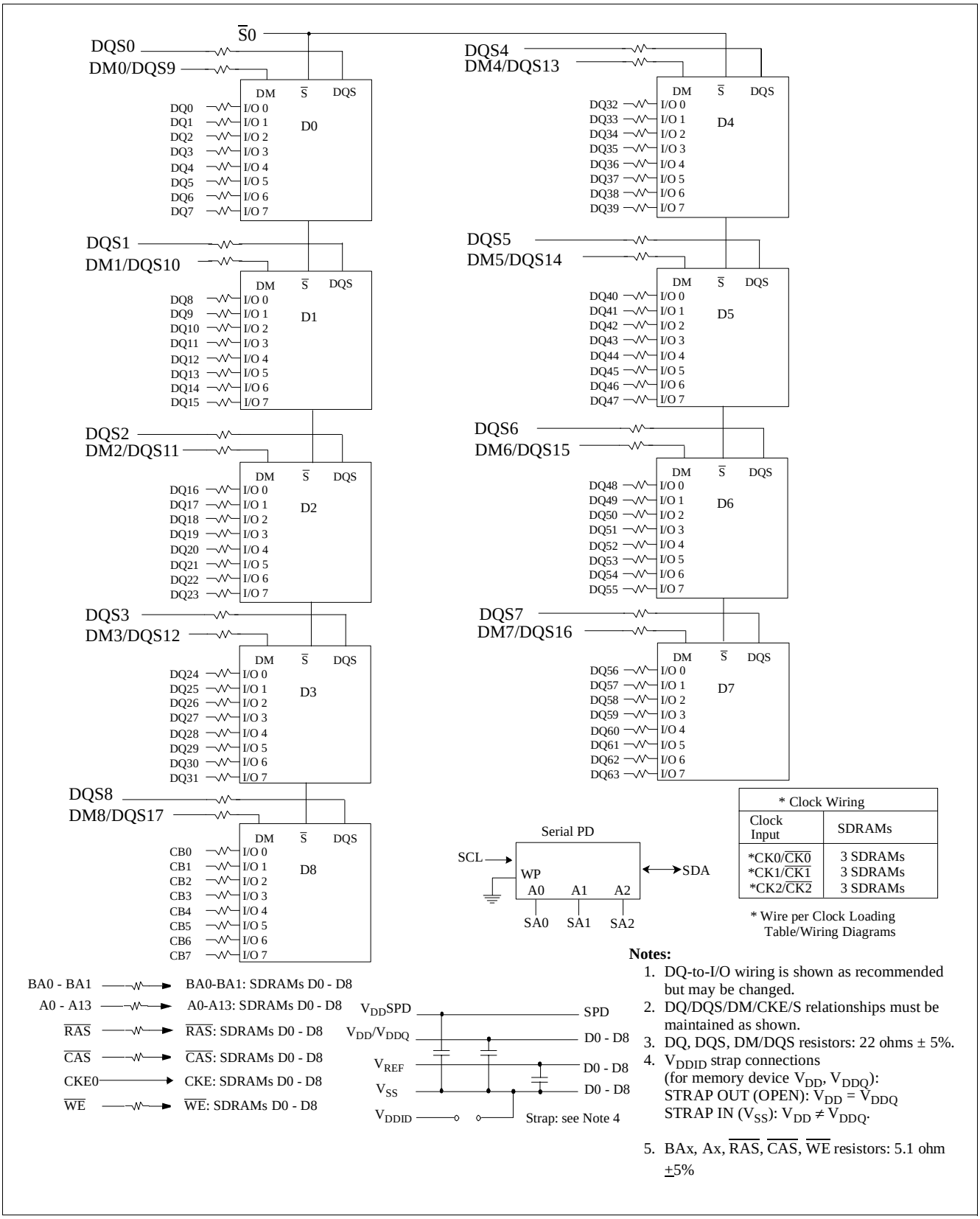
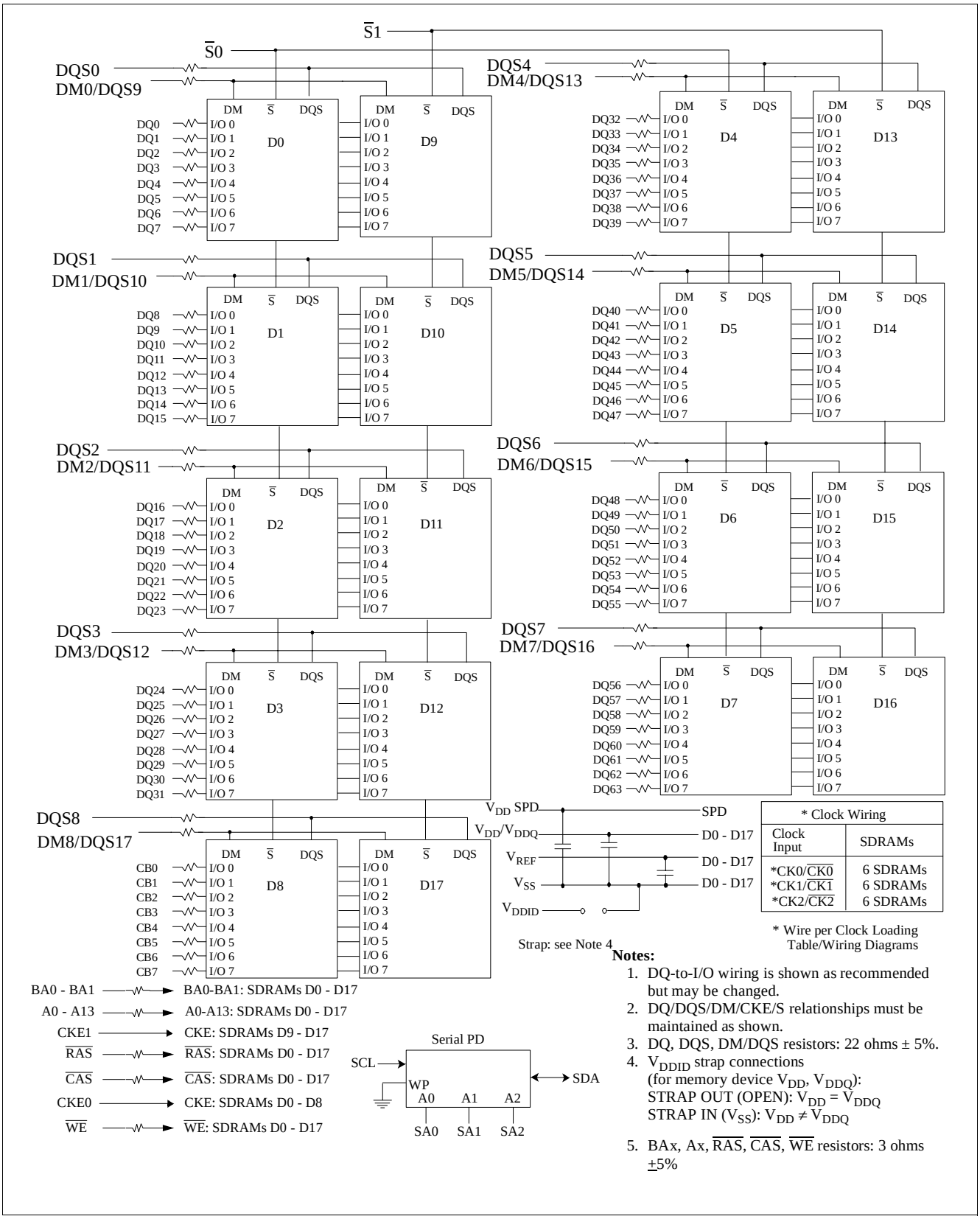


Figure 3 Block Diagram - One Rank 64M × 72 DDR SDRAM DIMM HYS72D64300HU-[5/6/7F]-B



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 3 ohms ±5%

Figure 4 Block Diagram - Two Ranks 128M × 72 DDR SDRAM DIMM HYS72D128320HU-[5/6/7F]-B

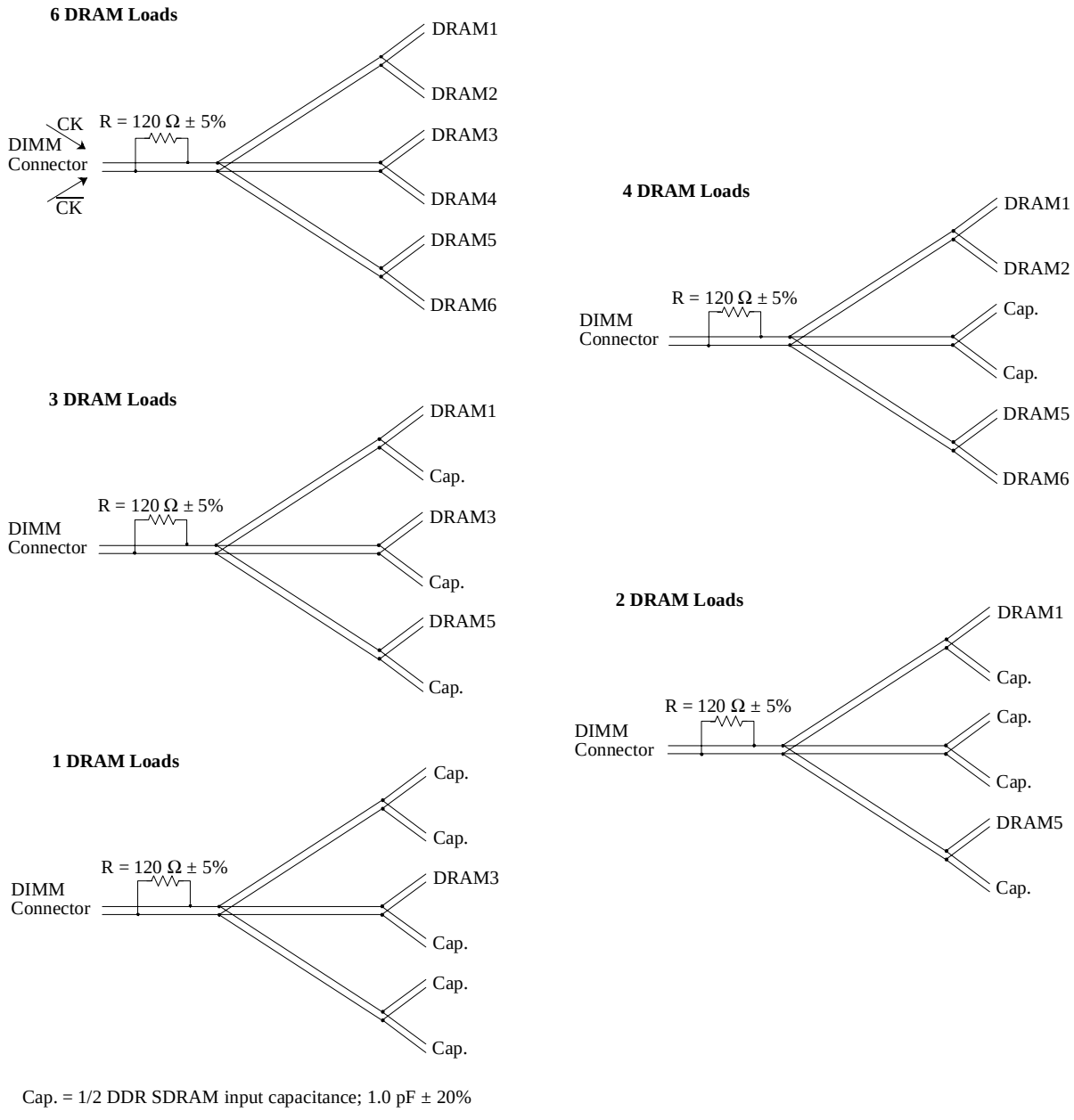


Figure 5 Clock Net Wiring

3 Electrical Characteristics

3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	f_{CK} ≤166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	f_{CK} ≤166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]

Table 7 Electrical Characteristics and DC Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Input Leakage Current	I_I	–2		2	µA	Any input 0 V ≤V_{IN} ≤V_{DD}; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V ≤V_{OUT} ≤V_{DDQ} [8)]
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V [8)]
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V [8)]

1) 0 °C ≤T_A ≤70 °C
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Inputs are not recognized as valid until V_{REF} stabilizes.
9) Values are shown per DDR SDRAM component

Table 8 AC Timing - Absolute Specifications –6/–5

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition [1]
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.5	+0.5	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	6	12	5	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.45	—	0.4	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.45	—	0.4	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	tbd	—	ns	2)3)4)5)6)

Table 8 AC Timing - Absolute Specifications –6/–5 (cont'd)

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition [1]
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	tbd	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
		—	+0.45	—	+0.40	ns	TSOPII 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
		—	+0.55	—	+0.50	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	42	70E+3	40	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	60	—	55	—	ns	2)3)4)5)

Table 8 AC Timing - Absolute Specifications –6/–5 (cont'd)

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition [1]
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	72	—	65	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	18	—	15	—	ns	2)3)4)5)
Precharge command period	t_{RP}	18	—	15	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	18	—	15	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	12	—	10	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}					t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤T_A ≤70 °C; V_{DDQ} = 2.5 V ±0.2 V, V_{DD} = +2.5 V ±0.2 V (DDR333); V_{DDQ} = 2.6 V ±0.1 V, V_{DD} = +2.6 V ±0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

Table 9 AC Timing - Absolute Specifications –7/–7F

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition [1]
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)

Table 9 AC Timing - Absolute Specifications –7/–7F (cont'd)

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition [1]
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK3}	7	12	7	12	ns	CL = 3.0 2)3)4)5)
	$t_{CK2.5}$	7	12	7	12	ns	CL = 2.5 2)3)4)5)
	t_{CK2}	7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.5	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.5	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.5	—	+0.5	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	0.75	—	0.75	ns	2)3)4)5)
DQ/DQS output hold time	t_{QH}	t_{HP} – t_{QHS}	—	t_{HP} – t_{QHS}	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	45	120 E+3	45	120 E+3	ns	2)3)4)5)

Table 9 AC Timing - Absolute Specifications –7/–7F (cont'd)

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition 1)
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
Active to Active/Auto-refresh command period	t_{RC}	65	—	60	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	75	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	15	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	15	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	20	—	15	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤T_A ≤70 °C; V_{DDQ} = 2.5 V ±0.2 V, V_{DD} = +2.5 V ±0.2 V

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333, DDR266

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

3.2 Current Conditions and Specification

Table 10 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤$V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤$V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 11 IDD Specification and Conditions

Part Number & Organization	HYS64D64300HU-7-B		HYS72D64300HU-7F-B		HYS64D128320HU-7-B		HYS72D128320HU-7F-B		Unit	Note 1)2)
	512MB		512MB		1GB		1GB			
	×64		×72		×64		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–7		–7		–7		–7			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	600	720	675	810	832	1000	936	1125	mA	3)
I_{DD1}	680	800	765	900	912	1080	1026	1215	mA	3)4)
I_{DD2P}	24	32	27	36	48	64	54	72	mA	5)
I_{DD2F}	160	192	180	216	320	384	360	432	mA	5)
I_{DD2Q}	120	168	135	189	240	336	270	378	mA	5)
I_{DD3P}	72	104	81	117	144	208	162	234	mA	5)
I_{DD3N}	232	192	261	315	464	560	522	630	mA	5)
I_{DD4R}	560	680	630	765	792	960	891	1080	mA	3)4)
I_{DD4W}	600	720	675	117	832	384	936	432	mA	3)
I_{DD5}	1640	1960	1845	2205	1872	2240	2106	2520	mA	3)
I_{DD6}	23	46	26	51	46	91	52	103	mA	5)
I_{DD7}	1760	2080	1980	2340	1992	2360	2241	2655	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 12

Part Number & Organization	HYS64D64300HU-6-B		HYS72D64300HU-6-B		HYS64D128320HU-6-B		HYS72D128320HU-6-B		Unit	Note 1)2)
	512MB		512MB		1GB		1GB			
	×64		×64		×64		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–6		–6		–6		–6			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	720	840	810	945	1000	1168	1125	1314	mA	3)
I_{DD1}	760	920	855	1035	1040	1248	1170	1404	mA	3)4)
I_{DD2P}	24	32	27	36	48	64	54	72	mA	5)
I_{DD2F}	200	240	225	270	400	480	450	540	mA	5)
I_{DD2Q}	136	192	153	216	272	384	306	432	mA	5)
I_{DD3P}	88	120	99	135	176	240	198	270	mA	5)
I_{DD3N}	280	328	315	369	560	656	630	738	mA	5)
I_{DD4R}	680	840	765	945	960	1168	1080	1314	mA	3)4)
I_{DD4W}	720	880	810	990	1000	1208	1125	1359	mA	3)
I_{DD5}	1760	2120	1980	2385	2040	2448	2295	2754	mA	3)
I_{DD6}	46	23	52	27	46	93	52	104	mA	5)
I_{DD7}	2200	2600	2475	2925	2760	2928	3105	3294	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 13

Part Number & Organization	HYS64D64300HU-5-B		HYS72D64300HU-5-B		HYS64D128320HU-5-B		HYS72D128320HU-5-B		Unit	Note 1)2)
	512MB		512MB		1 GB		1 GB			
	×64		×72		×64		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–5		–5		–5		–5			
Symbol	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**	**typ.**	**max.**		
I_{DD0}	800	920	900	1035	1112	1296	1251	1458	mA	3)
I_{DD1}	880	1040	990	1170	1192	1416	1341	1593	mA	3)4)
I_{DD2P}	24	32	27	36	48	64	54	72	mA	5)
I_{DD2F}	240	288	270	324	480	576	540	648	mA	5)
I_{DD2Q}	152	208	171	234	304	416	342	468	mA	5)
I_{DD3P}	96	128	108	144	192	256	216	288	mA	5)
I_{DD3N}	312	376	351	423	624	752	702	846	mA	5)
I_{DD4R}	800	960	900	1080	1112	1336	1251	1503	mA	3)4)
I_{DD4W}	840	1000	945	1125	1152	1376	1296	1548	mA	3)
I_{DD5}	1960	2360	2205	2655	2272	2736	2556	3078	mA	3)
I_{DD6}	24	47	27	53	48	94	54	106	mA	5)
I_{DD7}	2480	2920	2790	3285	2792	3296	3141	3708	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

4 SPD Contents

Table 12 SPD Codes for –5

	Part Number & Organization	HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–5	–5	–5	–5
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type DDR-I = 07h	07	07	07	07
3	# of Row Addresses	0D	0D	0D	0D
4	# Number of Column Addresses	0B	0B	0B	0B
5	# of DIMM Banks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	50	50	50	50
10	tAC SDRAM @ CLmax (Byte 18) [ns]	50	50	50	50
11	DIMM Configuration Type (non- / ECC)	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM width	08	08	08	08
14	Error Checking SDRAM width	00	08	00	08
15	tCCD [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM	04	04	04	04
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	WE (Write) Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	60	60	60	60
24	tAC SDRAM @ CLmax -0.5 [ns]	50	50	50	50
25	tCK @ CLmax -1 (Byte 18) [ns]	75	75	75	75
26	tAC SDRAM @ CLmax -1 [ns]	50	50	50	50
27	tRPmin (ns)	3C	3C	3C	3C

Table 12 SPD Codes for –5

	Part Number & Organization	HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–5	–5	–5	–5
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
28	tRRDmin [ns]	28	28	28	28
29	tRCDmin [ns]	3C	3C	3C	3C
30	tRASmin [ns]	28	28	28	28
31	Module Density per Bank	80	80	80	80
32	tAS, tCS [ns]	60	60	60	60
33	tAH, TCH [ns]	60	60	60	60
34	tDS [ns]	40	40	40	40
35	tDH [ns]	40	40	40	40
36 - 40	not used	00	00	00	00
41	tRCmin [ns]	37	37	37	37
42	tRFCmin [ns]	41	41	41	41
43	tCKmax [ns]	28	28	28	28
44	tDQSQmax [ns]	28	28	28	28
45	tQHSmax [ns]	50	50	50	50
46 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	3E	50	3F	51
64	JEDEC ID Code for Infineon	C1	C1	C1	C1
65	JEDEC ID Code for Infineon	00	00	00	00
66	JEDEC ID Code for Infineon	00	00	00	00
67	JEDEC ID Code for Infineon	00	00	00	00
68	JEDEC ID Code for Infineon	00	00	00	00
69	JEDEC ID Code for Infineon	00	00	00	00
70	JEDEC ID Code for Infineon	00	00	00	00
71	JEDEC ID Code for Infineon	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44

Table 12 SPD Codes for –5

	Part Number & Organization	HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–5	–5	–5	–5
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	35	35	55	55
84	Part Number, Char 12	42	42	35	35
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Serial Number	xx	xx	xx	xx
96	Module Serial Number	xx	xx	xx	xx
97	Module Serial Number	xx	xx	xx	xx
98	Module Serial Number	xx	xx	xx	xx
99 -127	not used	0	0	0	0

Table 13 SPD Codes for –6

	Part Number & Organization	HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–6	–6	–6	–6
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type DDR-I = 07h	07	07	07	07
3	# of Row Addresses	0D	0D	0D	0D
4	# Number of Column Addresses	0B	0B	0B	0B
5	# of DIMM Banks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	60	60	60	60
10	tAC SDRAM @ CLmax (Byte 18) [ns]	70	70	70	70
11	DIMM Configuration Type (non- / ECC)	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM width	08	08	08	08
14	Error Checking SDRAM width	00	08	00	08
15	tCCD [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	WE (Write) Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	70	70	70	70

Table 13 SPD Codes for –6

	Part Number & Organization	HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–6	–6	–6	–6
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00	00
27	tRPmin (ns)	48	48	48	48
28	tRRDmin [ns]	30	30	30	30
29	tRCDmin [ns]	48	48	48	48
30	tRASmin [ns]	2A	2A	2A	2A
31	Module Density per Bank	80	80	80	80
32	tAS, tCS [ns]	75	75	75	75
33	tAH, TCH [ns]	75	75	75	75
34	tDS [ns]	45	45	45	45
35	tDH [ns]	45	45	45	45
36 - 40	not used	00	00	00	00
41	tRCmin [ns]	3C	3C	3C	3C
42	tRFCmin [ns]	48	48	48	48
43	tCKmax [ns]	30	30	30	30
44	tDQSQmax [ns]	2D	2D	2D	2D
45	tQHSmax [ns]	55	55	55	55
46 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	42	54	43	55
64	JEDEC ID Code for Infineon	C1	C1	C1	C1
65	JEDEC ID Code for Infineon	00	00	00	00
66	JEDEC ID Code for Infineon	00	00	00	00
67	JEDEC ID Code for Infineon	00	00	00	00
68	JEDEC ID Code for Infineon	00	00	00	00
69	JEDEC ID Code for Infineon	00	00	00	00
70	JEDEC ID Code for Infineon	00	00	00	00
71	JEDEC ID Code for Infineon	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx

Table 13 SPD Codes for –6

	Part Number & Organization	HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–6	–6	–6	–6
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	42	42	36	36
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Serial Number	xx	xx	xx	xx
96	Module Serial Number	xx	xx	xx	xx
97	Module Serial Number	xx	xx	xx	xx
98	Module Serial Number	xx	xx	xx	xx
99 - 127	not used	0	0	0	0

Table 14 SPD Codes for –7/–7F

	Part Number & Organization	HYS64D64300HU–7–B	HYS72D64300HU–7F–B	HYS64D128320HU–7–B	HYS72D128320HU–7F–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–7	–7F	–7	–7F
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type DDR-I = 07h	07	07	07	07
3	# of Row Addresses	0D	0D	0D	0D
4	# Number of Column Addresses	0B	0B	0B	0B
5	# of DIMM Banks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	70	70	70	70
10	tAC SDRAM @ CLmax (Byte 18) [ns]	75	75	75	75
11	DIMM Configuration Type (non- / ECC)	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM width	08	08	08	08
14	Error Checking SDRAM width	00	08	00	08
15	tCCD [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	WE (Write) Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	75	75	75	75
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00	00
27	tRPmin (ns)	50	3C	50	3C

Table 14 SPD Codes for –7/–7F

	Part Number & Organization	HYS64D64300HU–7–B	HYS72D64300HU–7F–B	HYS64D128320HU–7–B	HYS72D128320HU–7F–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–7	–7F	–7	–7F
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
28	tRRDmin [ns]	3C	3C	3C	3C
29	tRCDmin [ns]	50	3C	50	3C
30	tRASmin [ns]	2D	2D	2D	2D
31	Module Density per Bank	80	80	80	80
32	tAS, tCS [ns]	90	90	90	90
33	tAH, TCH [ns]	90	90	90	90
34	tDS [ns]	50	50	50	50
35	tDH [ns]	50	50	50	50
36	not used	00	00	00	00
37	not used	00	00	00	00
38	not used	00	00	00	00
39	not used	00	00	00	00
40	not used	00	00	00	00
41	tRCmin [ns]	41	3C	41	3C
42	tRFCmin [ns]	4B	4B	4B	4B
43	tCKmax [ns]	30	30	30	30
44	tDQSQmax [ns]	32	32	32	32
45	tQHSmax [ns]	75	75	75	75
46 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	F4	D9	F5	DA
64	JEDEC ID Code for Infineon	C1	C1	C1	C1
65	JEDEC ID Code for Infineon	00	00	00	00
66	JEDEC ID Code for Infineon	00	00	00	00
67	JEDEC ID Code for Infineon	00	00	00	00
68	JEDEC ID Code for Infineon	00	00	00	00
69	JEDEC ID Code for Infineon	00	00	00	00
70	JEDEC ID Code for Infineon	00	00	00	00
71	JEDEC ID Code for Infineon	00	00	00	00

Table 14 SPD Codes for –7/–7F

	Part Number & Organization	HYS64D64300HU–7–B	HYS72D64300HU–7F–B	HYS64D128320HU–7–B	HYS72D128320HU–7F–B
		512MB	512MB	1GB	1GB
		×64	×72	×64	×72
		1 Rank	1 Rank	2Ranks	2Ranks
		–7	–7F	–7	–7F
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	37	37	55	55
84	Part Number, Char 12	42	46	37	37
85	Part Number, Char 13	20	42	42	46
86	Part Number, Char 14	20	20	20	42
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Serial Number	xx	xx	xx	xx
96	Module Serial Number	xx	xx	xx	xx
97	Module Serial Number	xx	xx	xx	xx
98	Module Serial Number	xx	xx	xx	xx
99 - 127	not used	0	0	0	0

5 Package Outlines

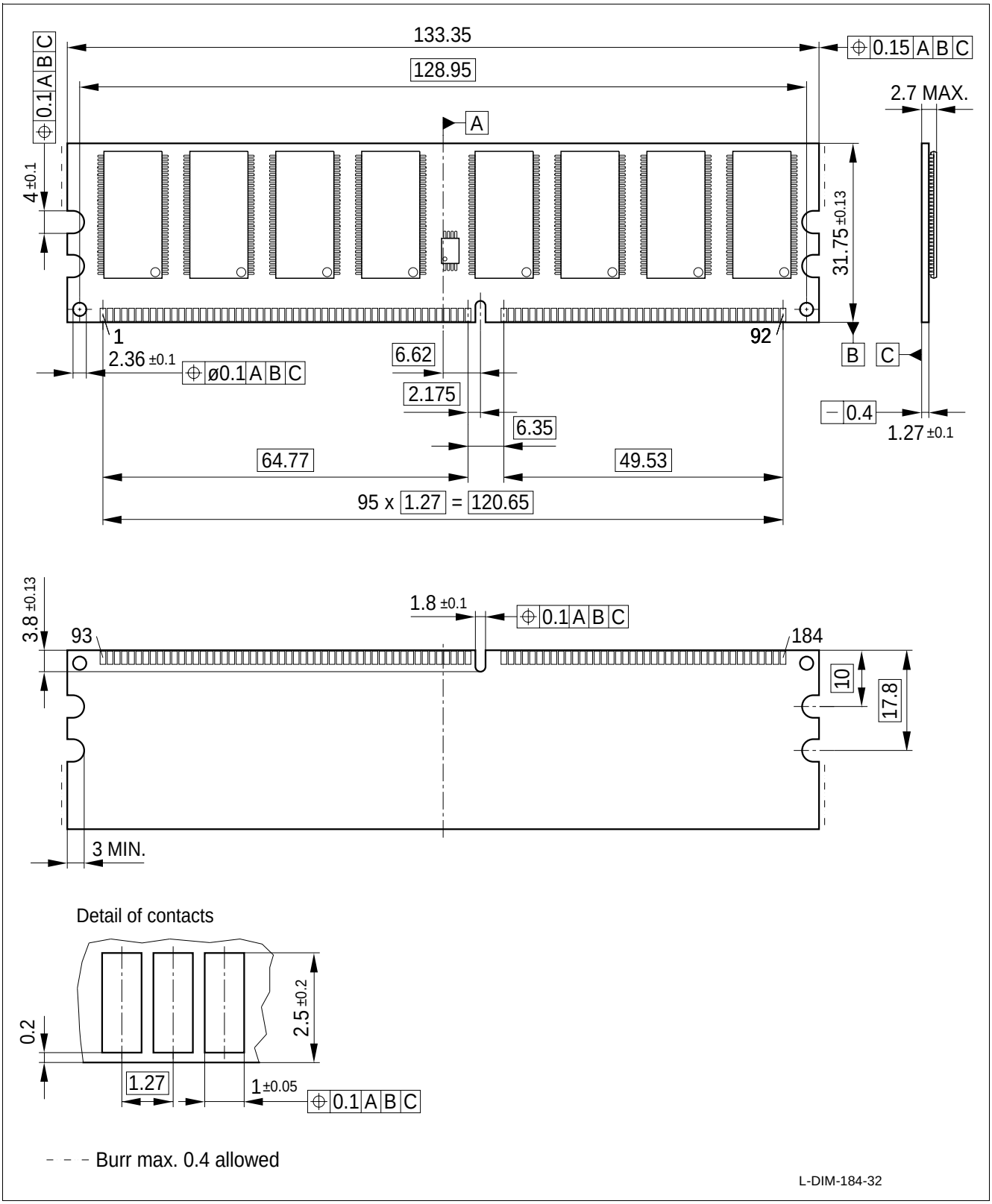


Figure 6 Raw Card A DDR UDIMM HYS64D64300HU-[5/6/7]-B (1 Rank Module)

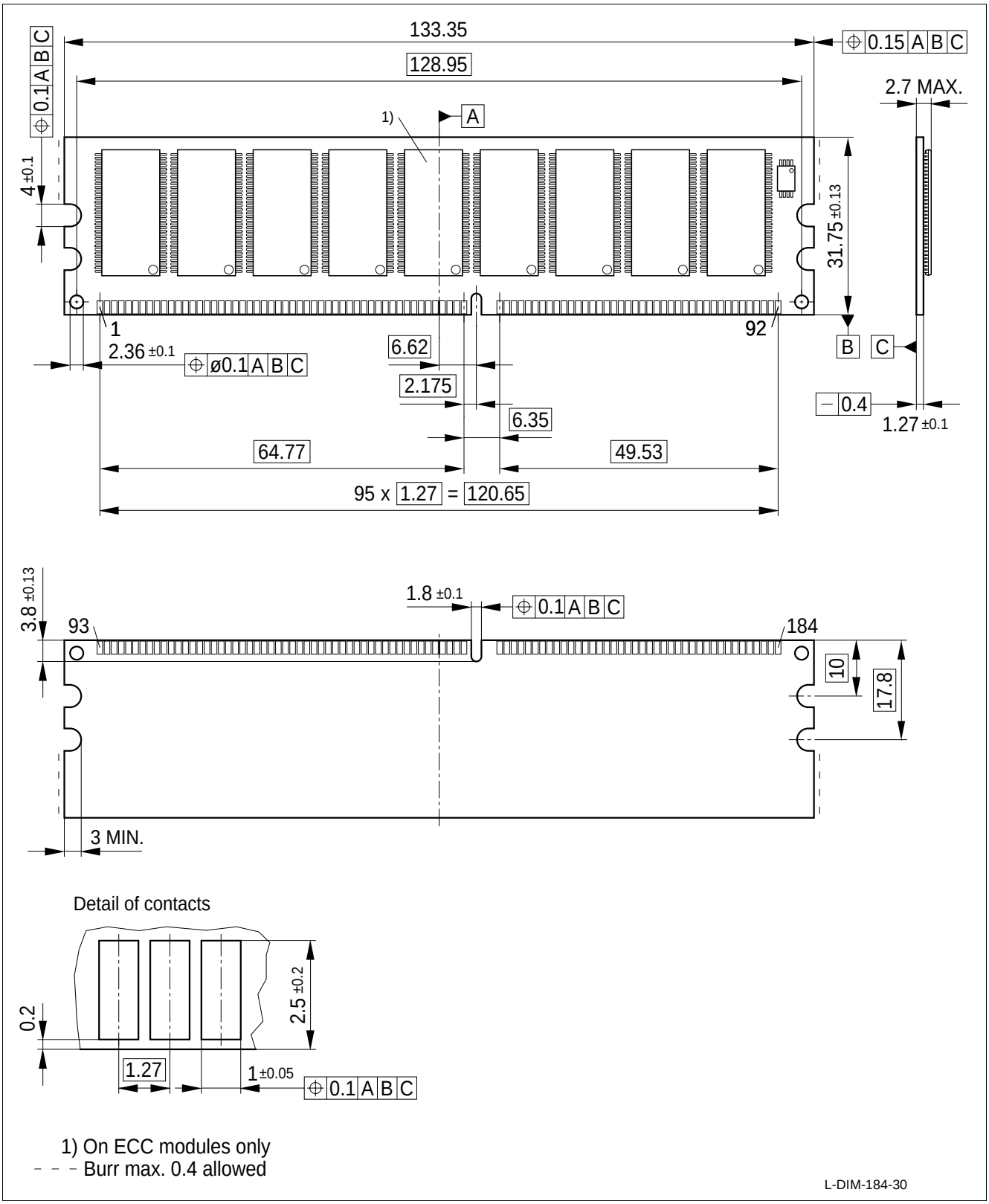


Figure 7 Raw Card A DDR UDIMM HYS72D64300HU-[5/6/7F]-B (1 Rank Module)

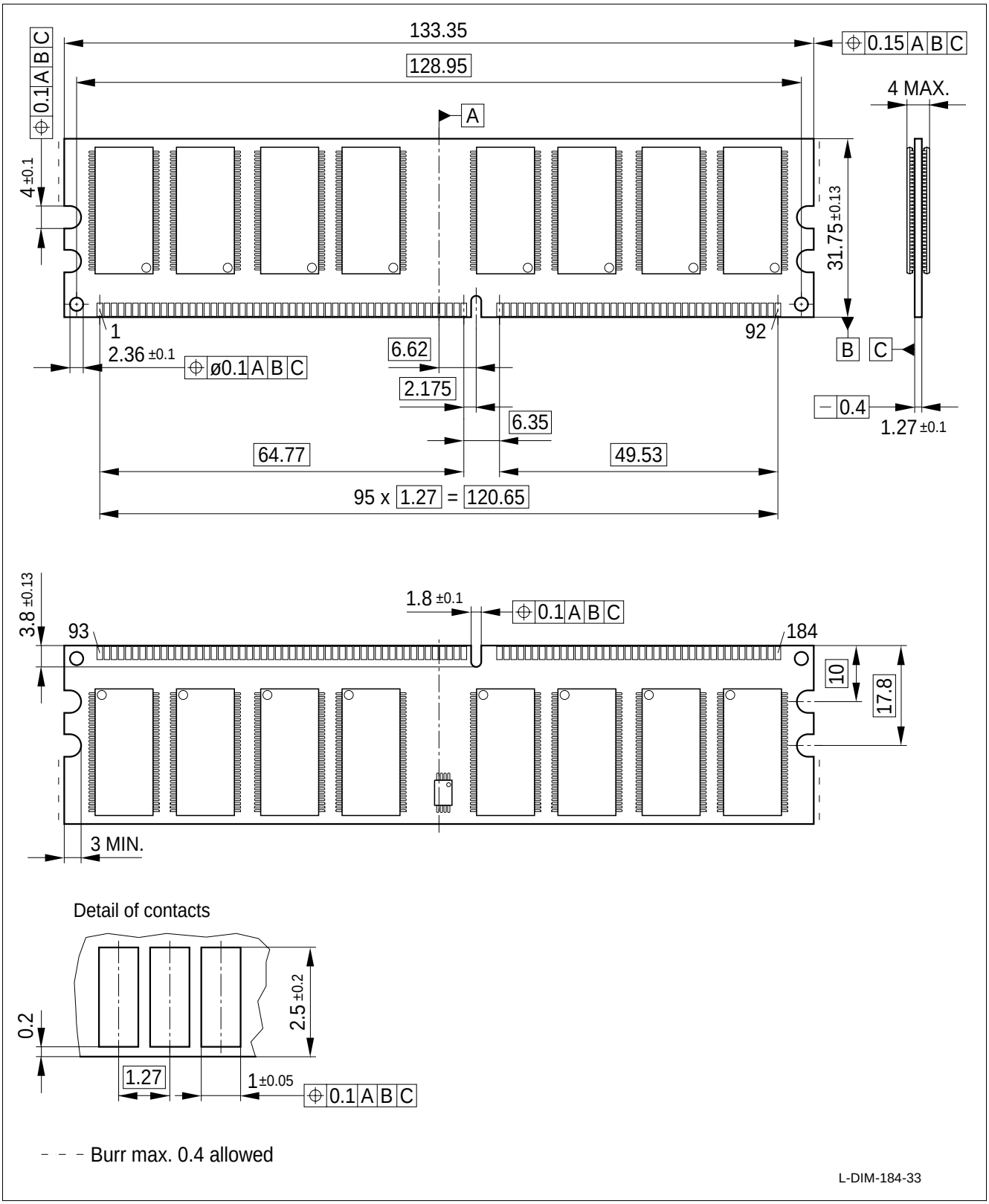


Figure 8 Raw Card B DDR UDIMM HYS64D128320HU-[5/6/7]-B (2 Ranks Module)

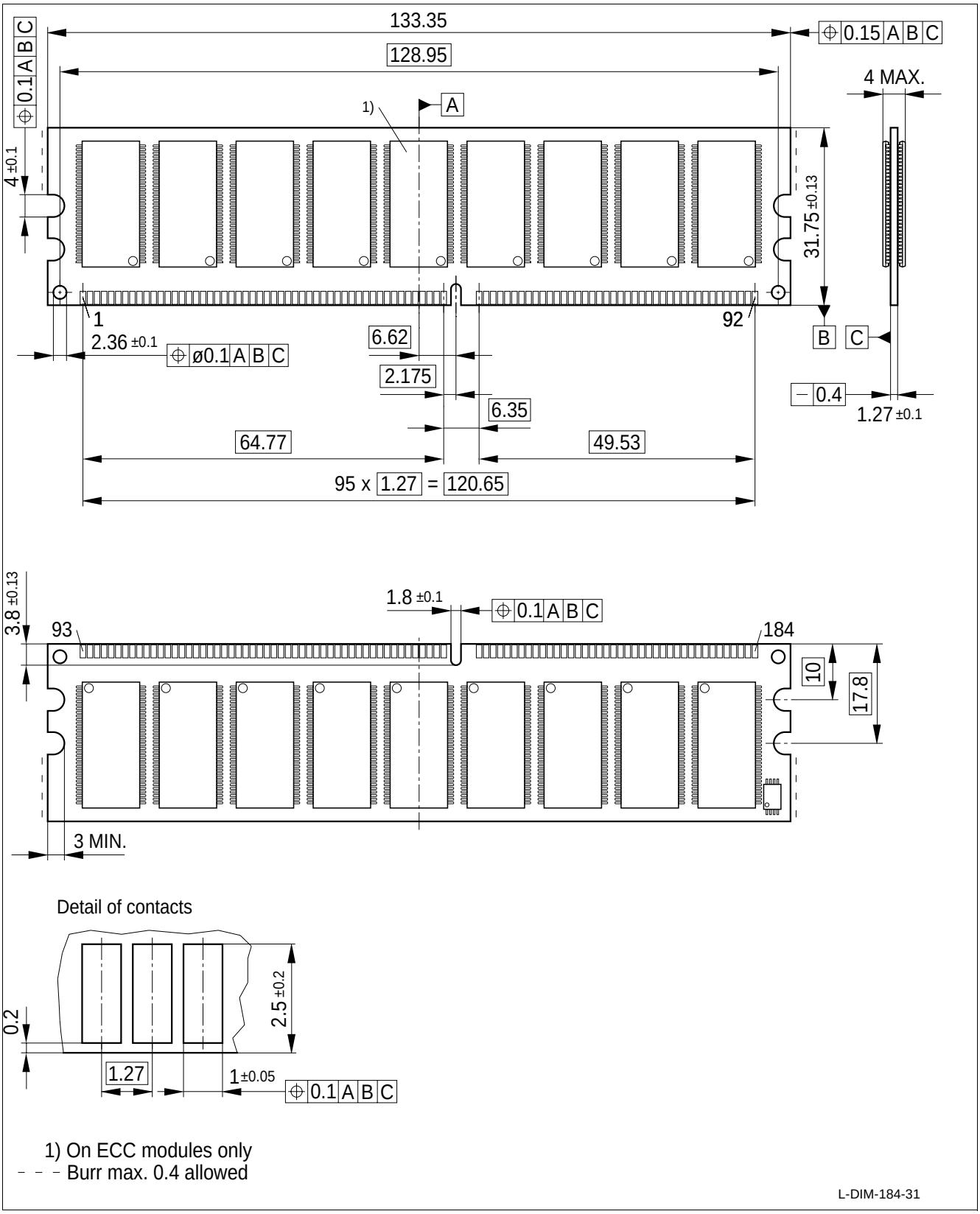


Figure 9 Raw Card B DDR UDIMM HYS72D128320HU-[5/6/7/-B (2 Rank Module)

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