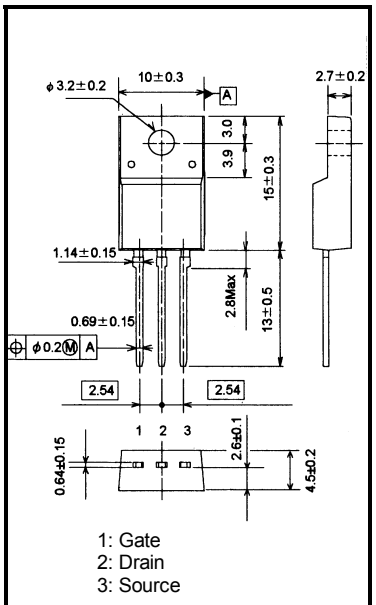
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSVI)

2SK3767

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 3.3 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 1.6S (typ.)
- Low leakage current: I_{DSS} = 100 μA (V_{DS} = 600 V)
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10U1B

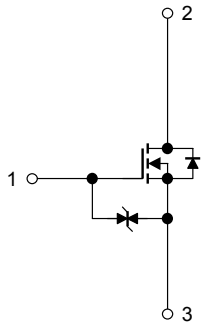
Weight : 1.7 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	600	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	600	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	2	A
	Pulse (Note 1)	I_{DP}	5	
Drain power dissipation (Tc = 25°C)		P_D	25	W
Single pulse avalanche energy (Note 2)		E_{AS}	93	mJ
Avalanche current		I_{AR}	2	A
Repetitive avalanche energy (Note 3)		E_{AR}	4	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	5.0	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C/W



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 41mH, R_G = 25 Ω, I_{AR} = 2 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Please handle with caution.

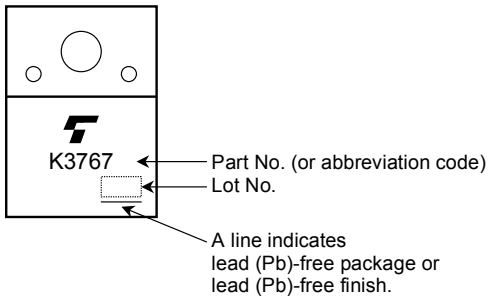
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate-source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	600	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 1 A	—	3.3	4.5	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 1 A	0.8	1.6	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	320	—	pF
Reverse transfer capacitance		C_{rss}		—	30	—	
Output capacitance		C_{oss}		—	100	—	
Switching time	Rise time	t_r	10 V, V_{GS}, 0 V; I_D = 1A; Output; R_L = 200 Ω; 50 Ω; V_{DD} ≃ 200 V; Duty ≦ 1%, t_w = 10 μs	—	15	—	ns
	Turn-on time	t_{on}		—	55	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	80	—	
Total gate charge		Q_g	V_{DD} ≃ 400 V, V_{GS} = 10 V, I_D = 2A	—	9	—	nC
Gate-source charge		Q_{gs}		—	5	—	
Gate-drain charge		Q_{gd}		—	4	—	

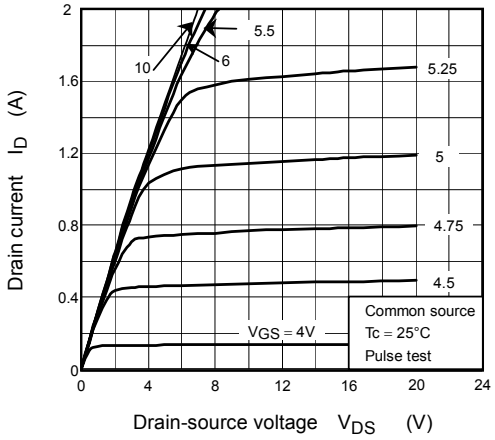
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	2	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	5	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 2 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 2 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	1000	—	ns
Reverse recovery charge	Q_{rr}		—	3.5	—	μC

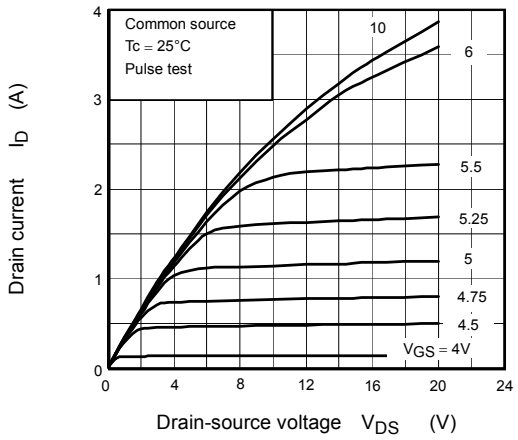
Marking



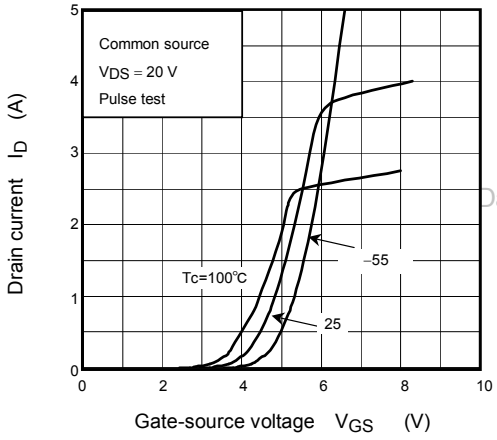
$I_D - V_{DS}$



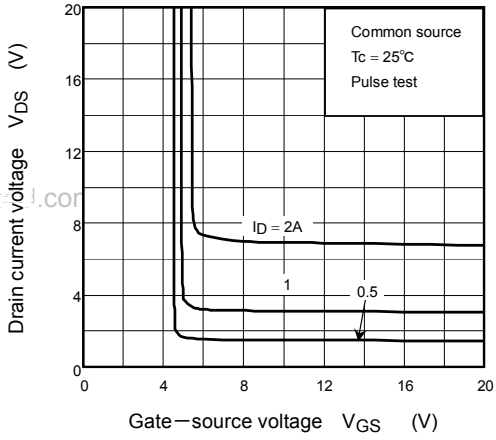
$I_D - V_{DS}$



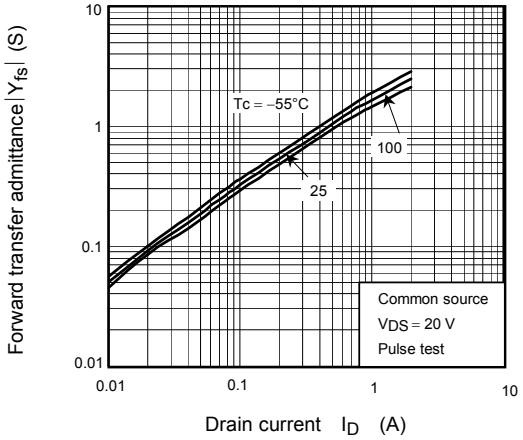
$I_D - V_{GS}$



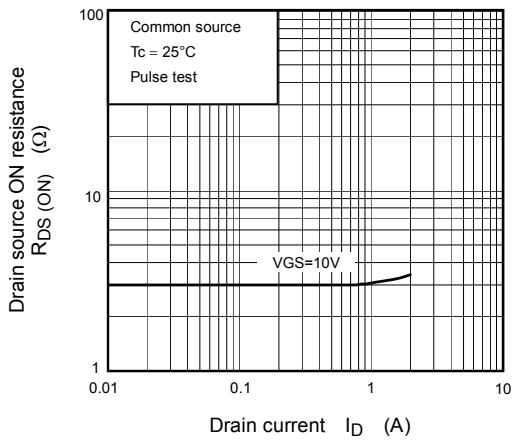
$V_{DS} - V_{GS}$



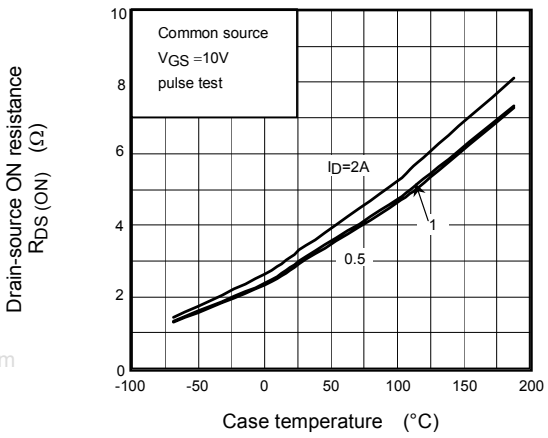
$|Y_{fs}| - I_D$



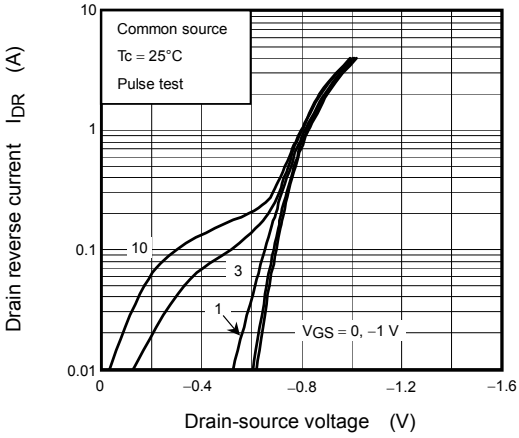
$R_{DS\ (ON)} - I_D$



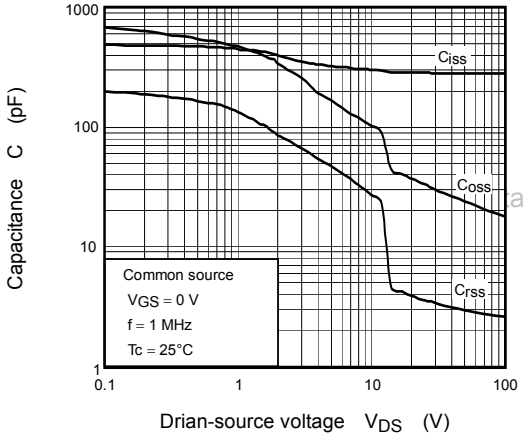
$R_{DS\ (ON)}$ – Tc



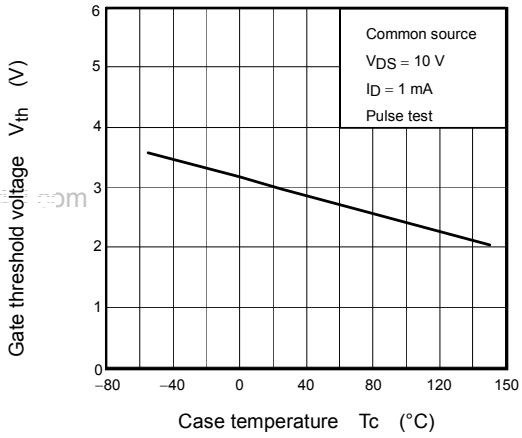
I_{DR} – V_{DS}



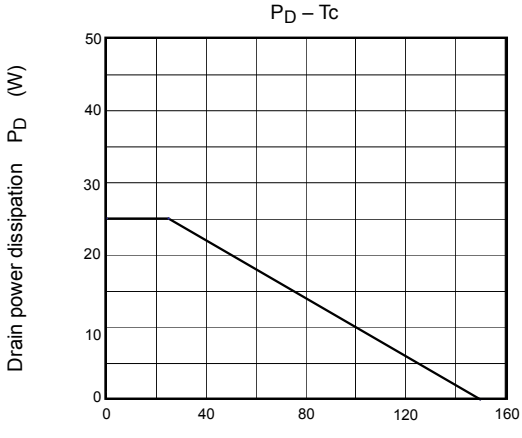
Capacitance – V_{DS}



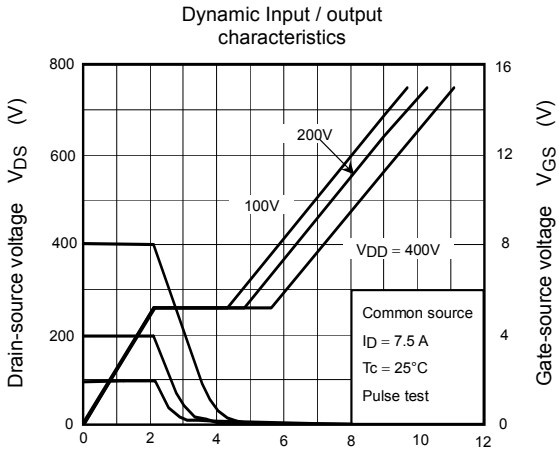
V_{th} – Tc



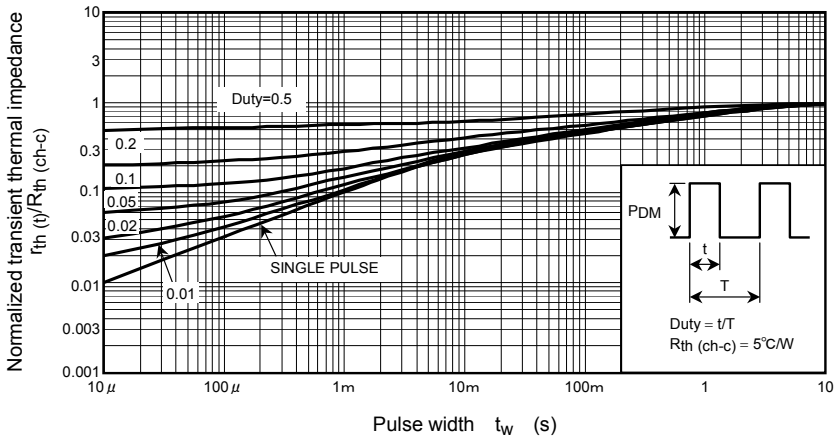
P_D – Tc



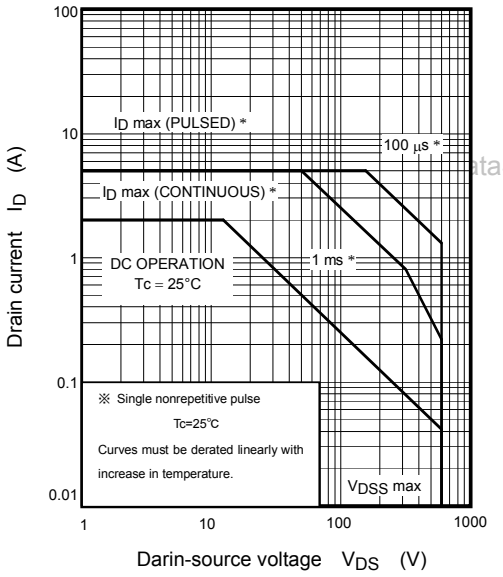
Dynamic Input / output characteristics



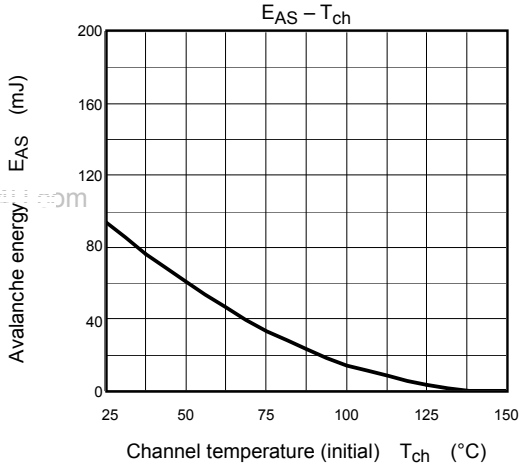
$r_{th} - t_w$

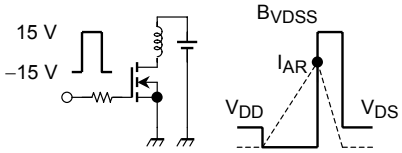


Safe operating area



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 41mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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