NN5118165A / NN5118165B series
EDO (Hyper Page) Mode
CMOS 1M × 16bit Dynamic RAM

NPNX

DESCRIPTION

The NN5118165A / NN5118165B series is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words by 16 bits. The NN5118165A / NN5118165B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN5118165A / NN5118165B series features an EDO (Hypar Page) mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 1024 address combinations of A0 to A9 during a 16 ms period.

Multiplexed address inputs permit the NN5118165A / NN5118165B series to be packaged in a standard 42-pin plastic SOJ.,50-pin plastic TSOP TYPE II. The package sizes provide high system bit densities . System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

FEATURES

- 1,048,576 × 16 bit Organization
- Single 5.0V ±10% Power Supply
- Performance Ranges

NN5118165A

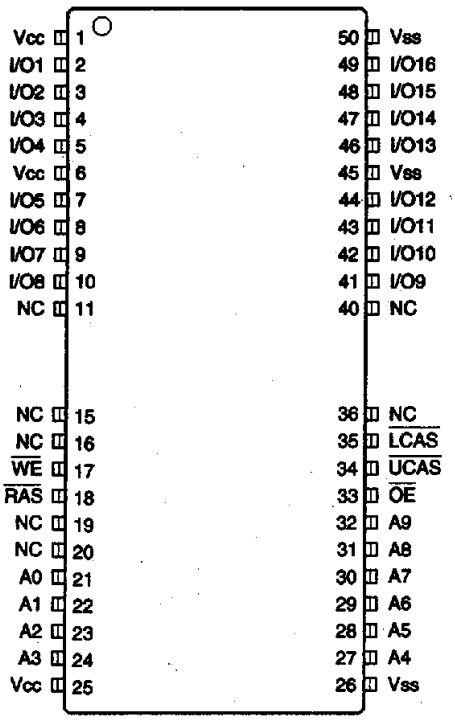
Parameter	-50	-60	-70
Max. $\overline{RAS}$ Access Time (t_{RAC})	50ns	60ns	70ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	30ns	35ns
Max. Read/Write Cycle Time (t_{RC})	100ns	110ns	130ns

NN5118165B

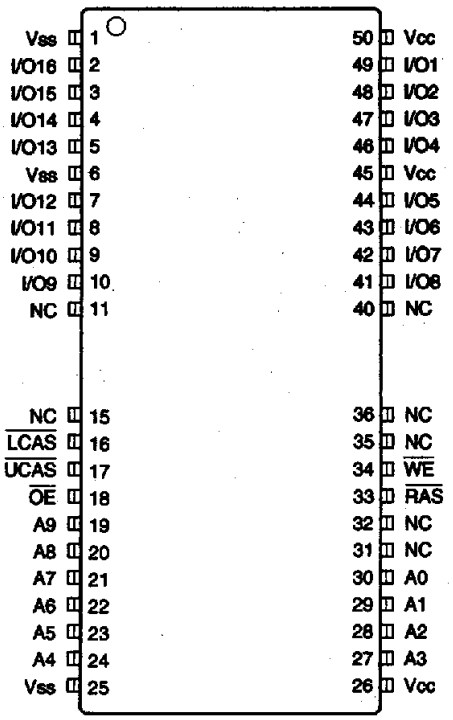
Parameter	-40	-50	-60
Max. $\overline{RAS}$ Access Time (t_{RAC})	40ns	50ns	60ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	11ns	13ns	15ns
Max. Column Address Access Time (t_{AA})	20ns	25ns	30ns
Min.Read/Write Cycle Time (t_{RC})	80ns	90ns	110ns

- EDO (Hyper Page) Mode Operation
- Separate $\overline{CAS}$ ($\overline{UCAS}$, $\overline{LCAS}$) for Byte Selection
- Byte Read/Write Mode Operation
- Low Power Operation
  Low Standby Current (CMOS level input)
  -Standard 1mA
  -L version 150µA
- 1024 Refresh Cycles
  -Standard 16ms
  -L version 128ms
- Self Refresh Mode
  (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
  $\overline{RAS}$ only
  $\overline{CAS}$ before $\overline{RAS}$
  Hidden Refresh
- High Reliability Package
  Plastic 42pin SOJ (P42SJ-2B-L)
  Plastic 50pin TSOP TYPE II (P50/44TP-3B-L)

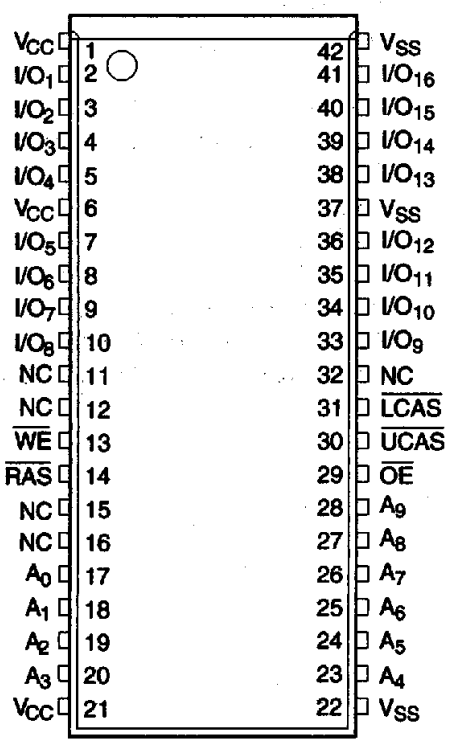
PIN CONFIGURATION



50/44-pin TSOP TYPE (II)
Normal Bend (400mil)
P50/44TP-3B-L



50/44-pin TSOP TYPE (II)
Reverse Bend (400mil)
P50/44TP-3B-L

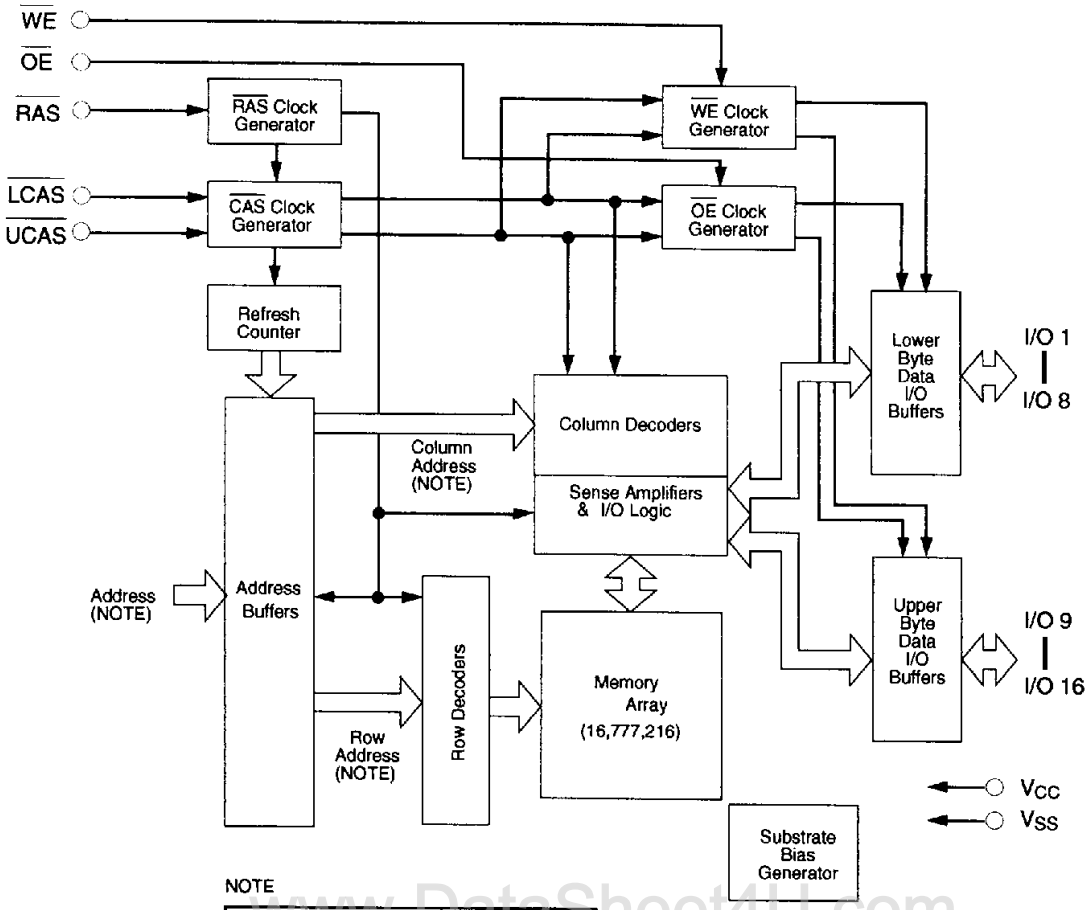


42-pin SOJ (400mil)
P42SJ-2B-L

PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe Upper Byte Control
$\overline{LCAS}$	Column Address Strobe Lower Byte Control
$\overline{OE}$	Output Enable
I/O1~I/O16	Data-in / Data-out
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



NOTE

Address / Row Address	Column Address
A0 - A9	A0 - A9

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin,Vout	−1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	−1 to 7	V
Storage Temperature (Plastic)	Tstg	−55 to +125	°C
Power Dissipation	Pd	1.0	W
Ambient Operating Temperature	Ta	0 to + 70	°C
Short Circuit Output Current	Iout	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	−1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

TRUTH TABLE

INPUTS					I / O		OPERATION	NOTES
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1~I/O8	I/O9~I/O16		
H	H	H	H	H	High-Z	High-Z	Standby	1,3
L	H	H	H	H	High-Z	High-Z	Refresh	1,3
L	L	H	H	L	Dout	High-Z	Lower byte read	1,3
L	H	L	H	L	High-Z	Dout	Upper byte read	1,3
L	L	L	H	L	Dout	Dout	Word read	1,3
L	L	H	L	H	Din	Don't care	Lower byte write	1,2,3
L	H	L	L	H	Don't care	Din	Upper byte write	1,2,3
L	L	L	L	H	Din	Din	Word write	1,2,3
L	L	L	H	H	High-Z	High-Z		1,3
H→L	L	H	H	—	High-Z	High-Z	CBR refresh or Self refresh	1,3
H→L	H	L	H	—	High-Z	High-Z		
H→L	L	L	H	—	High-Z	High-Z		

Notes: 1. H:high (inactive) , L:low (active) , —:unconcerned with H or L.
2. $t_{WCS} \geq 0$ns : early write mode.
$t_{WCS} < 0$ns : $\overline{OE}$ controlled write mode.
3. Operation mode is set by the earliest of LCAS and UCAS active edge and reset by the latest of $\overline{LCAS}$ and $\overline{UCAS}$ inactive edge.
However write operation and High-Z control are done independently by each $\overline{LCAS}$,$\overline{UCAS}$.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%) (NN5118165A)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-50 -60 -70		190 170 150	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			150	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-50 -60 -70		190 170 150	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	EDO (Hyper Page) Mode Current	-50 -60 -70		120 110 100	mA mA mA	t_{HPC} = t_{HPC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1,2
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-50 -60 -70		190 170 150	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1
I_{CC6}	Refresh Current (L version : $\overline{CAS}$ before $\overline{RAS}$ refresh)			500	µA	1024 cycles / 128ms t_{RAS} ≤ 200ns, WE ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current (L version)			300	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\|I_{LI}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min.), $\overline{CAS}$ ≥ V_{IH}(min.) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A9)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1 ~ I/O16	—	7	pF

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%) (NN5118165B)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-40 -50 -60		200 180 160	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			150	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-40 -50 -60		200 180 160	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	EDO (Hyper) Page Mode Current	-40 -50 -60		130 120 110	mA mA mA	t_{HPC} = t_{HPC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1,2
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-40 -50 -60		200 180 160	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1
I_{CC6}	Refresh Current $\overline{CAS}$ before $\overline{RAS}$ refresh)			500	µA	1,024 cycles / 128ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current			300	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\|I_{L1}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min), $\overline{CAS}$ ≥ V_{IH}(min) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A9)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1~I/O16	—	7	pF

AC ELECTRICAL CHARACTERISTICS (NN5118165A)

Test conditions : V_{IH} / V_{IL} = 2.4V / 0.8V V_{OH} / V_{OL} = 2.4V / 0.4V output loading C_L = 100pF + 2TTL

Operating conditions : (0 °C≤Ta≤70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5, 17)

NO.	NOTES		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	35	—	45	—	55	—	ns	
6	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	8	100K	10	100K	15	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	—	37	—	42	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	7	—	10	—	12	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	13	—	18	—	23	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	35	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	39	—	47	—	54	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	10	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	15	—	15	—	20	ns	
25	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	20	—	ns	
26	t_{GH2GL2}	t_{OPZ}	$\overline{OE}$ Pulse Width for Output Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	$\overline{OE}$ Setup Time to $\overline{CAS}$ High	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	$\overline{OE}$ Setup Time to $\overline{RAS}$ High	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	10	—	10	—	ns	
30	t_{GL2QX}	t_{OLZ}	$\overline{OE}$ to Output in low-Z	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	15	0	15	ns	10
32	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	10	0	15	0	15	ns	
33	t_{RHQZ}	t_{OFR}	Output Buffer Turn-off Delay Time Referenced to $\overline{RAS}$	0	13	0	15	0	15	ns	16
34	t_{WL2QZ}	t_{WEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{WE}$	0	13	0	15	0	15	ns	

NO.	SYMBOL		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	15	—	15	—	20	—	ns	
36	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
37	t_{CH2RH1}	t_{RHCP}	$\overline{RAS}$ Hold Time Referenced $\overline{CAS}$ Precharge	30	—	35	—	40	—	ns	
38	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	30	—	40	—	ns	
39	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	100	—	110	—	130	—		
40	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	100K	60	100K	70	100K	ns	
41	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	µs	
42	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO (Hyper Page) Mode)	50	100K	60	100K	70	100K	ns	
43	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	13	35	13	45	13	50	ns	6
44	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	ns	
45	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	23	11	30	11	35	ns	7
46	t_{RL2QX}	t_{RLZ}	$\overline{RAS}$ To Output in Low-Z	0	—	0	—	0	—	ns	
47	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	64	—	77	—	89	—	ns	11
48	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
49	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	9
50	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
51	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	100	—	110	—	130	—	ns	
52	t_{CL2CL2}	t_{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	20	—	25	—	30	—	ns	13,14
53	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	120	—	140	—	160	—	ns	
54	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	55	—	65	—	75	—	ns	13,14
55	t_{REF}	t_{REF}	Refresh Period	—	16	—	16	—	16	ms	15
56	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	10	—	10	—	ns	
57	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
58	t_T	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	4,5
59	t_{WL1WH1}	t_{WPZ}	$\overline{WE}$ Pulse Width for Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
60	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	10	—	15	—	ns	
61	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
62	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
63	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	15	—	20	—	ns	
64	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	15	—	20	—	ns	
65	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	10	—	10	—	10	—	ns	
66	t_{RL1WH2}	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	10	—	10	—	10	—	ns	

AC ELECTRICAL CHARACTERISTICS (NN5118165B)

Test conditions : V_{IH} / V_{IL} = 2.4V / 0.8V V_{OH} / V_{OL} = 2.4V / 0.4V output loading C_L = 100pF + 2TTL

Operating conditions : (0 °C≤Ta≤70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

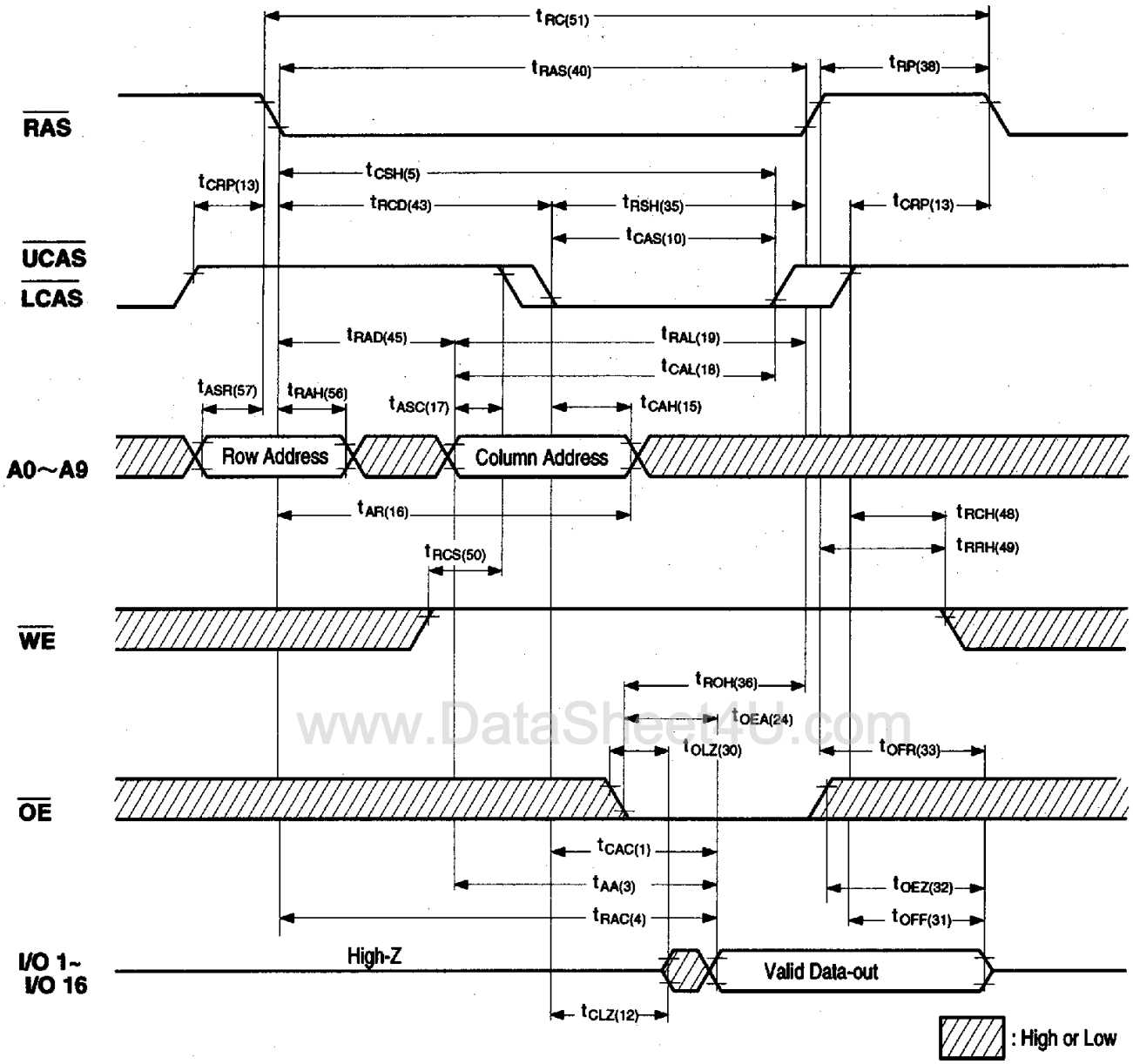
NO.	NOTES		PARAMETER	-40		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	11	—	13	—	15	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	25	—	30	—	35	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	20	—	25	—	30	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	40	—	50	—	60	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	30	—	35	—	40	—	ns	
6	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	7	—	7	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	8	100K	8	100K	10	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	—	32	—	37	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	7	—	7	—	10	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	30	—	35	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to CAS Lead Time	10	—	13	—	18	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	39	—	39	—	47	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	7	—	7	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	11	—	13	—	15	ns	
25	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	13	—	15	—	ns	
26	t_{GH2GL2}	t_{OPZ}	$\overline{OE}$ Pulse Width for Output Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	OE Setup Time to $\overline{CAS}$ High	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	$\overline{OE}$ Setup Time to $\overline{RAS}$ High	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	15	—	15	—	ns	
30	t_{GL2QX}	t_{OLZ}	$\overline{OE}$ to Output in low-Z	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	15	ns	10,17
32	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	13	0	13	0	15	ns	
33	t_{RHQZ}	t_{OFR}	Output Buffer Turn-off Delay Time Referenced to $\overline{RAS}$	0	13	0	13	0	15	ns	16
34	t_{WL2QZ}	t_{WEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{WE}$	0	13	0	13	0	15	ns	

NO.	SYMBOL		PARAMETER	-40		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	10	—	13	—	15	—	ns	
36	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
37	t_{CH2RH1}	t_{RHCP}	$\overline{RAS}$ Hold Time Referenced $\overline{CAS}$ Precharge	25	—	30	—	35	—	ns	
38	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	25	—	30	—	ns	
39	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	72	—	90	—	110	—	ns	
40	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	40	100K	50	100K	60	100K	ns	
41	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	µs	
42	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO (Hyper Page) Mode)	40	100K	50	100K	60	100K	ns	
43	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	27	13	35	13	45	ns	6
44	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	
45	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	9	25	11	25	11	30	ns	7
46	t_{RL2QX}	t_{RLZ}	$\overline{RAS}$ To Output in Low-Z	0	—	0	—	0	—	ns	
47	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	—	64	—	77	—	ns	11
48	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
49	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	9
50	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
51	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	80	—	90	—	110	—	ns	
52	t_{CL2CL2}	t_{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	16	—	20	—	25	—	ns	13,14
53	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	110	—	120	—	140	—	ns	
54	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	52	—	55	—	65	—	ns	13,14
55	t_{REF}	t_{REF}	Refresh Period	—	16	—	16	—	16	ms	15
56	t_{RL1AX}	t_{RAH}	Row Address Hold Time	6	—	8	—	8	—	ns	
57	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
58	t_T	t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4,5
59	t_{WL1WH1}	t_{WPZ}	$\overline{WE}$ Pulse Width for Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
60	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	7	—	10	—	10	—	ns	
61	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	7	—	10	—	10	—	ns	
62	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
63	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	7	—	10	—	ns	
64	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	—	7	—	10	—	ns	
65	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
66	t_{RL1WH2}	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time	10	—	10	—	10	—	ns	

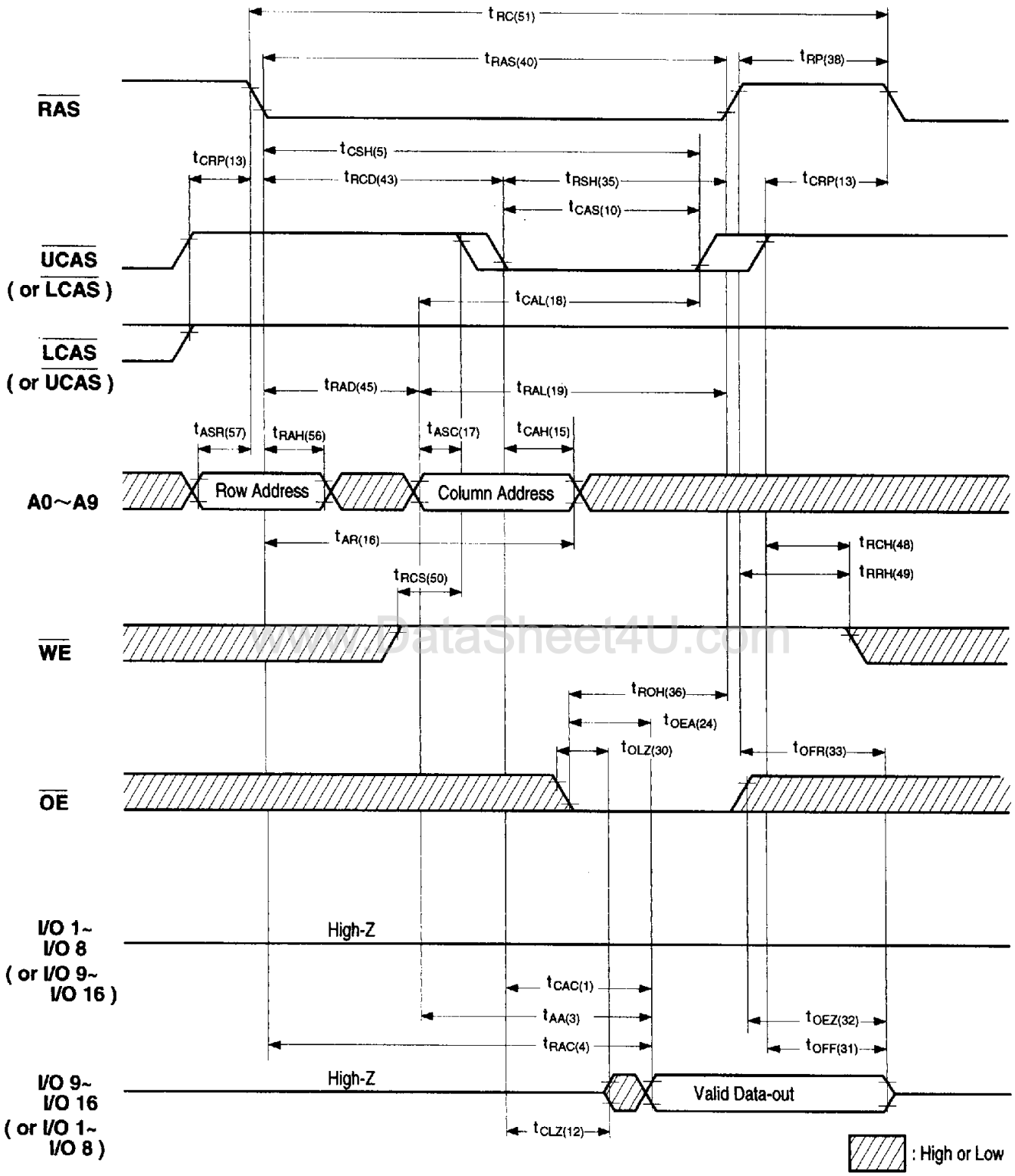
Notes:

3. Eight Initialization Cycles are required following a 200µs pause after Power Up.
   These Initialization Cycles may consist of one of the following : $\overline{RAS}$ only refresh Cycles, Read Cycles, Write Cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh Cycles.
4. AC measurements assume t_T=3ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 100pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
8. Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. t_{REF}=128msec for Long Refresh version (L version).
16. t_{OFR} applies only when $\overline{CAS}$ is high.
17. V_{OH}=2.0V and V_{OL}=0.8V are reference levels for measuring EDO mode.(NN5118165A)

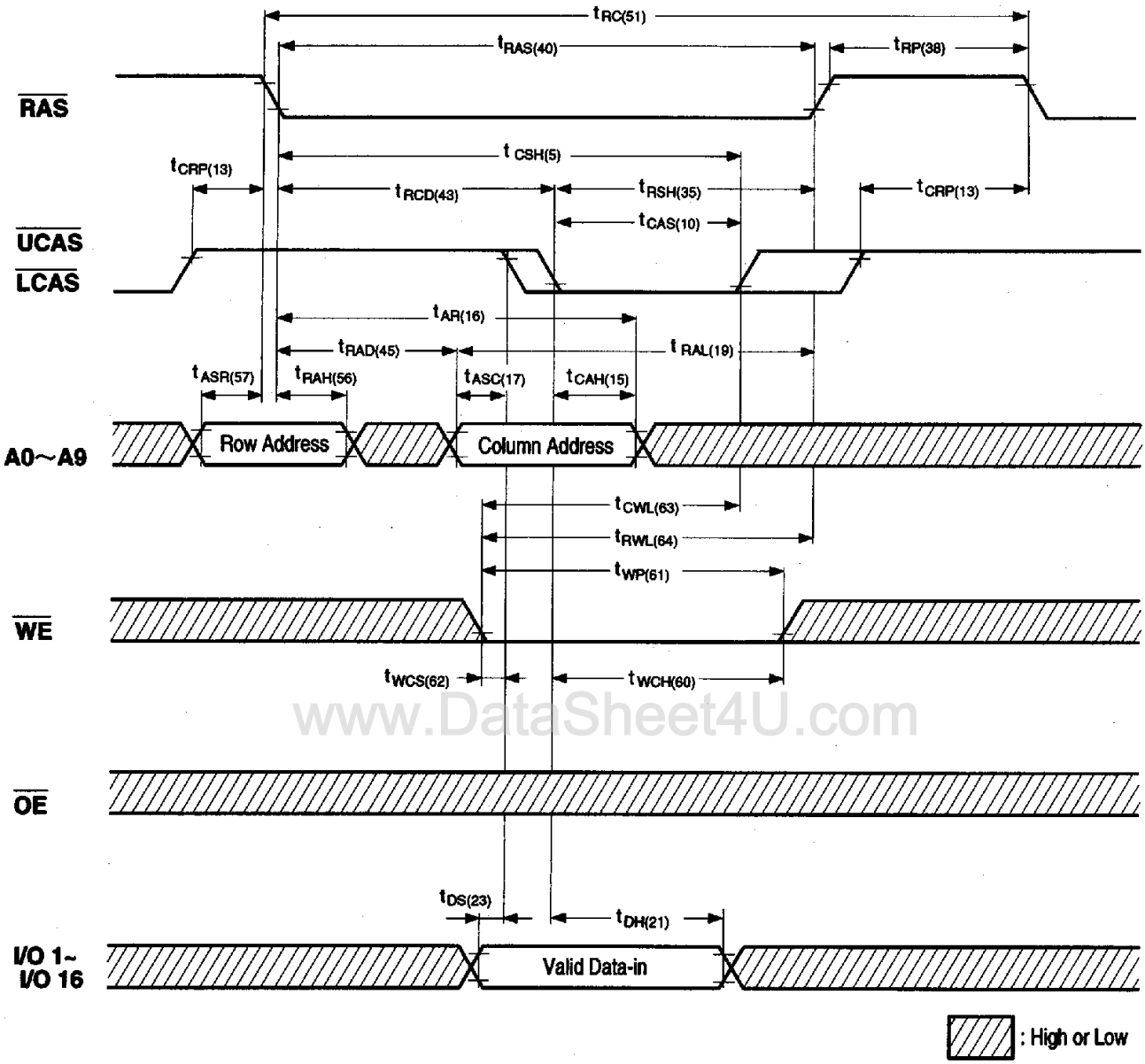
WORD READ CYCLE



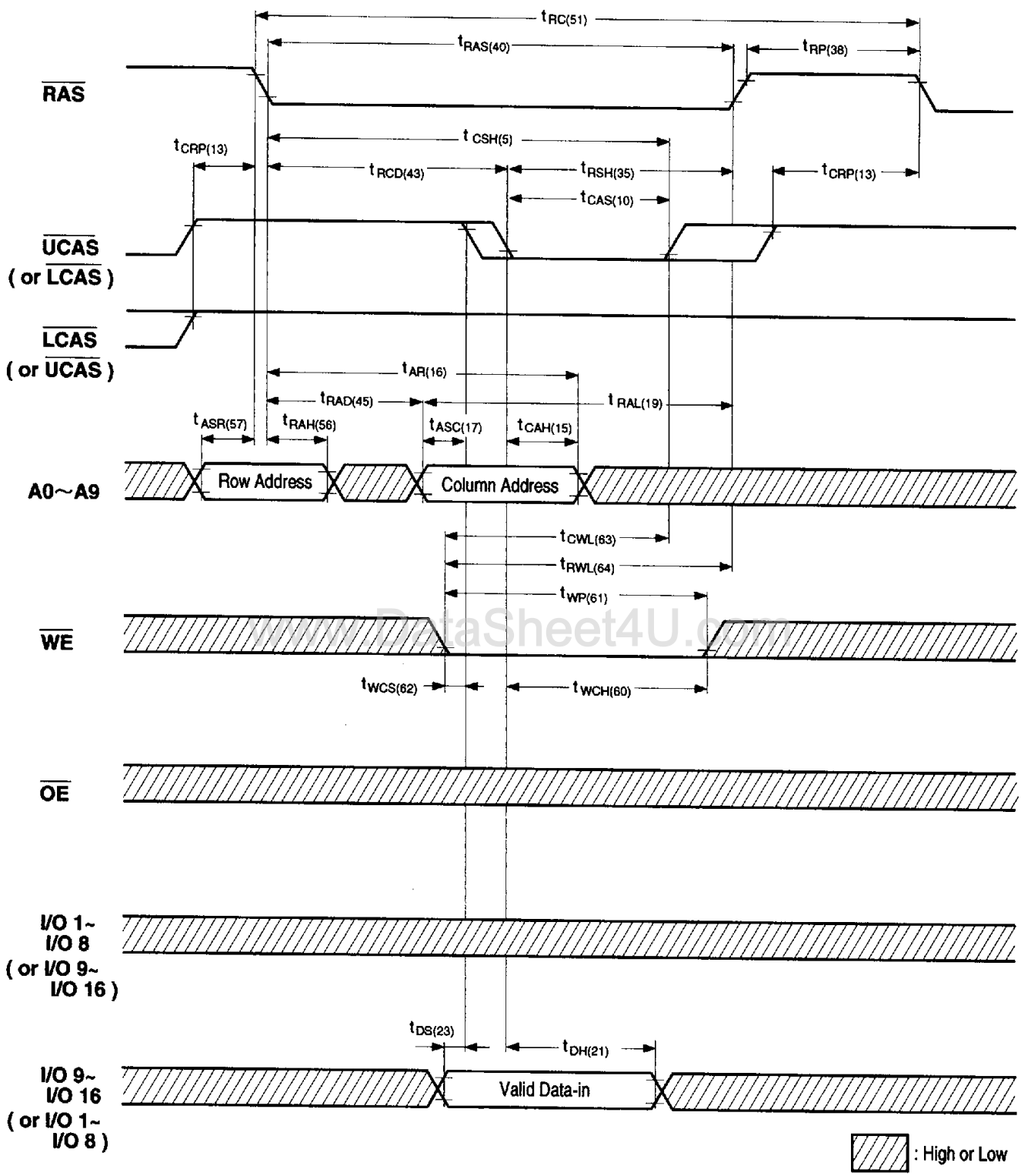
BYTE READ CYCLE



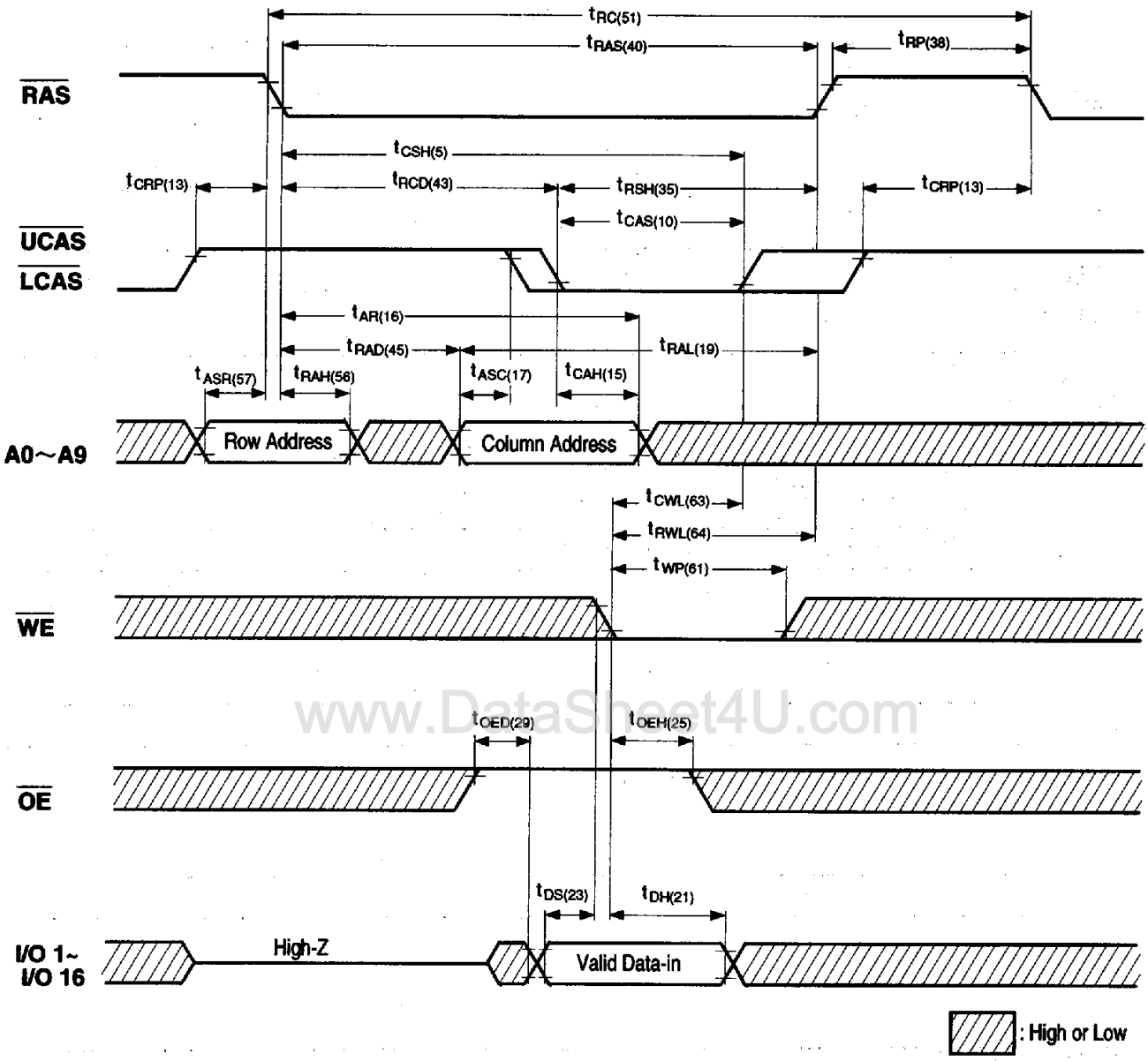
WORD WRITE CYCLE (EARLY WRITE)



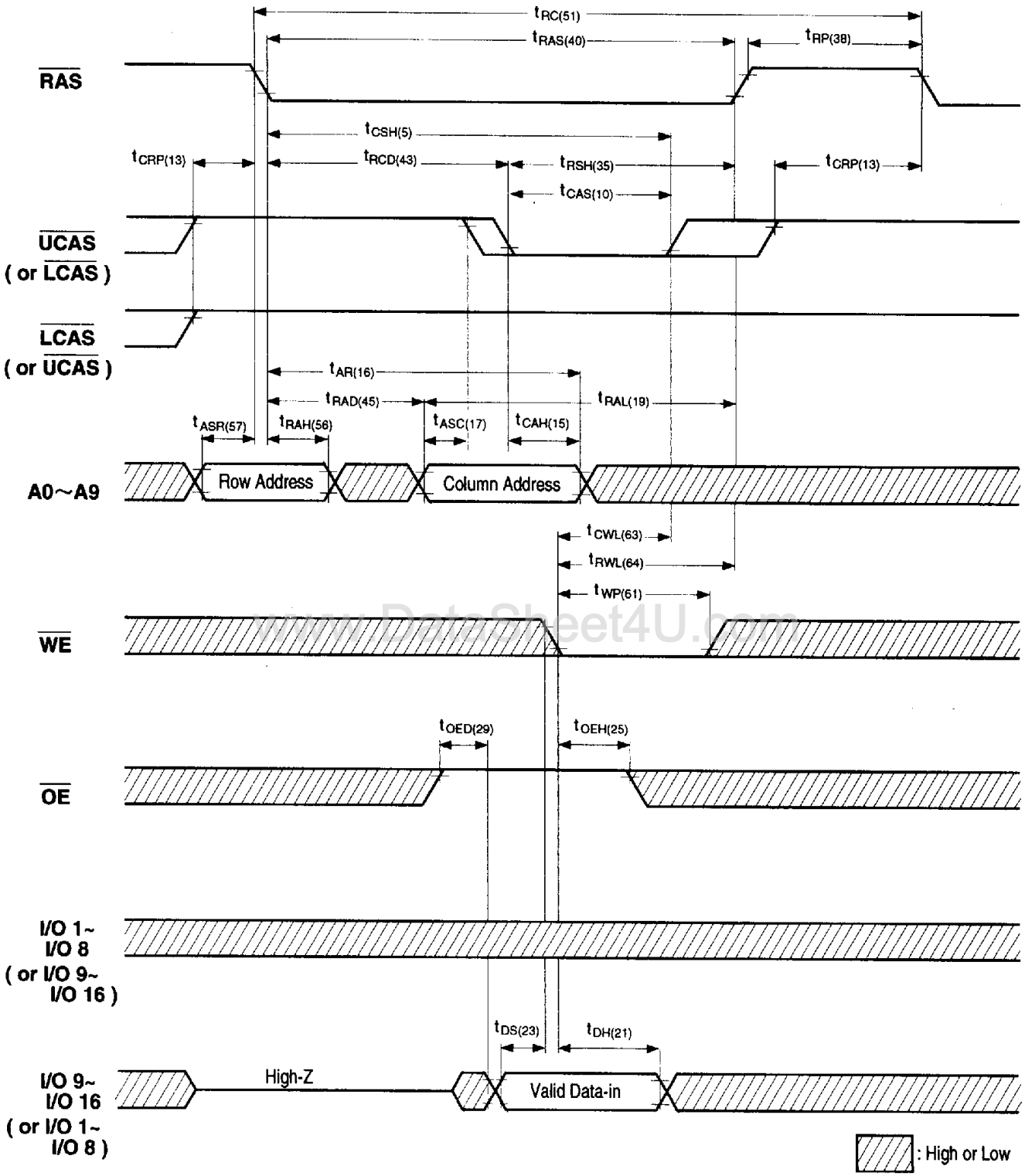
BYTE WRITE CYCLE (EARLY WRITE)



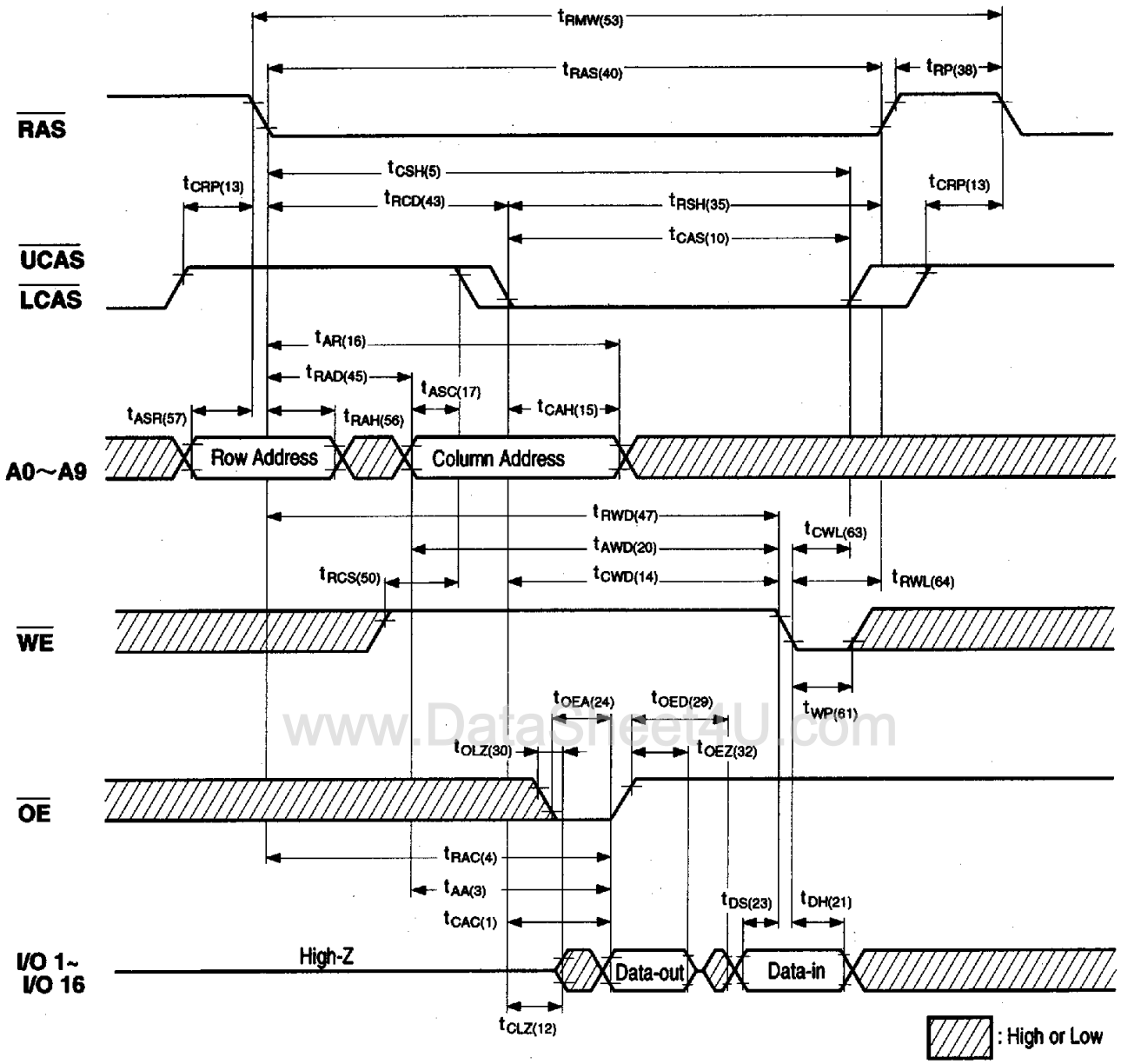
WORD WRITE CYCLE ($\overline{OE}$-CONTROLLED WRITE)



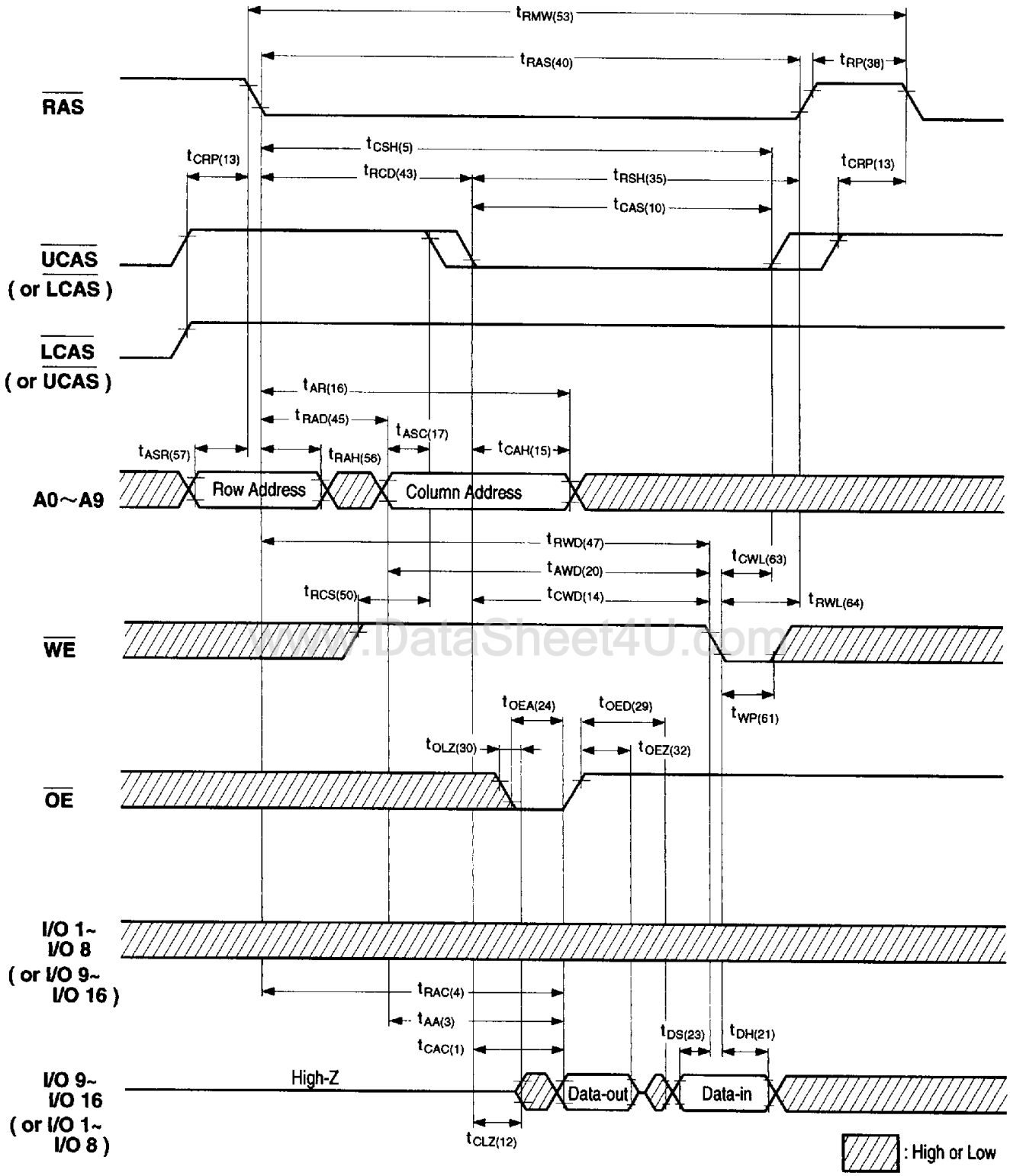
BYTE WRITE CYCLE (OE-CONTROLLED WRITE)



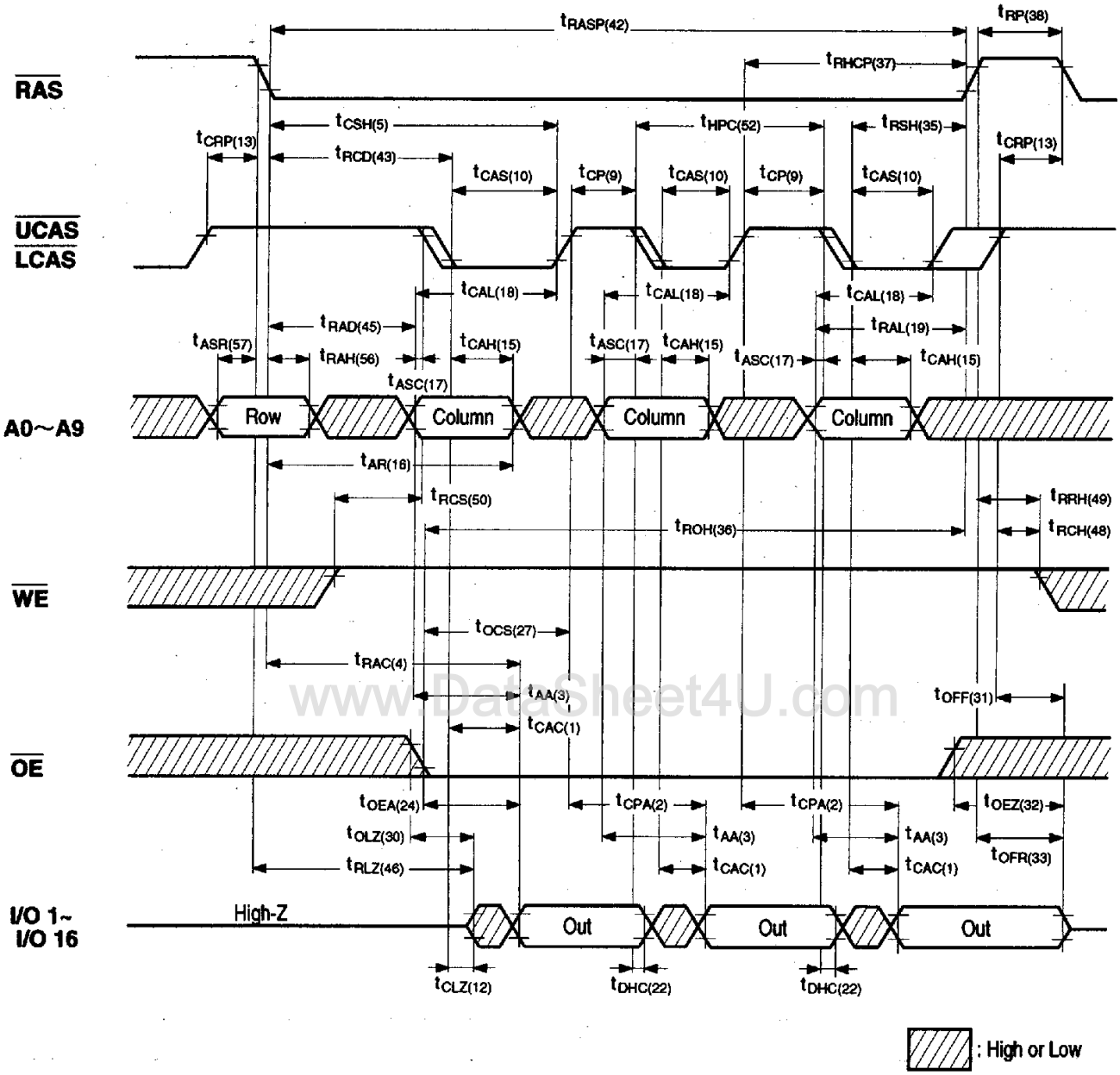
WORD READ-MODIFY-WRITE CYCLE



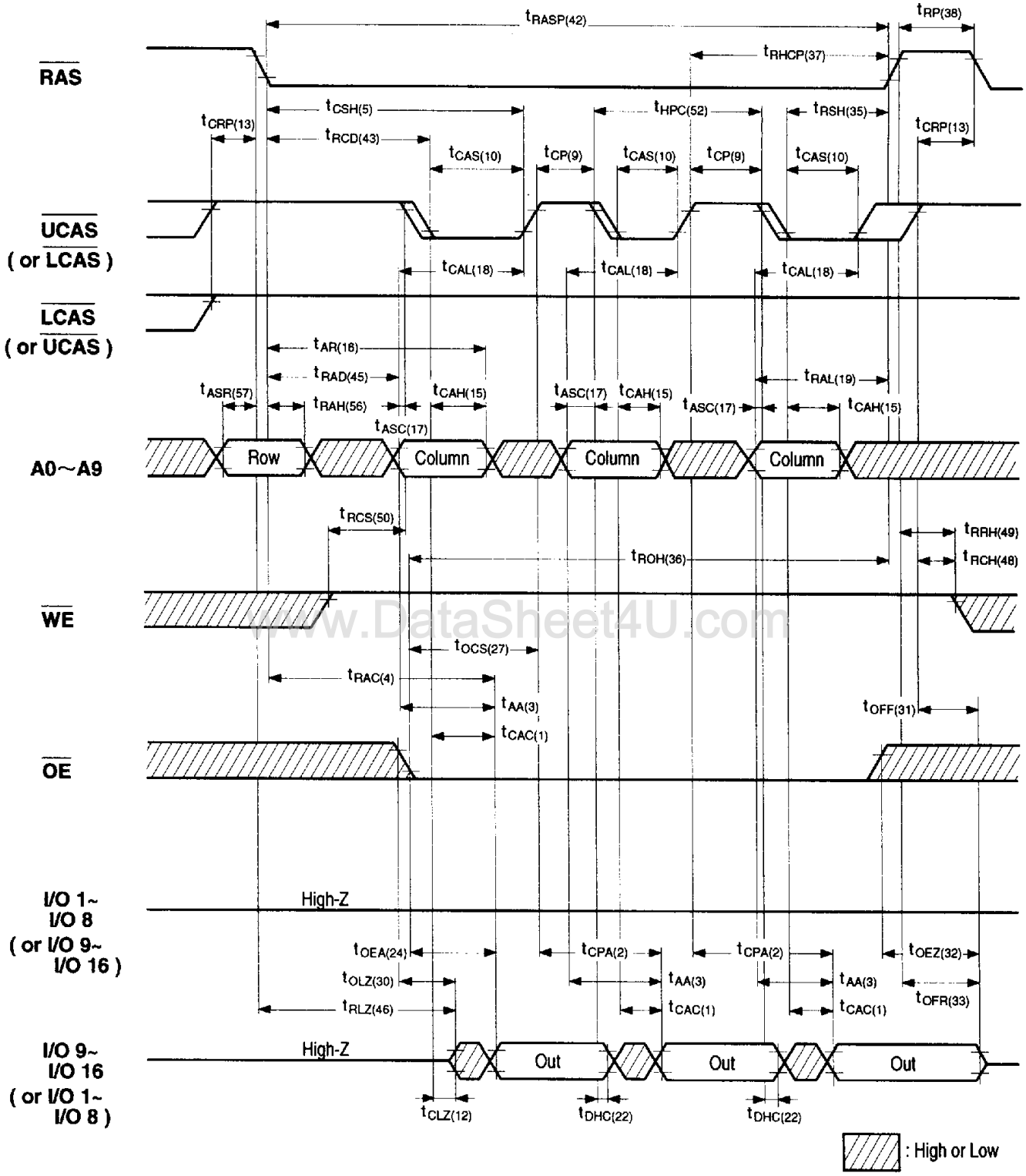
BYTE READ-MODIFY-WRITE CYCLE



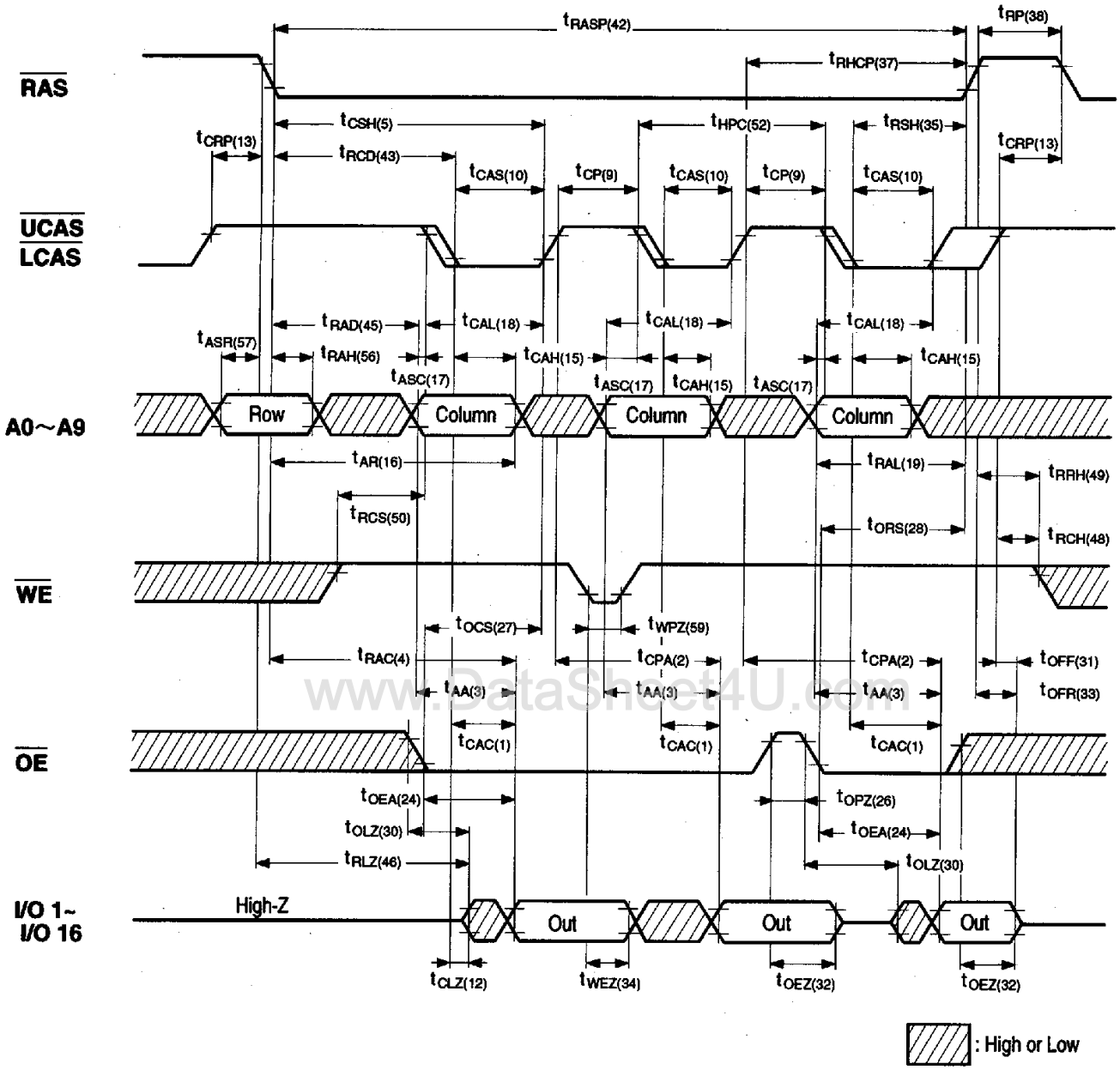
EDO (HYPER PAGE) MODE WORD READ CYCLE



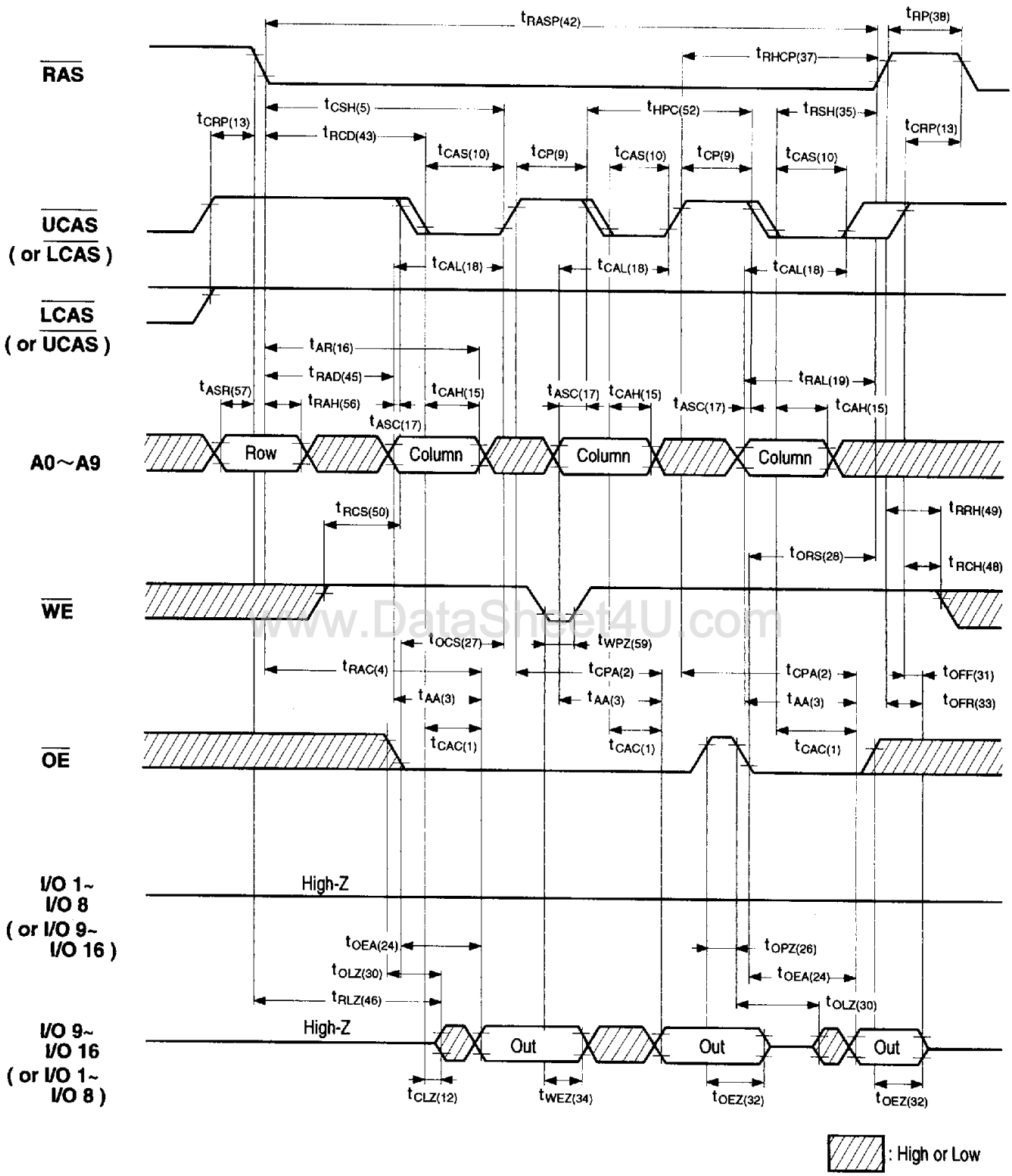
EDO (HYPER PAGE) MODE BYTE READ CYCLE



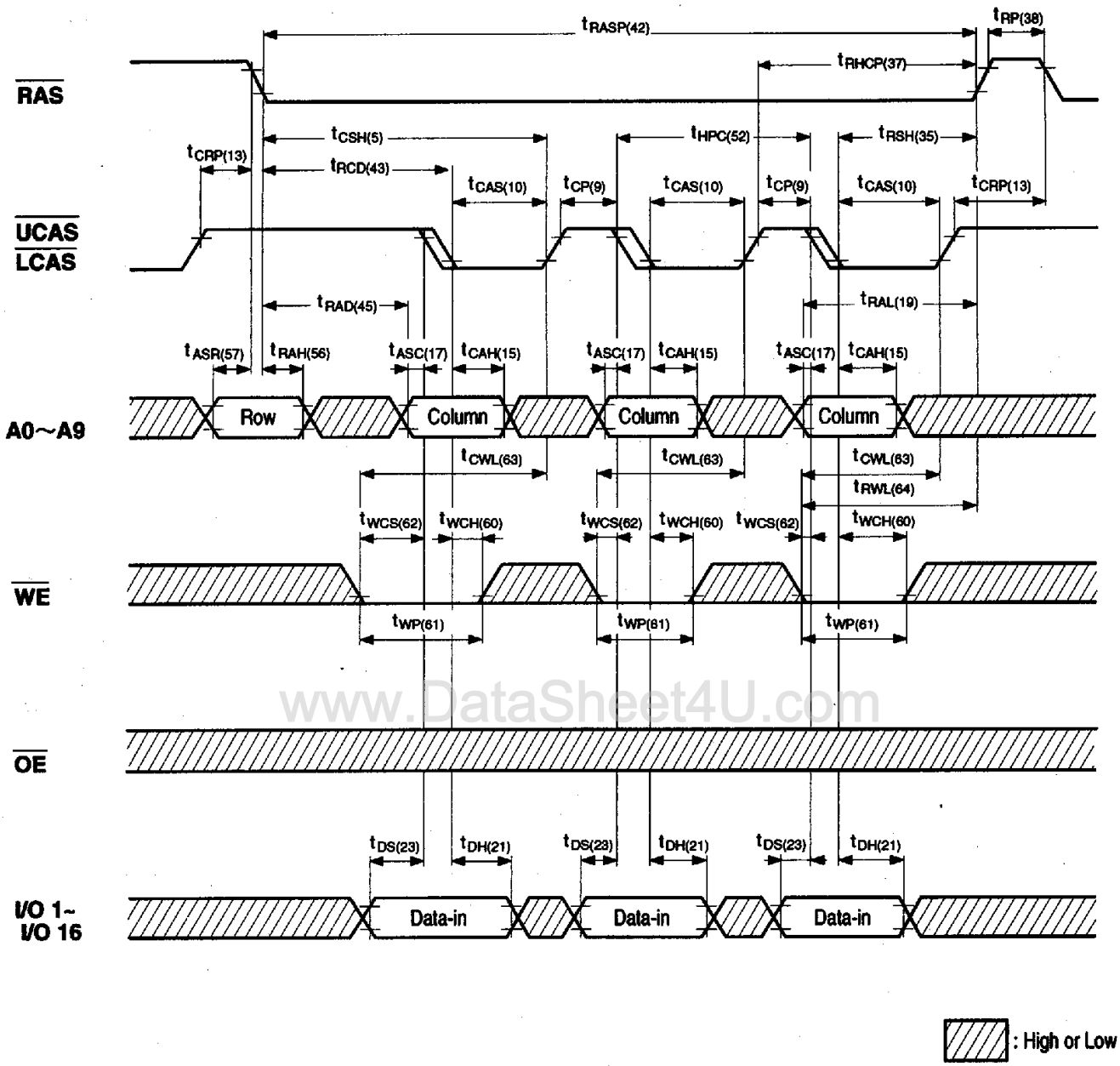
EDO (HYPER PAEGE) MODE WORD READ CYCLE ($\overline{OE}$ AND $\overline{WE}$ CONTROLLED OUTPUT)



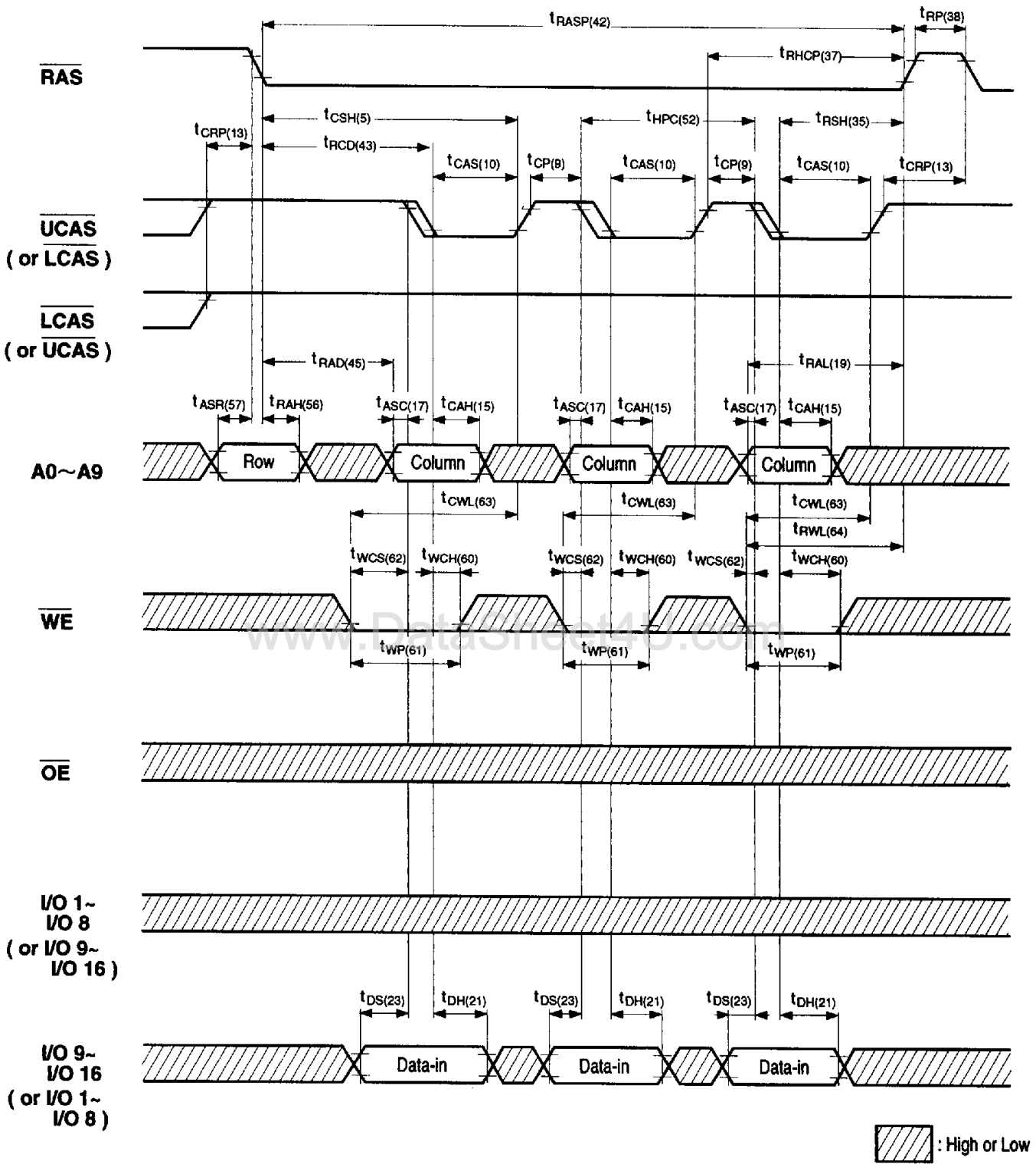
EDO (HYPER PAGE) MODE BYTE READ CYCLE ($\overline{OE}$ AND $\overline{WE}$ CONTROLLED OUTPUT)



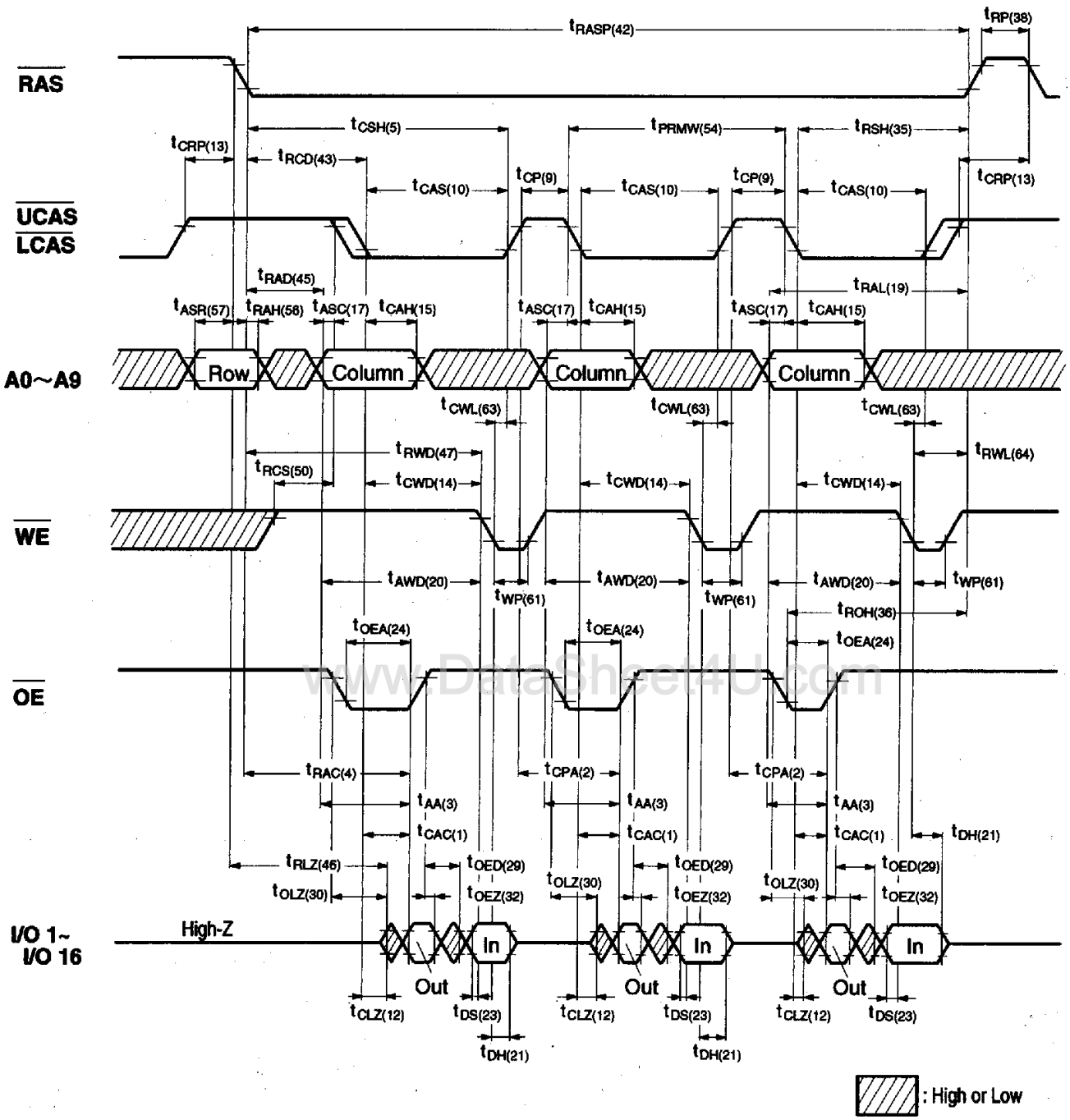
EDO (HYPER PAGE) MODE EARLY WORD WRITE CYCLE



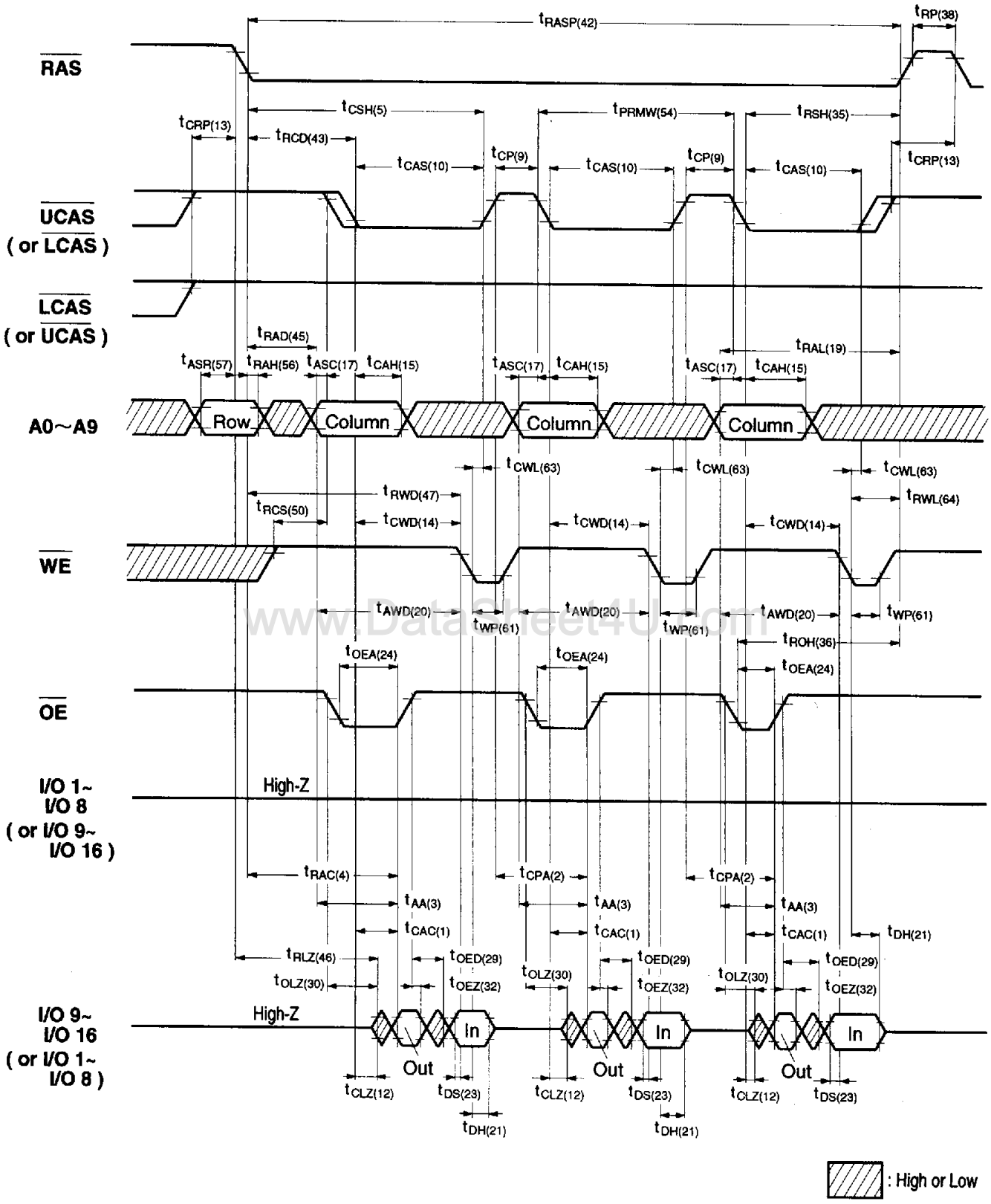
EDO (HYPER PAGE) MODE EARLY BYTE WRITE CYCLE



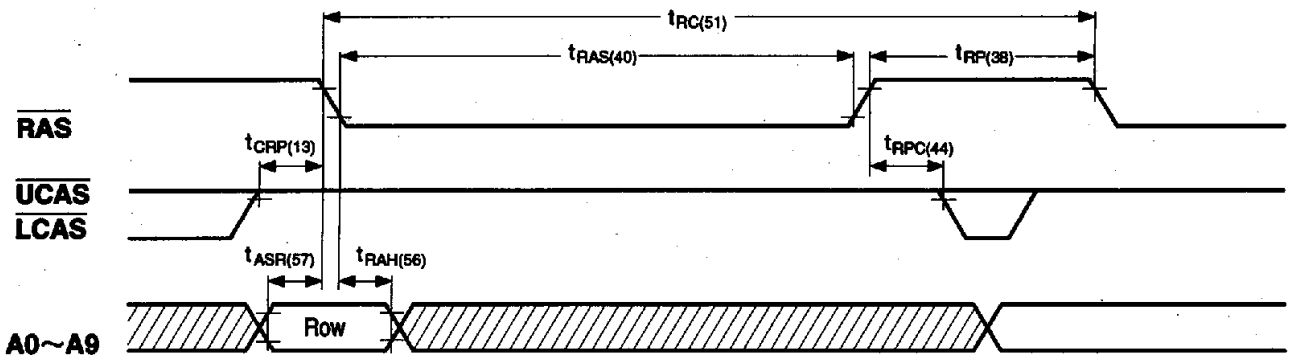
EDO (HYPER PAGE) MODE WORD READ-MODIFY-WRITE CYCLE



EDO (HYPER PAGE) MODE BYTE READ-MODIFY-WRITE CYCLE

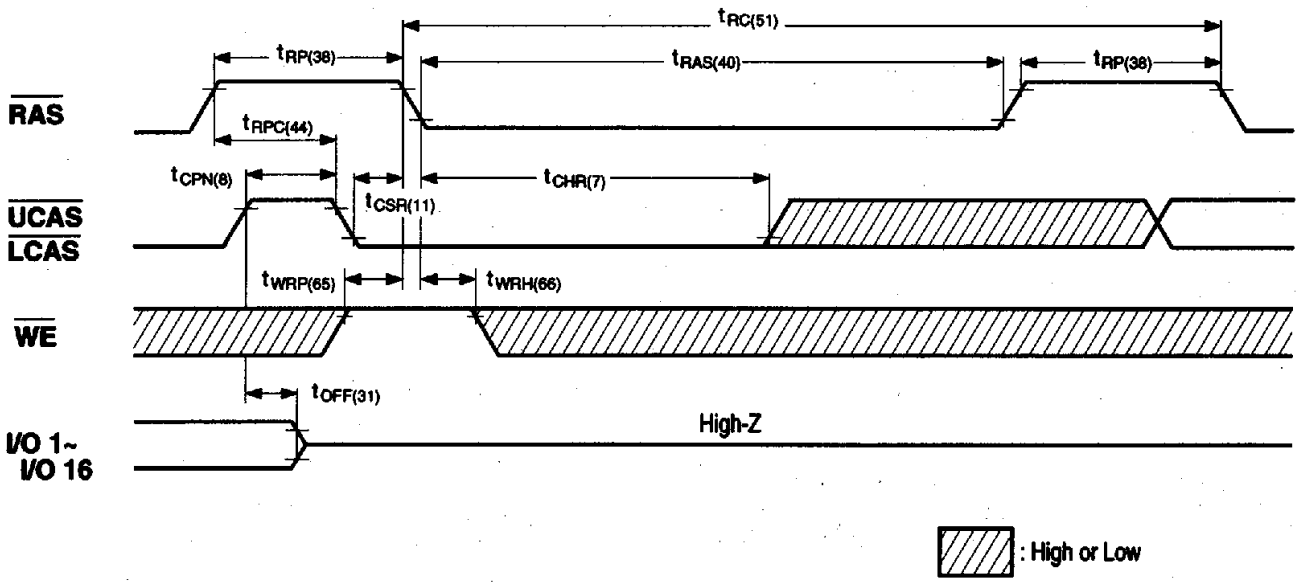


$\overline{RAS}$ ONLY REFRESH CYCLE



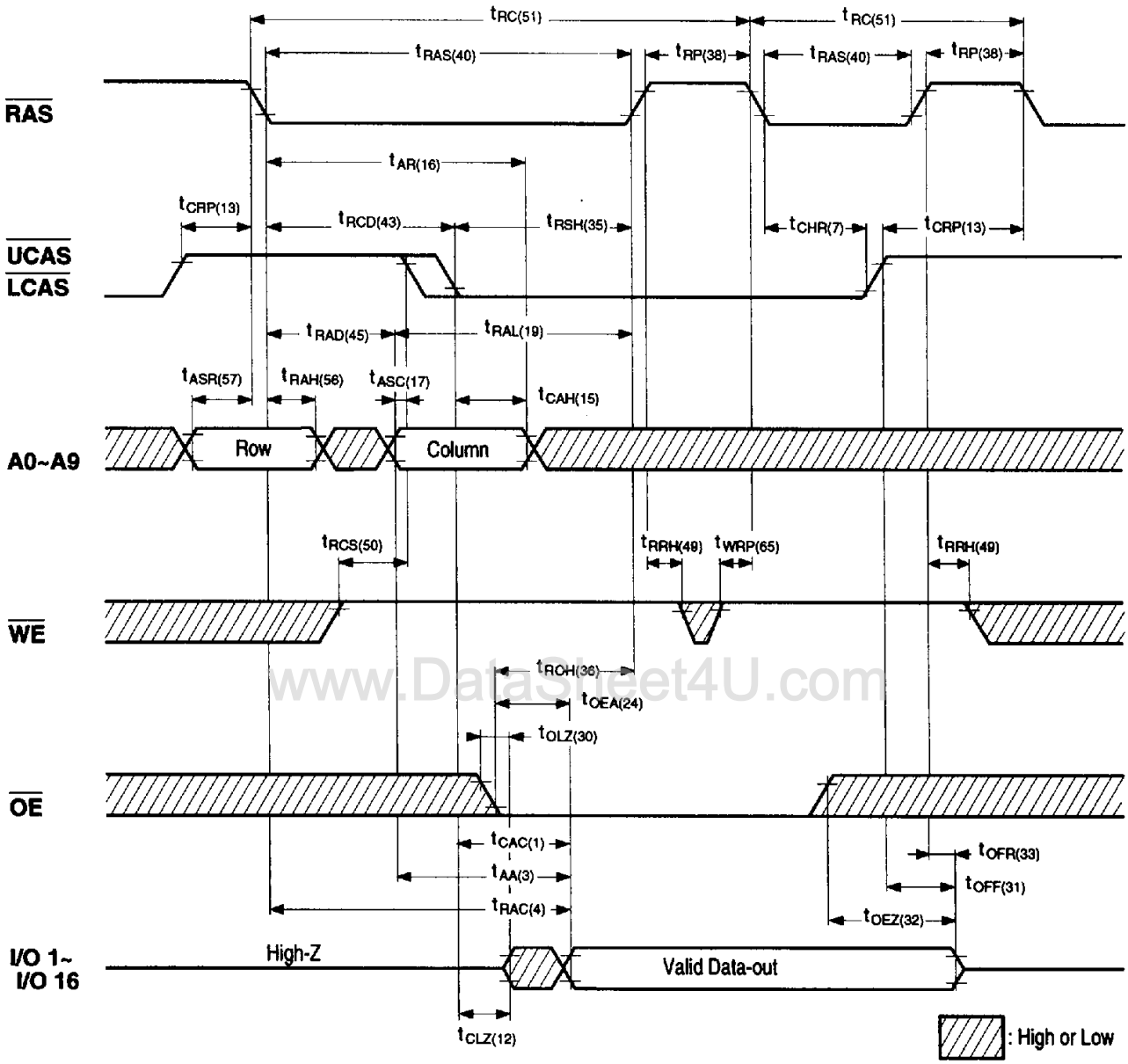
Note : $\overline{WE}$, $\overline{OE}$ = Don't care.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

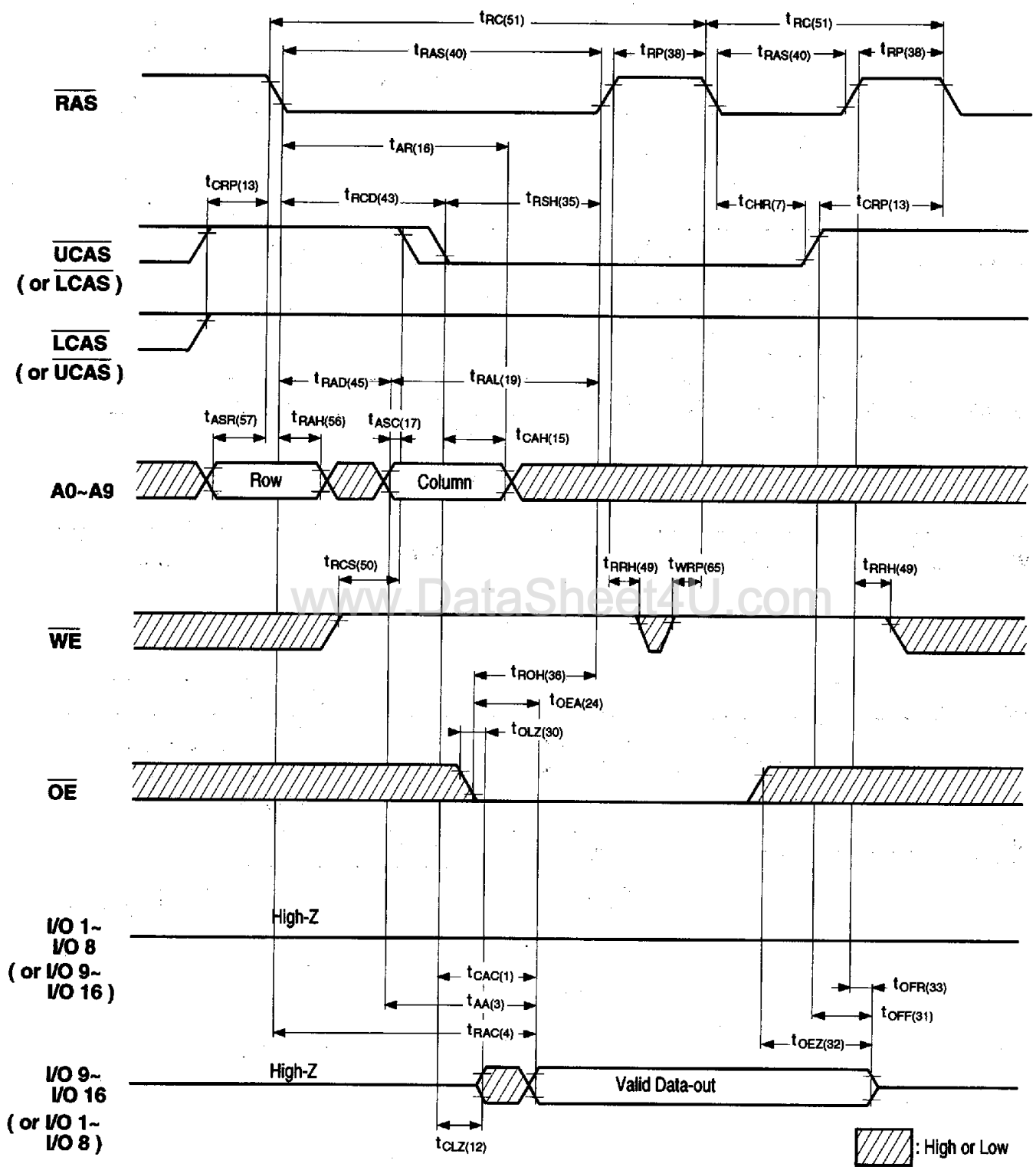


Note: $\overline{OE}$, A0~A9 = Don't care.

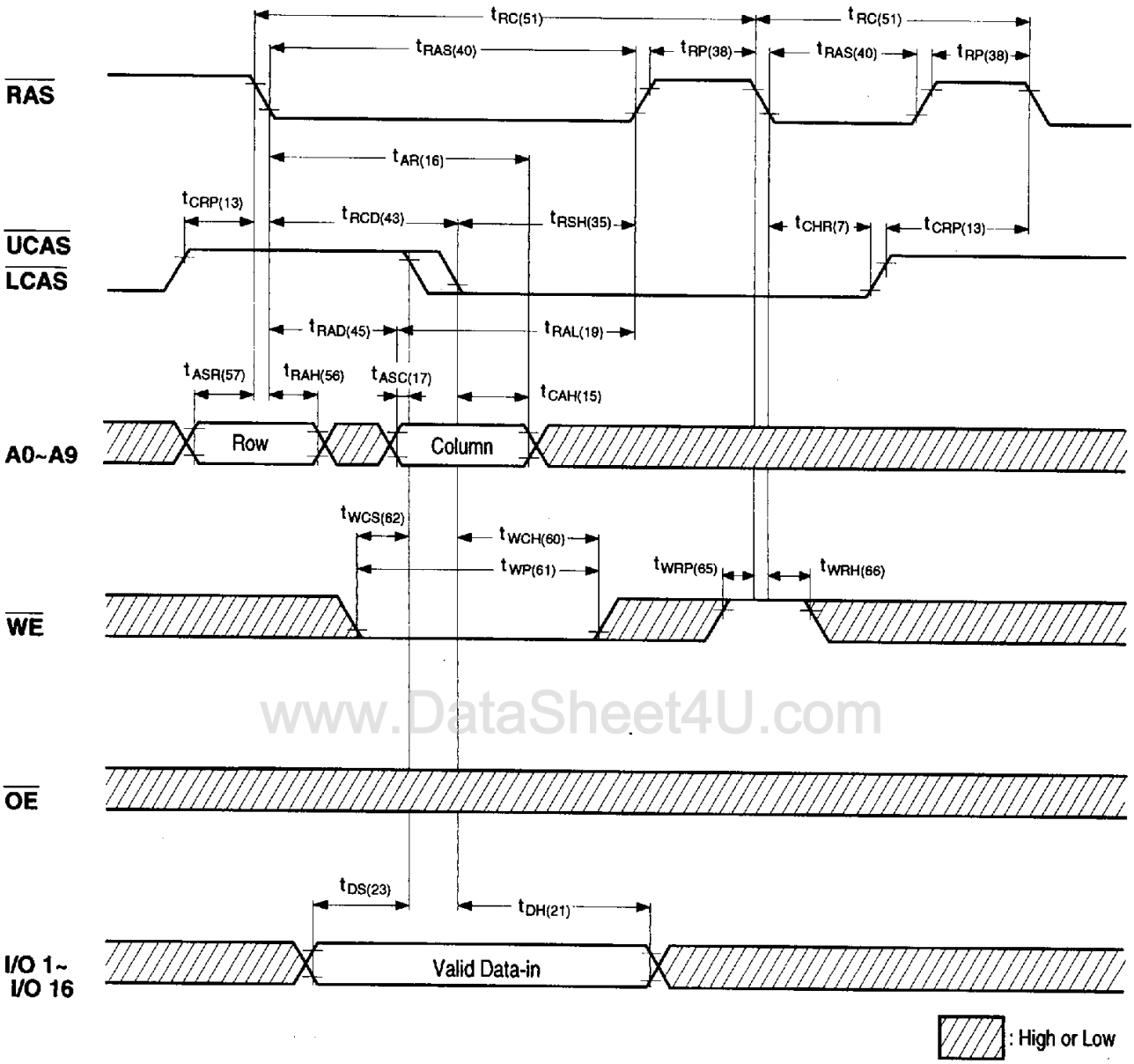
HIDDEN REFRESH CYCLE (WORD READ)



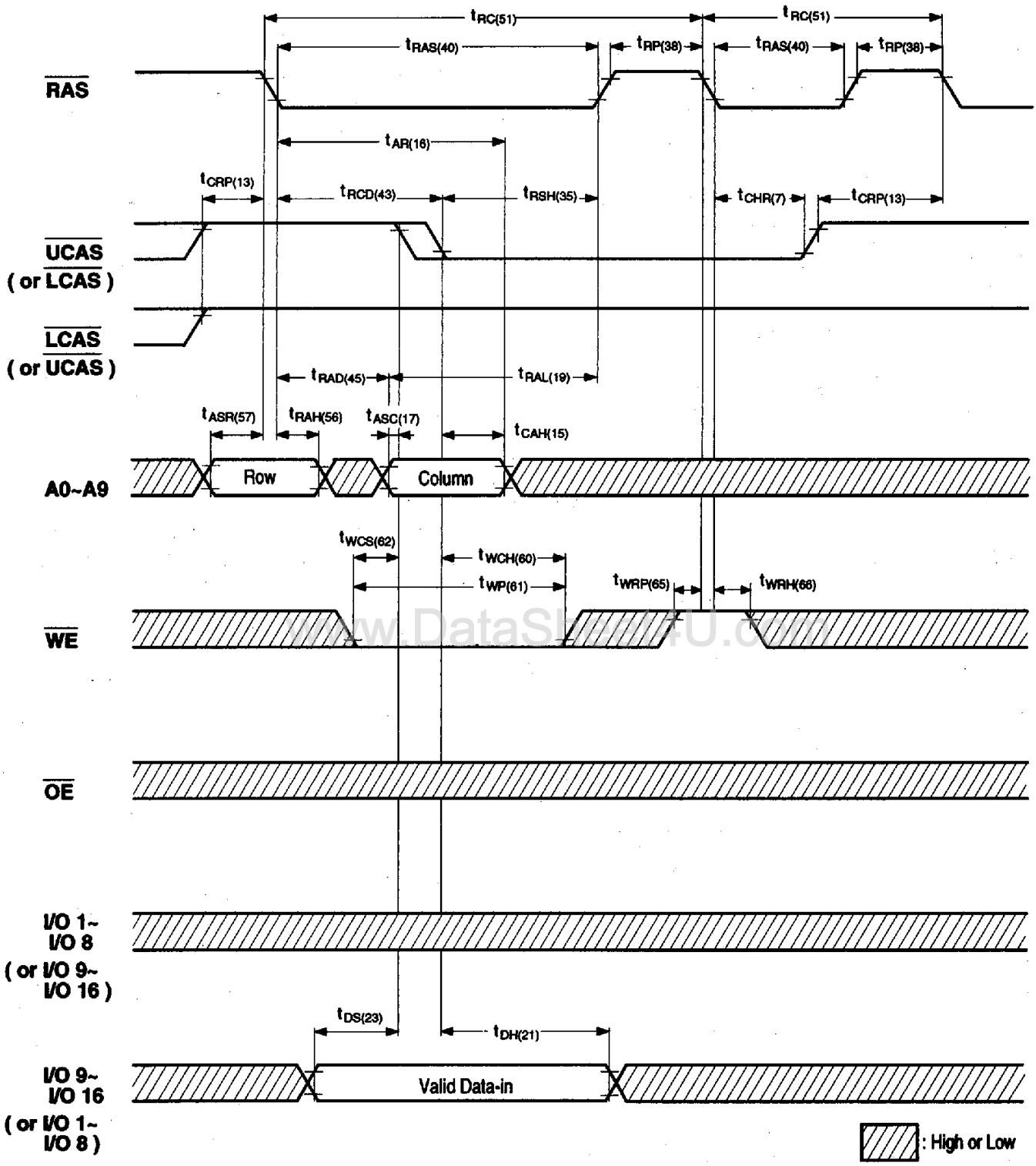
HIDDEN REFRESH CYCLE (BYTE READ)



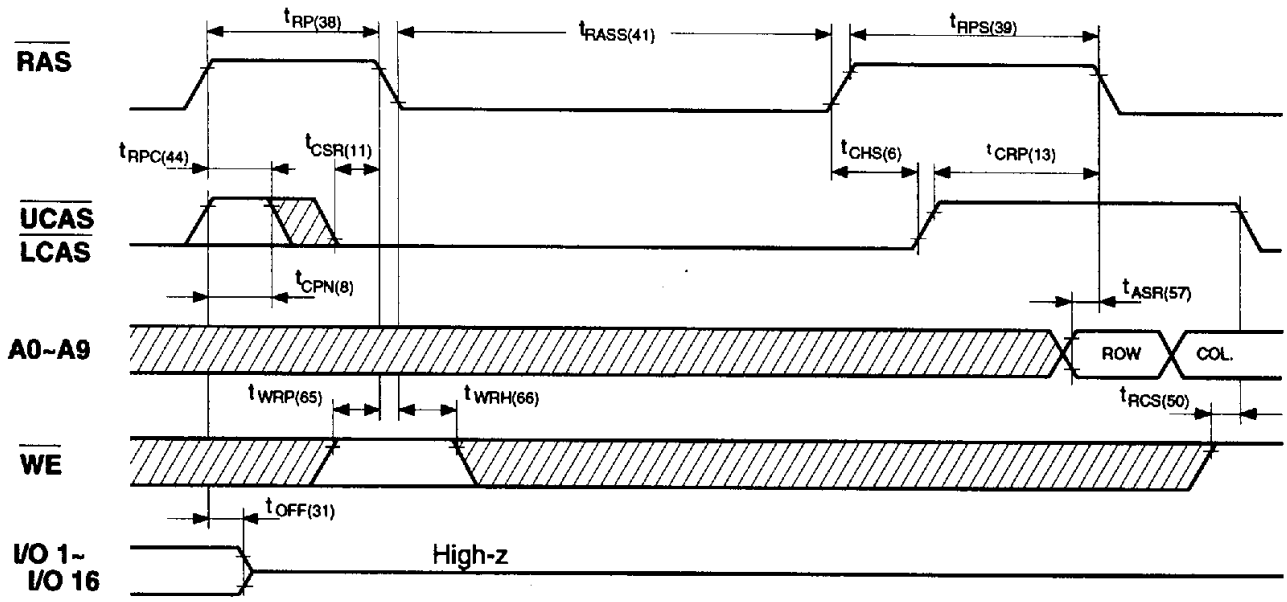
HIDDEN REFRESH CYCLE (EARLY WORD WRITE)



HIDDEN REFRESH CYCLE (EARLY BYTE WRITE)



SELF REFRESH MODE



: High or Low

■ The NN5118165A / NN5118165B (L version) has a Self Refresh Mode.

a. Entering the Self Refresh Mode:
The NN5118165AL / NN5118165BL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal " low " longer than 300μs.

b. Continuing the Self Refresh Mode:
The Self Refresh Mode is continuing by holding $\overline{RAS}$ " low " after entering the Self Refresh Mode.
It does not depend on $\overline{CAS}$ being " high " or " low " after entering the Self Refresh Mode to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:
The NN5118165AL / NN5118165BL exits will exit the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

ORDERING INFORMATION

NN5118165AXX(X) - XX

SPEED	50	:	50ns
	60	:	60ns
	70	:	70ns
PACKAGE	J	:	Plastic SOJ
	TT	:	Plastic TSOP TYPE II (Normal Bend)
	RR	:	Plastic TSOP TYPE II (Reverse Bend)
VERSION	BLANK	:	Standard Version
	L	:	Long Refresh Version 128ms Refresh
DESIGN CODE	A		
MODE	18165	:	EDO (Hyper Page) Mode 2$\overline{CAS}$,1M x 16 ,1024 refresh cycle

NN5118165BXX(X) - XX

SPEED	40	:	40ns
	50	:	50ns
	60	:	60ns
PACKAGE	J	:	Plastic SOJ
	TT	:	Plastic TSOP TYPE II (Normal Bend)
	RR	:	Plastic TSOP TYPE II (Reverse Bend)
VERSION	BLANK	:	Standard Version
	L	:	Long Refresh Version 128ms Refresh
DESIGN CODE	B		
MODE	18165	:	EDO (Hyper Page) Mode 2$\overline{CAS}$,1M x 16 ,1024 refresh cycle