



UTRON

Rev. 1.2

UT61L5128

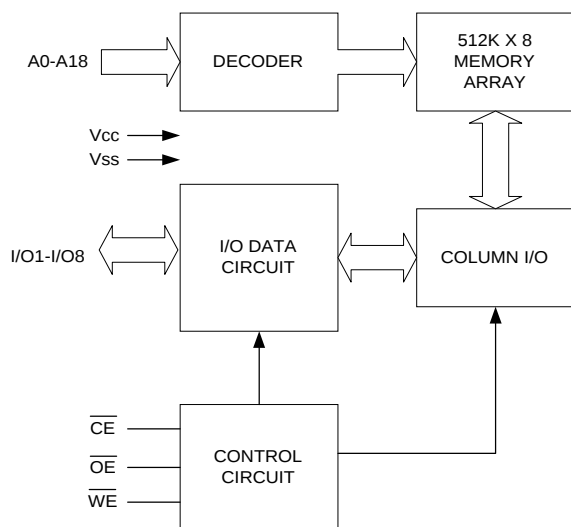
512K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	Draft Date
Preliminary Rev. 0.1	Original.	Jun 5, 2001
Preliminary Rev.1.0	1.Add test condition for I_{SB} . 2.Add note to V_{CC} for access time=10ns.	Jun 23,2001
Preliminary Rev.1.1	1.Revised access time : 10/12/15 ns →8ns (max.) for V_{CC} =3.15V~3.6V 10ns (max.) for V_{CC} =3.0V~3.6V 2.Add CMOS low power operating : Operating current : 260/220mA (I_{CC} max.) Standby current : 10/2mA(max.) 3.Add Data retention characteristics 4.Revised Terminal Voltage with Respect to $V_{SS}(V_{TERM})$: -0.5 to $V_{CC}+0.5$ → -0.5 to 4.6 5.Revised Input high voltage (V_{IH}): 2.2(min)/ $V_{CC}+0.5$ (max)→2.0(min)/ $V_{CC}+0.3$ (max)	Sep 06,2002
Rev.1.2	1. Revised Standby current : 10/2mA(max)→0.5mA(typ.) 2. Delete I_{CC1} , I_{CC2} 3. Revised I_{SB} : 30mA→3mA, I_{SB1} :10mA→2mA, 4. Add I_{SB} & I_{SB1} (typ.) : 1mA & 2mA 5. Add Overshoot : $V_{IH} \leq +6.0V$ for $t \leq t_{RC}/2$. Undershoot : $V_{IL} \leq -2.0V$ for $t \leq t_{RC}/2$. 6. Revised Data retention I_{DR} (max) : 3mA→1mA 7. Add order information for lead free product	May 20,2003

**FEATURES**

- Fast access time :
 - 8ns (max.) for Vcc=3.15V~3.6V
 - 10/12ns (max.) for Vcc=3.0V~3.6V
- CMOS Low operating power
 - Operating current : 260/240/220 mA (Icc max.)
 - Standby current : 0.5 mA (typ.)
- Single 3.0V~3.6V power supply
- Operating temperature :
 - Commercial : 0 ~70
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
 $\overline{UB}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP-II

FUNCTIONAL BLOCK DIAGRAM**PIN DESCRIPTION**

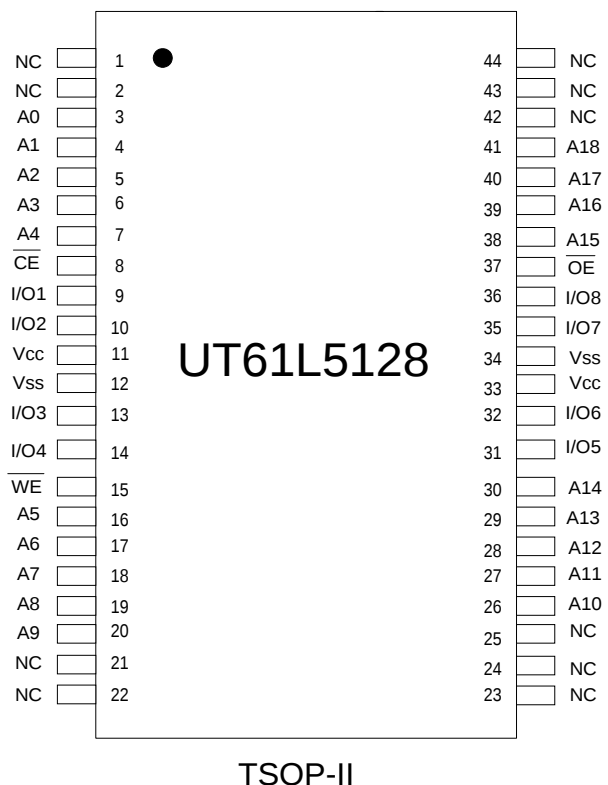
SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

GENERAL DESCRIPTION

The UT61L5128 is a 4,194,304-bit high-speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61L5128 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L5128 operates from a single 3.0V~3.6V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION

**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to 4.6	V
Operating Temperature	T _A	0 to 70	
Storage Temperature	T _{STG}	-65 to 150	
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{solder}	260	

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High - Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Voltage	V _{CC}		3.0	3.3	3.6	V
Input High Voltage	V _{IH} ^{*1}		2.0	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ^{*2}		-0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{SS} V _{IN} V _{CC}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{SS} V _{I/O} V _{CC} ; Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
Operating Power Supply Current	I _{CC}	Cycle time=min, 100%duty, I/O=0mA, $\overline{CE}$ =V _{IL}	-8	-	260	mA
			-10	-	240	mA
			-12	-	220	mA
Standby Current (TTL)	I _{SB}	$\overline{CE}$ =V _{IH} , other pins = V _{IL} or V _{IH}	-	1	3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CE}$ =V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V	-	0.5	2	mA

Notes:

1. Overshoot : V_{CC}+3.0v for pulse width less than 6ns.
2. Undershoot : V_{SS}-3.0v for pulse width less than 6ns.
3. Overshoot and Undershoot are sampled, not 100% tested.



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CAPACITANCE ($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$, $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L5128-8 3.15V~3.6V		UT61L5128-10 3.0V~3.6V		UT61L5128-12 3.0V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Enable Access Time	t_{ACE}	-	8	-	8	-	8	ns
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	4	-	5	-	6	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	4	-	5	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

(2) WRITE CYCLE

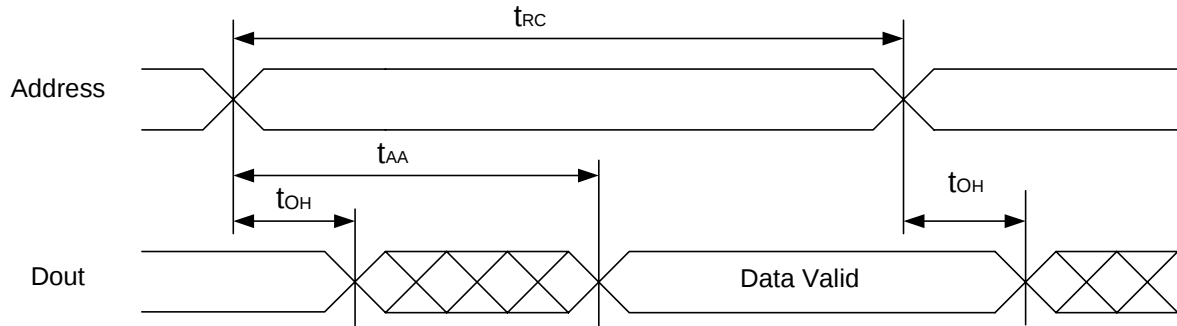
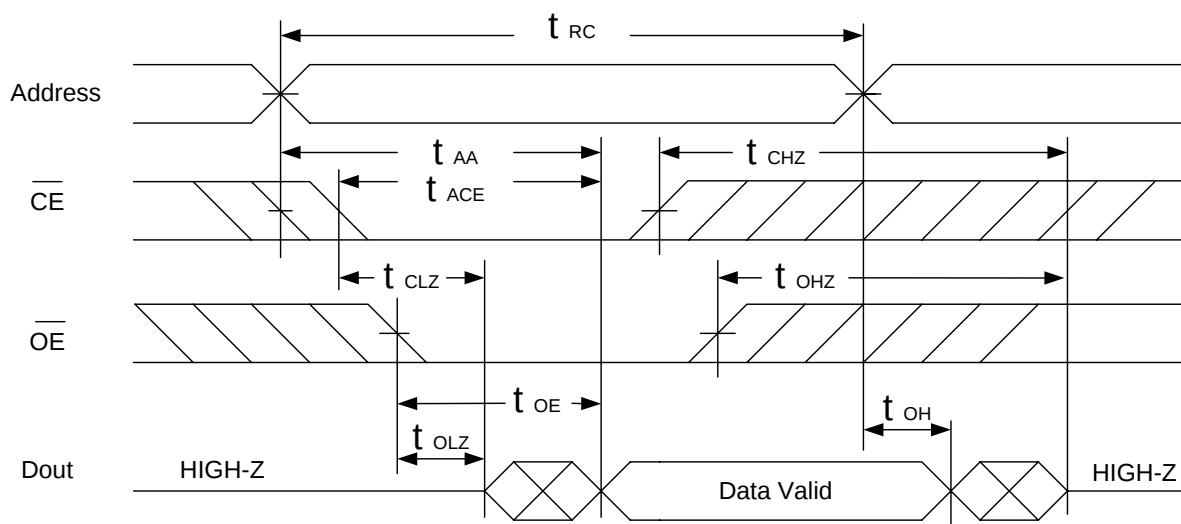
PARAMETER	SYMBOL	UT61L5128-8 3.15V~3.6V		UT61L5128-10 3.0V~3.6V		UT61L5128-12 3.0V~3.6V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	9	-	ns
Chip Enable to End of Write	t_{CW}	7	-	8	-	9	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	7	-	8	-	9	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5.5	-	6	-	7	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	3	-	3	-	0	-	ns
Write to Output in High Z	t_{WHZ}^*	-	4	-	5	-	6	ns

*These parameters are guaranteed by device characterization, but not production tested.



TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

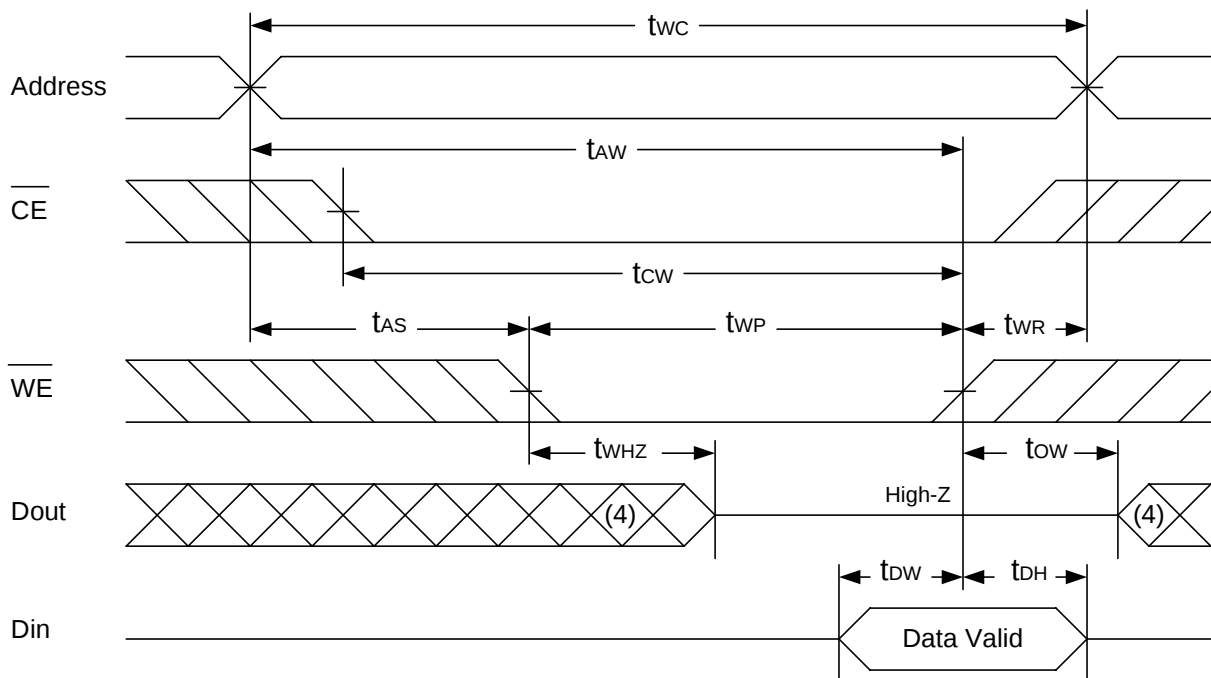
READ CYCLE 2 ($\overline{CE}$, and $\overline{OE}$ Controlled) (1,3,5,6)

Notes :

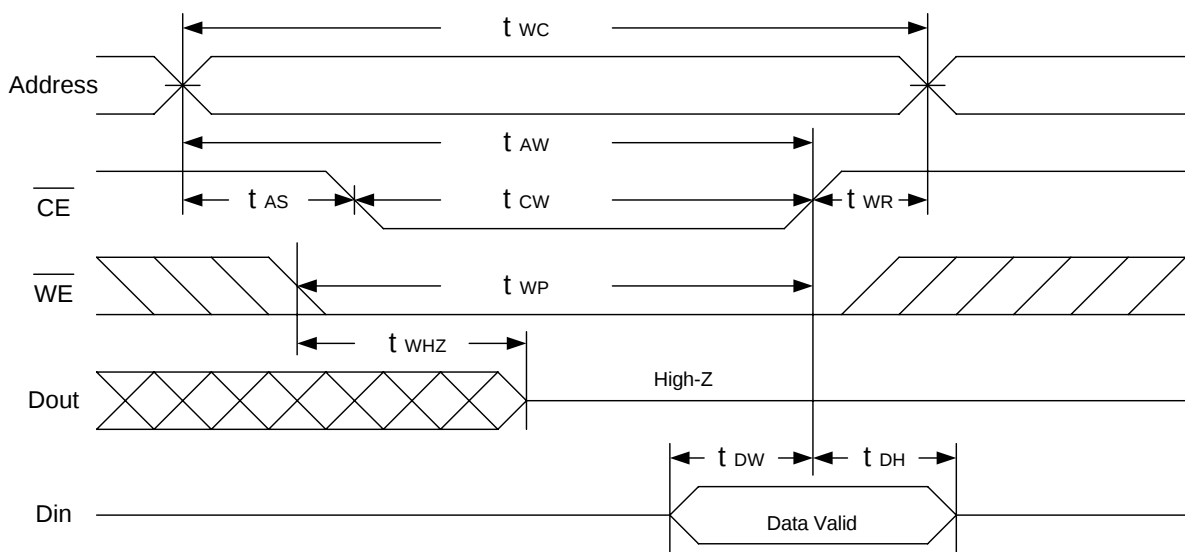
1. $\overline{WE}$ is HIGH for a read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)

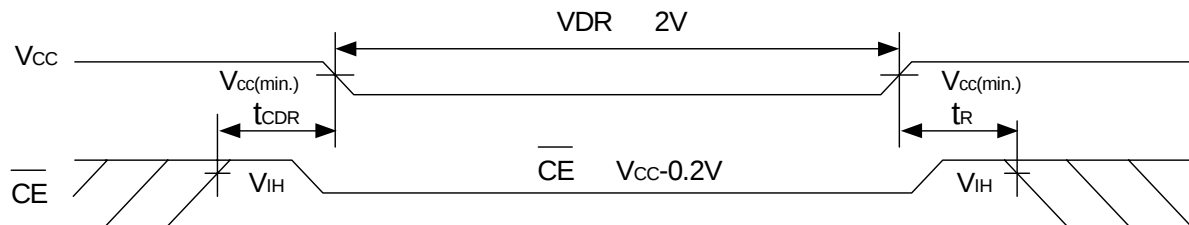


Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high Impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.

**DATA RETENTION CHARACTERISTICS** ($T_A = 0$ to $+70$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE}$ $V_{CC}-0.2V$,	2.0	3.6	V
Data Retention Current	I_{DR}	$V_{CC}=2V$ $\overline{CE}$ $V_{CC}-0.2V$,	-	1	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	ms
Recovery Time	t_R		5	-	ms

DATA RETENTION WAVEFORM**Low Vcc Data Retention Waveform (1)** ($\overline{CE}$ controlled)



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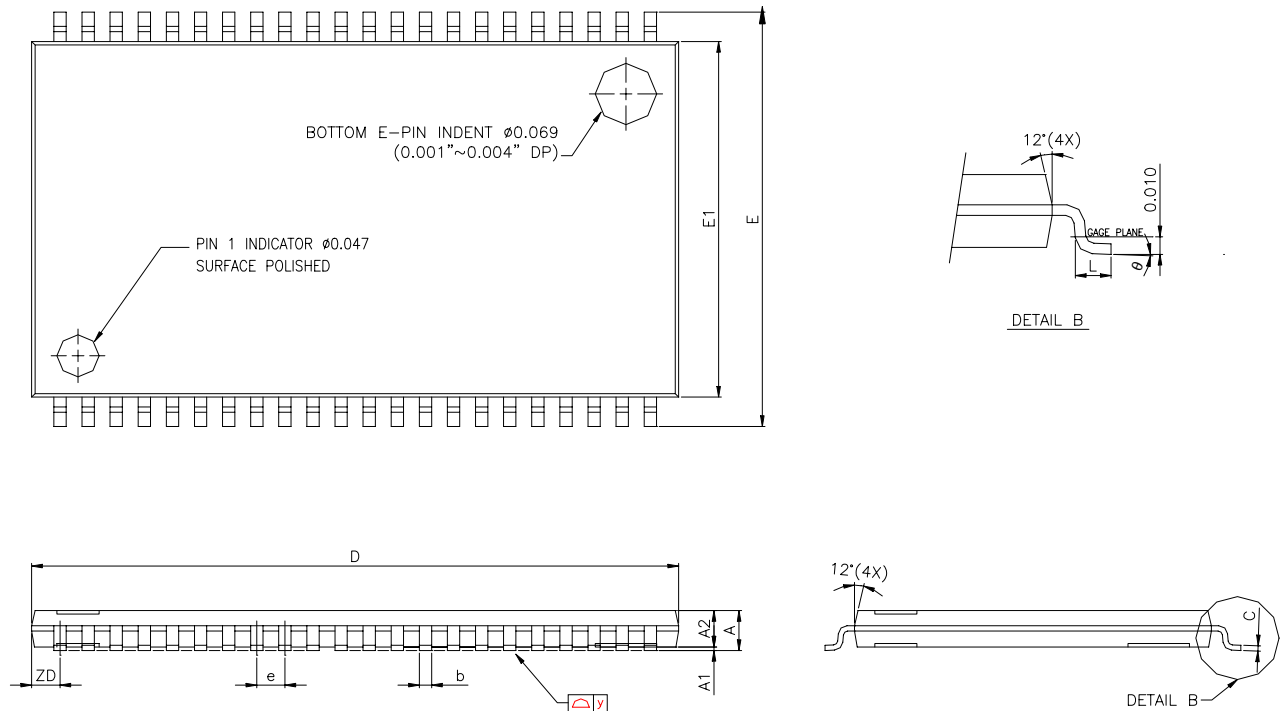
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PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP- Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0°	-	5°	0°	-	5°



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ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L5128MC-8	8	44 PIN TSOP-II
UT61L5128MC-10	10	44 PIN TSOP-II
UT61L5128MC-12	12	44 PIN TSOP-II

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L5128MCL-8	8	44 PIN TSOP-II
UT61L5128MCL-10	10	44 PIN TSOP-II
UT61L5128MCL-12	12	44 PIN TSOP-II



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