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GigaBit Logic

10G012B
10G013

10G012BK 10G012BM
10G013K 10G013M

Dual Complementary Driver/Comparator
1.75 GHz / 500 ps Delay
10G PicoLogic™ Family

FEATURES

- High gain comparator input
- Fixed 50% output duty cycle (10G012B)
- Adjustable output overlap (10G013)
- <50 ps skew between complementary outputs
- >70 mA output drive capability
- 150 ps output rise & fall times
- On-chip GaAs/ECL threshold reference voltage supply
- Temperature and voltage compensated design
- Available in 40 pin C-leaded, leadless chip carriers and die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

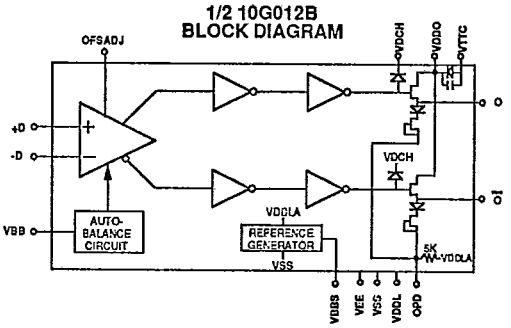
APPLICATIONS

- Differential Line Driver
- Differential Line Receiver
- 2 - phase clock generator
- Laser Diode Driver
- High Speed Comparator
- Capacitive Load Driver

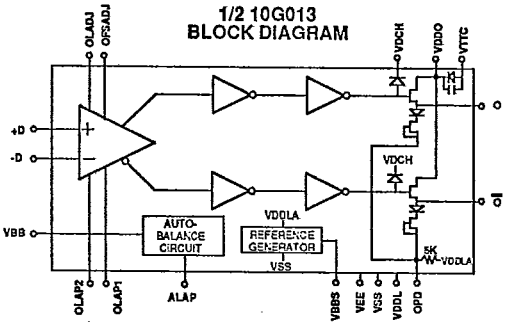
FUNCTIONAL DESCRIPTION

The 10G012B and 10G013 are versatile high speed dual drivers/comparators with differential outputs. The 10G013 provides controls to adjust the output overlap (time during which both outputs are simultaneously high or low). The 10G012B hard wires these controls internally so that the outputs exhibit a fixed 50% duty cycle with no overlap between them. Both devices feature 375 ps typical propagation delay with greater than 70 mA of output current drive capability. 150 ps output transition times and <50 ps output delay skew makes them ideally suited for driving a variety of capacitve loads with precision timing and high signal quality. The high gain differential input provides sensitivity to low level analog signals as well as ECL and GaAs levels. A convenient on-chip threshold reference supply (VBBS) can be strapped to either input when the device is driven single-ended from ECL or GaAs logic. The 10G012B / 10G013 can be driven with up to 1.75 GHz input signals. Operation to >2.5 GHz is permissable but will result in less than 1Vp-p output signal swing. Small signal unity gain is approximately 2.0 GHz.

1/2 10G012B BLOCK DIAGRAM



1/2 10G013 BLOCK DIAGRAM



10G012B/10G013 ORDERING INFORMATION

Package Type (40-Pin)	Speed (min. 0°C to 85°C)				_ = K: Speed (Min. -40°C to +100°C) M : Speed (Min. -55°C to +125°C)			
	10G012B		10G013		10G012BK & 10G012BM		10G013K & 10G013M	
	1.75 GHz	1.5 GHz	1.75 GHz	1.5 GHz	1.5 GHz	1.2 GHz	1.5 GHz	1.2 GHz
C-Leaded CC Leadless CC Die	10G012B-C 10G012B-L	10G012B-3C 10G012B-3L 10G012B-3X	10G013-C 10G013-L	10G013-3C 10G013-3L 10G013-3X	10G012B_-C 10G012B_-L	10G012B_-3C 10G012B_-3L 10G012B_-3X	10G013_-C 10G013_-L	10G013_-3C 10G013_-3L 10G013_-3X

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10G012B/10G013 OPERATION

The 10G012B and 10G013 feature several control pins which allows the user to tailor their performance in a wide variety of applications.

VBB & VBBS

The VBB input should be connected to the threshold of the signal applied to the input whether it is single ended or differential. When driving from PicoLogic, this threshold level is VBBS (nom. -1.3V), and the VBB input must be connected to the VBBS output pin. When the 10G012B/10G013 are driven single ended from ECL, the VBB input and either the -D or +D input (whichever is used as the switching reference level) should be connected to the ECL VBB threshold reference voltage. This will insure that the ECL and PicoLogic thresholds will track across the interface so that maximum signal noise immunity is maintained. Similarly, when the 10G012B or 10G013 is driven from an analog signal source with an arbitrary threshold voltage (within the common mode range) applied to one of the two D inputs, this same reference voltage must also be connected to the VBB input. Unlike other PicoLogic devices, the10G012B/10G013 VBB input does not set the device input switching threshold level. It is used only as the reference input to the device's auto-balance circuit.

OFSADJ (Input Offset Adjust)

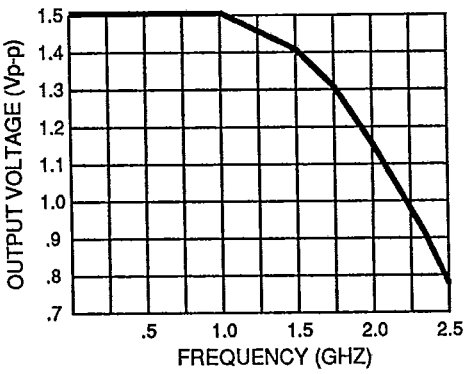
This input pin allows the input offset voltage of either part to be nulled. This may be easily accomplished by applying a ≤50 mV sinewave signal centered at -1.3V (or other level within the common mode range) to the +D input, with the -D input set to the same DC level, and varying OFSADJ in the range -6.0V≤OFSADJ≤-4.5V to produce a 50% duty cycle output. Because of the very high gain of these devices at even 1 GHz, it may be impractical to adjust the input offset by setting both +D and -D inputs to the same voltage level since the output is likely to oscillate betweeen high and low states. the OFSADJ input is internally pulled downed to VEE and may be left unconnected when not used.

OPD (Output Pull Down)

When OPD is connected to VSS, the outputs of both comparators are actively pulled low, with an approximate 10-15 mA current sink, without need for an external pull-down resistor to VTT. This simplifies the cascading of multiple devices when the interconnecting line length is kept short (≤0.2 in.). When interfacing to TTL/CMOS, OPD should be connected to +5.0V.

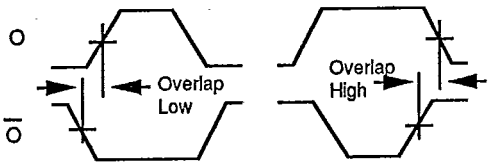
OPERATING FREQUENCY

The graph below shows peak-to-peak output voltage vs. frequency for a 1Vp-p sinewave input. This illustrates that the 10G012B/013 are useable to higher frequencies than their top 1.75 GHz rating if some degradation in the output peak to peak level is permissable and allowing for a VOL level more positive than -1.7V. For a 1 Vp-p input, 1 Vp-p is available at the output to beyond 2.0 GHz although VOL will increase slightly above -1.7V.



10G013 OUTPUT OVERLAP PROGRAMMING

In clock buffering applications, it is useful to create overlap-low or overlap-high output phases of the input clock signal. Overlap-low means that the O and $\overline{O}$ outputs are both low for part of each input clock cycle, and are never simultaneously high. Overlap-high means that O and $\overline{O}$ are both high for some part of the clock cycle, and are never both low. This is illustrated in the diagram below. Pins OLAP1, OLAP2 and OLADJ (Overlap Adjust) control the amount of overlap between O and $\overline{O}$ outputs. Adjusting the output overlap via these three controls simultaneoulsly changes the duty cycle of the complementary outputs in opposite directions.



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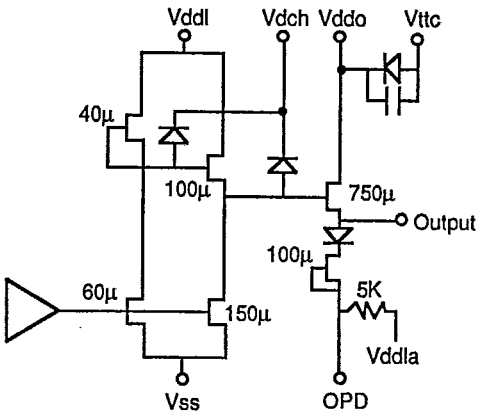
Since the overlap controls change the input threshold of the two differential inputs equally, the amount of overlap adjustment is directly proportional to the input signal rise and fall times. Fast input edge rates result in a small overlap adjustment range. 10G013 output overlap is programmed according to the table below:

Output Overlap	OLAP1	OLAP2	OLADJ
Adjustable from low to 0 to high	VEE	Open	VEE to VSS
Extra overlap high	VEE	VEE	VEE to VSS
No overlap	VEE	Open	ALAP

With OLAP1 set to VEE and OLAP2 left open, the amount of output overlap can be adjusted from overlap low to no overlap to overlap high by varying the voltage on pin OLADJ from VEE to VSS. Additional overlap high can be realized by setting OLAP2 to VEE. Zero output overlap can be set by connecting the OLADJ pin to the ALAP output pin with OLAP1 at VEE and OLAP2 open. This configures the 10G013 to operate the same as the 10G012B.

10G012B/10G013 OUTPUT CIRCUIT



PIN DESCRIPTIONS

+D	True data input.
-D	Complementary data input.
VDDO	Output driver ground connection. VDDOA and VDDOB are electrically separate. Side A and B can be powered down separately.
VDDL	Logic ground connection. VDDLA and VDDLB are electrically separate. Side A and B can be powered down separately.
VSS	- 3.4 V power supply
VEE	- 5.2 V power supply
OFSADJ	Input offset trim. (See text). May be left unconnected if not used.
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. See App. Note 4 for detail.
OLAP1, OLAP2	Used to adjust output overlap. (See text)
OLADJ	Overlap adjust input. (See text). When not used, may be left unconnected.
O	True data output.
$\overline{O}$	Complementary data output.
OPD	Active pull down for outputs. Leave open or connect to VSS. OPD can also be used in combination with an external pulldown resistor. Tie OPD to +5 V for TTL output interface.
ALAP	Auto-balance circuit output. Connect to OLADJ for zero output overlap.
VBB	Input signal threshold reference input to the auto-balance circuit.
VBBS	PicoLogic/ECL threshold reference voltage output. Note that VBBS is derived from VDDLA. Therefore the A side must be powered to obtain VBBS.

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DC CHARACTERISTICS

Tc = -55°C to +125°C (10G012BM, 10G013M); -40°C to +100°C (10G012BK, 10G013K); 0°C TO 85°C (10G012B, 10G013), VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I in	Input Current (012B, 013)	-100	60	200	µA	VIN = -1.0V to -1.6V
Iin	Input Current (012BK, 012BM, 013K, 013M)	-100	60	500	µA	VIN = -0.8V to -1.8V
VCM	Input common mode range	-1.8		-0.8	V	
ISS	Power Supply Current (012B, 013)		75	100	mA	
ISS	Power Supply Current (012BK, 012BM, 013K, 013M)		75	110	mA	
IEE	Power Supply Current (012B, 013)		37	50	mA	
IEE	Power Supply Current (012BK, 012BM, 013K, 013M)		37	60	mA	
PD	Power Dissipation (012B, 013)		450	600	mW	
PD	Power Dissipation (012BK, 012BM, 013K, 013M)		450	700	mW	

NOTE: The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note1)

10G012B/10G013

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.75		1.75	1.9		1.75		GHz	
T2	Input to output delay	300	500	300	350	500	300	500	ps	
T3	Delay skew		50		20	50		50	ps	
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	2

10G012B-3/10G013-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.5		1.5	1.7		1.5		GHz	
T2	Input to output delay	300	500	300	375	500	300	500	ps	
T3	Delay skew		50		30	50		50	ps	2
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	

10G012BK 10G013K
10G012BM 10G013M

SYMBOL	PARAMETER	-40°C (K) -55°C (M)		+25°C (K & M)			100°C (K) 125°C (M)		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.5		1.75	1.9		1.5		GHz	
T2	Input to output delay	300	500	300	350	500	300	500	ps	
T3	Delay skew		50		20	50		50	ps	
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	2

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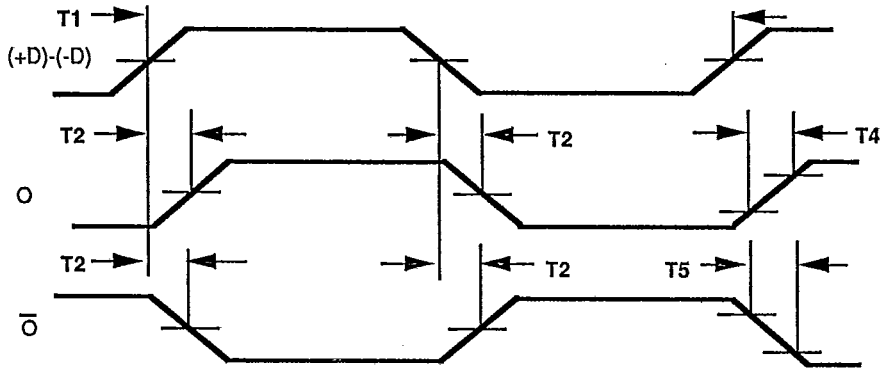
10G013K 10G013M

10G012BK-3 10G013K-3
10G012BM-3 10G013M-3

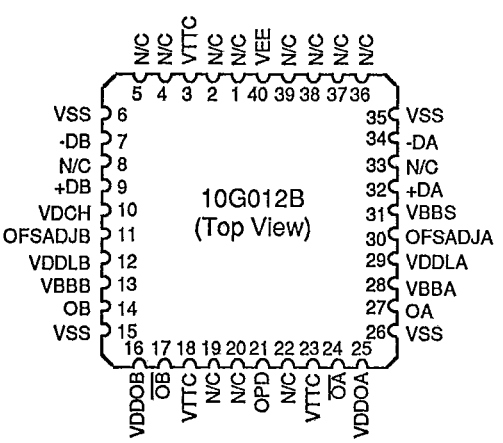
SYMBOL	PARAMETER	Tc = -40°C		Tc = +25°C			Tc=100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Max. input frequency	1.2		1.5	1.7		1.2		GHz	
T2	Input to output delay	330	550	300	375	500	330	550	ps	
T3	Delay skew		50		30	50		50	ps	
T4	Output rise time		175		125	175		200	ps	2
T5	Output fall time		150		125	150		175	ps	2

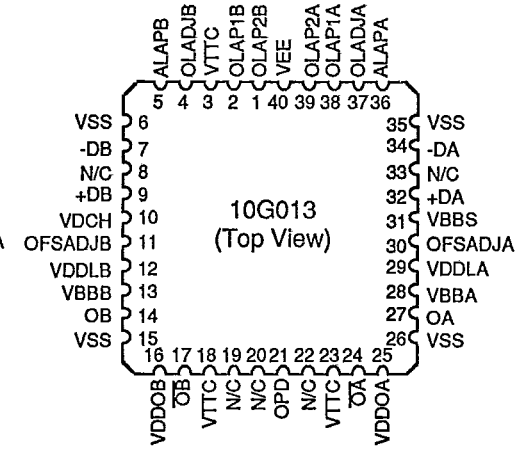
NOTES :
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V, -D = -1.2V, Oladj = Autolap, Olap1 = VEE, Olap2 = N/C.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



40 I/O PACKAGE PINOUTS - PACKAGE TYPES "L" AND "C"





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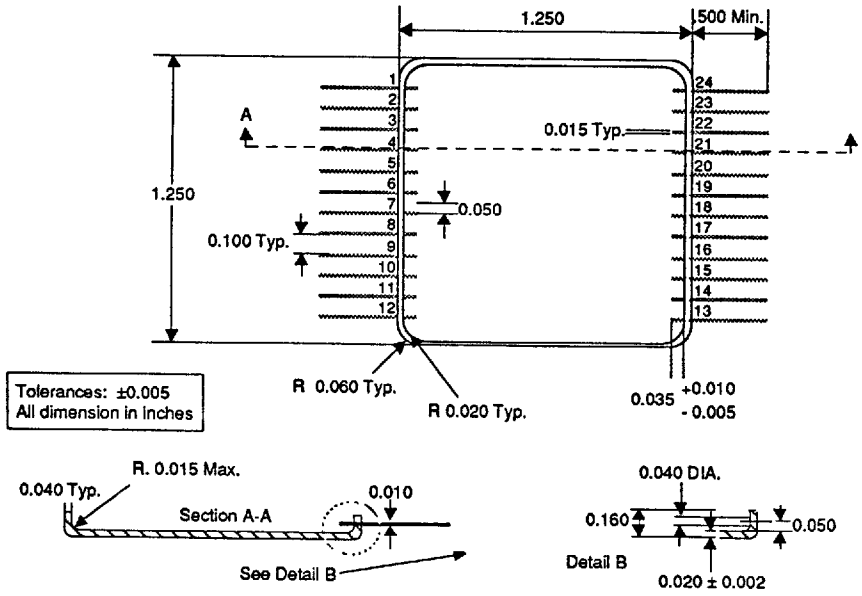
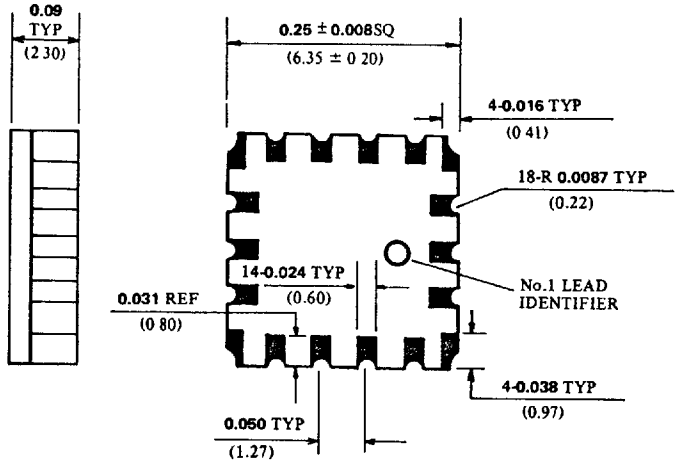
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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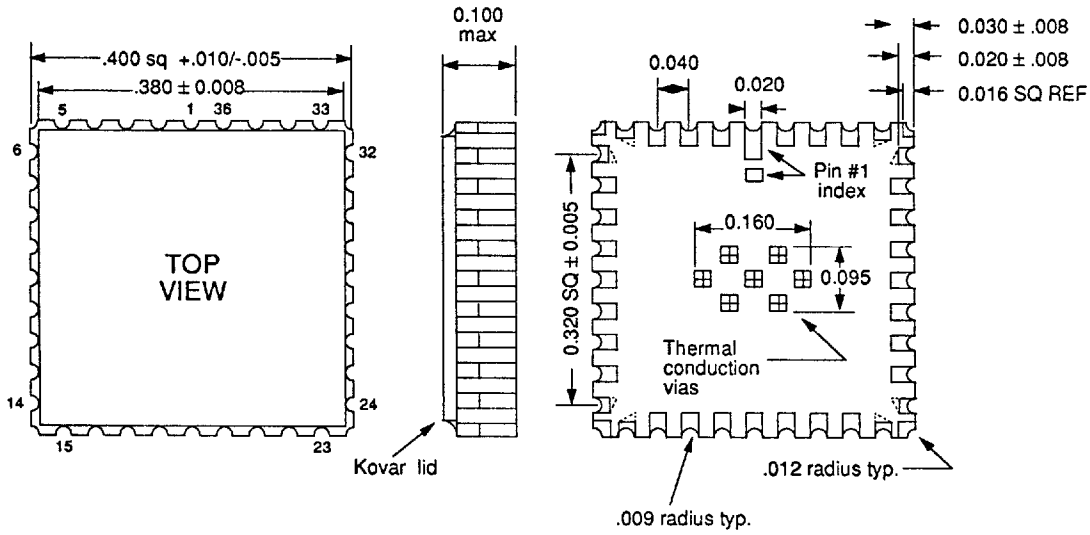
GigaBit Logic

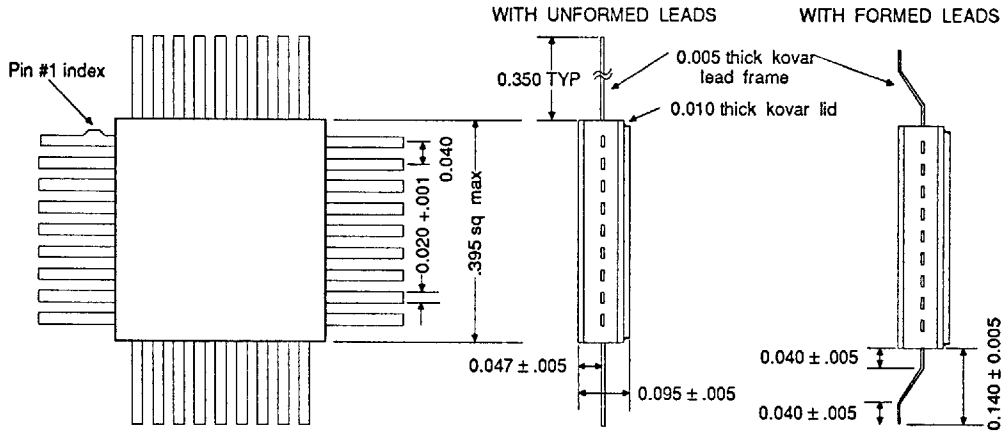
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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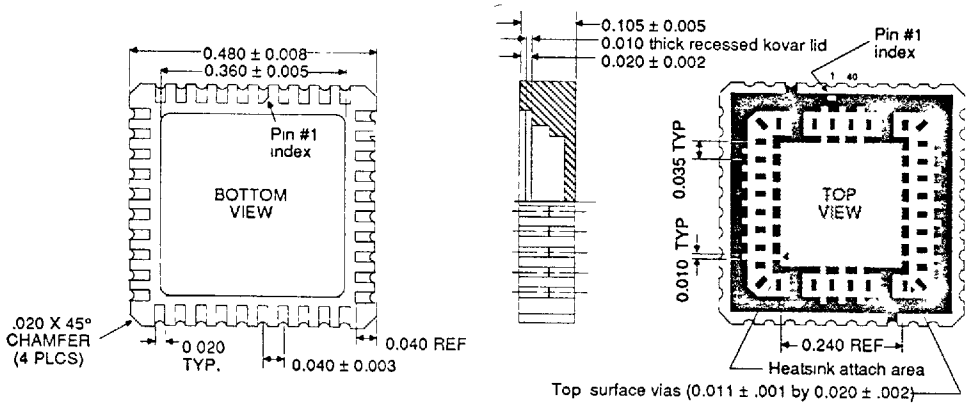
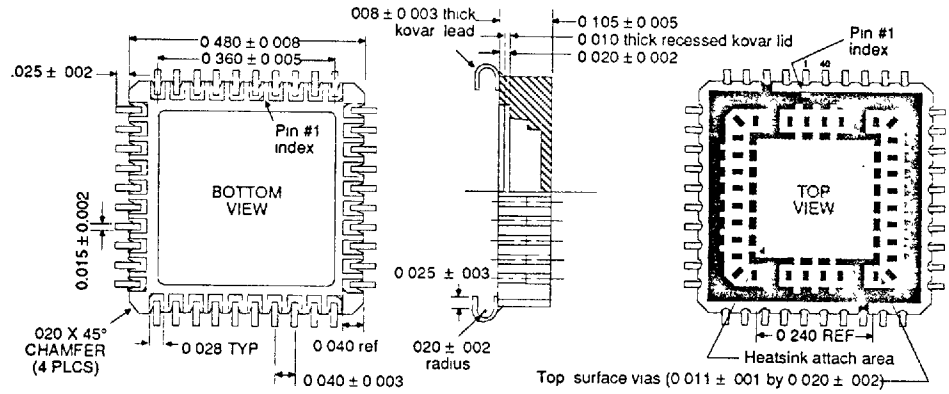
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

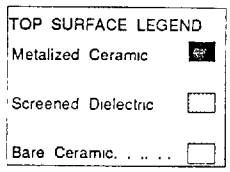


40 PIN LEADED CHIP CARRIER
TYPE C

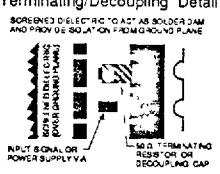


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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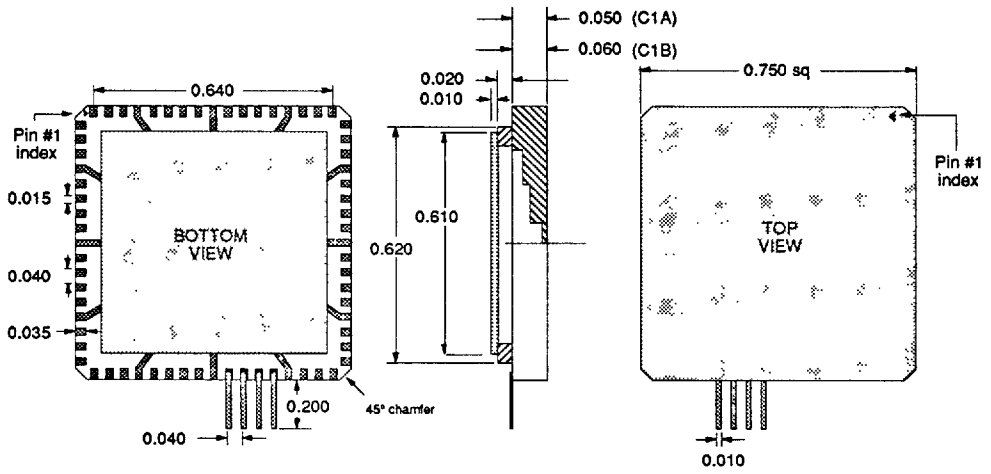
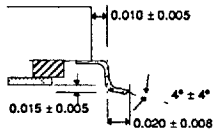
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3