10A Synchronous Buck Regulator with Integrated Power MOSFETs that Requires No Compensation

ISL95210

The ISL95210 single-output integrated MOSFET regulator provides a precision voltage regulation system for point-of-load applications. It implements a 2-bit DAC reference with tri-state inputs for selecting a variety of regulator output voltages. Additionally, an external resistor divider or digital voltage margining may be used to accurately set the output voltage to a value other than the pre-selected DAC voltages. An additional tri-state input pin is used to set the frequency to three pre-selected values with no need for external components.

The ISL95210 implements a modified version of Intersil's previous high performance R^3™ modulator topology in the new R^4™ modulator. This modulation scheme provides improved transient performance, while also including key performance updates that remove the need for loop compensation and produce highly accurate switching frequencies. These updates, along with an integrated digital feature set, allow for a high-performance regulator that is highly compact and needs few external components.

Protection features of this integrated regulator IC include a set of sophisticated overvoltage, undervoltage, overcurrent and thermal protections. Combined, these features provide advanced protection for the load and power system.

Related Literature

- See AN1485, "ISL95210 10A Integrated FET Regulator Evaluation Board Setup Procedure"

Features

- True 10A Solution up to +90°C Ambient with No Air Flow
- Excellent Efficiency
  - 95% Peak
  - 87% at 800kHz, 10A and 1.05V$_{OUT}$
- Best in Class MOSFET r$_{DS(ON)}$
  - 15mΩ High-Side
  - 4mΩ Low-Side
- ±0.6% Output Voltage Accuracy Over-Temperature
- Intersil's R^4™ Modulator Technology
  - Optimal Transient Response
  - No Compensation Required
- Full Digital Feature Set for Minimal Component Count
- DAC Output Voltage Control with Margining
- 32 Lead, 6mmx4mm QFN Package

Applications

- Notebook Computers
  - V$_{DDQ}$ for DDR1/2/3
  - Chipset Voltages
- MXM Graphics Card Modules
- Point of Load Applications
- General Purpose Applications

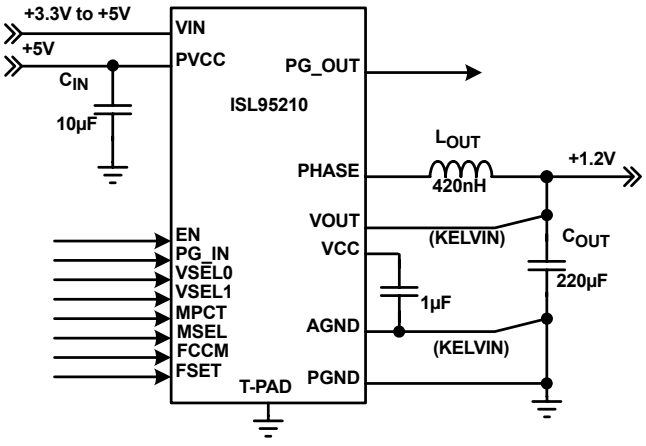


FIGURE 1. ISL95210 TYPICAL 800kHz APPLICATION

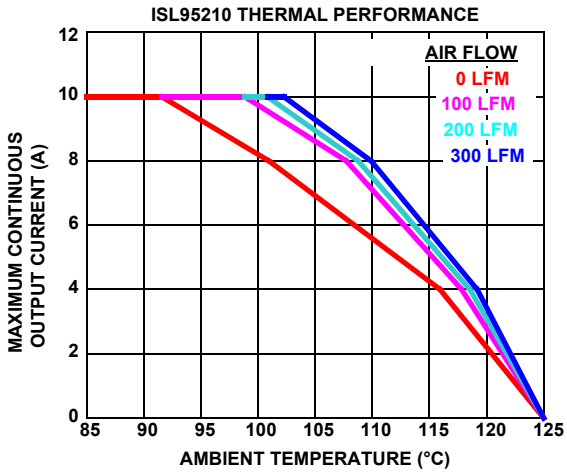
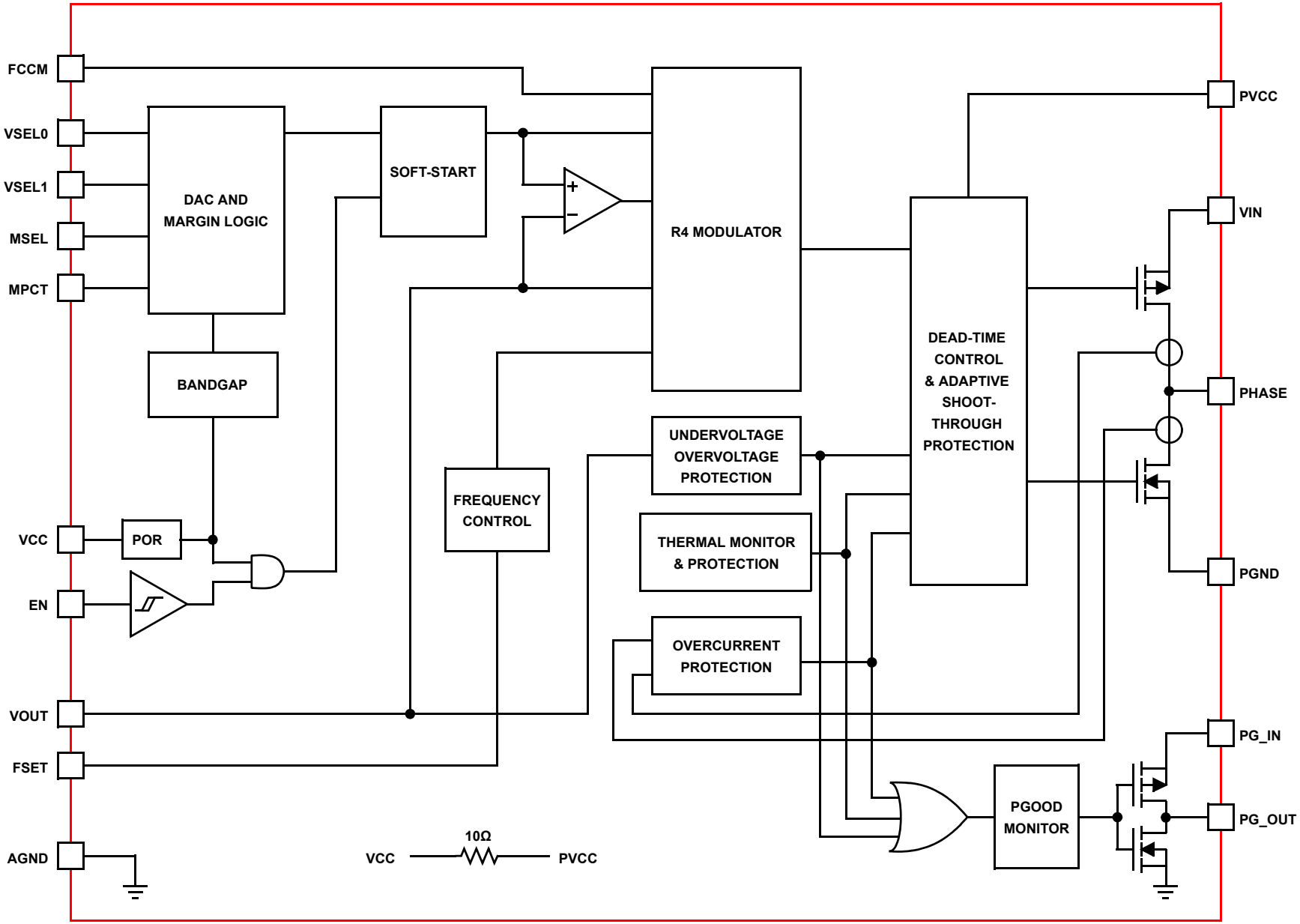


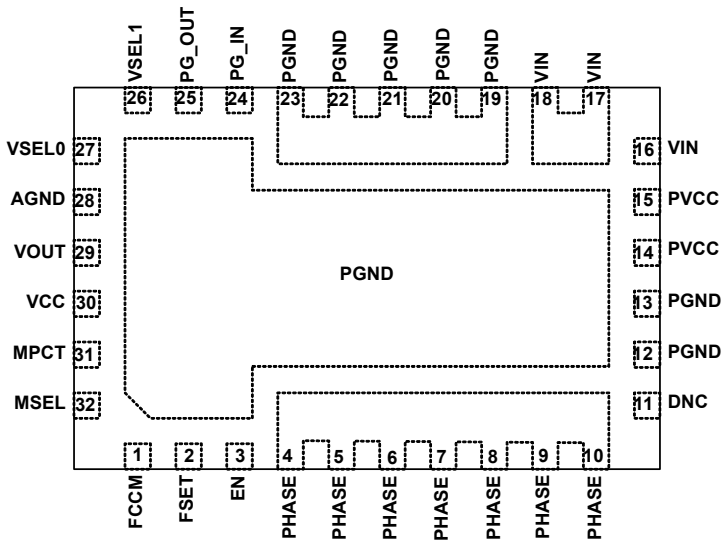
FIGURE 2. KEY PERFORMANCE CURVE

Functional Block Diagram



Pin Configuration

ISL95210
(32 LD QFN)
TOP VIEW



Functional Pin Descriptions

PIN	NAME	FUNCTION
Thermal Pad	PGND	Power ground. This thermal pad provides a return path for power stage and switching currents as well as a thermal path for removing heat from the IC into the board. Place thermal vias in the pad to the PGND plane.
1	FCCM	Logic input for operating mode selection. Connect this pin to VCC for CCM regulation only. Connect this pin to AGND to allow discontinuous conduction mode for light-load efficiency. Float this pin for audio mode light-load switching.
2	FSET	Tri-state digital input for programming the regulator switching frequency. Pull this pin to VCC for 800kHz switching. Pull this pin to GND for 400kHz switching. Leave this pin floating for 533kHz switching.
3	EN	Logic input for enabling and disabling output voltage regulation. Pull this pin to VCC to begin regulation. Pull this pin to AGND to disable regulation.
4, 5, 6, 7, 8, 9, 10	PHASE	Power stage switching node for output voltage regulation. Connect to the output inductor. All PHASE pins **must** be shorted on the printed circuit board.
11	DNC	No connect. This pin **must** be left floating under all conditions.
12, 13, 19, 20, 21, 22, 23	PGND	Power ground. This pin provides a return path for power stage and switching currents. All PGND pins **must** be shorted on the printed circuit board.
14, 15	PVCC	Power input for the integrated MOSFET gate drivers. Connect to a +5V supply. Both PVCC pins **must** be shorted on the printed circuit board.
16, 17, 18	VIN	Power input for buck regulation stage. Bypass to PGND with one 10µF or 22µF ceramic capacitor. Connect to a +3.3V to +5V supply. All VIN pins **must** be shorted on the printed circuit board.
24	PG_IN	Input voltage for the power-good CMOS output. Connect this pin to the desired PGOOD output high level.
25	PG_OUT	Active CMOS output for power-good indication. High state is indicated when the output voltage is in regulation, and output is logic low otherwise. Logic high level is set by the voltage on the PG_IN pin.
26	VSEL1	DAC logic MSB input. Used to program preset output voltages of 0.60V, 0.75V, 0.90V, 1.00V, 1.05V, 1.10V, 1.20V, 1.50V, and 1.80V.
27	VSEL0	DAC logic LSB input. Used to program preset output voltages of 0.60V, 0.75V, 0.90V, 1.00V, 1.05V, 1.10V, 1.20V, 1.50V, and 1.80V.
28	AGND	Ground reference for analog signals. Connect this pin to the ground plane.
29	VOUT	Sense point for output voltage regulation and output soft-discharge. Connect to the desired regulation point.

Functional Pin Descriptions (Continued)

PIN	NAME	FUNCTION
30	VCC	Analog power supply input. Used for bias and precision references. Place a high frequency ceramic capacitor (0.1µF to 1µF) to AGND. Internally connected to PVCC through a 10Ω resistor.
31	MPCT	3-state logic input for programming the amount of output voltage margining as controlled by the MSEL pin. Pull the pin to GND for ±15% margining, to VCC for ±20% margining, and float the pin for ±10% margining.
32	MSEL	Digital input for control of output voltage margining. Pull this pin to VCC to margin the output voltage to the high value. Leave this pin floating to margin the output voltage low. Pull this pin to AGND to regulate the nominally programmed output voltage value. The margin amount is dictated by the MPCT pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL95210HRZ	95210 HRZ	-10 to +100	32 Ld 6x4 QFN	L32.6x4B
ISL95210IRZ	95210 IRZ	-40 to +100	32 Ld 6x4 QFN	L32.6x4B
ISL95210EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95210. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

All pins . . . . . -0.3V to +6V

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±10%
PVCC Supply Voltage . . . . . +5V ±10%
VIN Supply Voltage . . . . . +3.3V to +5V ±10%
Junction Temperature (ISL95210HRZ) . . . . . -10°C to +125°C
Junction Temperature (ISL95210IRZ) . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	40	4

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range (-10°C to +100°C for ISL95210HRZ; -40°C to +100°C for ISL95210IRZ).**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
BIAS SUPPLIES					
Shutdown Supply Current [PVCC]	EN = low, VIN = PVCC = high		0.4	**10**	µA
Switching Supply Current [PVCC]	EN = high, VCC = high, FSET = GND(400kHz), FCCM = high		7.2		mA
	EN = high, VCC = high, FSET = FLOAT (533kHz), FCCM = high		8.9		mA
	EN = high, VCC = high, FSET = high (800kHz), FCCM = high		12.2		mA
Standby Supply Current [PVCC]	EN = high, VCC = high, FCCM = low, I_{OUT} = 0A		1.9	**2.7**	mA
VCC POR (Power-On Reset) Threshold	VCC rising	**4.25**		**4.50**	V
	VCC falling	**4.00**		**4.25**	V
PWM MODULATOR					
Oscillator Frequency Accuracy, F_{SW} (ISL95210HRZ)	FSET=GND(400kHz)/FLOAT(533kHz)/VCC (800kHz) T_A = +25°C	-5		5	%
	FSET = GND(400kHz)/FLOAT(533kHz)/VCC (800kHz), **-10°C to +100°C**	**-10**		**10**	%
Oscillator Frequency Accuracy, F_{SW} (ISL95210IRZ)	FSET = GND(400kHz)/FLOAT(533kHz)/VCC (800kHz) **-40°C to +100°C**	**-15**		**15**	%
CONTROL THRESHOLDS					
EN Rising Threshold				**2.0**	V
EN Falling Threshold		**1.0**			V
FCCM, MPCT, MSEL, FSET, VSEL_ Input Low Threshold		**1.20**	1.50	**1.80**	V
FCCM, MPCT, MSEL, FSET, VSEL_ Input Floating Voltage	Input impedance > 1MΩ	**1.85**	2.00	**2.15**	V
FCCM, MPCT, MSEL, FSET, VSEL_ Input High Threshold		**2.2**	2.50	**2.8**	V

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range (-10°C to +100°C for ISL95210HRZ; -40°C to +100°C for ISL95210IRZ). (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
REFERENCE AND DAC					
System Accuracy ISL95210HRZ **-10°C to +100°C**	V_{OUT} = {0.700V to 2.1625V}, V_{IN} = 5V	**-0.60**		**0.60**	%
	V_{OUT} = {0.48125V to 0.700V}, V_{IN} = 5V	**-0.75**		**0.75**	%
System Accuracy ISL95210IRZ **-40°C to +100°C**	V_{OUT} = {0.700V to 2.1625V}, V_{IN} = 5V	**-0.75**		**0.75**	%
	V_{OUT} = {0.48125V to 0.700V}, V_{IN} = 5V	**-1**		**1**	%
Line Regulation Accuracy	4.5V < V_{IN} < 5.5V		0.05		%
Load Regulation Accuracy	FCCM = high, Inductor DCR = 2mΩ		0.08		%
SOFT-START RAMP					
Soft-Start and VSEL Slew Rate		**1.6**	2.3	**3.0**	mV/µs
PROTECTION					
Overcurrent Trip Level	Valley Current Limit (8 PWM Pulse Count)	**10**	12.5	**14**	A
	Peak Way-Overcurrent (~1µs delay)	**28**	35	**43**	A
Undervoltage Threshold	V_{OUT}:V_{DAC}	**81**	84	**87**	%
Overvoltage Rising Threshold	V_{OUT}:V_{DAC}	**112**	116	**120**	%
Overvoltage Falling Threshold	V_{OUT}:V_{DAC}	**99**	102	**106**	%
Power-Good Pull-Up Resistance		**1.8**	2.3	**2.8**	kΩ
Power-Good Pull-Down Resistance		**30**	50	**70**	Ω
V_{OUT} Soft-Discharge Resistance	All Shutdown Conditions	**25**	45	**65**	Ω
POWER MOSFET ON-RESISTANCE					
High-Side PMOS	**+25°C only**	**-**	-	16.52	mΩ
High-Side PMOS		**-**	14.8	**19.5**	mΩ
Low-Side NMOS	**+25°C only**	**-**	-	4.28	mΩ
Low-Side NMOS		**-**	3.8	**5.7**	mΩ
OVER-TEMPERATURE SHUTDOWN (Note 6)					
Thermal Shutdown Setpoint			150		°C
Thermal Recovery Setpoint			125		°C

NOTES:

6. Thermal impedance measured in still air on the ISL95210EVAL1Z REV B evaluation board with 800kHz setup. See AN1485.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

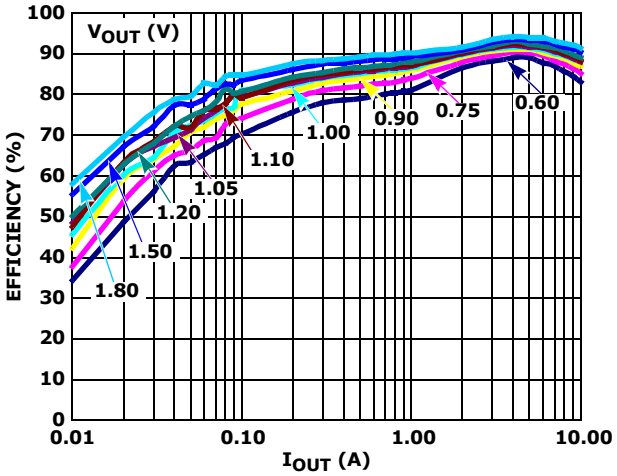


FIGURE 3. 800kHz EFFICIENCY FCCM = LOW

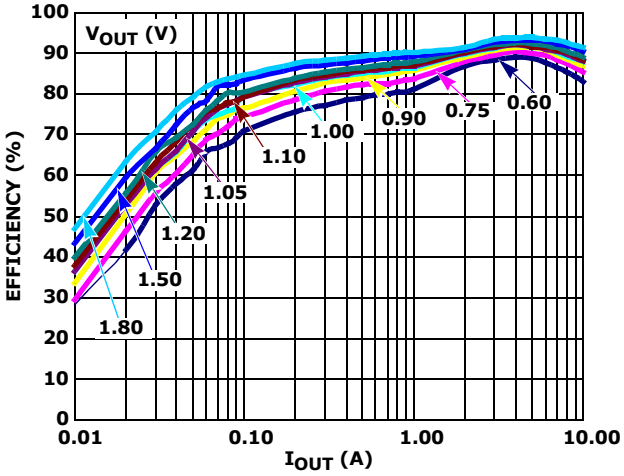


FIGURE 4. 800kHz EFFICIENCY FCCM = FLOAT

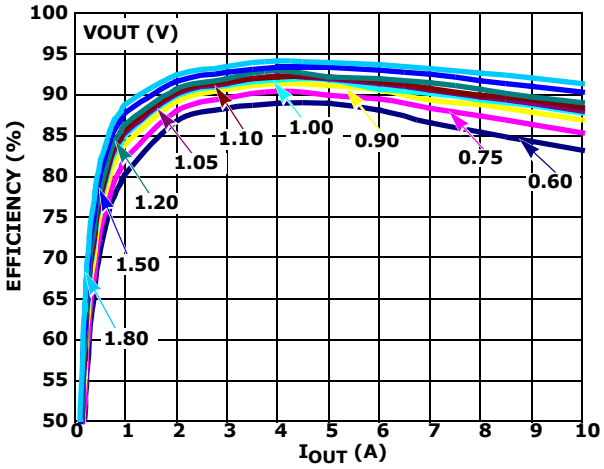


FIGURE 5. 800kHz EFFICIENCY FCCM = HIGH

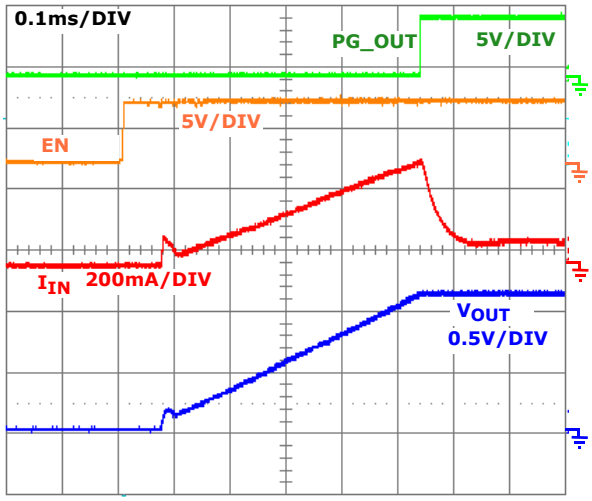


FIGURE 6. NORMAL START-UP

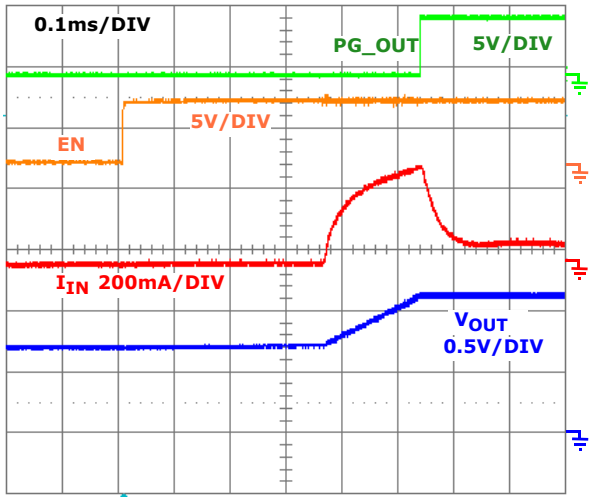


FIGURE 7. PRE-BIASED START-UP

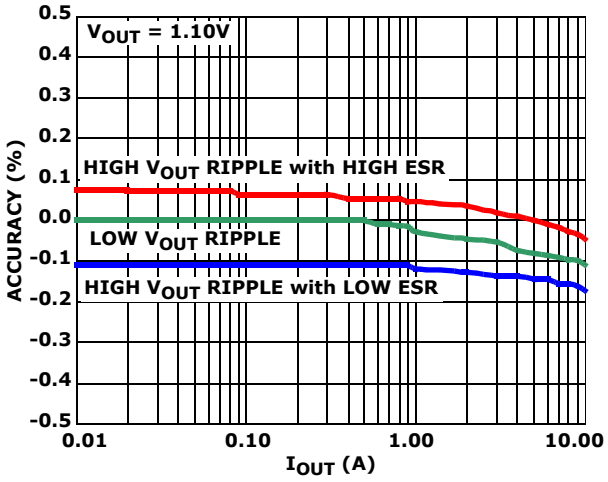


FIGURE 8. CCM OUTPUT VOLTAGE LOAD REGULATION

Typical Performance Curves (Continued)

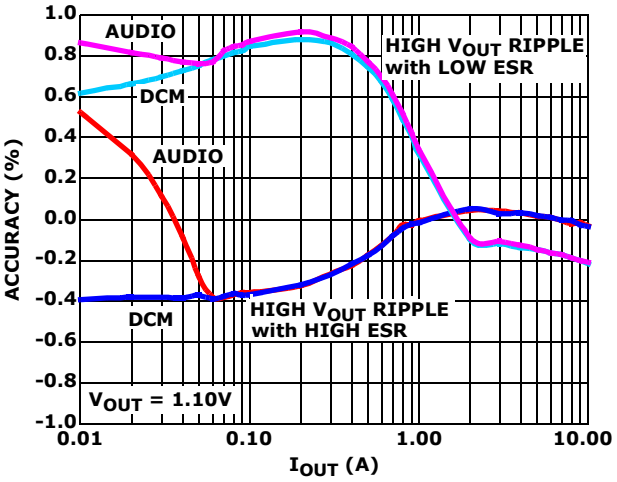


FIGURE 9. OUTPUT VOLTAGE LOAD REGULATION (LOG SCALE)

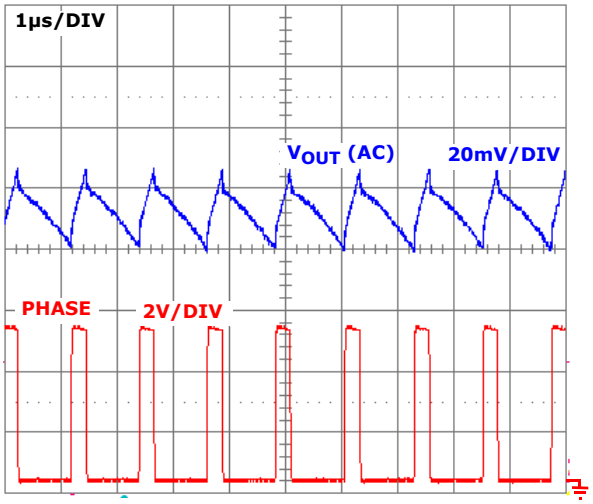


FIGURE 10. CCM STEADY-STATE

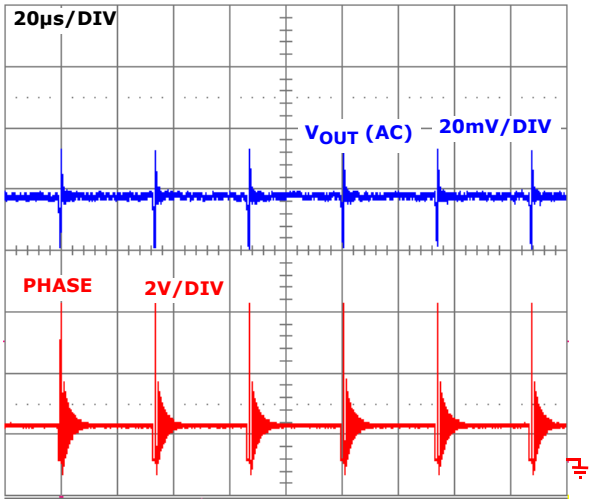


FIGURE 11. AUDIO MODE STEADY-STATE

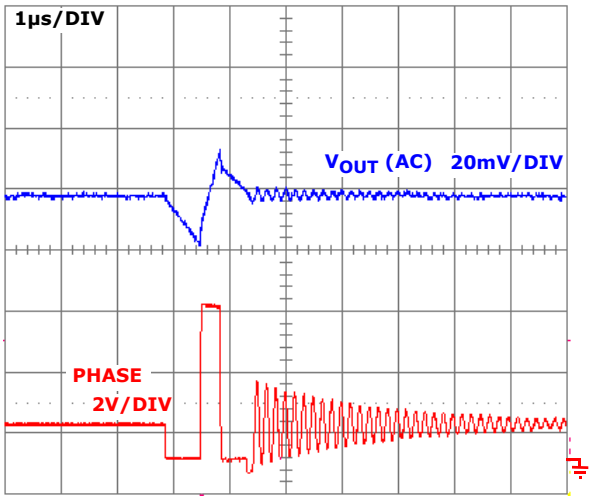


FIGURE 12. AUDIO MODE STEADY-STATE (ZOOM)

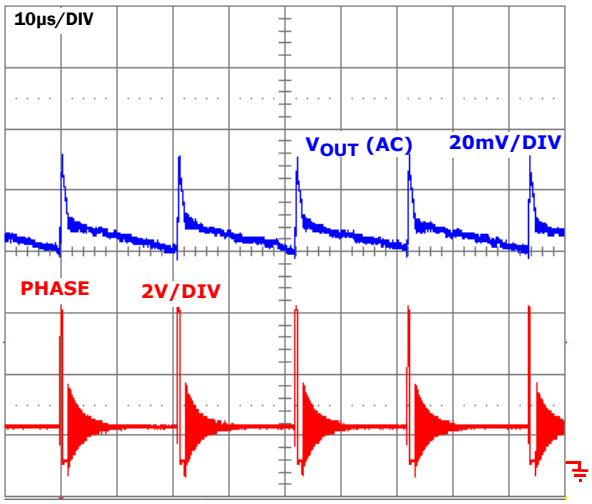


FIGURE 13. DCM STEADY-STATE (100mA)

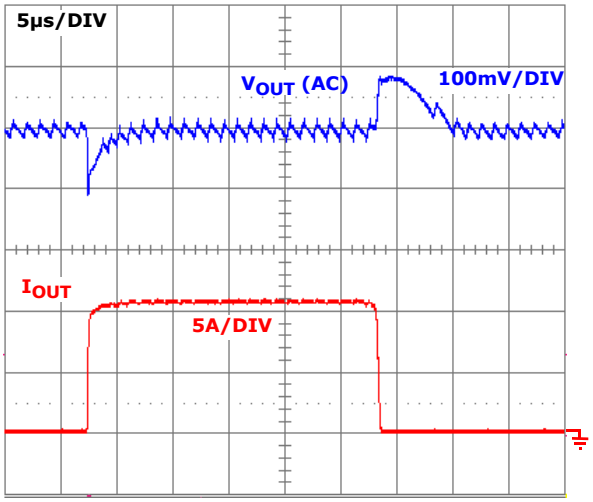


FIGURE 14. 10A LOAD TRANSIENT 50A/µs

Typical Performance Curves (Continued)

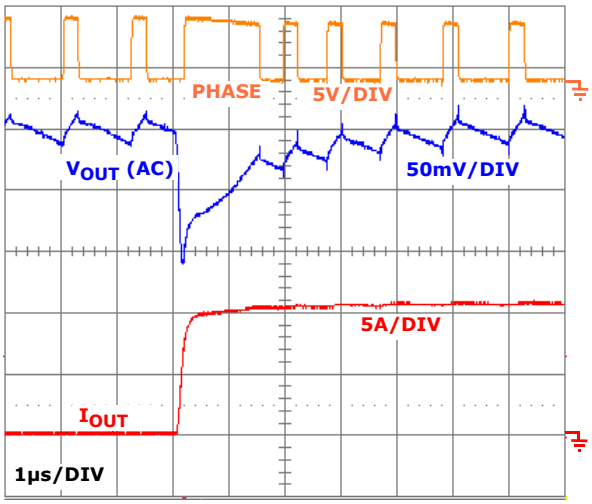


FIGURE 15. 10A LOAD TRANSIENT 50A/µs (ZOOM RISING EDGE)

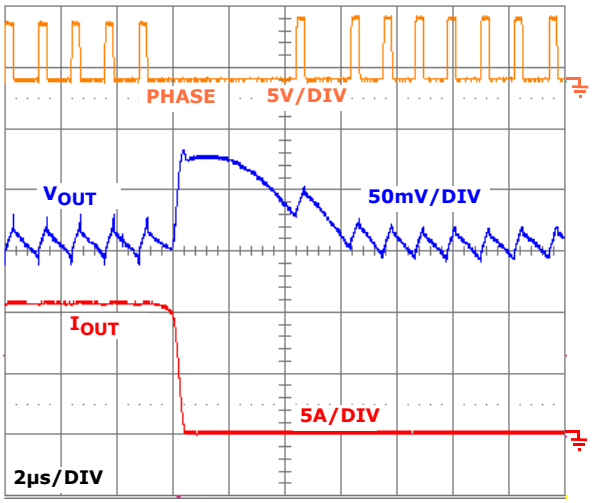


FIGURE 16. 10A LOAD TRANSIENT 50A/µs (ZOOM FALLING EDGE)

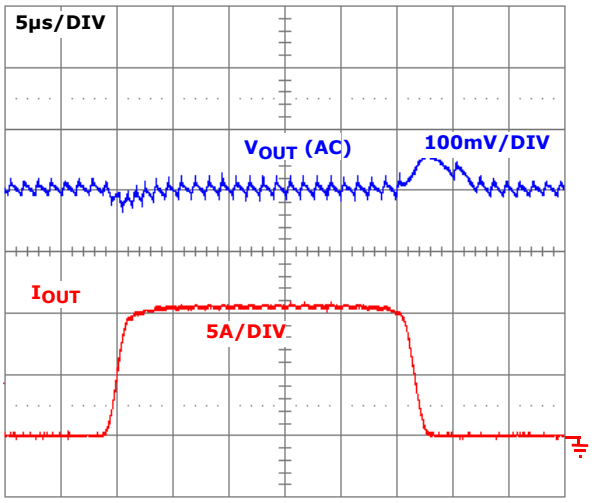


FIGURE 17. 10A LOAD TRANSIENT 5A/µs

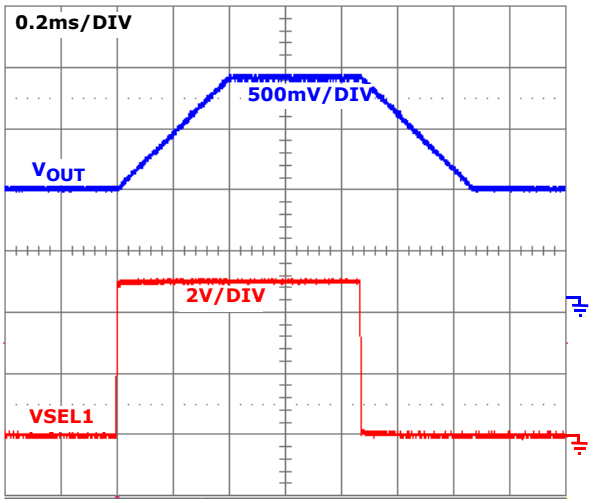


FIGURE 18. VSEL1 TRANSITIONS 0.90V TO 1.80V

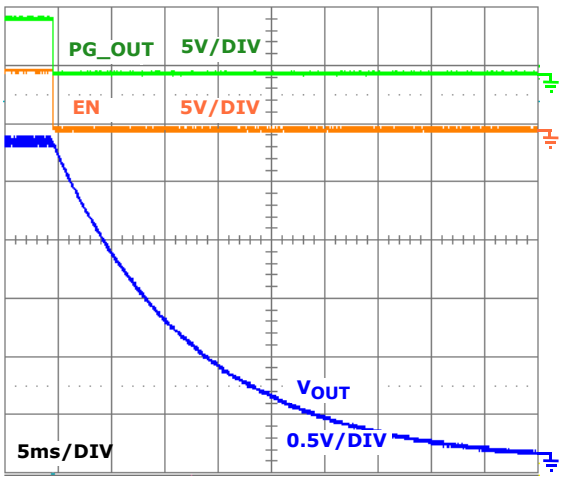


FIGURE 19. NORMAL SHUT-DOWN

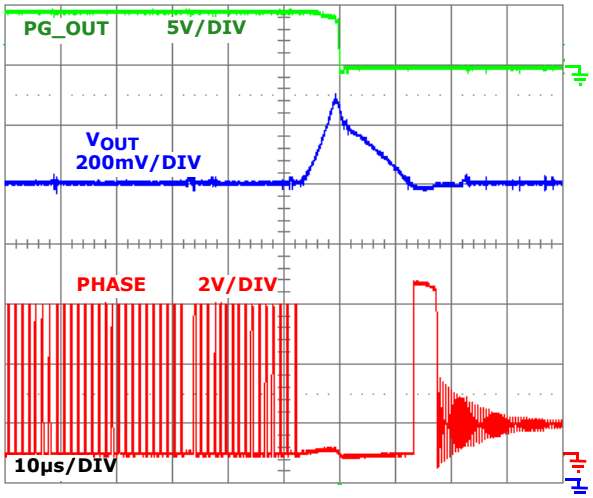


FIGURE 20. OVERVOLTAGE SHUT-DOWN (VDAC = 1.00V)

Typical Performance Curves (Continued)

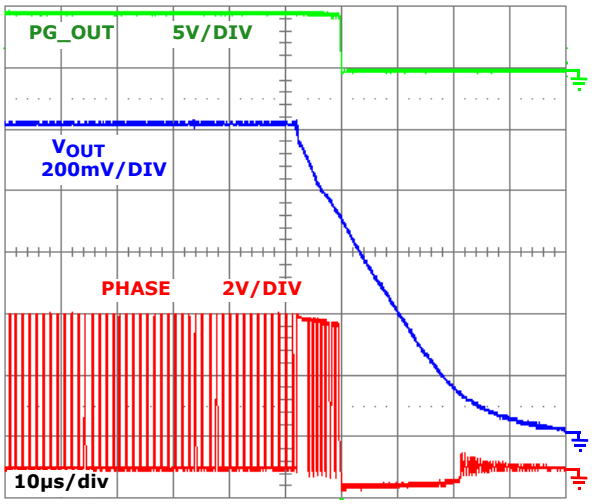


FIGURE 21. UNDERVOLTAGE SHUT-DOWN (VDAC = 1.00V)

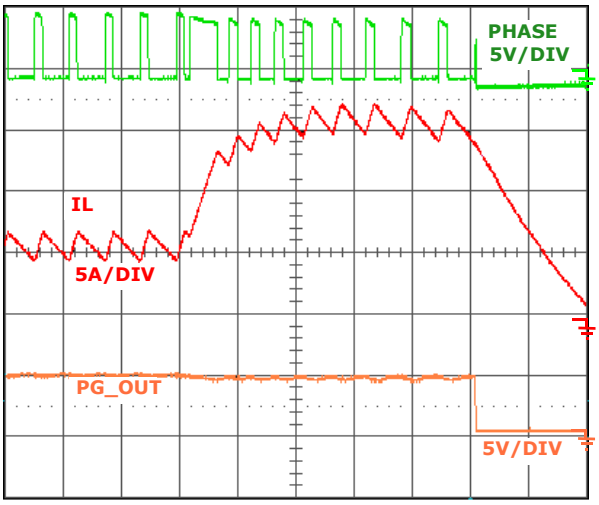


FIGURE 22. OVERCURRENT SHUTDOWN

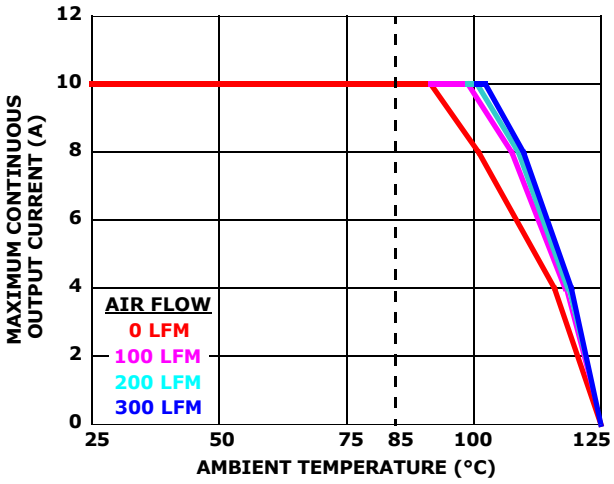


FIGURE 23. CURRENT DERATING OVER-TEMPERATURE

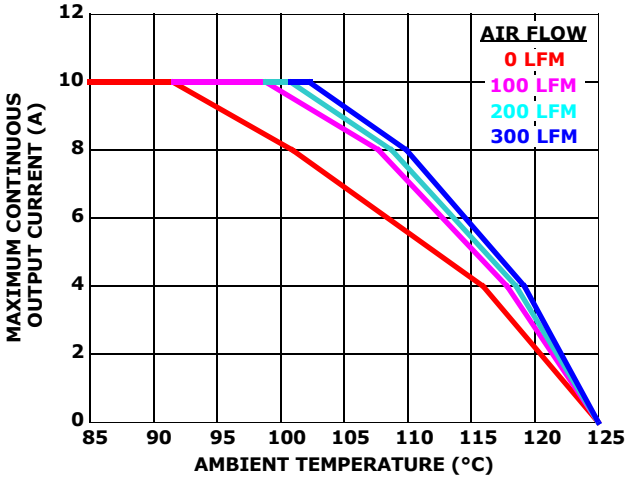


FIGURE 24. CURRENT DERATING OVER-TEMPERATURE (ZOOM)

NOTE: Figures 23 and 24 were generated on the ISL95210EVAL1Z REV B evaluation board (4-layers/2oz. copper). The test conditions were $5V_{IN}$ and $1.8V_{OUT}$. The junction temperature was characterized by measuring the shift over temperature of an integrated polysilicon resistor. For more details on the layer stack up of the evaluation board, please see the ISL95210 Application Note (AN1485).

Theory of Operation

The following sections will provide a detailed description of the inner workings of the ISL95210 10A integrated FET regulator.

Start -Up

The ISL95210 will not respond to any logic inputs until VCC and PVCC are above the power-on reset (POR) level as described in the “Electrical Specifications” Table on page 5. Once the POR condition is achieved, the ISL95210 will then acknowledge the states of its logic inputs. If the EN pin is pulled above the rising threshold, the regulator is commanded on and the soft-start sequence is initiated.

During soft-start, the programmed output voltage set point is determined by the logic states of VSEL0, VSEL1, MPCT and MSEL. The output then ramps digitally to the regulation voltage in 2.5mV/µs steps. Once the output voltage achieves regulation, the power-good monitor output (PG_OUT) is toggled high to the voltage provided on the PG_IN pin. Figure 25 illustrates the ideal soft-start behavior.

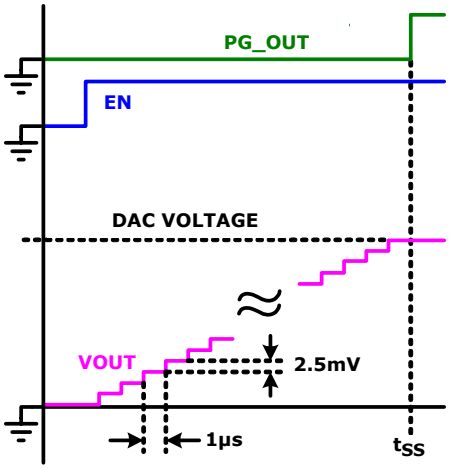


FIGURE 25. IDEALIZED SOFT-START WAVEFORM

Using the values in Tables 1 and 2, the soft-start interval can be easily calculated by Equation 1.

$$t_{SS} = \frac{V_{DAC}}{0.0025} \quad \text{(EQ. 1)}$$

The units of Equation 1 are in microseconds. For example:

- V_{DAC} = 1.200V
- t_{SS} = 1.200V / 0.0025 = 480µs

The fixed soft-start slew rate of 2.5mV/µs allows for easy calculation of the in-rush current.

$$I_{INRUSH} = (2500 \cdot C_{OUT}) \quad \text{(EQ. 2)}$$

Consequently, the in-rush is manageable for all practical values of output capacitance. For example:

- C_{OUT} = 330µF
- I_{INRUSH} = 2500*330µF = 0.825A

Output Voltage Programming

The highly integrated nature of the ISL95210 simplifies design and reduces component count. The VSEL0 and VSEL1 pins are 3-state logic inputs to an integrated DAC that controls the output voltage set point as prescribed in Table 1.

TABLE 1. DAC CONTROLLED OUTPUT VOLTAGE SETTINGS

VSEL1	VSEL0	V_{OUT} (V)
0	0	0.600
0	F	0.750
0	1	0.900
F	0	1.000
F	F	1.050
F	1	1.100
1	0	1.200
1	F	1.500
1	1	1.800

This allows the user to program the output voltage without the use of a resistor divider network. However, if the user wishes to program values of V_{OUT} away from the DAC values, a resistor divider can be used. Because the input impedance of the VOUT pin is relatively low, the top resistor in the divider stack (R1 in Figure 31) must be kept small to minimize regulation error as the internal resistance changes over-temperature and process tolerances. A 100Ω resistor is an ideal choice. The bottom resistor in the divider stack (R2 in Figure 31) can be derived from Equation 3:

$$R2 = \frac{R1 \cdot V_{DAC}}{V_{OUT} + \left(\frac{2 \cdot R1}{205k}\right) - \left(\frac{205k + R_1}{205k}\right) \cdot V_{DAC}} \quad \text{(EQ. 3)}$$

For example:

- V_{DAC} = 1.200V
- Desired V_{OUT} = 1.220V
- R1 = 100Ω
- R2 = 5.885kΩ

The use of a resistor network also limits the soft discharge feature of the ISL95210. More detail on this operation can be found in the “Soft-Discharge” on page 14.

In addition to digitally controlled output voltage programming, the ISL95210 includes the ability to margin the output voltage up and down from the set point for use in end-of-line manufacturing reliability tests. The MPCT pin controls the amount of margining desired by the user and the MSEL pin determines when margining is engaged. In all margining conditions, the output voltage is slewed to the new value at the soft-start rate of 2.5mV/µs. Table 2 shows the output voltage as dictated by MPCT and MSEL.

TABLE 2. OUTPUT VOLTAGE MARGINING CONTROL

MSEL	MPCT	RESULT
0	0	NO MARGINING
0	F	NO MARGINING
0	1	NO MARGINING
F	0	MARGIN DOWN DAC - 15%
F	F	MARGIN DOWN DAC - 10%
F	1	MARGIN DOWN DAC - 20%
1	0	MARGIN UP DAC + 15%
1	F	MARGIN UP DAC + 10%
1	1	MARGIN UP DAC + 20%

Each of the margin targets represents the DAC code nearest to the desired value. Table 3 shows the actual targets for each margin setting (see Table 4 on page 16 for the full output truth table).

TABLE 3. OUTPUT VOLTAGE MARGIN TARGETS

VOUT	-20%	-15%	-10%	+10%	+15%	+20%
0.600	0.481	0.513	0.538	0.663	0.688	0.719
0.750	0.600	0.638	0.675	0.825	0.863	0.900
0.900	0.719	0.763	0.813	0.988	1.038	1.081
1.000	0.800	0.850	0.900	1.100	1.150	1.200
1.050	0.838	0.894	0.944	1.156	1.206	1.263
1.100	0.881	0.938	0.988	1.213	1.263	1.325
1.200	0.963	1.019	1.081	1.319	1.381	1.438
1.500	1.200	1.275	1.350	1.650	1.7250	1.800
1.800	1.438	1.531	1.619	1.981	2.069	2.163

Both the DAC and margining features can be used “on the fly”, meaning the voltage can be changed during normal operation.

Regulation

R4 MODULATOR

The R^4 modulator is an evolutionary step in R^3 technology. Like R^3, the R^4 modulator allows variable frequency in response to load transients and maintains the benefits of current-mode hysteretic controllers. However, in addition, the R^4 modulator reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier. The result is a topology that can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model and removes the need for any compensation. This greatly simplifies the regulator design for customers and reduces external component count and cost.

STABILITY

The removal of compensation derives from the R^4 modulator’s lack of need for high DC gain. In traditional architectures, high DC gain is achieved with an integrator in the voltage loop. The integrator introduces a pole in the open-loop transfer function at low frequencies. That, combined with the double-pole from the output L/C filter, creates a three pole system that must be compensated to maintain stability.

Classic control theory requires a single-pole transition through unity gain to ensure a stable system. Current-mode architectures (includes peak, peak-through, current-mode hysteretic, R^3 and R^4) generate a zero at or near the L/C resonant point, effectively canceling one of the system’s poles. The system still contains two poles, one of which must be canceled with a zero before unity gain crossover to achieve stability. Compensation components are added to introduce the necessary zero.

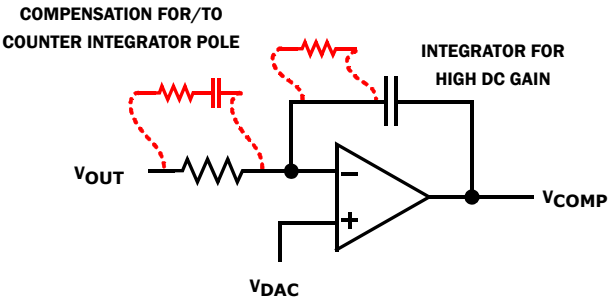


FIGURE 26. INTEGRATOR ERROR-AMPLIFIER CONFIGURATION

Figure 26 illustrates the classic integrator configuration for a voltage loop error-amplifier. While the integrator provides the high DC gain required for accurate regulation in traditional technologies, it also introduces a low-frequency pole into the control loop. Figure 27 shows the open-loop response that results from the addition of an integrating capacitor in the voltage loop. The compensation components found in Figure 26 are necessary to achieve stability.

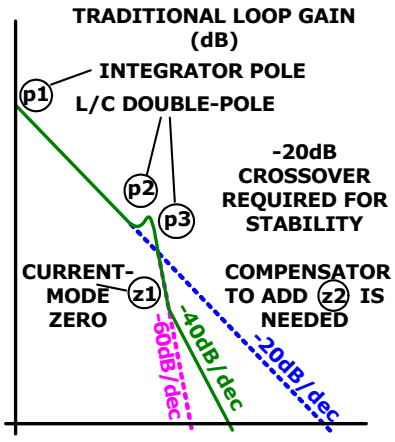


FIGURE 27. UNCOMPENSATED INTEGRATOR OPEN-LOOP RESPONSE

Because R^4 does not require a high-gain voltage loop, the integrator can be removed, reducing the number of inherent poles in the loop to two. The current-mode zero continues to cancel one of the poles, ensuring a single-pole crossover for a wide range of output filter choices. The result is a stable system with no need for compensation components or complex equations to properly tune the stability.

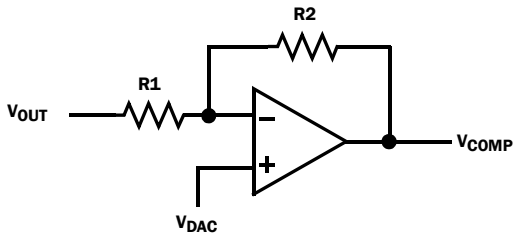


FIGURE 28. NON-INTEGRATED R4 ERROR-AMPLIFIER CONFIGURATION

Figure 28 shows the R^4 error-amplifier that does not require an integrator for high DC gain to achieve accurate regulation. The result to the open loop response can be seen in Figure 29.

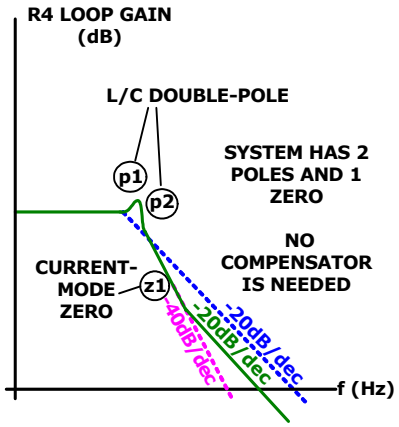


FIGURE 29. UNCOMPENSATED R4 OPEN-LOOP RESPONSE

TRANSIENT RESPONSE

In addition to requiring a compensation zero, the integrator in traditional architectures also slows system response to transient conditions. The change in COMP voltage is slow in response to a rapid change in output voltage. If the integrating capacitor is removed, COMP moves as quickly as V_{OUT}, and the modulator immediately increases or decreases switching frequency to recover the output voltage.

The dotted red and blue lines in Figure 30 represent the time delayed behavior of V_{OUT} and V_{COMP} in response to a load transient when an integrator is used. The solid red and blue lines illustrate the increased response of R^4 in the absence of the integrator capacitor.

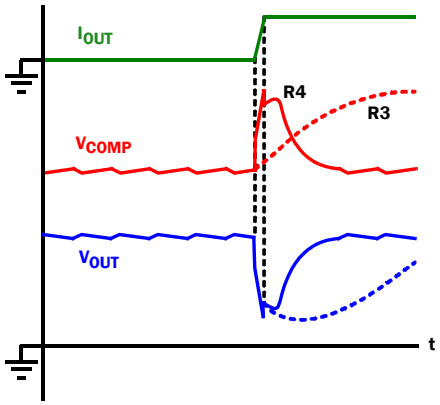


FIGURE 30. R3 vs R4 IDEALIZED TRANSIENT RESPONSE

DISCONTINUOUS CONDUCTION MODES

The ISL95210 supports two power saving modes of operation during light load conditions. If FCCM is asserted high, the regulator remains in continuous conduction mode (CCM) which offers the best transient response and the most stable operating frequency.

If the FCCM pin is pulled to ground potential, the regulator will operate in full discontinuous conduction mode (DCM). In this mode, the inductor current is monitored and prohibited from going negative. When the inductor current reaches zero, both internal power MOSFETs are turned off. The output voltage then decays solely as a function of load. The power FETs remain off until the output voltage droops enough to trigger a PWM on pulse. Because the rate of decay of V_{OUT} scales proportionally with load, so does the switching frequency. This increases efficiency as the relatively fixed power loss associated with switching the power FETs is averaged over the switching period.

If the FCCM pin is left floating, the ISL95210 will operate in audio mode DCM. This mode operates largely the same as full DCM mode with one exception; the switching period is monitored cycle by cycle. If the load diminishes to a point where the switching frequency begins to drop below ~28kHz, the ISL95210 control loop will issue a PWM on pulse to ensure the frequency remains above the upper threshold for human hearing. This allows flexibility for designs that are sensitive to audio frequency interference.

Like R^3, the R^4 architecture seamlessly enters and exits all power saving modes to ensure accurate regulation.

Protection and Shutdown Features

The ISL95210 offers a full suite of protection features to reduce the risk of damage to the IC and load. They include under and overvoltage monitoring and protection as well as protection against excessive current and thermal operating conditions.

UNDERVOLTAGE PROTECTION

If the output voltage dips too low during normal operation, the ISL95210 recognizes a fault condition and shuts down. When V_{OUT} goes 16% below V_{DAC}, the power-good monitor flags PG_OUT low and tri-states the PHASE node by turning off both integrated power MOSFETs. In addition, the soft-discharge MOSFET is turned on to gently pull the output voltage to ground potential for the next restart.

The undervoltage fault remains latched until a POR event or EN is toggled.

OVERVOLTAGE PROTECTION

During normal operation, the output voltage is monitored at all times to ensure it does not exceed the set point by more than 16%. Excessively high voltages can cause failure to output capacitors as well as the load. If V_{OUT} goes above 116% of DAC, the power-good monitor is flagged by toggling PG_OUT low and the IC enters overvoltage protection mode.

In overvoltage protection mode, the upper P-Channel MOSFET is latched off until the fault is cleared. In addition, V_{OUT} is compared against the reference DAC voltage. If V_{OUT} is above DAC, the lower N-channel MOSFET is turned on to pull V_{OUT} down. If V_{OUT} falls below DAC, the lower N-Channel MOSFET is turned off. This process repeats until the fault condition is cleared through VCC/PVCC POR or a recycling of the EN pin. This produces a soft-crowbar action that can effectively pull the output away from dangerously high voltage levels without causing the negative voltage swings on VOUT that are present with full crowbar implementations of overvoltage protection.

OVERCURRENT PROTECTION

If the current draw from the load becomes too high during operation, the IC protects itself and the load by latching off. The overcurrent mechanism is implemented as a two-fold protection scheme.

The ISL95210 continuously monitors the lower N-channel MOSFET current. It stores the valley of the inductor current each cycle and compares it against the lower overcurrent protection (OCP) threshold of 11A nominally. If the OCP threshold is achieved for 8 consecutive PWM cycles, an overcurrent fault is detected and the IC is shutdown. In this event, power-good monitor flags PG_OUT low and tri-states both switching power MOSFETs and turns on the soft-discharge FET. Inductor valley current is used to ensure that the minimum OCP threshold is above the maximum ISL95210's normal maximum load of 10A regardless of chosen inductor value.

In addition to valley current limit, the upper P-Channel MOSFET current is continuously monitored. If a catastrophic overcurrent event is encountered (e.g. short circuit on V_{OUT}), the ISL95210 immediately responds to protect the output by latching both MOSFETs off and engaging the soft-discharge FET. The power-good monitor flags PG_OUT low and the IC remains latched off until POR or EN is toggled.

THERMAL PROTECTION

The ISL95210 actively monitors the die temperature to protect against harmful thermal operating conditions. If the silicon temperature exceeds +150°C, the controller will suspend operation and shut down until the IC junction temperature falls below +135°C. Once the temperature has fallen below the lower protection threshold, the IC will resume normal operation following a POR event or toggling of the EN input.

POWER-GOOD MONITOR

A status indicator is provided to inform the system whether or not the ISL95210 output voltage is in regulation or if a fault has occurred. If VCC and PVCC are above the POR threshold, the part is enabled, and no faults have been detected, PG_OUT will toggle high.

The power-good monitor is a CMOS configuration (refer to the "Functional Block Diagram" on page 2). This allows the user to provide any voltage to indicate when power is good. The voltage provided on to the PG_IN pin will be used as the logic high value for PG_OUT. This has the advantage over open-drain configurations of saving a pull-up resistor. A pull-up resistor on PG_OUT can still be used if desired. In this configuration, the PG_IN pin needs to be floated.

SOFT-DISCHARGE

To ensure a known operating condition when the ISL95210 is in a standby state, the VOUT pin is actively discharged to PGND through an integrated 45Ω MOSFET. The MOSFET is commanded on if the EN pin is pulled low or if any of the previously mentioned fault conditions are achieved with the exception of overvoltage, which actively pulls down on V_{OUT} as a matter of protection.

It should be noted that if an external resistor divider is used to program V_{OUT} to values not found in the DAC table, the soft-discharge feature will be negatively impacted. Figure 31 illustrates this condition.

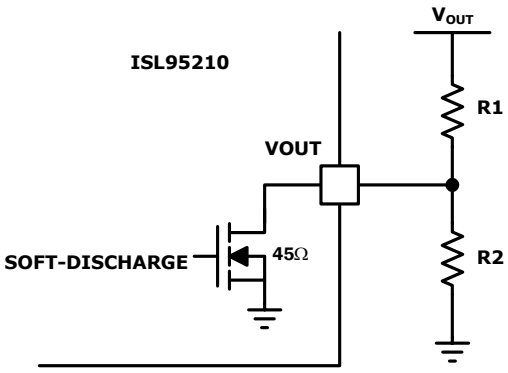


FIGURE 31. SIMPLIFIED SOFT-DISCHARGE CIRCUIT

The discharge resistance is increased by the presence of the resistor divider. The total discharge resistance is expressed in Equation 4:

$$-R_{DCHRG} = (45\Omega \text{ II } R2) + R1 \quad \text{(EQ. 4)}$$

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is written as Equation 5:

$$D = \frac{V_O}{V_{IN}} \quad \text{(EQ. 5)}$$

The output inductor peak-to-peak ripple current is written as Equation 6:

$$I_{PP} = \frac{V_O \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 6)}$$

A typical step-down DC/DC converter will have an I_{P-P} of 20% to 40% of the maximum DC output load current. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated by Equation 7:

$$P_{COPPER} = I_{LOAD}^2 \cdot DCR \quad \text{(EQ. 7)}$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written as Equation 8:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad \text{(EQ. 8)}$$

and Equation 9:

$$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}} \quad \text{(EQ. 9)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 32 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for a converter efficiency of 80%. The ripple current calculation is written as Equation 10:

$$I_{IN\_RMS,\,NORMALIZED} = \sqrt{(D - D^2) + \left(D \cdot \frac{x^2}{12}\right)} \quad \text{(EQ. 10)}$$

where:

- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 11:

$$D = \frac{V_O}{V_{IN} \cdot EFF} \quad \text{(EQ. 11)}$$

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

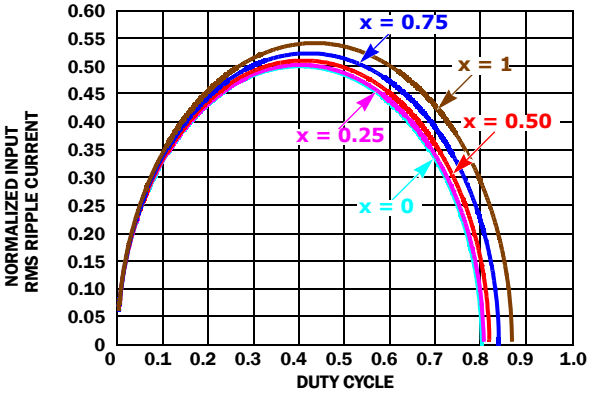


FIGURE 32. NORMALIZED RMS INPUT CURRENT

Layout Considerations

It is important to place power components as close as possible to the devices they decouple. Figure 33 provides an example of proper power component placement for the ISL95210. The colored shapes represent the following power planes:

PGND PHASE

VIN VOUT

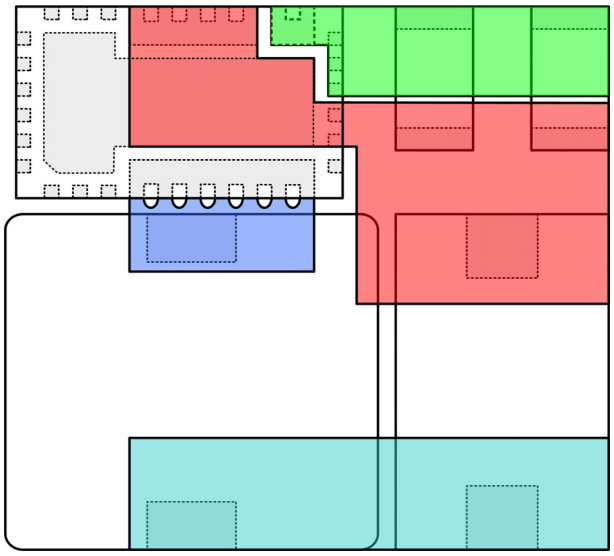


FIGURE 33. ISL95210 POWER COMPONENT LAYOUT EXAMPLE

Input capacitors are placed directly across VIN and PGND to filter switching currents between the PMOS and NMOS power FETs. The output inductor is placed directly adjacent to the PHASE pins.

Its “north-south” arrangements easily allow for the output voltage decoupling capacitor to be placed with its ground terminal very near the input capacitors grounds and the PGND pins of the ISL95210. This provides a low impedance return path for the inductor ripple current. This is one possible arrangement that will result in a good layout.

The analog ground connection (not shown) should be connected directly to the ground plane through a via. The VCC decoupling capacitor should be placed next to the VCC and AGND pins for optimal noise rejection.

Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly between VIN and PGND to suppress the turn-off voltage spike. This is achieved by placing the MLCC as close to the IC as possible and adjacent to VIN and PGND.

TABLE 4. OUTPUT VOLTAGE TRUTH TABLE

MSEL	MPCT	VSEL1	VSEL0	VOUT
F	1	0	0	0.48125
F	0	0	0	0.51250
F	F	0	0	0.53750
0	0	0	0	0.60000
0	F	0	0	0.60000
0	1	0	0	0.60000
F	1	0	F	0.60000
F	0	0	F	0.63750
1	F	0	0	0.66250

TABLE 4. OUTPUT VOLTAGE TRUTH TABLE (Continued)

MSEL	MPCT	VSEL1	VSEL0	VOUT
F	F	0	F	0.67500
1	0	0	0	0.68750
F	1	0	1	0.71875
1	1	0	0	0.71875
0	0	0	F	0.75000
0	F	0	F	0.75000
0	1	0	F	0.75000
F	0	0	1	0.76250
F	1	F	0	0.80000
F	F	0	1	0.81250
1	F	0	F	0.82500
F	1	F	F	0.83750
F	0	F	0	0.85000
1	0	0	F	0.86250
F	1	F	1	0.88125
F	0	F	F	0.89375
0	0	0	1	0.90000
0	F	0	1	0.90000
0	1	0	1	0.90000
F	F	F	0	0.90000
1	1	0	F	0.90000
F	0	F	1	0.93750
F	F	F	F	0.94375
F	1	1	0	0.96250
F	F	F	1	0.98750
1	F	0	1	0.98750
0	0	F	0	1.00000
0	F	F	0	1.00000
0	1	F	0	1.00000
F	0	1	0	1.01875
1	0	0	1	1.03750
0	0	F	F	1.05000
0	F	F	F	1.05000
0	1	F	F	1.05000
F	F	1	0	1.08125
1	1	0	1	1.08125
0	0	F	1	1.10000
0	F	F	1	1.10000
0	1	F	1	1.10000
1	F	F	0	1.10000
1	0	F	0	1.15000
1	F	F	F	1.15625

TABLE 4. OUTPUT VOLTAGE TRUTH TABLE (Continued)

MSEL	MPCT	VSEL1	VSEL0	VOUT
0	0	1	0	1.20000
0	F	1	0	1.20000
0	1	1	0	1.20000
F	1	1	F	1.20000
1	1	F	0	1.20000
1	0	F	F	1.20625
1	F	F	1	1.21250
1	0	F	1	1.26250
1	1	F	F	1.26250
F	0	1	F	1.27500
1	F	1	0	1.31875
1	1	F	1	1.32500
F	F	1	F	1.35000
1	0	1	0	1.38125
F	1	1	1	1.43750
1	1	1	0	1.43750
0	0	1	F	1.50000
0	F	1	F	1.50000
0	1	1	F	1.50000
F	0	1	1	1.53125
F	F	1	1	1.61875
1	F	1	F	1.65000
1	0	1	F	1.72500
0	0	1	1	1.80000
0	F	1	1	1.80000
0	1	1	1	1.80000
1	1	1	F	1.80000
1	F	1	1	1.98125
1	0	1	1	2.06875
1	1	1	1	2.16250

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/18/11	FN6938.2	Added “32 Lead, 6mmx4mm QFN Package” to “Features” on page 1.
5/10/11	FN6938.1	Initial Release to web.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL95210

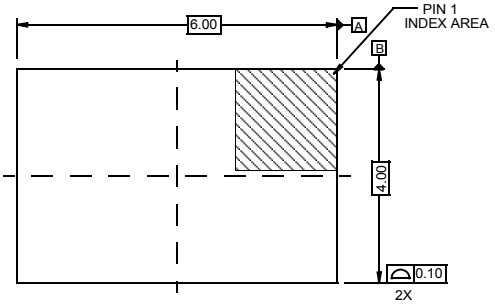
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

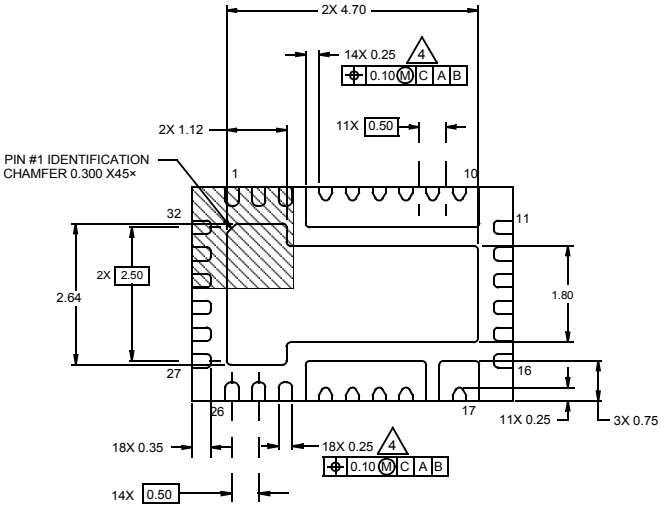
Package Outline Drawing

L32.6x4B

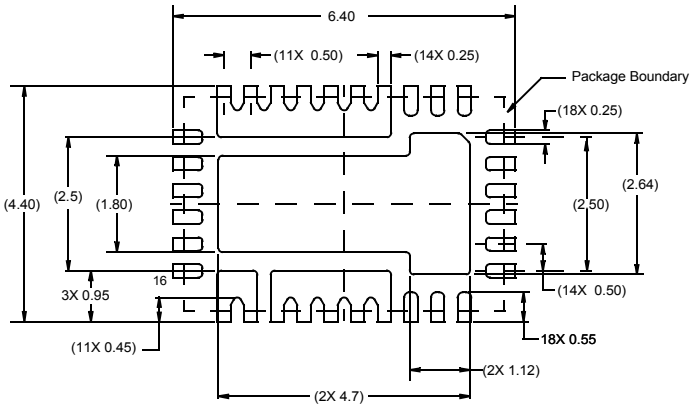
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 09/08



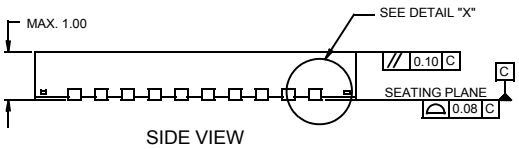
TOP VIEW



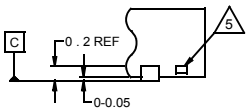
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.