

AC1016 • ACT1016

NATIONAL SEMICONDUCTOR LOGIC DATA SHEET 6501122 0062744 4

54AC/74AC1016 • 54ACT/74ACT1016

16 × 16 Parallel Multiplier

T-45-07

Description

The 'AC/ACT1016 is a high-speed, low power 16 × 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT technology, the '1016 offers a very low power alternative and exceptional performance.

The 'AC/ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'AC/ACT1016 operates from a single Vcc supply and is compatible with standard TTL logic levels.

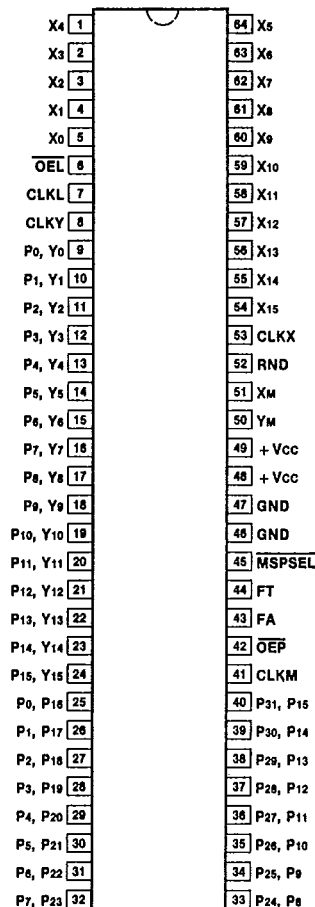
The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by $\overline{OEL}$ and the output port 3-state control is controlled by $\overline{OEP}$. The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the twos complement X and Y mode controls, Xm and Ym, respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

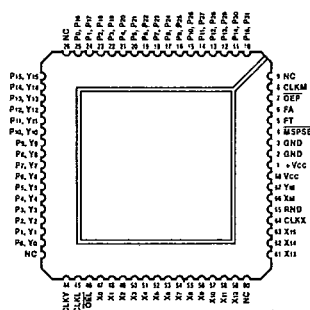
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

- 16 × 16 Parallel Multiplier
- Selectable Rounding Modes
- Twos Complement, Unsigned Magnitude and Mixed Mode Multiplication
- Pin and Functionally Compatible with TRW MPY016H
- Provides Low Voltage, High-Speed Operation
- Single Vcc Supply
- ± 2000 V ESD Protection
- Source/Sink 8 mA
- 3-State Outputs
- 'ACT1016 has TTL-Compatible Inputs

Connection Diagrams



Pin Assignment for DIP



Pin Assignment for PCC

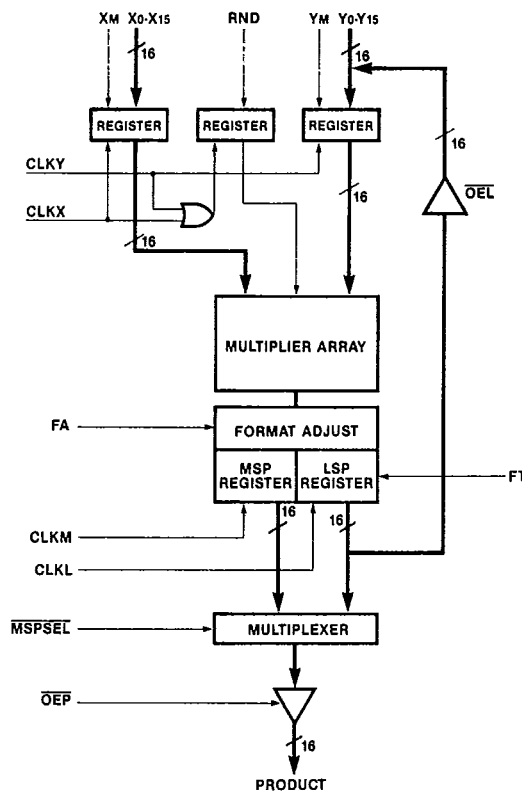
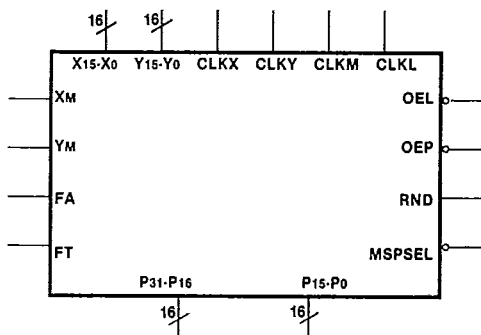
Ordering Code: See Section 6

Logic Diagram

Pin Names

X ₁₅ - X ₀	Multiplicand Data Inputs
Y ₁₅ - Y ₀	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
CLKM	Input Clock, MSP
CLKL	Input Clock, LSP
X _M , Y _M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{\text{OEL}}$	3-State Enable, LSP Routing
$\overline{\text{OEP}}$	3-State Enable, Product Output Port
RND	Round Control, MSP
MSPSEL	MSP Select
P ₃₁ - P ₁₆	MSP Outputs
P ₁₅ - P ₀	LSP Outputs

Logic Symbol



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Signal Descriptions

Inputs

XIN (X15 - X0)

Sixteen multiplicand data inputs.

YIN (Y15 - Y0)

Sixteen multiplier data inputs. This is also an output port for P15 - P0.

Input Clocks

CLKX

The rising edge of this clock loads the X15 - X0 data input register along with the X mode and round registers.

CLKY

The rising edge of this clock loads the Y15 - Y0 data input register along with the Y mode and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL

The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

X_M, Y_M

Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA

When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT

When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

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OEL

The OEL input is the 3-state enable for routing LSP through YIN/LSPOUT port.

OEP

The OEP is the 3-state enable for the product output port.

RND

The Round control is used for the rounding of the MSP. When this control is HIGH, a '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2⁻¹⁶ bit (P14). If FA is HIGH when RND is HIGH, a '1' will be added to the 2⁻¹⁵ bit (P15). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

MSPSEL

When MSPSEL is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP (P31 - P0)

The MSP is the Most Significant Product output.

LSP (P15 - P0)

The LSP is the Least Significant Product output.

Y15-0/LSPOUT (Y15 - Y0 or P15 - P0)

This is the Least Significant Product (LSP) output available when OEL is LOW. It is also an output port for Y15 - Y0.

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Figure 1: Fractional Twos Complement Notation

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BINARY POINT

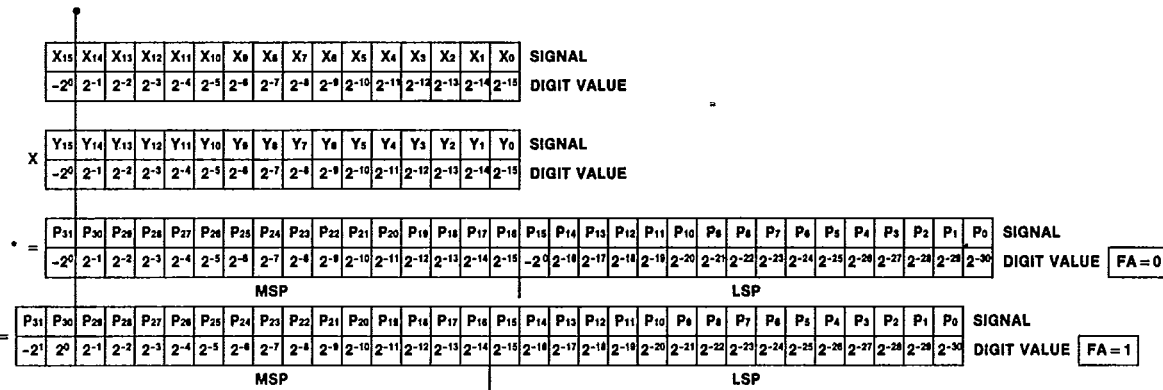


Figure 2: Fractional Unsigned Magnitude Notation

BINARY POINT

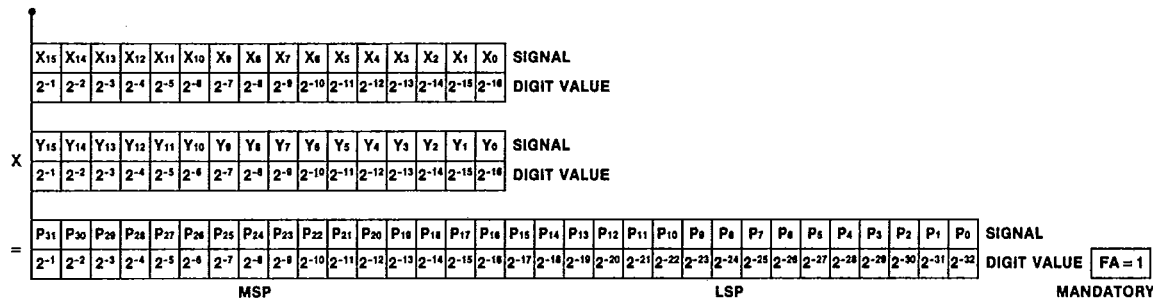
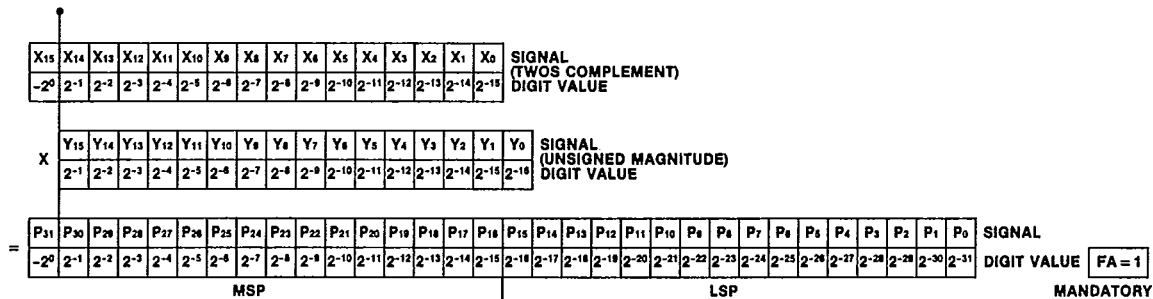


Figure 3: Fractional Mixed-Mode Notation

BINARY POINT



*In this format an overflow occurs in the attempted multiplication of the two's complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2³⁰ in the integer case.

Figure 4: Integer Twos Complement Notation

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BINARY POINT

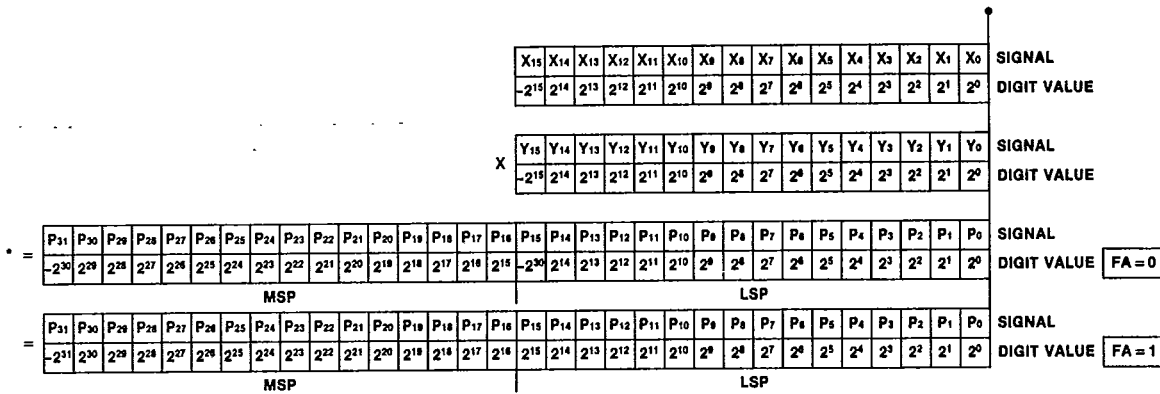


Figure 5: Integer Unsigned Magnitude Notation

BINARY POINT

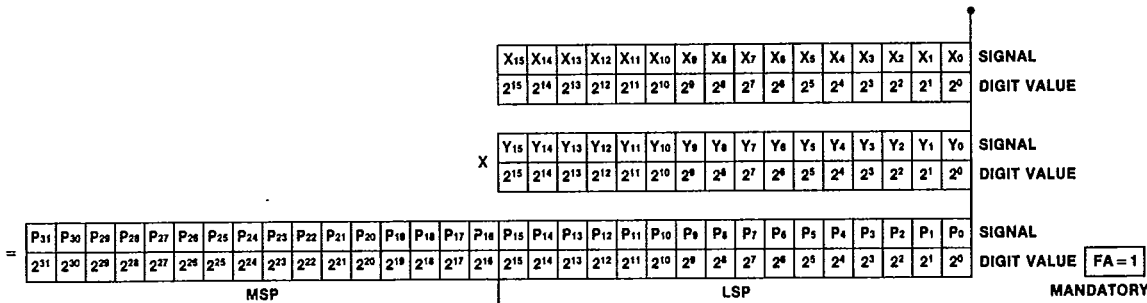
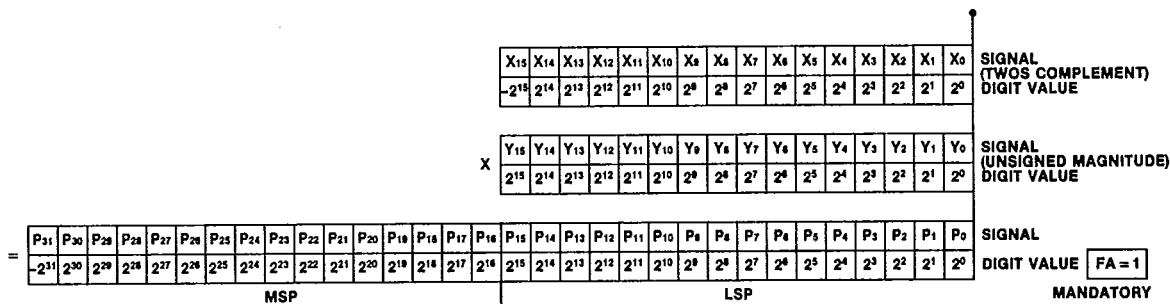


Figure 6: Integer Mixed Mode Notation

BINARY POINT



*In this format an overflow occurs in the attempted multiplication of the twos complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2³⁰ in the Integer case.

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Recommended Operating Conditions

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Symbol	Parameter	Conditions	Limits	Units
V _{CC}	Supply Voltage (unless otherwise specified)		2.0 to 6.0	V
V _I	Input Voltage		0 to V _{CC}	V
V _O	Output Voltage		0 to V _{CC}	V
T _A	Operating Temperature	74AC/ACT 54AC/ACT	-40 to +85 -55 to +125	°C °C
S _r	Maximum Slew Rate (except for Schmitt inputs)	V _{IN} V _{meas} V _{CC} @4.5V V _{CC} @5.5V	0.8 to 2.0 0.8 to 2.0 10.0 8.0	V V ns ns

Absolute Maximum Ratings*

Symbol	Parameter	Conditions	Limits	Units
V _{CC}	Supply Voltage		-0.5 to 7.0	V
I _{IK}	DC Input Diode Current or DC Input Voltage	V _I = 0.5 V _I = V _{CC} + 0.5	-20 20 -0.5 to V _{CC} + 0.5	mA mA V
I _{OK}	DC Output Diode Current or DC Output Voltage	V _O = -0.5 V _O = V _{CC} + 0.5	-20 20 -0.5 to V _{CC} + 0.5	mA mA V
I _O	DC Output Source or Sink Current, Per Output Pin		±15	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current		±20	mA
T _{STG}	Storage Temperature		-65 to +150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

AC Test Conditions

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 7 and 8

Capacitance

Symbol	Parameter	Max	Unit	Conditions
C _{IN}	Input Capacitance	7.0	pF	V _{IN} = 0 V
C _{OUT}	Output Capacitance	5.0	pF	V _{OUT} = 0 V

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

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Symbol	Parameter	74AC/ACT	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I _{IN}	Maximum Input Current		± 0.1	± 10.0	± 1.0	μA V _{CC} = Max V _{IN} = V _{CC} , 0
I _{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA High Z, V _{CC} = Max V _{OUT} = 0, V _{CC}
I _{CCQ}	Supply Current, Quiescent	0.50	2.0	10.0	10.0	mA V _{CC} = Max, V _{IN} = 0 V
I _{CCD}	Supply Current, 12.4 MHz Loaded	300		325	325	mA V _{CC} = Max, f = 12.4 MHz Test Load: See Note 1
I _{CCD}	Supply Current, 20 MHz Loaded	325		350	350	mA V _{CC} = Max, f = 20 MHz Test Load: See Note 1
V _{OH} *	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA, V _{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA, V _{CC} = 5.5 V
			3.86	3.70	3.76	V I _{OH} = -8 mA, V _{CC} = 4.5 V
			4.86	4.70	4.76	V I _{OH} = -8 mA, V _{CC} = 5.5 V
V _{OL} *	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V V _{IN} = V _{IL} or V _{IH} , I _{OUT} = 50 μA, V _{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V V _{IN} = V _{IL} or V _{IH} , I _{OUT} = 50 μA, V _{CC} = 5.5 V
			0.45	0.50	0.50	V I _{OL} = 8 mA, V _{CC} = 4.5 V
			0.45	0.50	0.50	V I _{OL} = 8 mA, V _{CC} = 5.5 V
I _{OLD}	Minimum Dynamic Output Current			32	32	mA V _{CC} = 5.5 V, V _{OLD} = 2.2 V. See Note 2.
I _{OH}	Minimum Dynamic Output Current			- 32	- 32	mA V _{CC} = 5.5 V, V _{OH} = 3.3 V. See Note 2.

Note 1: Test Load 50 pF, 500 ohm to Ground

Note 2: Only one output loaded at a time, maximum duration of test 2 ms.

*All outputs loaded.

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	54AC				74AC				Units	Fig. No.
			TA = - 55°C to + 125°C				TA = - 40°C to + 85°C					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
tMUC	Unclocked Multiply Time	3.3 5.0									ns	11
tMC	Clocked Multiply Time	3.3 5.0									ns	11, 12
tPDSEL	MSPSEL to Product Out	3.3 5.0									ns	11
tPDP	Output Clock to P	3.3 5.0									ns	11
tPDY	Output Clock to Y	3.3 5.0									ns	11
tENA	3-State Enable Time ²	3.3 5.0									ns	10
tDIS	3-State Disable Time ²	3.3 5.0									ns	10
tHCL	Clock LOW Hold Time CLKXY Relative to CLKML ¹	3.3 5.0									ns	11, 12
ts	Setup Time X,Y, RND	3.3 5.0									ns	9, 11
th	Hold Time X, Y, RND	3.3 5.0									ns	9, 11
tw	Clock Pulse Width HIGH or LOW	3.3 5.0									ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ± 500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 3.3 is 3.3 V $\pm$ 0.3 V

Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	54ACT				74ACT				Units	Fig. No.
			TA = - 55°C to + 125°C				TA = - 40°C to + 85°C					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
tMUC	Unlocked Multiply Time	5.0						80.0		65.0	ns	11
tMC	Clocked Multiply Time	5.0						65.0		55.0	ns	11, 12
tPDSSEL	MSPSEL to Product Out	5.0						13.0		13.0	ns	11
tPDP	Output Clock to P	5.0						20.0		20.0	ns	11
tPDY	Output Clock to Y	5.0						20.0		20.0	ns	11
tENA	3-State Enable Time ²	5.0						10.0		10.0	ns	10
tDIS	3-State Disable Time ²	5.0						12.5		12.5	ns	10
tHCL	Clock LOW Hold Time CLKXY Relative to CLKML ¹	5.0					0		0		ns	11, 12
ts	Setup Time X,Y, RND	5.0					5.5		5.5		ns	9, 11
th	Hold Time X, Y, RND	5.0					1.0		1.0		ns	9, 11
tw	Clock Pulse Width HIGH or LOW	5.0					3.5		3.5		ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ± 500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 7: AC Output Test Load

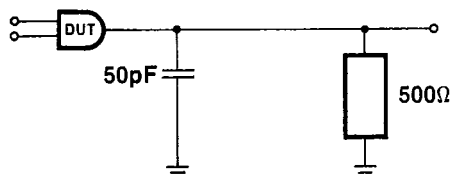


Figure 8: Output 3-State Delay Load

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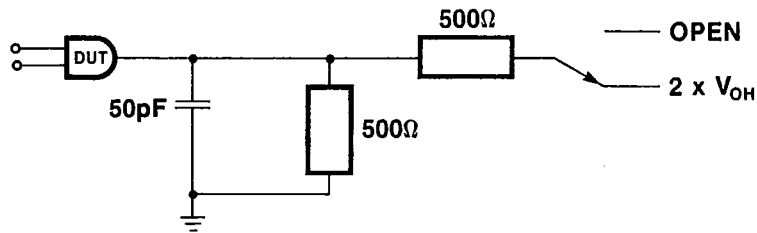
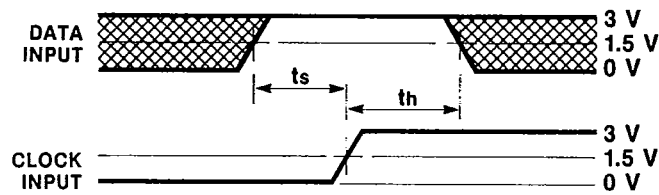


Figure 9: Setup and Hold Time



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Figure 10: 3-State Control Timing Diagram

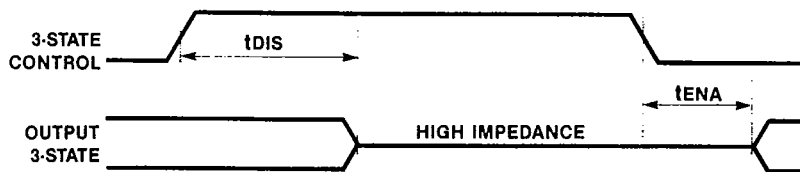


Figure 11: '1016 Timing Diagram

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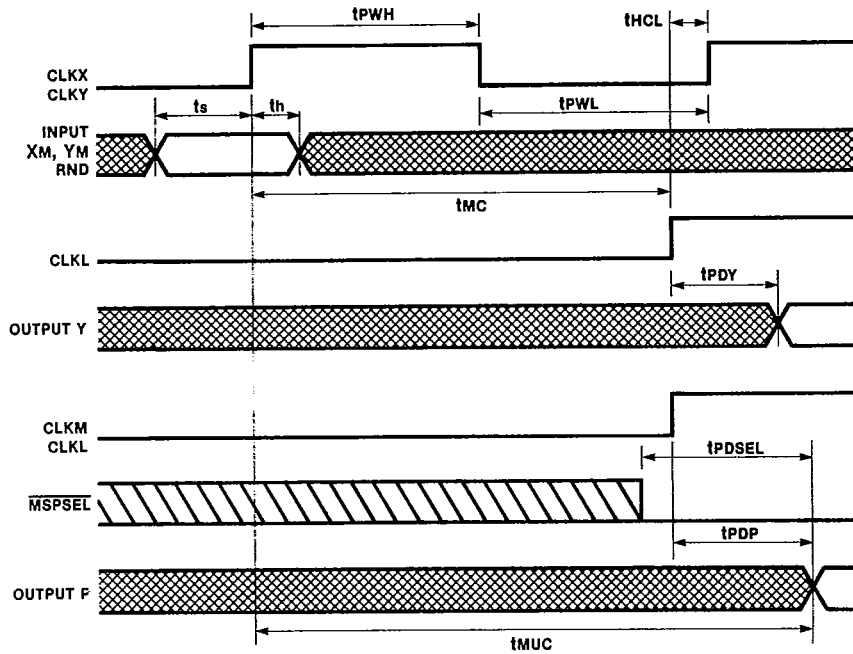


Figure 12: Simplified Timing Diagram — Typical Application

