Integrated
Circuit
Systems, Inc.

ICS2010
Product Preview

SMPTE / MIDI Time Code Processor

General Description

The ICS2010, SMPTE/MIDI chip, is a VLSI device designed in a low power CMOS process. This device provides the timing coordination for Multimedia sight and sound events. Although it is aimed at a PC Multimedia environment, the SMPTE/MIDI chip is easily integrated into products requiring SMPTE time code generation and/or reception in LTC (Longitudinal Time Code) or VITC (Vertical Interval Time Code) formats and MTC (MIDI Time Code) translation.

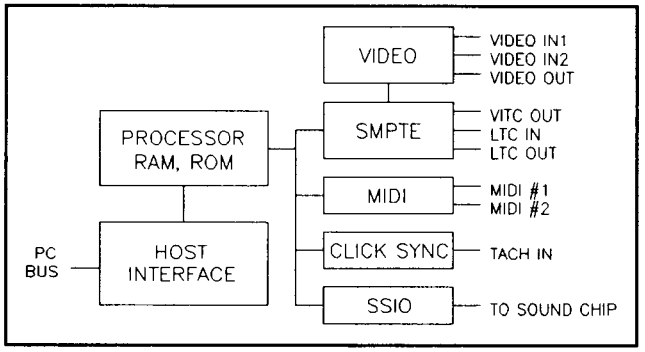
Taking its input from NTSC video, S-Video or an audio track, the ICS2010 can read SMPTE time code in VITC and LTC formats or MTC from a MIDI port. If no time code source is available, time codes can be internally generated. Time code output formats are, LTC, VITC and MTC. All are available simultaneously.

The embedded microprocessor, a 65C02, provides intelligence for time code modifications, corrections and translation between different formats.

The host interface is compatible with the IBM PC, and ISA bus compatible computers and is easily interfaced to other processors.

There are two sets of MIDI ports on the ICS2010. Each may be accessed by the host bus or by the embedded microprocessor to act as an intelligent MIDI port.

Special interface hooks have been added to send time code information to the DOC ICS, sound generator.



Block Diagram

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Features

Microprocessor based control

Internal and external sync sources
- Genlock to video or house sync inputs
- internally generated timing from oscillator input
- external click input

LTC and VITC Generators
- Real Time SMPTE Rates
  - o 30 Hz (B&W, some audio)
  - o 29.97 Hz (NTSC)
  - o 25 Hz (PAL)
  - o 24 Hz (film)
- Time Code Modes
  - o Drop Frame
  - o Color Frame
- VITC can be inserted on lines 10-41 (SMPTE specifies lines 10-20)
- update all data (time code, user data, and flag bits) on a frame by frame basis. This allows for "Jam Sync", "freewheeling", error bypass/correction, plus-one-frame and other intelligent generator functions.

LTC Receiver
- Meets SMPTE and EBU LTC specifications including drop frame, color frame, time data, user data and status bits
- Synchronize bit rates from 1/30th nominal to 80X nominal playback speed

VITC reader
- Reads code from any or all selected scan lines.
- Meets SMPTE VITC specifications including, drop frame, color frame, time data, user data and status bits

SMPTE to MTC conversion
- convert from any SMPTE source
- supports MIDI quarter frame and full messages

Time Code Burn-in Window selectable to overlay video with programmable screen position

PACKAGE PINOUT

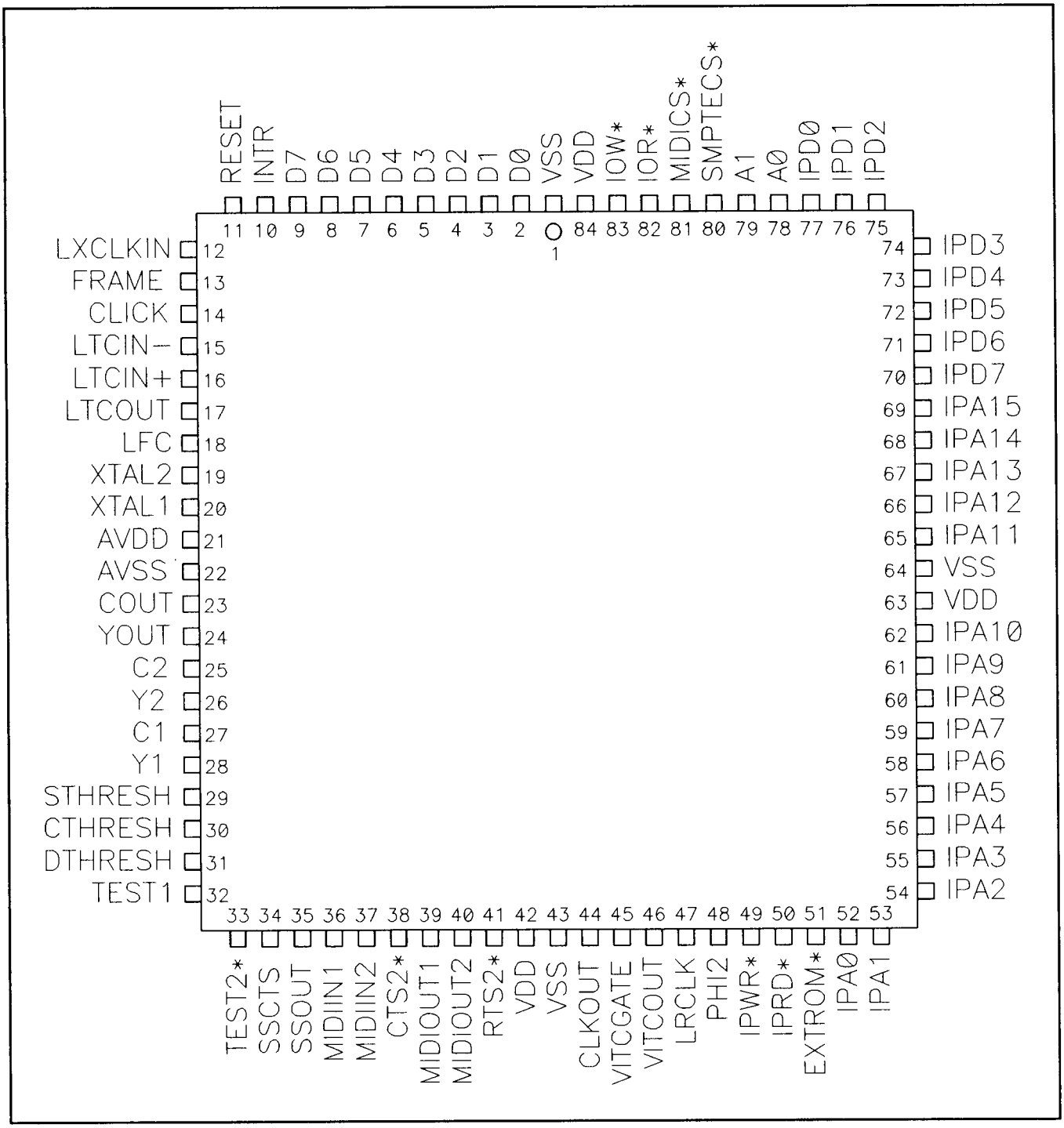


Figure 2 ICS2010 Pinout

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
Y1, Y2	AI	Video inputs from camera or other NTSC source. NOTE: This is also the Y (Luma) input for S-VHS and HI-8 systems.
C1, C2	AI	C (Chroma) inputs for S-VHS and HI-8 systems. For NTSC systems, tie to Y input through a capacitor. See applications note.
DTHRESH	AI	Data Threshold bypass input.
STHRESH	AI	SYNC Threshold bypass input.
CTHRESH	AI	Clamp Threshold bypass input.
YOUT	AO	NTSC video output. This is also the Y (Luma) output in S-Video mode.
COUT	AO	C (Chroma) output for S-VHS and HI-8 systems.
FRAME	AI	Frame A/B input.
CLICK	AI	LTC SYNC input.
LTCIN+	AI	SMPTE LTC input +.
LTCIN-	AI	SMPTE LTC input -.
LTCOUT	AO	SMPTE LTC output.
LTXCLKIN	I	SMPTE External LTC transmit clock.
LXCLK	O	SMPTE LTC transmit clock output.
LTCSYNC	O	SMPTE LTC transmit SYNC output.
LRCLK	O	SMPTE LTC receive clock output.
VITC	O	SMPTE VITC output to video mixer circuit.
VITCGATE	O	VITC gate indicates VITC code is being output for video overlay.
MIDIIN1,2	I	MIDI input ports 1 and 2.
MIDIOUT1,2	O	MIDI output ports 1 and 2.
CTS2*	I	Clear to Send port 2.
RTS2*	O	Ready to Send port 2.
XTAL1	I	14.318 MHz crystal input. This pin may be driven directly from a TTL 14.318 MHz source.
XTAL2	O	14.318 MHz crystal oscillator output.
LFC	AI	External RC circuit.
A1-A0	I	Address bus.
IOR*	I	Read Enable (active low)
IOW*	I	Write Enable (active low)
SMPTECS*	I	SMPTE port chip select (active low)
MIDICS*	I	MIDI ports chip select (active low)
RESET	I	Master reset (active high)
D7-D0	I/O	Bi-directional data bus
INTR	O	Interrupt Request (active high)
SSOUT	O	Synchronous Serial Data Output
SSCTS	I	Synchronous Serial Clear to Send (active high)
CLKOUT	O	Synchronous Serial Output Clock

A - Analog I - Input
P - Power O - Output

Pin Description (continued)

PIN	TYPE	DESCRIPTION
IPA15-IPA0	O	Internal processor address bus
IPD7-IPD0	I/O	Internal processor data bus
IPWR*	O	Internal processor write strobe (active low)
IPRD*	O	Internal processor read strobe (active low)
PHI2	O	Internal processor bus cycle clock
EXTROM*	I	External ROM enable (active low)
TEST1	I	Test mode (1 - test, 0 - normal operation)
TEST2*	I	Test mode (1 - normal operation, 0 - test)
AVDD	P	Analog V_{DD}
AGND	P	Analog Ground
VDD	P	Digital V_{DD}
GND	P	Digital Ground

A - Analog I - Input
P - Power O - Output

Functional Description

The following is a functional description of the hardware registers in the ICS2010 chip. It also describes how those registers can be utilized by the software to facilitate specific application services.

Hardware Environments

A 65C02 processor embedded in the ICS2010 allows it to operate as a peripheral to a host processor such as a PC, or it can stand-alone. These will be referred to as "host mode" and "stand-alone mode". The mode is selected when the RESET pin goes inactive. If SMPTECS* and MIDICS* are low when RESET goes inactive, stand-alone mode is selected. Otherwise, host mode is selected.

LTC Input

LTCIN is an analog input feeding a comparator with hysteresis. It requires capacitive coupling to the LTC source. The output of the comparator goes to the LTC receiver which is capable of receiving LTC in a forward or backward direction at a rate from 1/30th to 80x nominal frame rates. The incoming LTC data is sampled with a phase locked clock and loaded into the receive buffer following the receipt of a valid LTC SYNC pattern. When a complete frame has been received, an interrupt to the control processor is generated.

LTC Output

The LTC output can be analog or digital. When set up as an analog output it can drive a Hi-Z load.

The LTC generator outputs a LTC frame at the selected frame rate, 24Hz, 25Hz, 29.97Hz or 30Hz, and starts the frame based on a start time generated by the selected SYNC source.

Video Inputs

There are two sets of video inputs. In an composite NTSC or PAL system, the Y input is the only one used. It is capacitively coupled to the source. In S-Video systems, capacitively couple Y and C to their respective sources. Proper termination of the source should be observed. One of the two video sources is selected by the VIDSEL bit in the SMPTE control registers as the video SYNC source. Internal timers are synchronized with the incoming video to extract timing information used to receive and generate VITC.

The VITC receiver samples the incoming video looking for a valid VITC code on selected scan lines. When a valid code is received it is written to a VITC receive buffer. More than one line can contain VITC code, and the codes can be different. For this reason, VITC codes from selected lines of a frame are written to separate VITC buffers.

Video Output

The video output combines the selected video input with the outputs from the VITC generator and the character generator. It can be a composite or an S-Video output as selected by the SVID bit in the SMPTE control registers.

VITC code is generated from data in the VITC generator buffer and output during the selected line time(s). The CRC and synchronizing bits are automatically generated by the VITC generator, but all of the data fields are sent directly from the buffer with no modification.

A character generator is provided to insert the time code in a burn-in window which overlays the incoming video. The vertical and horizontal position of the burn-in window is programmable.

MIDI Ports

Two UARTs are provided for MIDI ports. Each can function as a MIDI IN and a MIDI OUT. Each can generate an interrupt on receiver full and/or transmitter empty to the host system via the INTR pin. One of the UARTs supports modem controls so that it can be used as a generic serial control port.

SMPTE SYNC Sources

A time code generator must have a SYNC input from a stable source in order to position the LTC code properly on a audio track of video tape or film. Three SYNC sources, video, click input, and free running, are available. In the case of a video tape, LTC code must start within plus or minus one line of the beginning of line 5. This requires "Gen-Locking" to the incoming video. The video timing section locks to the video's horizontal and vertical SYNC signal and generates a SMPTE SYNC. If some external SYNC source is available it can be input on the CLICK input. Otherwise, a free running SMPTE SYNC is generated from the oscillator at the selected frame rate.

Video Timing Generator

The video timing generator is "Gen-Locked" to the video input's SYNC separator. It extracts NTSC or PAL timing information from the video input and generates line and pixel rate timing for the VITC receiver, VITC generator, LTC generator and character generator. If

no video input is present, it generates free running timing.

Overlay Character Generator
It is sometimes desirable to display the time code on a video display along with the picture. A character generator is provided for that purpose. The time code display, or burn-in window, can be positioned anywhere on the screen.

Synchronous Serial Output Port
A synchronous serial output port is provided to send timing information to a music output device such as the DOC ICS. Bytes are sent with one start bit and one stop bit at the oscillator clock rate. In order for the receiver to keep from overflowing its buffer, the SSCTS input, when low, holds off the sending of the next byte. SSCTS can go low during a byte transmission without halting the data stream. It will complete the transmission of the byte.

INTR Output
The INTR output pin is the interrupt source from ICS2010 to the host processor. There are three devices within ICS2010 which can activate INTR. They are the 65C02 host interface and the two MIDI emulation ports. Each has its own interrupt enable bit in its associated control/command register.

External Memory
The ICS2010 is supplied with a pre-programmed 4K byte internal ROM which supports the functionality detailed in the "Software Interface" section of this document. However, the ICS2010 can be made to access an external memory for its initialization and functional microcode by driving the EXTROM* input pin low. This will cause all memory accesses made by the embedded 65C02 within an address range of 0300h to FFFFh to be to or from external memory. Pins IPA15-IPA0, IPD7-IPD0, IPWR*, IPRD* and PHI2 provide the interface to external memory. Accesses of addresses 0000h to 02FFh are always made to registers and RAM internal to the ICS2010.

Host CPU Interface

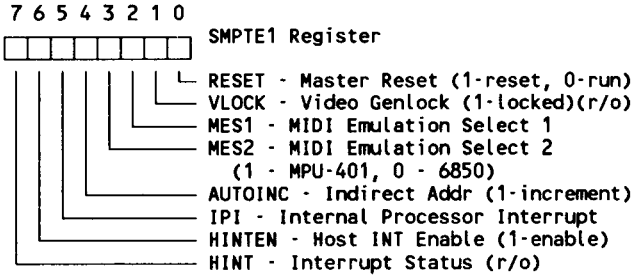
The ICS2010 supports standard microprocessor interfaces and busses, such as the PC bus, to allow access of eight control/status and data registers. These eight registers are organized into two groups of four registers, one set for SMPTE control and the other set for direct MIDI port control. Each set of registers is selected with its own chip select, SMPTECS* and MIDICS*.

SMPTE Registers

The SMPTE register set allows access to 258 available registers. The first two are direct access registers addressed at locations 0 and 1. The remaining 256 registers are accessed by writing an indirect register address into location 2 and reading from or writing to location 3. If the AUTOINC bit in SMPTE1 is set to 1 the indirect register address is automatically incremented after an access to location 3. This eases the task of reading or writing sequential indirect locations.

All of the indirect registers are given soft definitions, because they are controlled by the internal processor's firmware. See the applications section for an example.

SMPTECS*	A1	A0	Register
0	0	0	SMPTE1 Control/Status
0	0	1	SMPTE2 Soft Status
0	1	0	Indirect Register Address
0	1	1	Indirect Register Data



RESET - This is the master reset bit for the chip. It resets the internal processor and hardware. The bit will come up zero, allowing the embedded processor to run with no external intervention required. The host processor can use this bit to reset the ICS2010 and to cause the embedded processor to re-execute its power-on confidence routine. Both a set and then a reset of this bit must be performed by the host processor in order to perform a master reset operation. While this bit is set to one, the host processor will not be able to access the internal RAM.

VLOCK - This is a hardware driven bit which indicates that genlock has been achieved with the selected video source.

MES1, MES2 - These bits select the UART emulation mode. When set, MPU-401 emulation mode is selected. When reset to zero, 6850 emulation mode is selected. The state of these bits affects the function of the MIDI Status Registers and the address of the data and command/status registers. These bits are reset to zero, 6850 mode, by power on reset.

AUTOINC - When set, the Indirect Address Register will increment automatically after every access. When reset to zero, the address register will not increment.

IPI - When this bit is set, the EPI bit in the Interrupt Status Register will be set. If the EPIEN bit (controlled by the 65C02) is also set, the 65C02 processor will receive an interrupt. This bit is used by the host software to facilitate host to 65C02 communications. This bit is automatically reset to zero when the 65C02 reads its Interrupt Status Register.

HINTEN - This bit, when set, enables interrupts to the host processor issued from the 65C02. On master reset it is disabled.

HINT - This bit indicates that the 65C02 has issued an interrupt to the host processor. The INTR output will be activated when this bit is set to one and HINTEN is also set to one. HINT will be cleared when the SMPTE2 Soft Status register is read. This bit is used to facilitate 65C02 to host communications.

SMPTE2 is a soft status register which is controlled by the 65C02 processor. The definitions of the individual bits for the standard part appear in the "Software Interface" section of this document.

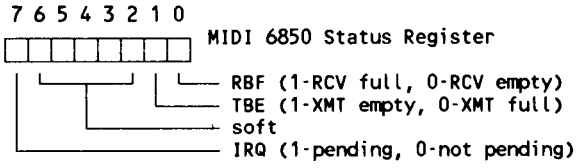
MIDI Registers

The specific function of these registers is determined by the state of the MES1 and MES2 bits in the SMPTE 1 Register. Two emulation modes are supported, 6850 UART and MPU-401. The emulations are soft and, therefore, can be modified to add other intelligence.

MIDICS*	A1	A0	Register
0	0	0	MIDI Port 1 Register 1
0	0	1	MIDI Port 1 Register 2
0	1	0	MIDI Port 2 Register 1
0	1	1	MIDI Port 2 Register 2

MIDI Command/Status Registers

In 6850 emulation, the command/status register is MIDI Port Register 1. As a status register, bits 0,1 and 7 will be controlled by the hardware and will emulate the function of a 6850 UART.

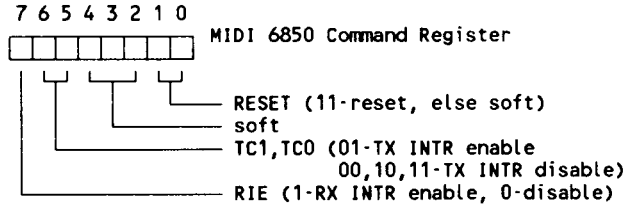


RBF - Bit 0, Receive Buffer Full, indicates the status of the receive buffer. When new data is received this bit is set to a one. After a read of the data register it is reset to zero. It is reset to zero on master reset.

TBE - Bit 1, Transmit Buffer Empty, indicates the status of the transmit buffer. When the transmitter is able to accept new data, this bit is set to one. While the transmitter is busy and unable to accept a new byte it is reset to zero. It is reset to zero on master reset and held in this state until the reset condition in the 6850 Command Register is removed by the host processor.

IRQ - Bit 7 indicates the state of the emulated 6850's interrupt request output. Any time interrupt request is active, the IRQ bit will be set to one to indicate the interrupt or service request status. IRQ is cleared by a read operation from the receive data register or a write operation to the transmit data register.

As a command register, bits 5, 6 and 7 control the transmit and receive interrupts in hardware. Other functions are firmware controlled.

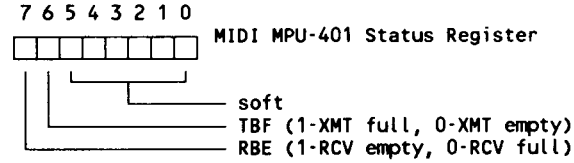


RESET - When set to 11, this field causes TBE and RBF in the status register to be zero for proper 6850 emulation. At power-on reset, the UARTS are reset and need to be taken out of reset by writing a value other than 11 to this field before any other UART operations.

TC1, TC0 - Since RTS is not required for MIDI operation the definition of this field has been reduced to transmit interrupt control. Only UART2 supports BREAK and RTS/CTS modem controls. When this field is loaded with a value of 01, and TBE in the status register is set to one, a transmit interrupt is indicated via the INTR line to the host processor being activated. A value other than 01 disables the transmit interrupt. TC1 and TC0 are readable by the 65C02, and, therefore, their definition is somewhat soft.

RIE - This bit is the receive interrupt enable. When set and bits 0 or 5 of the status register are set to one, the INTR line to the host processor is activated.

In MPU-401 emulation, the command/status register is MIDI Port Register 2. Bits 6 and 7 of the status port are controlled by the hardware.



TBF - Transmit Buffer Full, bit 6, when zero, indicates to the 65C02 processor that the transmit buffer is ready to accept a new command or data byte. When the host writes a byte into the data port, bit 6 will be set to one by the hardware, and will remain set until the 65C02 reads the byte from the data port. In MPU-401 mode, the Transmit Buffer Full condition has no effect on the INTR line to the host processor. It is reset to zero on master reset.

RBE - Receive Buffer Empty, bit 7, indicates when data is available to the host processor. When there is no

data available, bit 7 is set to one. When the 65C02 writes a byte into the data port, bit 7 is reset to zero. After the host processor reads the data byte, bit 7 will be set to one until the 65C02 writes another byte into the data port. In MPU-401 mode, the Receive Buffer Full condition is always indicated by the INTR line to the host processor being activated. There is no disable for this interrupt condition as there is in the 6850 mode.

MIDI Data Registers

These are the UART data register ports used to transmit data between the host processor and the 65C02 MIDI UART ports. Software may be used for intelligent modes which allow merging of MIDI data, as well as time stamping of MIDI events. The functionality provided in the 4K byte internal ROM is detailed in the "Software Interface" section.

In 6850 emulation, the data register is MIDI Port Register 2. In MPU-401 mode, the data register is MIDI Port Register 1.

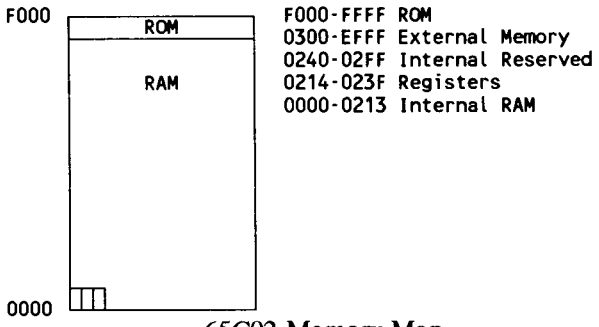
Internal Processor

The internal processor is a 65C02 running at 3.58MHz. There is 4K of internal control store ROM and 544 bytes of internal RAM.

ROM is mapped to the top 4K of the 65C02's 64K memory space when the EXTROM* pin is high. Otherwise, the internal ROM is disabled, and 0300h to FFFFh is all external memory.

RAM is mapped starting at page zero and ending 20 bytes into page two. Page zero RAM is multiported to allow access by the host interface and the SMPTE receivers and generators.

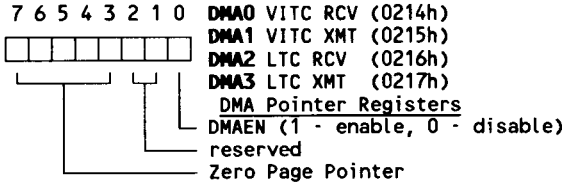
UARTs and internal control/status registers are mapped into page two.



65C02 Memory Map

65C02 Processor Registers

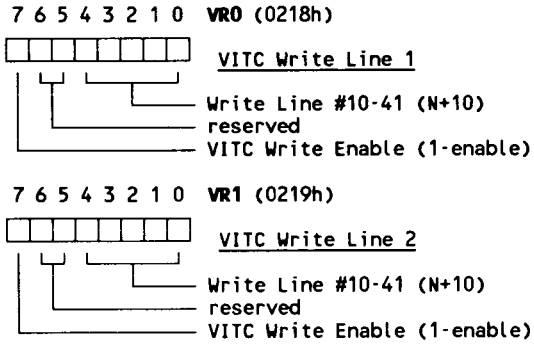
These four registers control the DMA operation of the four SMPTE devices.



DMAEN - Bit 0, DMA Enable, allows data to be read or written to the SMPTE transmitter or receiver. When set to one, DMA operations are enabled. Otherwise, DMA is disabled.

Zero Page Pointer - This field sets the upper address bits of the DMA controller's pointer to 8-byte blocks in the 65C02's page zero RAM. The receiver or transmitter provides the lower bits. Each of these 8-byte blocks are used by the associated DMA as output or input buffers for LTC and VITC time codes. Time code data (64 bits) are stored with bits 7-0 in the pointer+0 byte, bits 15-8 in the pointer+1 byte and so on. The zero page pointer in DMA0 points to two contiguous 8-byte blocks for the data from the two VITC receive lines. As a result, DMA0 bit 3 is ignored and the pointer bit 3 is hardware controlled with a 0 for VITC Read Line 1 and a 1 for VITC Read Line 2.

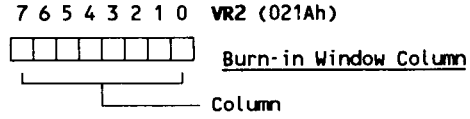
VITC code is normally output on two separate video lines in each field for redundancy. These two registers allow the individual line selection and output enables for the two VITC lines.



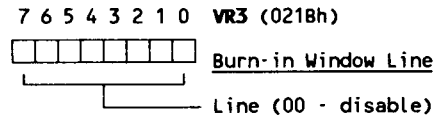
Write Line - Selects the video line on which the VITC code will be output. The video line on which the code is output will be the number in this register plus 10, e.g. writing a 1 to this register will cause the code to be output on line 11.

VITC Write Enable - Enables the output of VITC code on the specified line.

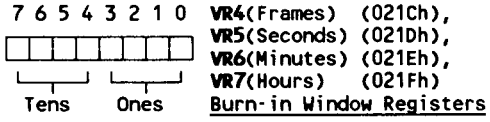
Two registers control the position of the SMPTE video display, burn-in, window within the video raster. The window size is about one third the width of the screen and 32 lines high. VR2 selects the video column in which the burn-in window starts.



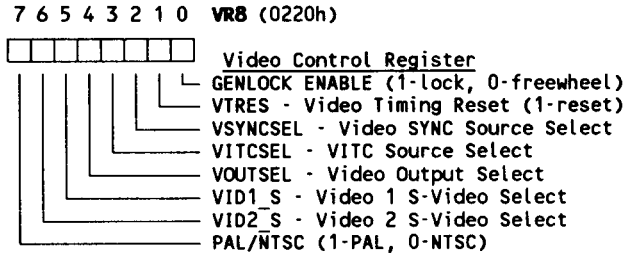
VR3 selects the video line which starts the SMPTE video display window in the video output. When this register is set to 0, there will be no Burn-In Window displayed in the video output.



These registers contain the character codes used for the SMPTE time code in the burn-in window which overlays the source in the video output. An internal character generator converts the BCD nibbles to display characters.



Code	Character	Code	Character
0	0	8	8
1	1	9	9
2	2	A	reserved
3	3	B	?
4	4	C	underscore
5	5	D	underscore
6	6	E	square
7	7	F	blank



GENLOCK ENABLE - When set, this bit enables the genlock circuits to sync to the selected video input signal. When reset to zero, the video sync will "freewheel", generating video timing from the internal oscillator. The freewheel mode would be selected when striping LTC to allow synchronization with a MIDI sequencer or other strictly timed audio source.

VTRES - When set, this bit clears the video timing counters to dot zero of line 1 of field 1. This is useful when the video is free running, not genlocked and LTC sync needs to be synchronized to an event such as the CLICK input.

VSYNCSEL - When set to one, this bit selects the video input source from Video 2 (Y2) to be the SYNC source for the internal video timing. Otherwise, when reset to zero, Video 1 (Y1) is selected.

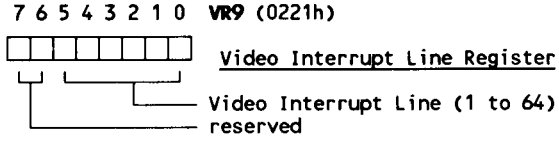
VITCSEL - When set to one, this bit selects the video input source from Video 2 (Y2) to be the VITC time code source for the VITC receiver. Otherwise, when reset to zero, Video 1 (Y1) is selected.

VOUTSEL - When set to one, this bit selects the video input source from Video 2 (Y2, C2) to be output on the video outputs (YOUT, COUT). When reset to zero Video 1 (Y1, C1) are selected.

VID1_S - When set to one, this bit causes the video 1 source to be treated as S-Video. Otherwise, when cleared to zero the video 1 source is treated as composite video.

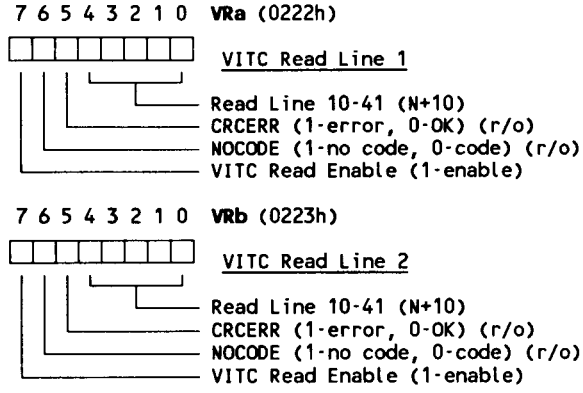
VID2_S - When set to one, this bit causes the video 2 source to be treated as S-Video. Otherwise, when cleared to zero the video 2 source is treated as composite video.

PAL/NTSC - When set to one, this bit causes the video to be synchronized with PAL timing. Otherwise, when cleared to zero, video is synchronized with NTSC timing.



Video Interrupt Line - This register selects the video line after which the Video Line Interrupt will occur. The actual video line number is the number in the register plus one.

As with the VITC Write Line Register, these registers allow control of the individual redundant VITC read lines. The 65C02 firmware can also reprogram these dynamically to allow for scanning of VITC code when the source lines are unknown.



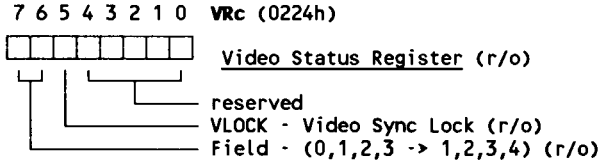
Read Line - Selects the line from which VITC code is to be read within each field. It works identically to the

Write Line in that the video line selected is the number in this register plus 10.

CRCERR - This bit is reset to zero when a valid VITC code has been received. It is valid from the end of the selected video line until the end of the selected line in the next field.

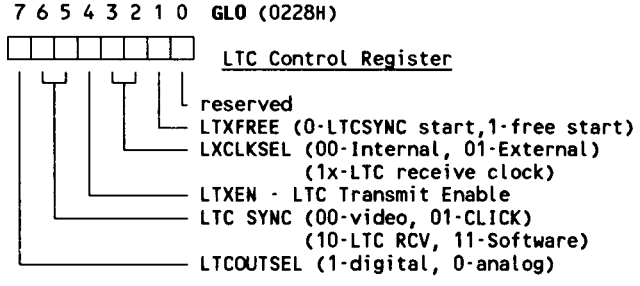
NOCODE - This bit is set when a framing error occurs in the VITC code, i.e. not all the bits of the code were received by the time the end of the video line occurred. Both CRCOK and NOCODE must be zero to qualify a VITC code.

The video status register is a read only register which contains the field/frame status and the video lock status.



VLOCK - This is a hardware driven bit which indicates that genlock has been achieved with the selected video source.

Field - The hardware sync separator detects the field and frame from the incoming video. The field numbers 1 to 4 are read as 0 to 3 respectively. The odd/even fields are identified by bit 6. The frame, A/B, is identified by bit 7. Both bits are required for VITC code generation, bit 6 for Field/Phase Mark and bit 7 for Color Frame flag. If the video source is a consumer VCR or other low quality video source, the hardware may not be able to detect the frame ID accurately. In this case, the FRAME input in the LTC Control Register can be used as a frame reference. Bit 7 (Frame) is valid after line 31 in NTSC mode or line 6 in PAL mode. Bit 6 (Field) is valid after line 4 in NTSC mode or line 1 in PAL mode.



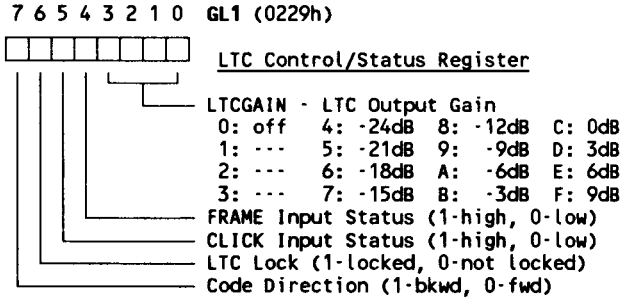
LTXFREE - This bit controls the LTC frame start of the LTC transmitter. When reset to zero the start of a LTC output frame is triggered by the selected LTC SYNC source. Otherwise, when set to one, the end of a LTC frame will trigger the start of the next. The first LTC transmit frame must be triggered by one of the SYNC sources.

LXCLKSEL - This bit controls the source for the LTC transmit clock divider input. A 00 selects the internal 14.318MHz clock, a 01 selects the LXCLKIN external input, and a 1x selects the LTC receive clock. When the LTC receive clock is selected as the source to the LTC transmit clock divider, the clock rate is first doubled before being input to the divider so that loading a divider value of 001 will result in the LTC transmit clock running at the exact same rate as the LTC receive clock.

LTXEN - This bit, when set to one, enables output of LTC code on the LTCOUT output pin. LTXEN is synchronized with the selected LTC SYNC source to ensure that only complete LTC frames are transmitted. The data to be sent by the LTC transmitter should be loaded into the associated RAM buffer before the LTCEN bit is set.

LTC SYNC - These bits select the LTC transmit sync source. Values 00, 01, 10 and 11 select start of video line 5, rising edge of CLICK, LTC receive sync pattern detect and write to GL6 respectively as the sync event. Care should be taken to disable LTXEN before changing the LTC SYNC select. Otherwise, an erroneous sync may be generated.

LTCOUTSEL - This bit, when set to 1, causes the LTCOUT pin to be a digital output. When cleared to zero, the LTCOUT pin is an analog output with gain control.



LTCGAIN - Sets the signal gain on the LTC audio output. The output gain is selectable in 3dB increments from -24dB to +9dB referenced to 0VU = -10dbV. When this register is set to zero, there is no LTC audio output.

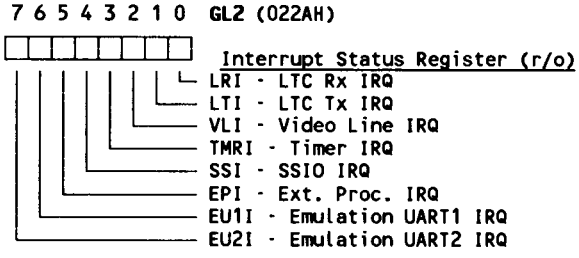
FRAME - This read only bit indicates the state if the FRAME input pin. It is provided as an alternate to the sync separator's color frame status, VR8 bit 7. It is useful when the quality of the video source is low.

CLICK - This read only bit reflects the CLICK input pin status. It is one of the selectable LTC sync sources.

LTC Lock - This read only bit indicates whether the LTC receiver has locked on to a valid incoming LTC data stream. A one indicates LTC lock, and a zero indicates no lock. Lock occurs when a valid forward or backward LTC sync pattern is detected.

Code Direction - This read only bit indicates the direction of the LTC input code. A one indicates the code is coming in backwards. A zero indicates forward or no LTC input.

GL2 is a read only register which reflects the status of each of the potential interrupt sources to the 65C02 processor. When a bit is set to one and the corresponding enable bit in the Interrupt Control Register is also set, the 65C02 will receive an interrupt. The LRI, LTI, VLI, TMRI and EPI interrupts will be cleared by reading the Interrupt Status Register, GL2. The 65C02 firmware will need to save the state of this register, in case multiple interrupts occur during a single interrupt service routine.



LRI - This bit indicates that a LTC receive interrupt has occurred. In order for an actual processor interrupt to occur, the LRIEN bit must also be set. An LRI interrupt occurs upon reception of the last byte of LTC receive data which was preceded by a valid LTC SYNC pattern. That is after the 64th LTC receive bit time in the forward direction. At normal frame rates if the LTC transmitter is synchronized with the LTC receiver there is about 3 milliseconds after this interrupt before the LTC transmit data for the next output frame is transferred to the output buffer.

LTI - This bit indicates that a LTC transmit interrupt has occurred. When this bit is set, and the corresponding LTIEN bit has been set, the 65C02 will receive an interrupt. The LTC transmit interrupt is activated after the last LTC transmit data byte has been read from memory by the LTC XMT DMA. This last read occurs at the start of the 48th bit time. The processor has approximately 10 milliseconds to respond to the interrupt to update the frame value before the hardware accesses the associated RAM buffer in preparation for the start of the next LTC code output.

VLI - This is a status bit that indicates that the video line selected via the Video Interrupt Line Register, VR9, has passed. When the VLIEN bit is also set, the 65C02 processor will be interrupted. This interrupt will be used by the 65C02 firmware to determine when to sample the VITC time code when time locked to a video source. It will also be used to facilitate detection of LTC time code dropout and off speed LTC code, e.g. shuttling operations.

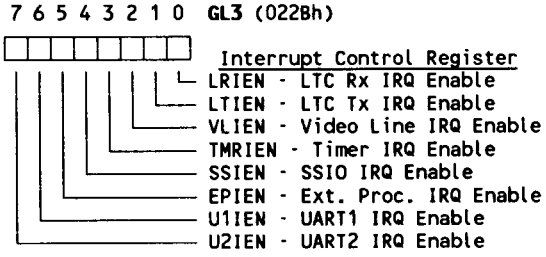
TMRI - This is a status bit that indicates a timer interrupt has occurred. When the TMRIEN bit is also set, the 65C02 processor will be interrupted. This interrupt will be used by the 65C02 firmware to time MIDI Clocks when Song Pointer/Clock mode is selected, and to time Quarter Frame messages when MIDI Time Code mode is selected.

SSI - This is a status bit that indicates when a Synchronous Serial I/O's output register is empty. When the SSIEN bit is also set to one, the 65C02 processor will be interrupted. The SSI interrupt is cleared to zero when the SS0 register is written.

EPI - This bit reflects the status of the IPI bit in the SMPTE 1 register, which can be set by the host processor to generate interrupts to the 65C02 processor. When the EPIEN bit is also set to one, the 65C02 processor will be interrupted. This interrupt will facilitate communications from the host processor to the 65C02.

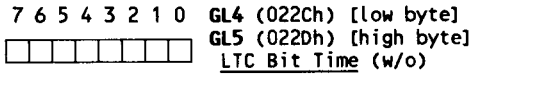
U1I, U2I - These are status bits that indicate interrupt requests from the hardware UARTS. When the corresponding enable bit (U1IEN, U2IEN) is also set to one, the 65C02 processor will be interrupted. The U1I and U2I bits are reset to zero by reading or writing from or to the associated UART's data register.

This register contains interrupt enable bits for each of the 65C02 interrupts. See the Interrupt Status Register for a description of the function of these bits.

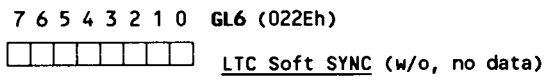


These next two write only registers control the LTC transmit bit rate. The transmit clock generator is a 12 bit divider. The upper four bits of GL5 are not used. Each bit requires two clocks. Therefore, the LTC transmit bit rate is the input clock divided by the divider value + 1, then divided by two. Since there are 80 bit times for each LTC frame, the LTC frame rate is the bit rate divided by 80.

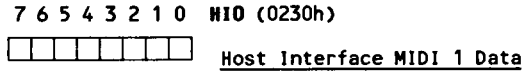
LTC Tx Clock = Clock/(Divider Value + 1)
LTC Bit Rate = LTC Tx Clock/2
LTC Frame Rate = LTC Bit Rate/80



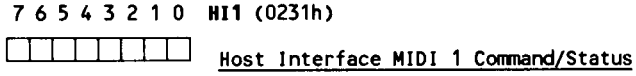
GL6 is not a register at all. It is simply an address which when written and the LTC SYNC select is set for Soft SYNC, generates LTC SYNC for the LTC transmitter.



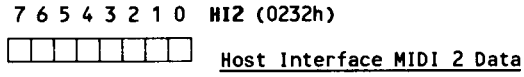
The HI0 register consists of two registers, a read and a write register. The read register is loaded by the host processor when it executes a write to its UART 1 transmit register. When the 65C02 reads this register, the host side transmit status bit is set to indicate empty. The write register is readable by the host processor. When the 65C02 writes to this register, the host side receive status bit is set to full. The appropriate bits in the Host Interface MIDI Interrupt Control Register can be set such that an interrupt may be generated whenever the host processor reads or writes to these registers. This allows the 65C02 to respond quickly as a UART emulator.



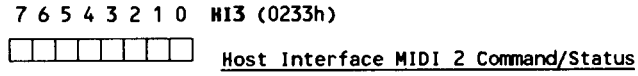
The HI1 register contains two registers, a read register for UART commands and a write register for UART status. The read register is written by the host processor writing to MIDI 1 command register. The write register provides status information to the host processor. It should be noted that bit positions 4 to 0 correspond to the host's MIDI status register bits 6 to 2 respectively in 6850 emulation mode, and bits 5 to 0 correspond to bits 5 to 0 in MPU-401 emulation mode. The remaining bits are not used. Bit definitions for these registers are soft to allow for the multiple MIDI port emulations. The appropriate bit in the Host Interface MIDI Interrupt Control Register can be set such that an interrupt to the 65C02 will be generated when the host processor writes to the command register.



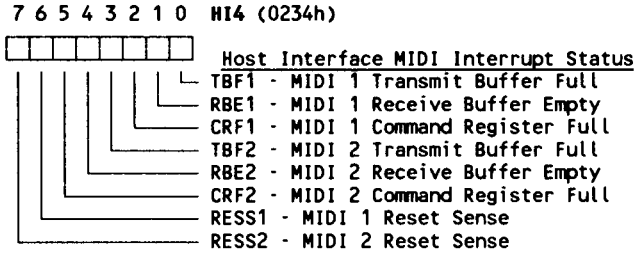
This register operates for MIDI port 2 identically as HC0 does for MIDI port 1.



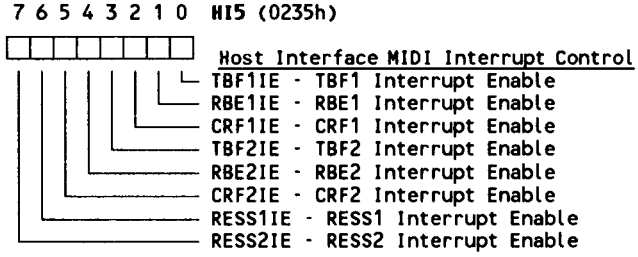
This register operates for MIDI port 2 identically as HC1 does for MIDI port 1.



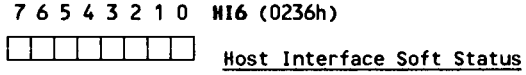
HI4 is a read only register which shows the 65C02 whether a register needs service. TBF is set, 1, when the host processor writes new data to the MIDI data register. It is cleared, 0, when the 65C02 reads the MIDI data register. RBE is cleared, 0, when the 65C02 writes data to the MIDI data register and is set, 1, when the host processor reads that data. CRF is set, 1, when the host processor writes to the command register, and it is cleared, 0, when the 65C02 reads the command. Bits 6 and 7 are valid when the associated MIDI port is in 6850 mode. In that case a one indicates the occurrence of an emulation UART reset. The bits are cleared to zero when HI4 is read. If the corresponding enable bit in HI5 is set when one of these status bits is set, 1, a 65C02 NMI interrupt is generated.



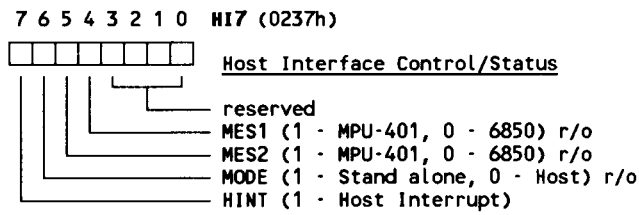
The HI5 register controls the generation of interrupts from the emulation MIDI ports. When an enable bit is set to a one and the corresponding status bit is also set to a one, a 65C02 NMI interrupt is generated.



The HI6 status register is controlled by the 65C02 firmware. The individual bit definitions for the standard part appear in the "Software Interface" section. The 65C02 will maintain critical information in this register for access by the host processor via the Soft Status Register.



The HI7 register provides the 65C02 with access to various bits in the host interface's SMPTE1 register.

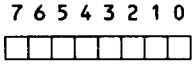


MES1, MES2 - These are status bits which are set by the host processor, via the SMPTE1 Control/Status Register, to select the interface emulation mode.

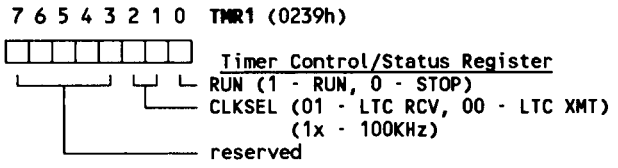
MODE - This is a status bit which tells the 65C02 if it is in stand-alone mode or in host mode. This will be used by the 65C02 firmware to determine what action should be taken on power-up and whether the host interface needs to be supported. In stand-alone mode, all commands to the 65C02 will come through the MIDI interface.

HINT - The 65C02 firmware will use this bit to send time critical information (e.g. frame interrupts) to the host processor. When set, the host interrupt status bit will be set (HINT in the SMPTE 1 register). If the INTREN bit is also set, the INTR pin goes active to interrupt the host processor. This bit is cleared when the SMPTE1 register is read.

The timer value register is a write only register who's value plus one is the timer interrupt interval based on the selected timer input clock.



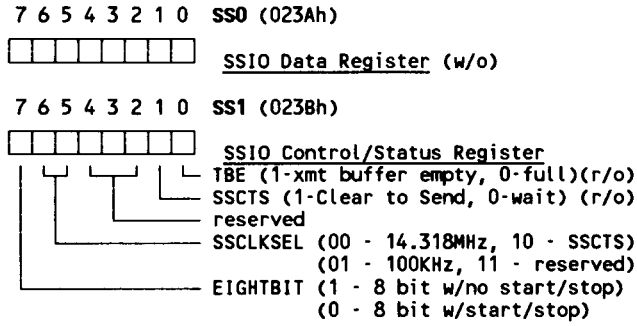
Interrupt Rate = Timer Clock Rate / (TMR0 + 1)



RUN - Bit 0, RUN, is the timer on/off control. When set to one, the timer counts down from the value in TMR0. When it reaches zero the timer count is reloaded with the value in TMR0, and count down continues. If enabled, an interrupt is generated on the zero to TMR0 value transition. When RUN is cleared to zero, the timer counter is forced to the value in TMR0 and does not count.

CLKSEL - Clock Select, is the timer's input clock select. A 1x selects a 100KHz clock. A 01 selects the LTC receiver clock. This clock is synchronized with the data coming in on the LTC input. Its period tracks the input data's bit time. A 00 selects the LTC transmitter clock. This is a fixed rate clock which can be synchronized with the video input when the LTC output is running.

These registers control the high speed synchronous serial interface. The data register is a write only register.



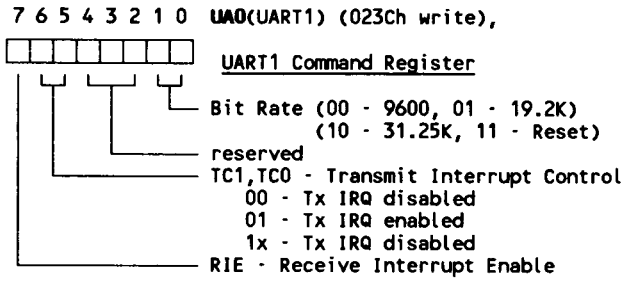
TBE - Bit 0, Transmit Buffer Empty, indicates the status of the SSIO transmit buffer. When the transmitter is able to receive new data, this bit is set to one. While the transmitter is busy and unable to accept a new byte it is reset to zero. It is set to one on master reset.

SSCTS - Bit1, Clear-to-Send, indicates the state of the SSCTS pin. When set to one, the transmitter is allowed to send data. A data frame will transmit in its entirety once transmission is started.

SSCLKSEL - This field selects the clock source for the synchronous serial output. The selected clock is output on the CLKOUT pin. When SSCTS is selected as the clock source, the SSCTS pin is treated as an external clock source and the internal clear-to-send function which controls the serial output is set active allowing serial data to be output whenever data is available to send.

EIGHTBIT - Bit 7 controls the data frame format of the synchronous serial output. When cleared to zero the frame consists of a start bit, 8 data bits and one stop bit. When set to one the frame is only the 8 data bits.

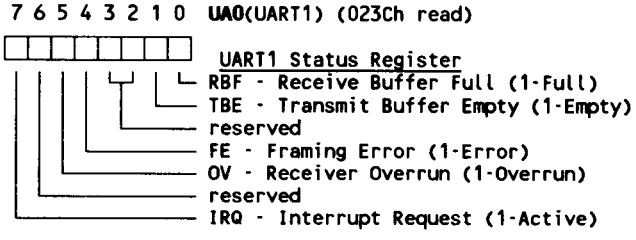
The UART registers operate like a 6850 UART's registers. UART1 does not support modem controls.



Bit Rate - This field selects the bit rate for data transmit and receive. After a master reset, its value is 11. One of the three bit rates must be selected in order to start the UART's operation. Writing a 11 will reset the UART.

TC1,TC0 - Bits 6 and 5, Transmit Control, provide control for transmit interrupt (when TBE is true).

RIE - Bit 7, Receive interrupt enable, when set to one enables the UART to interrupt the 65C02 when the receive buffer is full or a receive overrun has occurred.



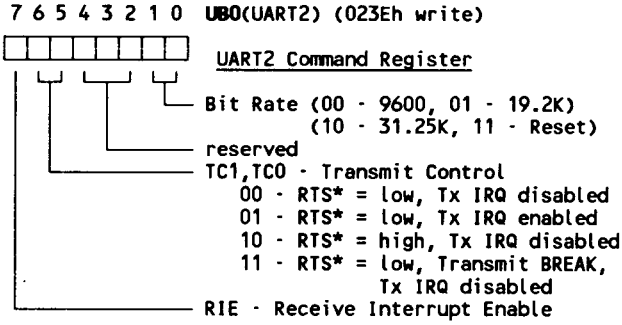
RBF - Bit 0, Receive Buffer Full, is set to one when read data is available in the UART data register. It is cleared to zero when the UART data register is read.

TBE - Bit 1, Transmit Buffer Empty, is cleared to zero when data is written to the UART data register. It is set to one when the UART transfers that data to its output shift register.

FE - Bit 4, Framing Error, when set to one indicates that the receive character was improperly framed by the start and stop bits. It is detected by the absence of the first stop bit. This indicator is valid as long as the character data is valid.

OV - Bit 5, Receiver Overrun, is an error flag indicating that one or more characters in the data stream has been lost. It is set to one when a new character overwrites an old character which has not been read. The overrun error is cleared to zero when a character is read from the UART data register.

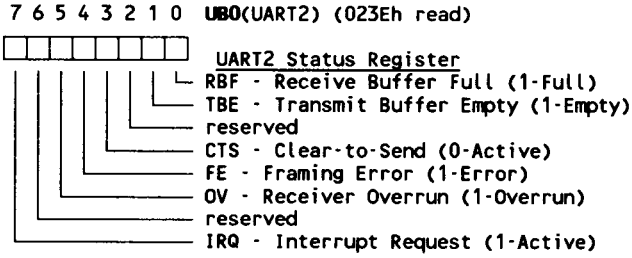
IRQ - Bit 7, Interrupt Request, is a status bit which reflects the state of the interrupt request from the UART to the 65C02. When IRQ is one, an interrupt is pending. Otherwise, no interrupt is pending.



Bit Rate - This field selects the bit rate for data transmit and receive. After a master reset, its value is 11. One of the three bit rates must be selected in order to start the UART's operation. Writing a 11 will reset the UART.

TC1,TC0 - Bits 6 and 5, Transmit Control, provide control for transmit interrupt (when TBE is true), RTS control and transmit BREAK level.

RIE - Bit 7, Receive interrupt enable, when set to one enables the UART to interrupt the 65C02 when the receive buffer is full or a receive overrun has occurred.



RBF - Bit 0, Receive Buffer Full, is set to one when read data is available in the UART data register. It is cleared to zero when the UART data register is read.

TBE - Bit 1, Transmit Buffer Empty, is cleared to zero when data is written to the UART data register. It is set to one when the UART transfers that data to its output shift register.

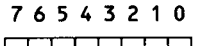
CTS - Bit 3, Clear-to-Send, is an active low status bit indicating the state of the CTS2* input pin. A zero in this bit position indicates that the modem or receiving device is ready to receive characters. A one indicates not ready. When CTS is inactive, one, TBE is held at zero, the not empty state.

FE - Bit 4, Framing Error, when set to one indicates that the receive character was improperly framed by the start and stop bits. It is detected by the absence of the first stop bit. This indicator is valid as long as the character data is valid.

OV - Bit 5, Receiver Overrun, is an error flag indicating that one or more characters in the data stream has been lost. It is set to one when a new character overwrites an old character which has not been read. The overrun error is cleared to zero when a character is read from the UART data register.

IRQ - Bit 7, Interrupt Request, is a status bit which reflects the state of the interrupt request from the UART to the 65C02. When IRQ is one, an interrupt is pending. Otherwise, no interrupt is pending.

Each UART data register is actually two registers, a transmit buffer and a receive buffer. Writing to the data register, causes the transmit buffer to be written. Reading from the data register, causes the receive buffer to be read.



UA1(UART1) (023Dh),
UB1(UART2) (023Fh)
UART Data Register

65C02 Register Summary

		7	6	5	4	3	2	1	0
DMA0	0214	VITC RCV POINTER [7:4]				0	0	0	DMAEN
DMA1	0215	VITC XMT POINTER [7:3]					0	0	DMAEN
DMA2	0216	LTC RCV POINTER [7:3]					0	0	DMAEN
DMA3	0217	LTC XMT POINTER [7:3]					0	0	DMAEN
VR0	0218	VITC1WE	0	0	VITC WRITE LINE 1				
VR1	0219	VITC2WE	0	0	VITC WRITE LINE 2				
VR2	021A	BURN-IN WINDOW COLUMN							
VR3	021B	BURN-IN WINDOW LINE							
VR4	021C	FRAMES							
VR5	021D	SECONDS							
VR6	021E	MINUTES							
VR7	021F	HOURS							
VR8	0220	PAL	VID2_S	VID1_S	VOUTSEL	VITCSEL	VSYNCSEL	VTRES	GEN_EN
VR9	0221	0	0	VIDEO LINE INTERRUPT (LINE #)					
VRa	0222	VITC1RE	NOCODE1	CRCERR1	VITC READ LINE 1				
VRb	0223	VITC2RE	NOCODE2	CRCERR2	VITC READ LINE 2				
VRc	0224	FRAME	FIELD	VLOCK	0	0	0	0	0
	0225	0	0	0	0	0	0	0	0
	0226	0	0	0	0	0	0	0	0
	0227	0	0	0	0	0	0	0	0
GL0	0228	LTCOUTSEL	LTCSYNCSEL		LTXEN	LXCLKSEL		LTXFREE	0
GL1	0229	CODEDIR	LTCLOCK	CLICK	FRAMEIN	LTC GAIN			
GL2	022A	U2I	U1I	EPI	SSI	TMRI	VLI	LTI	LRI
GL3	022B	U2IEN	U1IEN	EPIEN	SSIEN	TMRIEN	VLIEN	LTIEN	LRIEN
GL4	022C	FRAME RATE (low byte, write only)							
GL5	022D	0	0	0	0	FRAME RATE (high byte, write only)			
GL6	022E	SOFT LTC SYNC (write only, no data)							
	022F	0	0	0	0	0	0	0	0
HI0	0230	HOST EMULATION MIDI 1 DATA							
HI1	0231	HOST EMULATION MIDI 1 COMMAND/STATUS							
HI2	0232	HOST EMULATION MIDI 2 DATA							
HI3	0233	HOST EMULATION MIDI 2 COMMAND/STATUS							
HI4	0234	RESS2	RESS1	CRF2	RBE2	TBF2	CRF1	RBE1	TBF1
HI5	0235	RESS2IE	RESS1IE	CRF2IE	RBE2IE	TBF2IE	CRF1IE	RBE1IE	TBF1IE
HI6	0236	HOST INTERFACE SOFT STATUS							
HI7	0237	HINT	MODE	MES2	MES1	0	0	0	0
TMR0	0238	TIMER VALUE REGISTER (write only)							
TMR1	0239	0	0	0	0	0	CLKSEL		RUN
SS0	023A	SSIO DATA (write only)							
SS1	023B	EIGHTBIT	SSCLKSEL		0	0	0	SSCTS	TBE
UA0	023C	UART 1 COMMAND/STATUS REGISTER							
UA1	023D	UART 1 DATA REGISTER							
UB0	023E	UART 2 COMMAND STATUS REGISTER							
UB1	023F	UART 2 DATA REGISTER							
	0240	EMPTY FROM 0240h to 02FFh							

Software Interface

This section describes the functionality of the firmware contained in the ICS2010 internal 4K byte ROM of the standard part and how the embedded 65C02 processor running this firmware will interact with the host processor.

MIDI Ports

The selection of the MIDI port emulation (6850 or MPU-401) must be made in combination with a reset to the ICS2010. This can be accomplished in one of two ways:

1) The host processor first sets RESET bit 0 in the SMPTE1 register to a 1, then it sets the state of MES1 & MES2 bits 2 & 3 respectively in the SMPTE1 register for the emulation mode required (1 = MPU-401, 0 = 6850), and finally the host processor writes a 0 to RESET bit 0 in the SMPTE1 register.

2) The host processor first sets the state of MES1 & MES2 bits 2 & 3 respectively in the SMPTE1 register for the emulation mode required (1 = MPU-401, 0 = 6850) and then the host processor issues the SOFT RESET command to the ICS2010 via the Host-65C02 Communications described below.

In either case, the 65C02 will be caused to execute its internal Power-On Confidence routine which includes the initialization of internal variables related to the state of the MIDI Emulation Select bits MES1 and MES2.

6850 MIDI Emulation Mode

When a host MIDI port is placed into the 6850 Emulation Mode and once the initial 6850 UART Reset condition is released, it automatically comes up in the MIDI pass-through mode, i.e. data received on the MIDI input will be transferred to the host and data sent by the host will be transmitted to the corresponding MIDI output. Any information written to bits 4-0 of the 6850 Command Register will be ignored with the exception of the RESET UART setting.

MPU-401 MIDI Emulation Mode

When a host MIDI port is placed into the MPU-401 Emulation Mode, it comes up in a pseudo-smart mode of operation. While in this MPU-401 smart mode, the associated MIDI port of the ICS2010 will not operate on any data sent to it from the host side or any data received on the MIDI input. In addition, there are only three command codes which the ICS2010 internal firmware will accept in this mode: Reset (FFh), Return Interface Version Number (ACh), and Set Pass Thru/UART Mode (3Fh). Any command other than these 3 will be NAKed with an FFh Data-In response (refer to the appropriate MPU-401 documentation for further details of operation.) Once the host issues the Pass Thru/UART Mode command and gets the associated ACK FEh Data-In response, data received on the MIDI input will be transferred to the host and data sent by the host will be transmitted to the MIDI output.

In either the 6850 or MPU-401 Emulation modes, the MIDI ports can be programmed to merge the input of both MIDI inputs to host MIDI port 0 and/or to transmit MIDI data sent to host MIDI port 0 on both MIDI outputs. The enable/disabling of these Merge and Split functions is described in the following Host-65C02 Communications section of this specification. Also, all data received on the MIDI inputs are passed to the appropriate host MIDI port, including received MIDI Time Code (MTC) data.

Host-65C02 Communications

The ICS2010's embedded 65C02 processor communicates with the host processor through a mailbox located in the indirect register area of the RAM (zero page RAM of the 65C02).

When the host processor wants to send a message to the 65C02, it places the command byte into the first byte (address 00h) of the outgoing mailbox. Data bytes, if any, are placed in successive bytes of the mailbox. When the message is complete, the host signals the 65C02 by setting the IPI bit in SMPTE register 1. The 65C02 will acknowledge the message by setting the command byte to FEh or indicate an error by setting it to FFh. If the command requires a data response, the data will be found in the bytes following the command byte. Data values must be within the specified range as described below. Otherwise, the error code, FFh, will be returned.

Here is a code fragment that demonstrates how the host can be send a command to the 65C02:

```
MAILBOX:  equ    00h      ;MAILBOX is 1st RAM location
                          ;
   cli                    ;disable interrupts to make
                          ;certain that an ISR doesn't
                          ;disturb the address pointer
   mov  dx,SMPTE1         ;point to SMPTE1 reg
   in   al,dx             ;get current value
   or   al,010h           ;set for auto-increment
   out  dx,al             ;output to chip

   add  dx,2              ;point to indirect addr reg
   mov  al,MAILBOX        ;point to mailbox address
   out  dx,al             ;set address
   inc  dx                ;point to indirect data reg
   mov  cx,msgsize        ;size of message in bytes
   lea  si,message        ;pointer to message
   rep  outsb             ;output message

   sub  dx,3              ;point back to SMPTE1 reg
   in   al,dx             ;get current value
   or   al,IPI            ;set interrupt bit
   out  dx,al             ;output to chip
   sti                    ;enable interrupts

Single byte commands are much simpler:

   mov  dx,INDADDR        ;point to indirect addr reg
   mov  al,MAILBOX        ;point to mailbox address
   out  dx,al             ;set address

   inc  dx                ;point to indirect data reg
   mov  al,command        ;get command byte
   out  dx,al             ;output to chip
   sub  dx,3              ;point back to SMPTE1 reg
   cli                    ;disable interrupts
   in   al,dx             ;get current value
   or   al,IPI            ;set interrupt bit
   out  dx,al             ;output to chip
   sti                    ;enable interrupts
```

SMPTE2 Status Register

The SMPTE2 Status Register is used to communicate the nature of a host interrupt and other significant information to the host processor without requiring a command-response or going through the indirect address register. The bits of the status register are defined as follows:

Bit	Definition
7	Time Code Lock Interrupt
6	Time Code Loss Interrupt
5	Cuepoint Match Interrupt
4	Frame End Interrupt
3	Reserved
2-0	Power-On Confidence Progress Code

Command Set

SOFT RESET

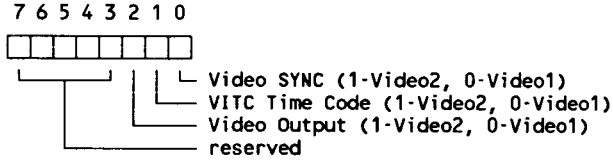
Format:00h

Causes the 65C02 to perform an internal software reset, initializing all variables and machine states to their reset condition. This command also results in the execution of the internal ROM Power-On Confidence routine; the status of which can be monitored via the bits in the SMPTE2 Status Register. The combined test and initialization requires approximately 25 milliseconds to run to completion.

SMPTE2 Value	Definition
00h	Beginning Power-On Confidence
FFh	All 1's Status Register Test
00h	All 0's Status Register Test
01h	Checksum of Last Page ROM
02h	Internal RAM Write/Read Test
03h	Checksum of Full Internal ROM
04h	Microcode Initialization
05h	Reserved
06h	Reserved
07h	Initialization Complete

SELECT VIDEO SOURCE

Format: 01H ss

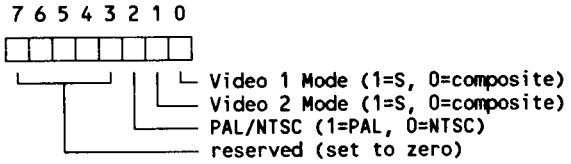


Video SYNC source selects the video input to which the internal video timing is genlocked.

VITC Time Code source selects the video input from which the time code will be extracted when VITC is selected via the SET TIME CODE SOURCE command.

Video Output source selects the video input to which VITC time code and/or the burn-in window will be added if both or either are enabled for output on the video output signal.

SELECT VIDEO INPUT MODE
Format: 02h ss



Bits 0 and 1 select the way in which the associated video input will be treated. A zero selects composite, and a one selects S-Video. Bit 2 selects PAL or NTSC video timing.

ENABLE GENLOCK
Format: 03h

Enables the genlock circuits to synchronize with the selected video source. Genlock should be enabled except when striping a new LTC time code that is not synchronized to video.

DISABLE GENLOCK
Format: 04h

Disables the genlock circuits.

SET VITC READ LINE NUMBERS
Format: 05h ll mm

ll = First line number
mm = Second line number

Sets the video line numbers to read the VITC code from. When syncing to VITC, the time code from the first line will be read. If it is OK, it will appear in the SMPTE time code location in the indirect register space. If not OK, the second line will be read and if it is OK, it will be placed in the SMPTE time code location. Only line numbers from 10 to 41 (0Ah to 29h) are permitted. Commands with data values outside this range will result in an error indication.

SET VITC WRITE LINE NUMBERS
Format: 06h ll mm

ll = First line number
mm = Second line number

Sets the video line numbers that the VITC code will be written on. The SMPTE specification recommends that the lines should be 2 lines apart. Only line numbers from 10 to 41 (0Ah to 29h) are permitted. Commands with data values outside this range will result in an error indication.

SET LTC GAIN
Format: 07h gg

gg = 00 (off)
gg = 01h-0Ch (-21dB to +12dB)
gg = 80h (select TTL LTC Output)

Sets the signal gain on the LTC analog output. The gain is selectable from -21dB to 12dB in 3dB

ENABLE LTC OUTPUT
Format: 08h

Enables LTC time code output. The start of the LTC output is synchronized with the selected LTC SYNC source. LTC frames are sent out only as complete frames.

DISABLE LTC OUTPUT
Format: 09h

Disables LTC time code output. The disabling of the output is synchronized with the LTC SYNC source to ensure that only valid complete frames are output.

SET FRAME RATE
Format: 0Ah rr

rr = 00 (30 Hz)
rr = 01 (29.97 Hz)
rr = 02 (25 Hz)
rr = 03 (24 Hz)

Sets the LTC sync rate. These bits must be set properly so that the LTC output can track the video rate.

SET LTC SYNC SOURCE
Format: 0Bh ss

ss = 00 (Video)
ss = 01 (Click)
ss = 02 (LTC Receiver)
ss = 03 (MIDI Time Code)
ss = 04 (Internal)

Selects the sync source for the LTC output. The sync can be from one of four external sources, the video, the CLICK input pin, the LTC receiver or the MIDI Time Code port or from internally generated timing synchronized to the START TIME CODE OUTPUT command.

SET TIME CODE SOURCE
Format: 0Ch ss

ss = 00 (VITC)
ss = 01 (LTC)
ss = 02 (MTC)
ss = 03 (Hunt)
ss = 04 (Internal)

Selects the time code source. If Hunt is selected, the 65C02 will select the first source that it senses with valid time code.

SET MIDI TIME CODE INPUT PORT
Format: 0Dh pp

pp = 00 (MIDI UART Port 1)
pp = 01 (MIDI UART Port 2)

Selects the MIDI port upon which time code will be input when MTC is selected via the SET TIME CODE SOURCE command and/or the SET LTC SYNC SOURCE command.

ENABLE VITC OUTPUT
Format: 0Eh

Enables VITC time code output.

DISABLE VITC OUTPUT
Format: 0Fh

Disables VITC time code output.

ENABLE MTC OUTPUT
Format: 10h

Enables MIDI time code output.

DISABLE MTC OUTPUT
Format: 11h

Disables MIDI time code output.

SET TIME CODE FORMAT
Format: 12h ff

ff = 00 (30 Hz)
ff = 01 (29.97 Hz Drop Frame)
ff = 02 (25 Hz)
ff = 03 (24 Hz)

Sets the SMPTE time code format.

SET SMPTE TIME CODE
Format: 13h hh mm ss ff

hh = hours (00 - 23)
mm = minutes (00 - 59)
ss = seconds (00 - 59)
ff = frames (00 - 29)

Sets the SMPTE time code value to be output on the next frame. This is done in preparation for striping time code to tape. These four bytes are in BCD format and must be within the valid limits. Otherwise, an error indication will result.

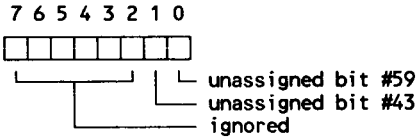
SET USER BIT SOURCE
Format: 14h ss

ss = 00 (SMPTE time code source)
ss = 01 (SET USER BITS command)

Selects the source of the user bits for SMPTE data output. When ss=00, the source of the user bits will be the source selected for the SMPTE time code. When ss=01, the source of the user bits is the memory loaded via the SET USER BITS command. These internally set user bits will also be the source if ss=00 and the specified time code source is set for Internal. (If the user bit settings are required to be sent on one or both of the MIDI UART ports, it is the responsibility of the host software to create and send the appropriate user bits MIDI message.)

SET USER BITS
Format: 15h g1 g2 g3 g4 g5 g6 g7 g8 g9

g1 = SMPTE User Bits Group#1 (bits #7-4)
g2 = SMPTE User Bits Group#2 (bits #15-12)
g3 = SMPTE User Bits Group#3 (bits #23-20)
g4 = SMPTE User Bits Group#4 (bits #31-28)
g5 = SMPTE User Bits Group#5 (bits #39-36)
g6 = SMPTE User Bits Group#6 (bits #47-44)
g7 = SMPTE User Bits Group#7 (bits #55-52)
g8 = SMPTE User Bits Group#8 (bits #63-60)
g9 = SMPTE Binary Group Flag bits which are bit mapped as follows:



Sets the SMPTE User Bit value to be output on the next frame. This can be done in preparation for striping time code to tape as well as for replacing existing user bits during a tape copy operation. Only the least significant nibble of g1-g8 and least significant 2 bits of g9 are used, the remaining bits of these bytes are ignored.

START TIME CODE OUTPUT
Format: 16h

Begins time code output on all enabled ports starting at the current frame number.

STOP TIME CODE OUTPUT
Format: 17h

Stops time code output after the current frame.

ENABLE FRAME INTERRUPTS
Format: 18h

Enable frame interrupts to the host processor. When enabled, the host processor will receive an interrupt at the end of each frame.

DISABLE FRAME INTERRUPTS
Format: 19h

Disable frame interrupts to the host processor.

ENABLE TIME CODE LOCK INTERRUPT
Format: 1Ah

Enable time code lock interrupts to the host processor. When enabled, the host processor will receive an interrupt when time code lock is achieved. The time code lock interrupt is not activated when the time code source is set to internal.

DISABLE TIME CODE LOCK INTERRUPT
Format: 1Bh

Disable time code lock interrupts to the host processor.

ENABLE TIME CODE LOSS INTERRUPT
Format: 1Ch

Enable time code loss interrupts to the host processor. When enabled, the host processor will receive an interrupt when time code sync is lost. This interrupt will occur after the time code read has been unsuccessful for the number of frames set by SET FREEWHEEL FRAMES. The time code loss interrupt is not activated when the time code source is set to internal.

DISABLE TIME CODE LOSS INTERRUPT
Format: 1Dh

Disable time code loss interrupts to the host processor.

SET FREEWHEEL FRAMES
Format: 1Eh ff

ff = 01h-FDh (Frame Count)
ff = FEh (Continuous Jam Sync)
ff = FFh (One-Time Jam Sync)

Sets the number of frames with invalid or missing time code before time code is considered lost. When set within the range of 00h-FDh, the 65C02 will fill in for up to 0-253 bad or missing frames, after which time code will be considered lost. When set to FEh, the 65C02 will fill in any size gaps in time code until a valid time code is encountered. When set to FFh, the 65C02 will sync to the first valid time code, then freewheel until stopped, no longer looking at the time code coming in. For both the FEh and FFh Jam Sync settings, time code is never considered lost.

ENABLE BURNIN WINDOW
Format: 1Fh

Enables the time code burnin window on the video outputs. Time code in character form will be overlaid on the video source.

DISABLE BURNIN WINDOW
Format: 20h

Disable the time code burnin window on the video outputs.

SET BURNIN WINDOW LOCATION
Format: 21h ll cc

ll = video line
cc = column

Sets the location of the time code burnin window on the video display. The default location is in the lower right hand corner of the screen.

SET CUEPOINT
Format: 22h hh mm ss ff

hh = hours
mm = minutes
ss = seconds
ff = frames

Sets the cuepoint location. When cuepoint interrupts are enabled, the host processor will receive an interrupt when the specified frame is encountered. These four bytes are in BCD format and are used in a frame by frame comparison for equality. Therefore, the cuepoint location value set by the host software must be a valid frame identifier for the SMPTE time code source and format as selected by the SET TIMECODE SOURCE and SET TIMECODE FORMAT commands respectively.

ENABLE CUEPOINT INTERRUPTS
Format: 23h

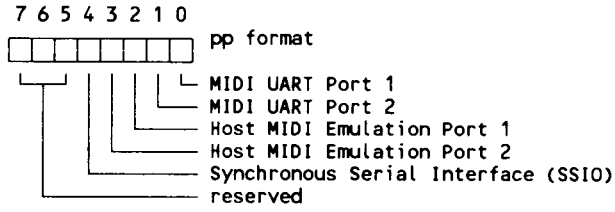
Enables cuepoint interrupts.

DISABLE CUEPOINT INTERRUPTS
Format: 24h

Disables cuepoint interrupts.

SET MIDI TIME CODE OUTPUT PORT
Format: 25h pp

Selects the MIDI port upon which time code will be output. The pp byte is bit-mapped with 1=Enable, 0=Disable:



The MIDI time code will be merged with any other MIDI data on the selected port(s). However, it is good practice to have MIDI time code on a port separate from other conventional MIDI data to avoid MIDI data stream clogging and for improved time code resolution.

ENABLE MIDI MERGE
Format: 26h

Merge the MIDI input from the two external MIDI inputs to the host MIDI emulation port 1. (NOTE: the MIDI merge function does not affect MIDI time code being input to the host on emulation UART ports 1 and/or 2.)

DISABLE MIDI MERGE
Format: 27h

Disables the merge function, putting both MIDI inputs back into pass-through mode.

ENABLE MIDI SPLIT
Format: 28h

Outputs MIDI data transmitted by the host to both MIDI output ports. When MIDI split is enabled, output data will only be accepted from the host interface MIDI emulation port 1.

DISABLE MIDI SPLIT
Format: 29h

Disables the MIDI split function putting both MIDI outputs back into pass-through mode.

LOAD RAM
Format:3Ah

This command allows the host to load and execute 65C02 microcode in externally configured RAM in the hex 0300-EFFF range. This permits the user to take advantage of the standard part's internal 4K byte ROM, while also executing additional specialized microcode where required for user specific applications.

Prior to performing a LOAD RAM sequence of commands with the ICS2010, the chip should be placed into a quiescent state by issuing a Soft Reset (00h) command. This will eliminate the possibility of any SMPTE or MIDI activity interfering with the LOAD RAM procedure.

The LOAD RAM records loaded by the host must be in Intel Hex Format, with each data record containing no more than 32 data bytes. Also, the checksum field of each record must be valid per the Intel Hex Format. An error in any of the record's parameters, such as an incorrect checksum, will result in the 65C02 returning an error indication to the host in the normal manner of setting the command byte to FFh.

Further details of the LOAD RAM record formats and their functions can be found in the ICS2010 External Memory Application Note.

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on any pin to GND .. -0.5V to V_{DD} + 0.5V
Voltage on V_{DD} to GND ..... -0.5V to +7.0V
Power Dissipation ..... 1.0 watt

NOTICE: Stress above those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only. Operating the device at these levels is not recommended, and specifications are not implied.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{DD} = 5V ±10%; GND = 0V

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD}+0.3	V
Input Leakage Current	I_{LI}			10	uA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tri-State Current	I_{OZ}			10	uA
Output Capacitance				10	pF
Bi-Directional Capacitance				10	pF
Analog Inputs					
Video Input Voltage (Y1, Y2, C1, C2)			1.0		V_{P-P}
LTC Differential Input Voltage		0.1			V_{P-P}
LTCIN+, LTCIN-, CLICK, FRAME input voltage		-0.3		V_{DD}+0.3	V
CLICK and FRAME bias voltage			$V_{DD}/3$		V
Analog Outputs					
Video Output Voltage (YOUT, COUT)			1.0		V_{P-P}
LTC Output Voltage (Volume set at max.; I_{out} = .35mA)			2.0		V_{P-P}
LTC Output Voltage Amplitude Control Step			3		dB
LTC Output Voltage Amplitude Range			33		dB
Analog V_{DD} Supply Current	I_{DD1}				mA
Digital V_{DD} Supply Current	I_{DD2}				mA

AC CHARACTERISTICS T_A = 0°C to +70°C; V_{DD} = 5V ±10%; GND = 0V; C_L = 50pF; XTAL2 = 14.318 MHz

Parameter	Symbol	Min	Typ	Max	Units
Host Address setup to IOR* or IOW* command	t_{ACS}	20			ns
Host Address hold from IOR* or IOW* command	t_{AH}	10			ns
IOR* pulse width	t_{RD}	50			ns
Address/CS* access time	t_{ACC}			150	ns
Host Data hold from IOR* high	t_{RDH}	10			ns
IOR* command inactive time	t_{RHRL}	210			ns
IOW* pulse width	t_{WR}	50			ns
Host data setup to IOW* high	t_{WDS}	20			ns
Host data hold from IOW* high	t_{WDH}	10			ns
IOW* command inactive time	t_{WHWL}	210			ns
PHI2 cycle time (note 1)	t_{CYC}		279		ns
IPA Delay from PHI2 High	t_{IAD}	25		60	ns
IPRD* or IPWR* Pulse Width (active time)	t_{CMD}		140		ns
IPA Setup to IPRD* or IOWR* Active	t_{IAS}	75			ns
IPA Hold from IPRD* or IPWR* Inactive	t_{IAH}	20			ns
Read Data Setup prior to IPRD* Inactive	t_{IRDS}	20			ns
Read Data Hold from IPRD* Inactive	t_{IRDH}	5			ns
Write Data Setup prior to IPWR* Inactive	t_{IWDS}	100			ns
Write Data Hold from IPWR* Inactive	t_{IWDH}	10			ns

note 1: With no internal wait states PHI2 is 4 cycles of the crystal oscillator clock.

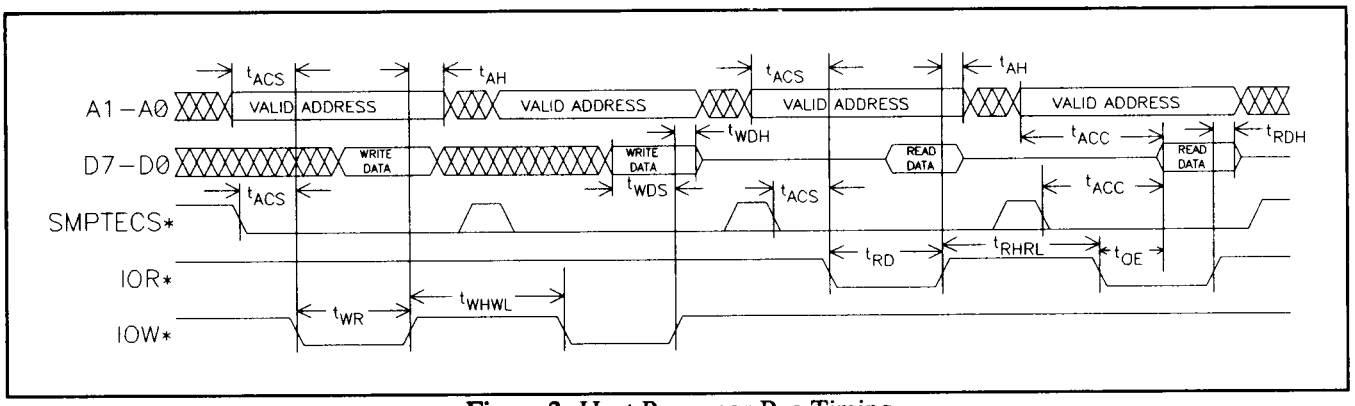


Figure 3 Host Processor Bus Timing

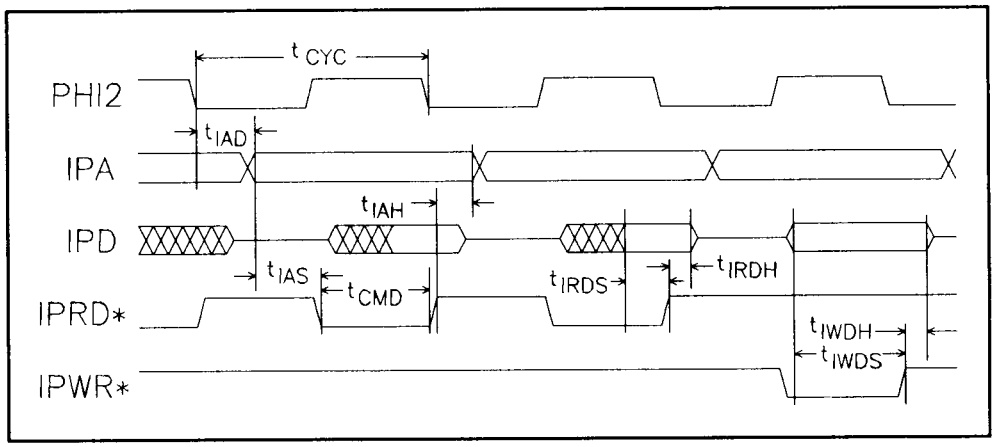


Figure 4 Internal Processor Bus Timing

AC CHARACTERISTICS T_A = 0°C to +70°C; V_{DD} = 5V ±10%; GND = 0V; C_L = 50pF

Parameter	Symbol	Min	Typ	Max	Units
Serial data delay	t_{SSD}				ns
SSCTS setup to CLKOUT high (note 2)	t_{CSU}				ns
SSCTS hold from CLKOUT high (note 2)	t_{CH}				ns

note 2: SSCTS is only sampled during a stop bit or inactive time.

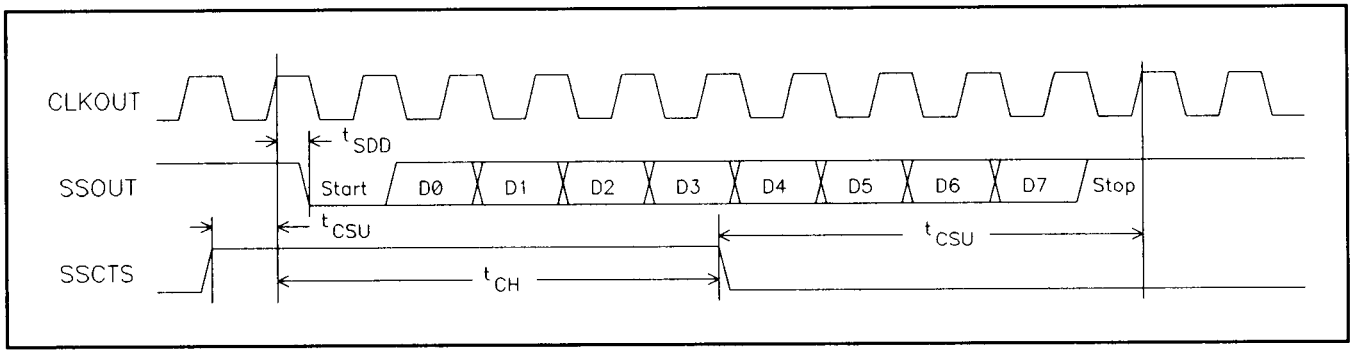


Figure 5 Synchronous Serial Interface Timing

Applications

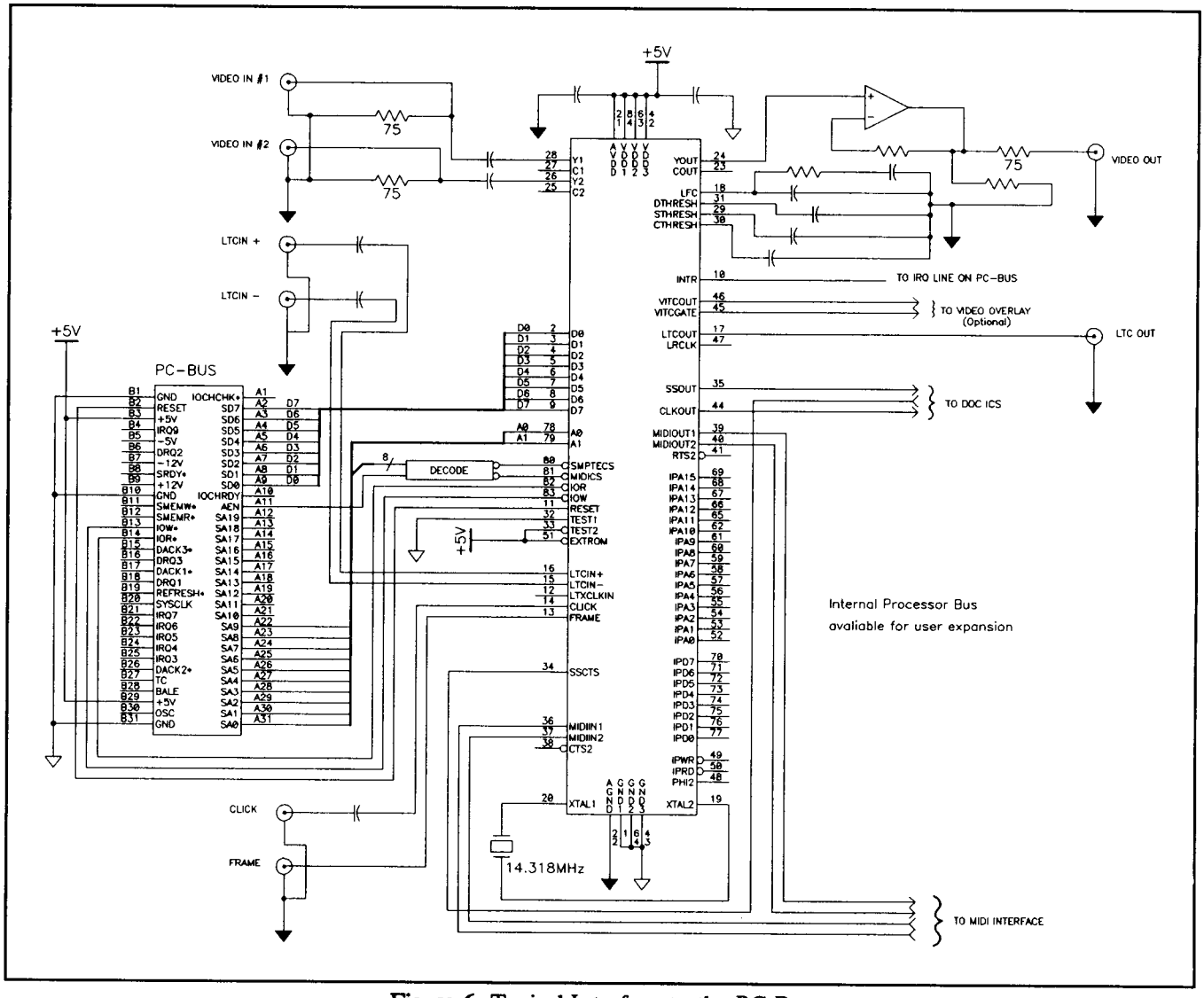


Figure 6 Typical Interface to the PC Bus

SMPTE / MIDI Time Code Processor

Loading Microcode Into External RAM

The internal 4K byte ROM contained in the ICS2010 standard part supports a LOAD RAM (3Ah) command. This command allows the host to load & execute 65C02 microcode in externally configured RAM in the hex 0300-EFFF range. This permits the user to take advantage of the standard part internal 4K byte ROM, while also executing additional specialized microcode where required for user specific applications.

Prior to performing a LOAD RAM sequence of commands with the ICS2010, the chip should be placed into a quiescent state by issuing a Soft Reset (00h) command. This will eliminate the possibility of any SMPTE or MIDI activity interfering with the LOAD RAM procedure.

The LOAD RAM records loaded by the host must be in Intel Hex Format, with each data record containing no more than 32 data bytes. Also, the checksum field of each record must be valid per the Intel Hex Format described in detail below. An error in any of the record's parameters, such as an incorrect checksum, will result in the 65C02 returning an error indication to the host in the normal manner of setting the command byte to FFh.

Each record to be loaded is written individually by the host into the ICS2010 via the Indirect Register Data starting at the command mailbox address 00h and the remainder of the bytes within the record following sequentially. That is, the very first byte of the Intel Hex Formatted record, which is always an ASCII ":", is written into the first byte of the ICS2010 Zero Page memory, with the remainder of the bytes of the record being written into the successive Zero Page memory locations. The host then activates the Internal Processor Interrupt by setting the IPI bit in the SMPTE1 register. This results in the 65C02 interpreting the leading ":" character as a command byte with value 3Ah which is the LOAD RAM command.

INTEL HEX FORMAT

Byte#	Field Name	Description
1	Record Marker	The first byte of every Intel Hex Format record is always an ASCII colon ":" which is a hexadecimal 3A.
2-3	Record Length	This field always consists of 2 ASCII characters which indicate the number of data bytes in the Data Field portion of this record. The 2 characters are created by converting the number of data bytes in hexadecimal into 2 ASCII characters, high digit first. (Example: A byte count of 30 is hex 1E, therefore, Byte #2 = the ASCII character "1" or hex 31, Byte #3 = the ASCII character "E" or hex 45.) A Data Record can have from 0 to 32 data bytes. An EOF Record normally has 2 ASCII "0" characters in this field; the ICS2010 LOAD RAM command will not validate the content of the Record Length for EOF Records other than including in the Checksum. A Start Address Record must have an ASCII "02" in the Record Length field for the 2 data bytes of the Start Address found in the Data Field of the record.
4-7	Load Address	This field always consists of 4 ASCII characters which indicate the starting RAM address at which a Data Record's data bytes will be stored into. The 4 characters are created by converting the hexadecimal representation of the 16-bit address into 4 ASCII characters: Byte #4 = High digit of Most Significant Address Byte Byte #5 = Low digit of Most Significant Address Byte Byte #6 = High digit of Least Significant Address Byte Byte #7 = Low digit of Least Significant Address Byte

8-9	Record Type	This field identifies the record type and will always contain one of the following 3 settings, each a pair of ASCII characters: "00" - Data Record "01" - EOF Record "03" - Start Address Record
10-N	Data	This field contains the record's data. Each byte of the data is represented by 2 ASCII characters which are created by conversion from the bytes hexadecimal value as previously described, high digit first. Since there are 2 ASCII characters for every byte of data, the Data Field of a record is twice as long as the data byte count indicated in the Record Length field. For a Data Record, the Data Field will contain 0 to 64 ASCII characters representing the up to 32 data bytes to be loaded into the ICS2010 external RAM. For a Start Address Record, the Data Field will contain exactly 4 ASCII characters representing the 16-bit address at which execution is to jump. These 4 characters are in the same format as those of the Load Address field described above. For an EOF Record, the Data Field is normally empty and thus the following Checksum Field begins at record Byte #10.
N+1, N+2	Checksum	The checksum is a simple 8-bit binary sum of the hexadecimal values of the Record Length Field, the Load Address Field, and the Data Field, which is then negated by performing a 2's complement subtract from 00h. The resultant value is then converted into 2 ASCII characters and stored in the Checksum Field, high digit first.

Data Records will contain from 0 to 32 bytes of data which will be copied to consecutive RAM locations beginning at the 16-bit address specified in the Load Address field of the Data Record. Intel Hex Format permits Data Records to contain up to 255 data bytes. However, the user must limit the ICS2010 LOAD RAM Data Records to 32 data bytes so as to avoid the record overlaying internal parameters of the 65C02 microcode when copied into the ICS2010 Zero Page memory. The 65C02 will acknowledge the LOAD RAM command for a Data Record in the normal manner of setting the command byte to FEh, after it has completed copy of the data bytes into RAM.

EOF Records will have their checksum verified and, if correct, will simply be acknowledged by the 65C02 without performing any other activity.

Start Address Records must contain 2 bytes of data which will reflect the 16-bit address to which execution is to jump. This execution jump occurs before an acknowledge is given to the host, thus making it the responsibility of the newly executing microcode to write the command byte to FEh. This permits any initialization of new microcode parameters to be completed prior to indicating the acknowledgement to the host.

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Fax: (206) 869-9841

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France
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Fax: (01) 69 41 28 46

Italy
Comprel S.P.A
Via Po, 37
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Milan
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Fax: (03) 62 553 967

Germany
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FRG-8033 Planegg
Phone: (089) 8 59 80 21
Fax: (089) 8 57 65 74

Scantec GmbH
Tannenbergstrasse 103
FRG-7312 Kirchheim/Teck
Phone: (7021) 5 40 27
Fax: (7021) 8 25 68

Topas Electronic GmbH
Striehlstrasse 18
FRG-3000 Hannover 1
Phone: (511) 13 12 17
Fax: (511) 13 12 16

Belgium
ACAL Auriema
Lozenberg 4
1940 Zaventem
Phone: 720 59 83
Fax: 725 10 14

Netherlands
ACAL Auriema
Doornakkersweg 26
5642 MP Eindhoven
Phone: 040-816565
Fax: 040-811815

Hong Kong
RTI Industries Co., Ltd.
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Proficient Ind. Center
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Fax: (852) 795-7839

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8-1, Nihonbashi Odenmacho
Chuo-ku, Tokyo 103
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Premier Ki Building, 4F
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Chiyoda-ku, Tokyo 101
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3F, No. 197
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Taipei, Taiwan ROC
Phone: (2) 713-0209
Fax: (2) 712-6780

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
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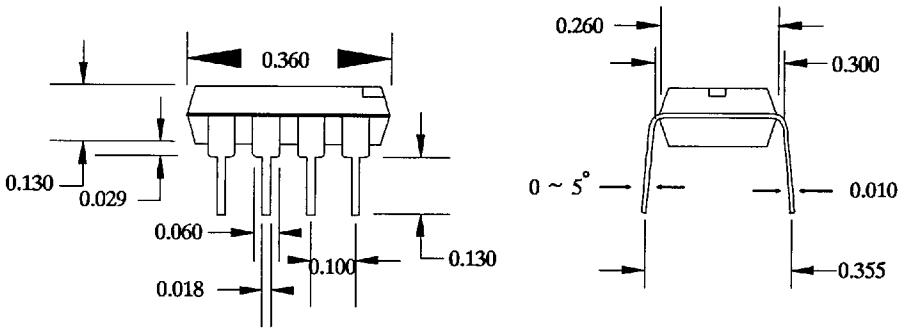
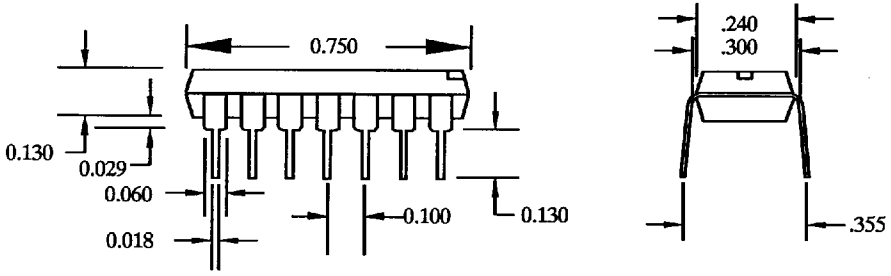
T-90-20

DIP Packages



8 Pin DIP Package



14 Pin DIP Package

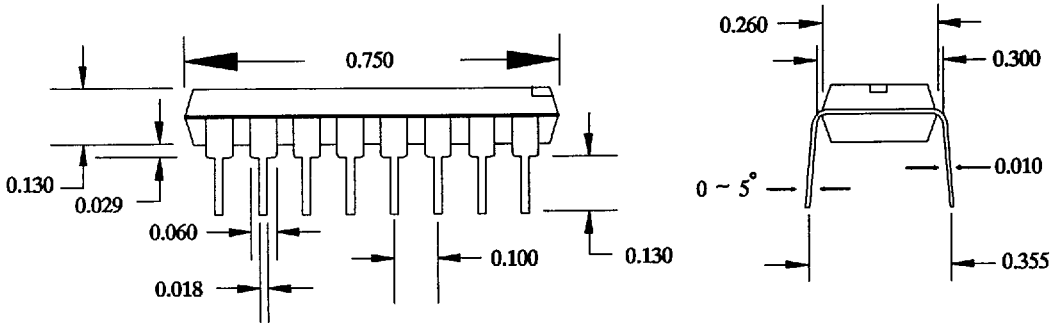
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

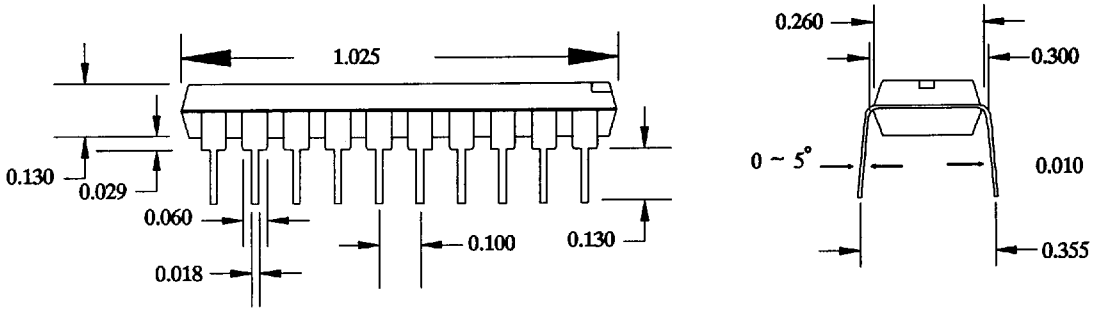
Example: ICSXXXXN

H

DIP Packages



16 Pin DIP Package



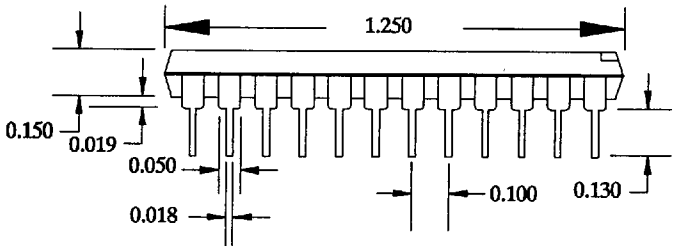
20 Pin DIP Package

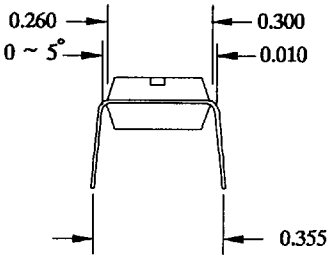
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

DIP Packages





24 Pin DIP Package

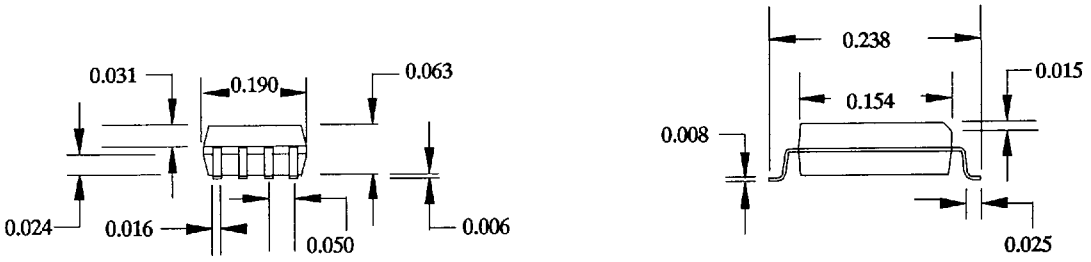
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

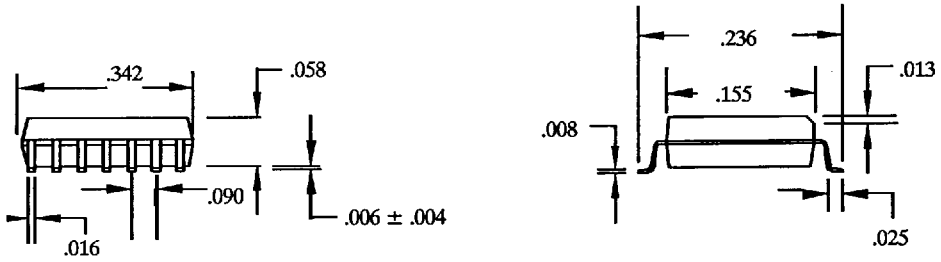
Example: ICSXXXXN

H

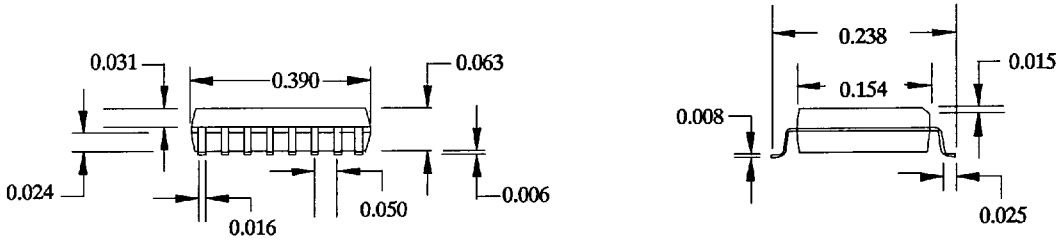
SO Packages



8 Pin SO Package



14 Pin SO Package



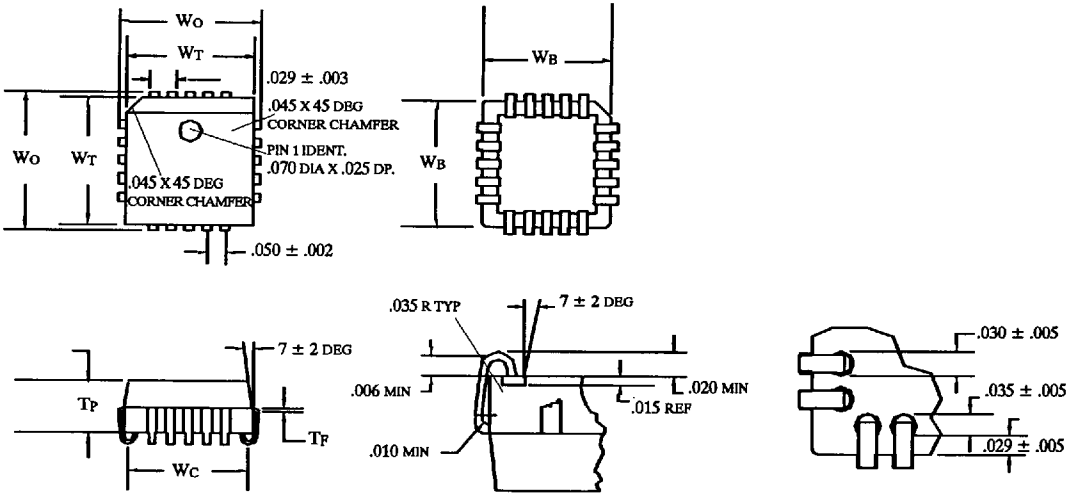
16 Pin SO Package

Ordering Information:

All ICS devices in SO packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM

PLCC Packages



LEAD COUNT	FRAME THICKNESS T_F +/-.0003	PKG. THICKNESS T_P +/-.004	PKG. WIDTH TOP W_T +/-.004	PKG. WIDTH BOTTOM W_B +/-.066	OVERALL PKG. WIDTH W_O +/-.005	CONTACT WIDTH W_O +.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

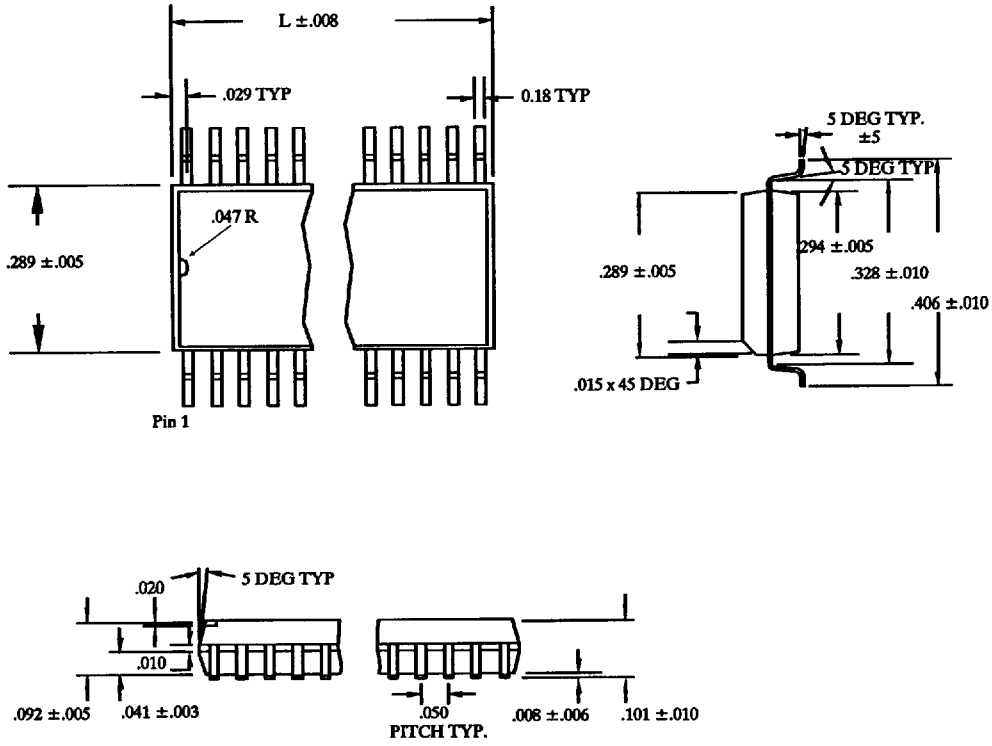
Ordering Information:

All ICS devices in PLCC packages carry a "V" designation. See individual data sheets for more specific information.

Example: ICSXXXXV

H

SOIC Packages



SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	.354	.404	.454	.504	.604	.704	.704

Ordering Information:

All ICS devices in SOIC packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM