C9850

High Performance Pentium®III Clock Generator

Product Features

- Four differential host clocks
- Two 3V Mref single ended for DRCG
- Four 3V, 66 MHz clocks
- Ten 3V, 33 MHz PCI clocks
- Two 48 MHz clocks
- Two 14.318 MHz reference clocks
- Select logic for Differential Swing Control, Test mode, Hi-Z, Power-down, Spread spectrum, and frequency selection
- External resistor for CPU current reference
- 56 Pin SSOP and TSSOP Package

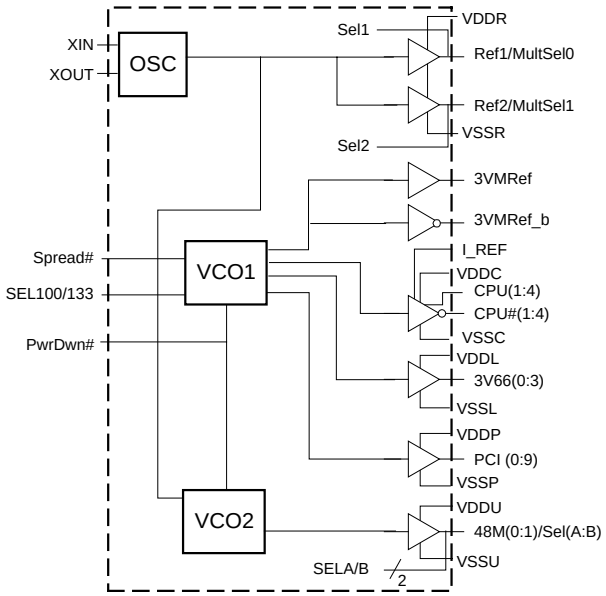
Product Description

This device is an advanced performance single package clock solution for high end Pentium III designs using Rambus memory system architectures. It provides all of the system motherboard's clocks needed to support the CPU, memory and peripheral devices. Included in the frequency table are specific +5% margin test frequencies to assist designers in verification of adequate timing margins in designs. All CPU (Host) clocks are deferential and comply with Intel specified timing requirements.

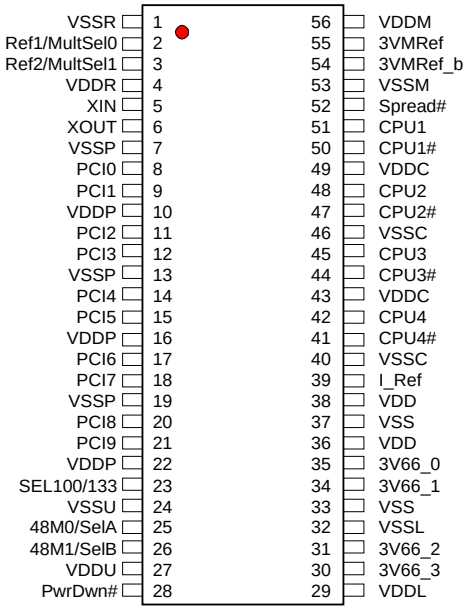
Frequency Selection Table

SEL 100/133	SELA	SELB	CPU(1:4), CPU# (1:4)	3VMRef/ 3VMRef_b	3V66 (0:3)	PCI (0:9)	48 M (0:1)	REF (1:2)
0	0	0	100 MHz	50 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
0	0	1	105 MHz	52.5 MHz	70.0 MHz	35.0 MHz	48 MHz	14.318 MHz
0	1	0	200 MHz	50 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
0	1	1	High Z	High Z	High Z	High Z	High Z	High Z
1	0	0	133.3 MHz	66.7 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
1	0	1	126.7 MHz	63.3 MHz	63.3 MHz	31.7 MHz	48 MHz	14.318 MHz
1	1	0	200 MHz	66.7 MHz	66.7 MHz	33.3 MHz	48 MHz	14.318 MHz
1	1	1	XIN/2	XIN/4	XIN/4	XIN/8	XIN/2	XIN

Block Diagram



Pin Configuration



Pin Description

PIN No.	Pin Name	I/O	Description
55	3VMRef	O	3V reference to memory clock driver. It is synchronous to the CPU clock. See table 1, pg 1 for spread selection.
54	3VMRef_b	O	3V reference to memory clock driver (180° out of phase with 3VMref).
52*	Spread#	I	Invokes Spread Spectrum functionality on the Differential Host clocks. MRef/MRef_b clocks, 66 MHz clocks, and 33 MHz PCI clocks. Active Low.
51	CPU1	O	CPU clock pair. These two clocks are 180° out of phase with each other. See the table on page 1 of this data sheet for the frequency selections.
50	CPU1#		
48	CPU2	O	CPU clock pair. These two differential clocks are 180° out of phase with each other. See the table on page 1 of this data sheet for the frequency selections.
47	CPU2#		
45	CPU3	O	CPU clock pair. These two differential clocks are 180° out of phase with each other. See the table on page 1 of this data sheet for the frequency selections.
44	CPU3#		
42	CPU4	O	CPU clock pair. These two differential clocks are 180° out of phase with each other. See the table on page 1 of this data sheet for the frequency selections.
41	CPU4#		
39	I_Ref		This pin is the reference current input for the CPU pairs. This pin takes a fixed precision resistor tied to ground in order to establish the appropriate current. See pg. 9.
35, 34, 31, 30	3V66 (0:3)	O	66.67 MHz 3.3 Volt outputs. These clocks are differential to the CPU clocks.
28*	PwrDwn#	I	Invokes power-down mode. Active Low. Sets all clocks low.
25*	48 M0/SelA		SelA and SelB inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 48 MHz clocks.
26*	48 M1/SelB		
23*	SEL100/133	I	CPU frequency select pin. See the table on page 1 of this data sheet for the frequency selections.
21, 20, 18, 17, 15, 14, 12, 11, 9, 8	PCI (0:9)	O	3.3V 33 MHz PCI output clocks. See the table on page 1 of this data sheet for the frequency selections.
6	XOUT	O	14.318 MHz crystal output.
5	XIN	I	14.318 MHz crystal input.
2	Ref1/MultSel (0)	I	MultSel0 and MultSel1 inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 14.318 MHz clocks. They sel I_Ref values, see pg. 9.
3	Ref2/MultSel (1)		
56	VDDM	P	Power pin recommended 3 Vmref and 3Vmref_b dedicated use.
53	VSSM	P	Ground pin recommended for 3Vmref and 3Vmref_b dedicated use.
49	VDDC	P	Power pin recommended for CPU/CPU# dedicated use.
46	VSSC	P	Ground pin recommended for CPU/CPU# dedicated use.
38, 36	VDD	P	Power pin recommended for dedicated core use.
37, 33	VSS	P	Ground pin recommended for dedicated core use.
29	VDDL	P	Power pins recommended for 3V66 dedicated use.
32	VSSL	P	Ground pin recommended for 3V66 dedicated use.

Pin Description (cont.)

PIN No.	Pin Name	I/O	Description
27	VDDU	P	Power pin recommended for 48 MHz dedicated use.
24	VSSU	P	Ground pin recommended for 48 MHz dedicated use.
22, 16, 10	VDDP	P	Power pins recommended for PCI dedicated use.
19, 13, 7	VSSP	P	Ground pins recommended for PCI dedicated use.
4	VDDR	P	Power pin recommended for Ref clock and Xtal dedicated use.
1	VSSR	P	Ground pin recommended for Ref clock and Xtal dedicated use.

Note: All pin numbers that are followed with an astirik (*) contain internal pull-up resistors. These internal devices are sufficient enough to guarantee a logic 1 will be sensed internally of no external circuitry is connected.

Power on Bi-Directional Pins

Power Up Condition:

Pins 2, 3, 25, and 26 are Power up bi-directional pins and are used for different features in this device (see Pin description, Page 2). During power-up, these pins are in input mode (see Fig 2, below), therefore, they are considered input select pins internal to the IC. After a settling time, the Selection data is latch into internal control registers and these pins become toggling clock outputs.

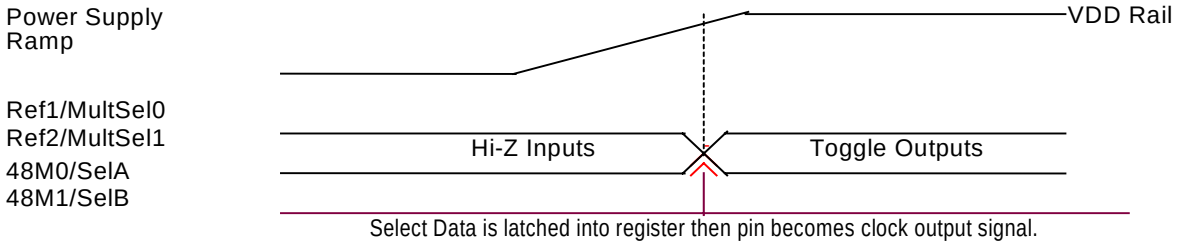


Fig. 1

Strapping Resistor Options for pins with internal Pull-ups:

The power up bidirectional pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 3mS settling time), then **it is recommended** to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig. 2A and Fig. 2B.

Fig. 2A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.2A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 2B represent a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

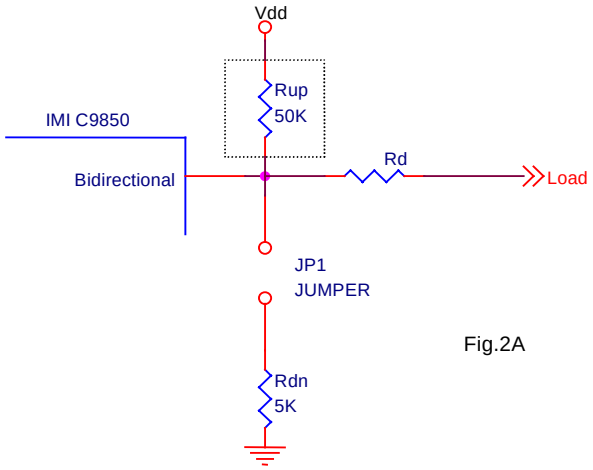


Fig.2A

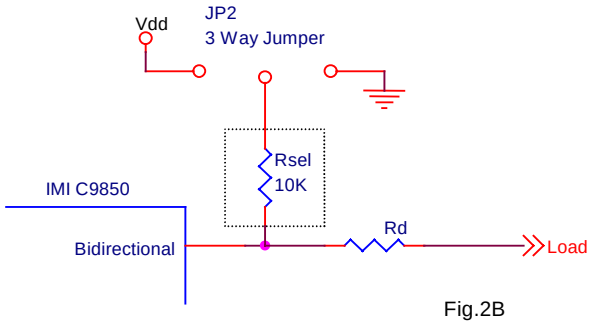


Fig.2B

Maximum Ratings[1]

Maximum Input Voltage:	VSS - 0.5V
Maximum Input Voltage:	VDD + 0.7V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	0°C to +85°C
Maximum ESD protection	2000V
Maximum Power Supply:	5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD)

[1] Note: 1. The voltage on any input or I/O cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Parameters

Characteristic	Symbol	Min	TYP	Max	Units	Conditions
Supply Voltage	VDD3	3.135		3.465	V	
Input High Voltage	Vih3	2.0		VDD +0.3	V	Note 1
Input Low Voltage	Vil3	VSS – 0.3		0.8	V	Note 1
Input Leakage Current	IiL	-5		+5	µA	$0 < V_{in} < V_{DD}$
Tri-State leakage Current	Ioz	-	-	±10	µA	
Input Low Current (@Vin = VSS)	IIL	-66		-5	µA	For pins with internal Pull up resistors, Note 3
Input High Current (@Vin = VDD)	IIH			5	µA	
Dynamic Supply Current	Idd	-	-	250	mA	475Ω current reference at Iout=*Iref, CPU=133MHz, Msel0 = 0, Msel1 = 1
Power Down Current (VDD)	Idd_{PD}	-	-	60	mA	PwrDwn# pin = low
Input Pin Capacitance	Cin			5	pF	Except XIN and XOUT
Crystal Pin capacitance	Cxtal	34	36	38	pF	Present between both Pin 5 and 6 to Ground.
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
Ambient Temperature	Ta	0		70	°C	No Airflow

Notes

1. All inputs are specified when using a 3.3V power supply.
2. Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.

AC Parameters

Characteristic	Symbol	133 MHz CPU		100 MHz CPU		Units	Notes
		Min	Max	Min	Max		
CPU CLK period - average	TPeriod	7.5	7.65	10.0	10.2	nS	11
Absolute minimum CPU CLK Period	Abs/MinPeriod	7.35	N/A	9.85	N/A	nS	11
Output Current (CPU) (Voltage at given load)	Ioh (Voh)	12.9 (0.66)	14.9 (0.76)	12.9 (0.66)	14.9 (0.75)	mA (V)	11
	Vol	VSS= 0.0	0.05	VSS = 0.0	0.05	V	11
Vcrossover	Vcrossover	45% Voh	55% Voh	45% Voh	55% Voh	V	11
Host/CPU CLK rise time	TRISE	175	700	175	700	pS	11, 12
Host/CPU CLK fall time	TFALL	175	700	175	700	pS	11, 12
Rise time and fall time matching	Rise/Fall Matching		20%		20%		11
	Overshoot		Voh + 0.2V		Voh + 0.2V		11
	Undershoot	-0.2		-0.2		V	11
Cycle to Cycle jitter	TJcc		200 pS		200 pS	pS	13
CPU to CPU clock skew	Tskew		150		150	pS	
Duty Cycle	Tdc	45	55	45	55	%	11
Mref, Mref_b CLK period	TPeriod	15.0	15.3	20.	20.4	nS	2, 9
Mref, Mref_b CLK high time	THIGH	5.25	N/A	7.5	N/A	nS	5, 10
Mref, Mref_b CLK low time	TLOW	5.05	N/A	7.3	N/A	nS	6, 10
Mref, Mref_b CLK rise time	TRISE	0.4	1.6	0.4	1.6	nS	8
Mref, Mref_b, CLK fall time	TFALL	0.4	1.6	0.4	1.6	nS	8
Mref and Mref_b Duty Cycle	Tdc	45	55	45	55	%	11
Mref & Mref_b Cycle to Cycle jitter	TJcc		250 pS		250 pS	pS	12
REF CLK rise time	TRISE	2.0		2.0		nS	8
REF CLK fall time	TFALL	2.0		2.0		nS	8
REF Duty Cycle	Tdc	45	55	45	55	%	11
REF Cycle to Cycle jitter	TJcc		1.0		1.0	nS	12
48M CLK rise time	TRISE	2.0		2.0		nS	8
48M CLK fall time	TFALL	2.0		2.0		nS	8
48M Duty Cycle	Tdc	45	55	45	55	%	11
48M Cycle to Cycle jitter	TJcc		350		350	pS	12

AC Parameters (Cont.)

Characteristic	Symbol	133 MHz CPU		100 MHz CPU		Units	Notes
		Min	Max	Min	Max		
3V66 CLK period	TPeriod	15.0	16.0	15.0	15.2	nS	
3V66 CLK high time	THIGH	5.25	N/A	5.25	N/A	nS	2, 9
3V66 CLK low time	TLOW	5.05	N/A	5.05	N/A	nS	5, 10
3V66 CLK rise time	TRISE	0.5	2.0	0.5	2.0	nS	6, 10
3V66 CLK fall time	TFALL	0.5	2.0	0.5	2.0	nS	8
3V66 Duty Cycle	Tdc	45	55	45	55	%	11
3V66 to 3V66 clock skew	Tskew		250		250	pS	
3V66 Cycle to Cycle jitter	TJcc		300 pS		300 pS	pS	12
PCI CLK period	TPeriod	30.0		30.0		nS	8
PCI CLK high time	THIGH	12.0		12.0		nS	2, 9
PCI CLK low time	TLOW	12.0		12.0		nS	5, 10
PCI CLK rise time	TRISE	0.5	2.0	0.5	2.0	nS	6, 10
PCI CLK fall time	TFALL	0.5	2.0	0.5	2.0	nS	8
PCI Duty Cycle	Tdc	45	55	45	55	%	11
PCI to PCI clock skew	Tskew		500		500	pS	
PCI Cycle to Cycle jitter	TJcc		500		500	pS	12
Output enable delay (all outputs)	tpZL, tpZH	1.0	10.0	1.0	10.0	nS	
Output disable delay (all outputs)	tpLZ, tpZH	1.0	10.0	1.0	10.0	nS	
All clock Stabilization from power-up	Tstable		3		3	nS	7

Notes:

1. All output drivers have monotonic rise/fall times through the specified VOL/VOH levels.
2. Period, jitter, offset and skew measured on rising edge @ 1.25V for 2.5V clocks and @1.5V for 3.3V clocks.
3. The PCI clock is the Host clock divided by four at Host = 133 MHz. PCI clock is the host clock divided by three at Host = 100 MHz.
4. 3V66 is internal VCO frequency divided by four for Host = 133 MHz. 3V66 clock is internal VCO frequency divided by three for Host = 100 MHz.
5. THIGH is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
6. TLOW is measured at 0.4V for all outputs.
7. The time specified is measured from when VDD achieves its nominal operating level (typical condition VDD = 3.3V) till the frequency output is stable and operating within specification.
8. TRISE and TFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.0V
9. The average period over any 1 uS period of time is greater than the minimum specified period.
10. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle.
11. CPU clock test load is Rs=33.2 Ohms, Rp = 49.9.
12. 20% and 80%
13. Measured at 1.25 Volts
14. Measured at 1.50 Volts

Group to Group Offset Limits

Groups	Offset	Measurement Loads (Lumped)	Measure Point
3V66 to PCI	1.5-3.5 nS 3V66 leads	3V66@ 30 pF, PCI @ 30 pF	3V66@ 1.5V, PCI @ 1.5 V

Notes:
1. All offsets are to be measured at rising edges.

Lumped Capacitive Test Loads for Single Ended Outputs

Clock	Max Load	Units
PCI Clocks (PCLK)	30	pF
Mref, Mref_b	20	pF
3V66	30	pF
48 MHz Clock	20	pF
REF	20	pF
CPU (1:4), (1:4)#	Rs = 33.2, Rp = 49.9	Ohm

Test and Measurement Setup

For Differential Output Signals
The following shows lumped test load configurations for the differential Host Clock Outputs. Multsel(0:1) = (0, 1)

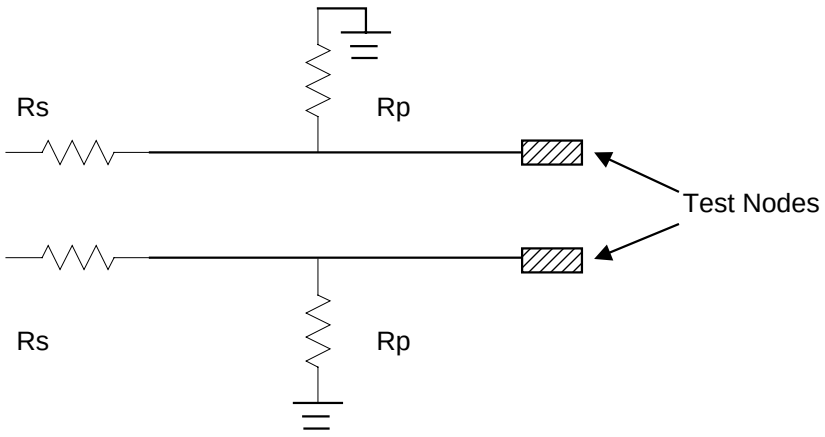
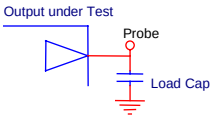
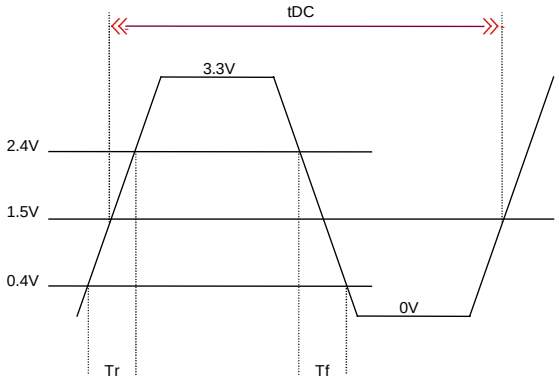


Figure 3. Lumped Test Load Configuration

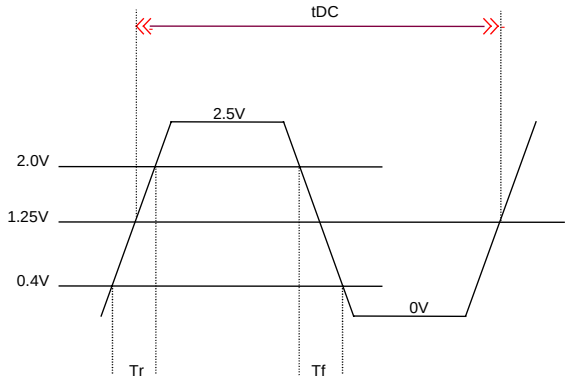
For Single Ended Output Signals



3.3V signals



2.5V signals



Spectrum Spread Clocking Description

Spread Spectrum is a modulation technique for distributing clock period over a certain bandwidth (called Spread Bandwidth). This technique allows the distribution of the energy (EMI) over a range of frequencies therefore reducing the radiation generated from clocks. As the spread is a percentage of the rested (non-spread) frequency, it is effective at the fundamental and all its harmonics.

In this device Spread Spectrum is enabled through pin 52 (Spread#). As the name suggests, spread spectrum is enabled when Spread# is low. This pin has a 250KΩ internal pull up, therefore, defaults to a high (Spread Spectrum disabled) unless externally forced to a low.

When Spread# is forced low, the device will be down spread (fig.5B) mode at –0.5%, and the center frequency is shifted down from its rested (non-spread) value by -0.25%. (ex.: assuming the center frequency is 100MHz in non-spread mode; when down spread is enabled, the center frequency shifts to 99.75MHz.), see fig.4 below.

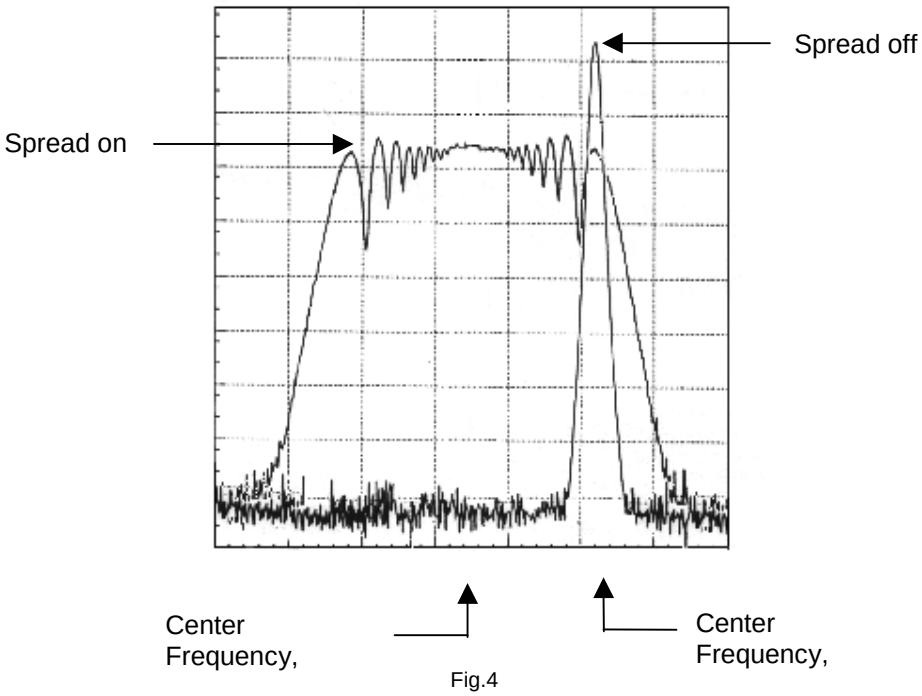


Fig.4

Spectrum Spreading Selection Table

Unspread Frequency in MHz	Down Spreading			
Desired	F Min (MHz)	F Center (MHz)	F Max (MHz)	Spread (%)
100.0	99.5	99.75	100.0	.5
133.3	132.2	132.6	133.3	.5

Host Swing Select Functions

MultSel0	MultSel1	Board Target Trace/TermZ	Reference Rr, Iref = Vdd/(3*Rr)	Output Current	Voh @Z, Iref = 2.32mA
0	**0**	**60 Ohms**	**Rf = 475 1%, Iref = 2.32mA**	**Ioh = 5*Iref**	**0.7V @ 60**
0	0	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6*Iref	0.85V @ 60
0	**1**	**50 Ohms**	**Rr = 475 1%, Iref = 2.32mA**	**Ioh = 6*Iref**	**0.71V @ 50**
1	0	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60V @ 30
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5Ma	Ioh = 7*Iref	0.84V @ 20

Note: The entries in boldface are the primary system configurations of interest. The outputs should be optimized for these configurations.

Buffer Characteristics

Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained in the previous table of this data sheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit - Ro (see Figure 5).
2. Minimum and maximum required voltage operation range of the circuit – Vop (see Figure 5).
3. Series resistance in the buffer circuit – Ros (see Figure 5).
4. Current accuracy at given configuration into nominal test load for given configuration.

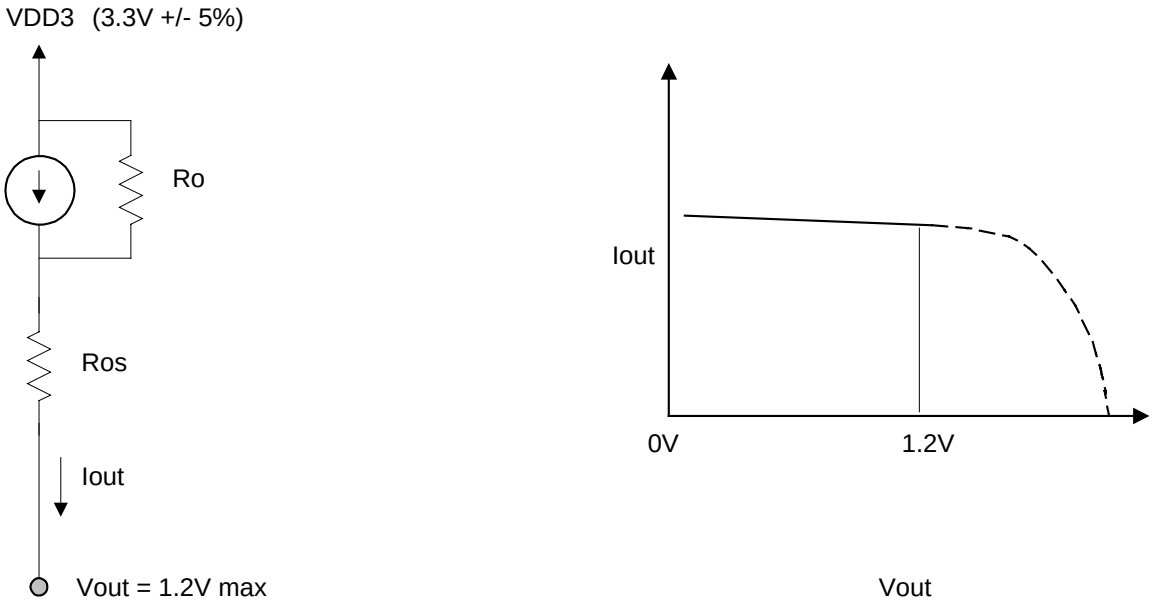


Figure 5

Host Clock (HCSL) Buffer Characteristics

Characteristic	Minimum	Maximum
Ro	3000 Ohms (recommended)	N/A
Ros		
Vout	N/A	1.2V

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is +/- 7% as shown in the table current accuracy (page 13).

Current Accuracy

	Conditions	Configuration	Load	Min	Max
Iout	VDD = nominal (3.30V)	All combinations of M0, M1 and Rr shown in host Swing Select Function Table	Nominal test load for given configuration	-7% Inom	+ 7% Inom
Iout	VDD = 3.30 +/- 5%	All combinations of M0, m1 and Rr shown in Host Swing Select Function Table	Nominal test load for given configuration	-12% Inom	+ 12% Inom

Note: Inom refers to the expected current based on the configuration of the device.

Buffer Characteristics for 48 MHz and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-12		-53	mA	VOH=VDDmin-0.5V (2.64V)
Pull-Up Current Max	IOH_{max}	-27		-92	mA	VOH=VDDmin/2 (1.56V)
Pull-Down Current Min	IOL_{min}	9		27	mA	VOL=0.4V
Pull-Down Current Max	IOL_{max}	26		79	mA	VOL=VDDmin/2 (1.56V)
3.3V Output Rise Edge Rate	Trh	0.5	-	2.0	V/nS	3.3V +/- 5% @ 0.4V – 2.4 V
3.3V Output Fall Edge Rate	Tfh	0.5	-	2.0	V/nS	3.3V +/- 5% @ 2.4V – 0.4 V
Output Impedance	Zo	20	40	60	Ω	

Buffer Characteristics for PCI, 3V66, MRef, MRef_b

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-11		-83	mA	VOH=VDD-0.5V (2.64V)
Pull-Up Current Max	IOH_{max}	-30		-184	mA	V OH=VDD/2 (1.56V)
Pull-Down Current Min	IOL_{min}	9		38	mA	VOL=0.4V
Pull-Down Current Max	IOL_{max}	28		148	mA	VOL=VDD/2 (1.56V)
3.3V Output Rise Edge Rate	Trh	1/1	-	4/1	V/nS	3.3V +/- 5% @ 0.4V – 2.4 V
3.3V Output Fall Edge Rate	Tfh	1/1	-	4/1	V/nS	3.3V +/- 5% @ 2.4V – 0.4 V
Output Impedance	Zo	12	30	55	Ω	

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	14.17	14.31818	14.46	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Stability	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

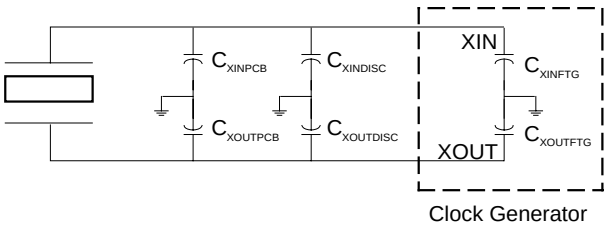
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit trace capacitance (C_{PCB}), and any onboard discrete load capacitance (C_{DISC}).

The following formula and schematic illustrates the application of the loading specification of a crystal (C_{XTAL})for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground

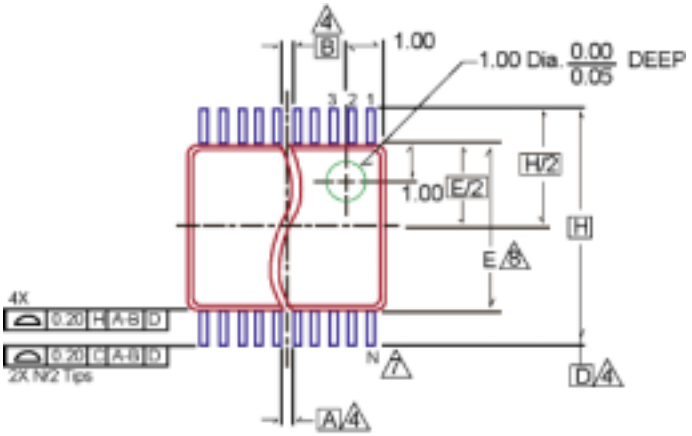


As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

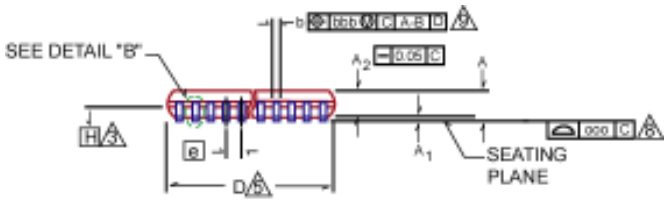
$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF

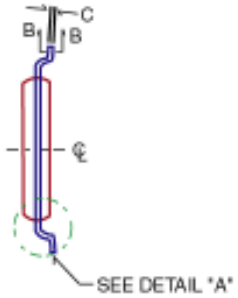
Package Drawing and Dimensions (56 Pin TSSOP)



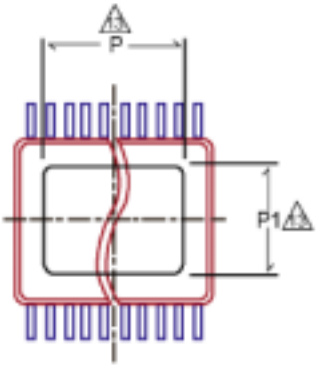
TOP VIEW



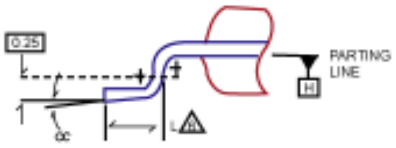
SIDE VIEW



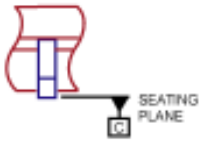
END VIEW



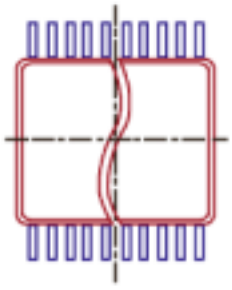
EXPOSED PAD VIEW



DETAIL "A"

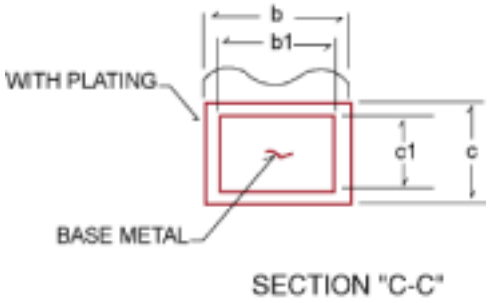


DETAIL "B"

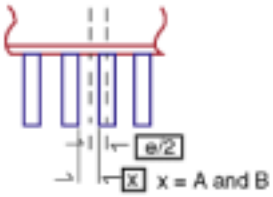


BOTTOM VIEW

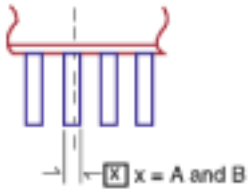
Package Drawing and Dimensions (Cont.)



SECTION "C-C"



EVEN LEAD SIDES
TOPVIEW



ODD LEAD SIDES
TOPVIEW

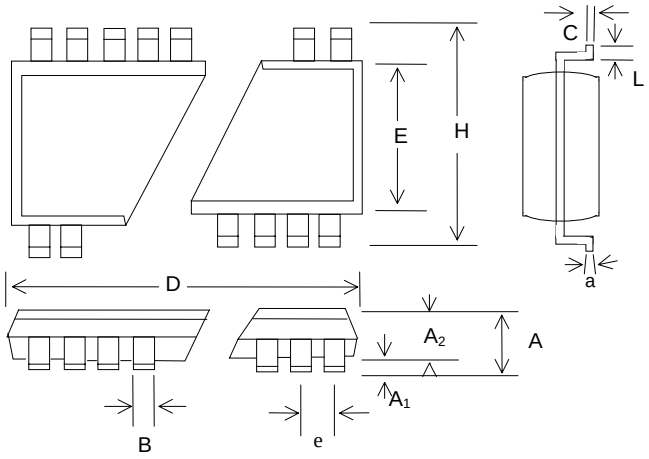
56 Pin TSSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.2794	-	-	1.10
A1	0.0013	0.0025	0.0038	0.05	0.10	0.15
A2	0.0216	0.0229	0.0241	0.85	0.90	0.95
000		0.00254			0.10	
b	0.0043	-	0.0069	0.17	-	0.27
b1	0.0043	0.0051	0.0058	0.17	0.20	0.23
bbb		0.0020			0.08	
c	0.0023	-	0.0051	0.09	-	0.20
c1	0.0023	0.0032	0.0041	0.09	0.127	0.16
θ	0°	-	8°	0°	-	8°
e		0.0127 BSC			0.50 BSC	
H		0.0206			8.10 BSC	
D	0.3531	0.3556	0.3581	13.90	14.00	14.10
E	0.1524	0.1549	0.1575	6.00	6.10	6.20
L	0.0127	0.0152	0.0191	0.50	0.60	0.75

NOTES:

1. Die thickness allowable is 0.279 +/- 0.0127 (0.0110 +/- .005 inches)
2. Dimensions & tolerance per ASME. Y14, 5M-1994.
3. Datum Plane H located at mold parting line and coincident with lead. Where lead exits plastic body at bottom of parting line.
4. Datums A-B and D to be determined where centerline between leads exits plastic body at Datum Plane H.
5. “D” and “E” are reference datums and do not include mode flash or protrusions, and are measured at the bottom parting line. Mold flash or protrusions shall not exceed 0.15mm on D and 0.25mm on E per side.
6. Dimension is the length of terminal for soldering to a substrate.
7. Terminal positions are shown for reference only.
8. Formed leads shall be planar with respect to one another within 0.076mm at seating plane.
9. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the lead width dimension located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead to be 0.08mm for 0.50mm pitch.
10. Section “C-C” to be determined at 0.10 to 0.25mm from the lead tip.
11. This part is compliant with JEDEC specification MO-153, variations DB, DC, DE ED, EE, and FE.

Package Drawing and Dimensions (56 Pin SSOP)



56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

Ordering Information

Part Number	Package Type	Production Flow
C9850AY	56 Pin SSOP	Commercial, 0ºC to +70ºC
C9850AT	56 Pin TSSOP	Commercial, 0ºC to +70ºC

Marking: Example: Cypress
C9850
Date Code, Lot #

C9850AY

Package
Y = SSOP
T = TSSOP

Revision

Device Number

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Document Title: C9850 High Performance Pentium® III Clock Generator
Document Number: 38-07067

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107122	06/11/01	IKA	Convert from IMI to Cypress
*A	122752	12/22/02	RBI	Add power up requirements to maximum ratings information