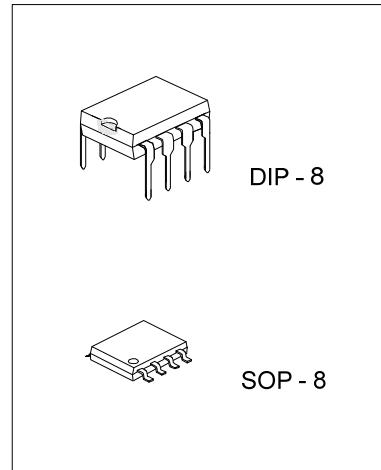


POWER FACTOR CORRECTOR

■ DESCRIPTION

The UTC **L8561** is a Power Factor Corrector, which can work in wide input voltage range applications (from 85V ~ 265V) with an excellent THD. It has very low start up current (about 20 uA) and a disable function on the ZCD pin, which is designed to keep lower current consumption in stand by mode.

The device is operating in transition mode, and is able to drive a Power MOS or IGBT with a ± 400mA current for sourcing and sinking.



■ FEATURES

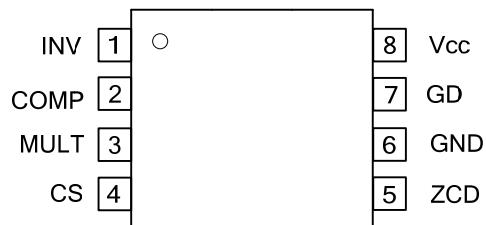
- * 1% Precision (@ $T_J = 25^\circ\text{C}$) Internal Reference Voltage
- * Output Overvoltage Protection
- * Very Low Power Start-Up Current
- * Current Sense Filter On Chip
- * Disable Function (with ZCD pin)
- * Transition Mode Operation
- * Gate Driving Current: ± 400mA
- * 15V Gate clamped

■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|-----------------|--------------|---------|-----------|
| Lead Free | Halogen Free | | |
| L8561L-D08-T | L8561G-D08-T | DIP-8 | Tube |
| L8561L-S08-R | L8561G-S08-R | SOP-8 | Tape Reel |

| | |
|--|--|
| (1)Packing Type (2)Package Type (3)Lead Free | (1) R: Tape Reel, T: Tube (2) S08: SOP-8, D08: DIP-8 (3) G: Halogen Free, L: Lead Free |
|--|--|

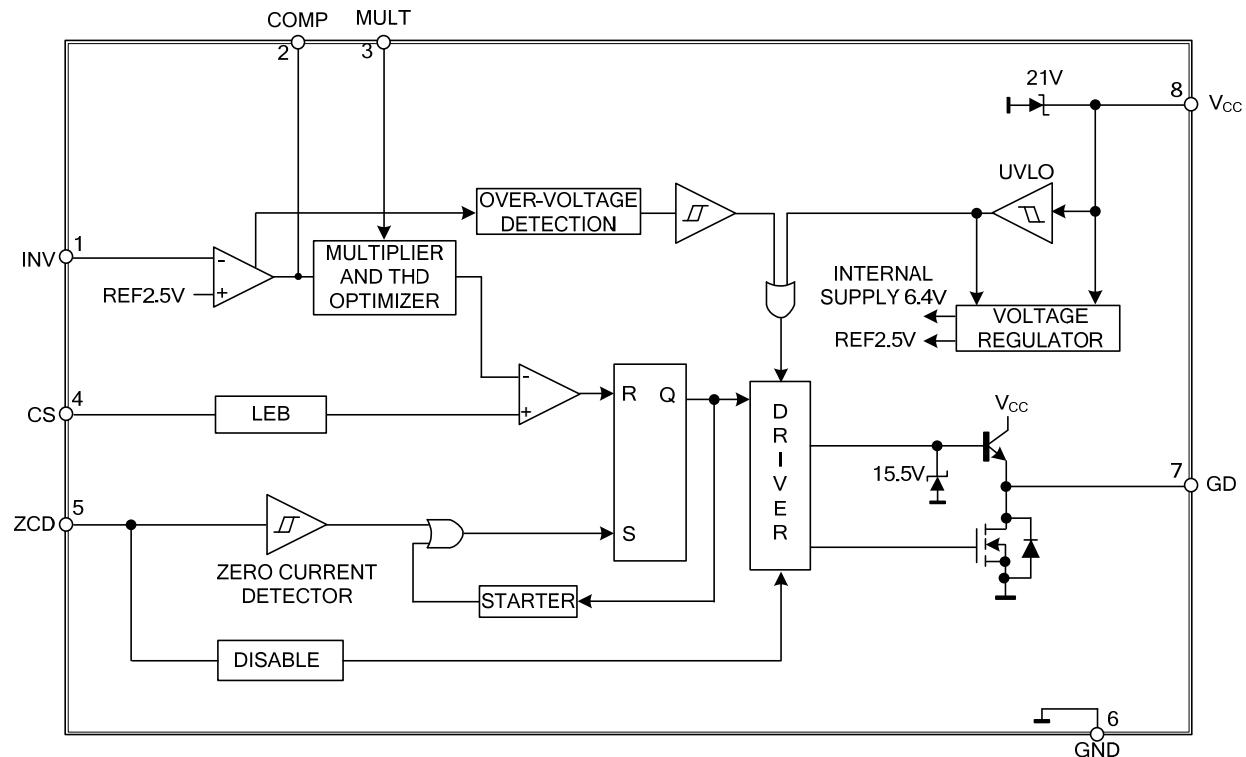
■ PIN CONFIGURATION



■ PIN DESCRIPTION

| PIN NO | PIN NAME | DESCRIPTION |
|--------|-----------------|---|
| 1 | INV | Inverting input of the error amplifier. |
| 2 | COMP | Output of the error amplifier. |
| 3 | MULT | Input of the multiplier stage. |
| 4 | CS | Input of the current sense stage. |
| 5 | ZCD | Input of the zero current detection . |
| 6 | GND | Ground. |
| 7 | GD | Gate driver output. |
| 8 | V _{CC} | Voltage supply. |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta=25°C, unless otherwise specified)

| PARAMETER | | SYMBOL | RATINGS | | UNIT |
|--------------------------------------|-------|------------------|---------------------------|--|----------|
| Analog Inputs & Outputs | | INV, COMP MULT | -0.3 ~ 7 | | V |
| Current Sense Input | | CS | -0.3 ~ 7 | | V |
| Iq+Iz (I _{GD} = 0) | | I _{VCC} | 30 | | mA |
| Output Totem Pole Peak Current (2ms) | | I _{GD} | ±700 | | mA |
| Zero Current Detector | | ZCD | 50 (source) -10 (sink) | | mA mA |
| Power Dissipation @ Ta=50°C | SOP-8 | P _{TOT} | 1 | | W |
| | DIP-8 | | 0.65 | | W |
| Junction Temperature | | T _J | 125 | | °C |
| Operating Temperature | | T _{OPR} | -20 ~ +85 | | °C |
| Storage Temperature | | T _{STG} | -40 ~ +150 | | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (Ta=-25°C ~ 125°C, V_{CC}=14.5V, unless otherwise specified)

| PARAMETER | PIN | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-----|---|---|-------|-------|-------|------|
| SUPPLY VOLTAGE SECTION | | | | | | | |
| Operating Range | 8 | V _{CC} | after turn-on | 11 | | 18 | V |
| Turn-on Threshold | 8 | V _{CC ON} | | 14 | 15.3 | 16.5 | V |
| Turn-off Threshold | 8 | V _{CC OFF} | | 7.2 | 7.9 | 8.7 | V |
| Hysteresis | 8 | Hys | | 6.5 | | 8.3 | V |
| SUPPLY CURRENT SECTION | | | | | | | |
| Start-up Current | 8 | I _{START-U} | V _{CCON} =1V | | 30 | 50 | µA |
| Quiescent Current | 8 | I _Q | | | 6 | 9 | mA |
| Operating Supply Current | 8 | I _{CC} | C _L =1nF @ 70KHz | 10 | 15 | | mA |
| | | | In OVP condition V _{pin1} =2.7V | | | 6.8 | mA |
| Quiescent Current | 8 | I _Q | V _{PIN5} ≤150mV, V _{CC} >V _{CC off} | | | 6 | mA |
| | 8 | | V _{PIN5} ≤150mV, V _{CC} <V _{CC off} | 4 | 7 | 10 | µA |
| Zener Voltage | 8 | V _Z | I _{CC} =20mA | 18 | 21 | 24 | V |
| ERROR AMPLIFIER SECTION | | | | | | | |
| Voltage Feedback Input Threshold | 1 | V _{INV} | Ta=25°C | 2.465 | 2.5 | 2.535 | V |
| | | | 10.3V<V _{CC} <18V | 2.44 | | 2.56 | V |
| Line Regulation | | | V _{CC} =10.3 ~ 18V | | 3 | 5 | mV |
| Input Bias Current | 1 | I _{INV} | | | -100 | -1000 | uA |
| Voltage Gain | | G _V | Open loop | 60 | 80 | | dB |
| Gain Bandwidth | | G _B | | | | 0.8 | MHz |
| Source Current | 2 | I _{COMP} | V _{COMP} =4V, V _{INV} =2.4V | -2 | -4 | -8 | mA |
| Sink Current | | | V _{COMP} =4V, V _{INV} =2.6V | 2.5 | 4.5 | | mA |
| Upper Clamp Voltage | 2 | V _{COMP} | I _{SOURCE} =0.5mA | 4.5 | 5 | 5.5 | V |
| Lower Clamp Voltage | | | I _{SINK} =0.5mA | 2.25 | 2.4 | 2.55 | V |
| MULTIPLIER SECTION | | | | | | | |
| Linear Operating Voltage | 3 | V _{MULT} | | 0~2.5 | 0~3.5 | | V |
| Output Max.Slope | | $\frac{\Delta V_{CS}}{\Delta V_{MULT}}$ | V _{MULT} =from 0V ~ 0.5V V _{COMP} =Upper ClamVoltage | 1.65 | 1.9 | | |
| Gain | | K | V _{MULT} =1V, V _{COMP} =4V | 0.5 | 0.7 | 0.9 | 1/V |

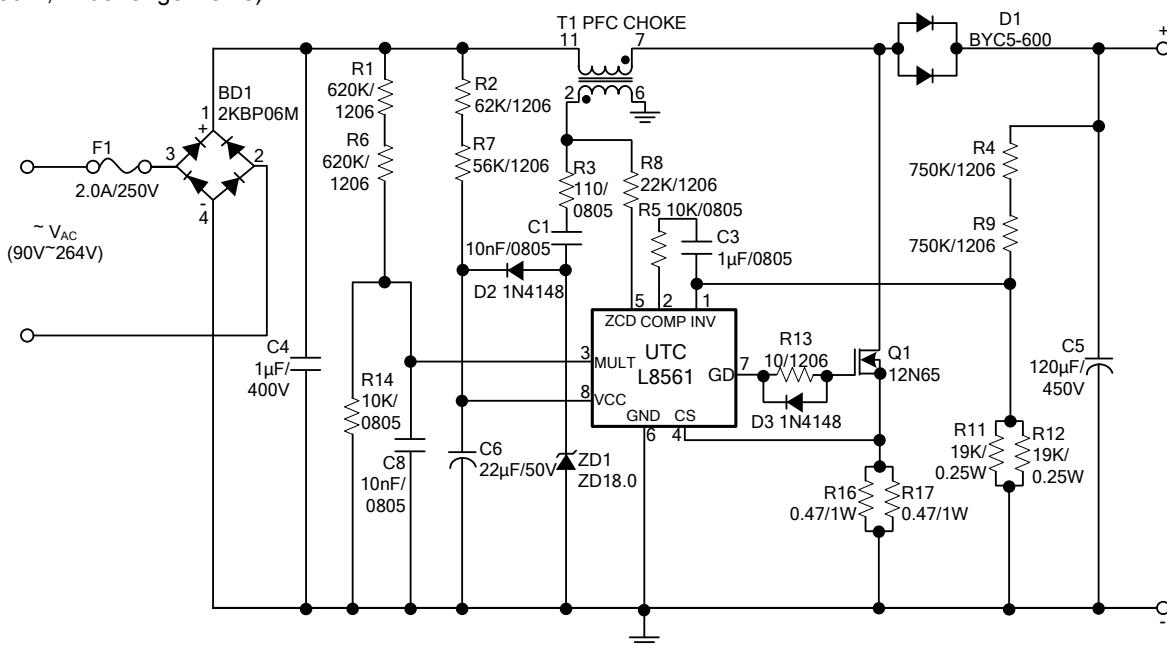
■ ELECTRICAL CHARACTERISTICS(Cont.)

| PARAMETER | PIN | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|-----|---------------|--|------|-------|------|---------|
| CURRENT SENSE COMPARATOR | | | | | | | |
| Current Sense Reference Clamp | 4 | V_{CS} | $V_{MULT}=2.5V$ $V_{COMP}=\text{Upper Clamp Voltage}$ | 1.6 | 1.7 | 1.8 | V |
| Input Bias Current | 4 | I_{CS} | $V_{OS}=0$ | | -0.05 | -1 | μA |
| Delay to Output | 4 | $T_{D(H-L)}$ | | | 200 | 450 | ns |
| ZERO CURRENT DETECTOR | | | | | | | |
| Input Threshold Voltage Rising Edge | 5 | V_{ZCD} | (Note 1) | | 2.1 | | V |
| Hysteresis | | | (Note 1) | 0.4 | 0.6 | 0.8 | V |
| Upper Clamp Voltage | 5 | V_{ZCD} | $I_{ZCD}=20\mu A$ | 5.9 | 6.5 | 7.3 | V |
| Upper Clamp Voltage | 5 | V_{ZCD} | $I_{ZCD}=3mA$ | 6.1 | 6.6 | 7.5 | V |
| Lower Clamp Voltage | 5 | V_{ZCD} | $I_{ZCD}=3mA$ | 0.3 | 0.7 | 1 | V |
| Sink Bias Current | 5 | I_{ZCD} | $1V \leq V_{ZCD} \leq 4.5V$ | | 2 | | μA |
| Source Current Capability | 5 | I_{ZCD} | | -3 | | -10 | mA |
| Sink Current Capability | 5 | I_{ZCD} | | 3 | | 10 | mA |
| Disable threshold | 5 | V_{DIS} | | 100 | 200 | 300 | mV |
| Restart Current After Disable | 5 | I_{ZCD} | $V_{ZCD} < V_{DIS}, V_{CC} > V_{COFF}$ | -20 | -50 | | μA |
| OUTPUT SECTION | | | | | | | |
| Dropout Voltage | 7 | V_{GD} | $I_{GD(SOURCR)}=200mA$ | | 1.2 | 2 | V |
| | | | $I_{GD(SOURCR)}=20mA$ | | 0.8 | 1.2 | V |
| | | | $I_{GD(SINK)}=200mA$ | | 1.2 | 1.9 | V |
| | | | $I_{GD(SINK)}=20mA$ | | 1.2 | | V |
| Output Voltage Rise Time | 7 | t_R | $C_L=1nF$ | | 40 | 100 | ns |
| Output Voltage Fall Time | 7 | t_F | $C_L=1nF$ | | 40 | 100 | ns |
| IGD Sink Current | 7 | $I_{GD(OFF)}$ | $V_{CC}=3.5V, V_{GD}=1V$ | 10 | 40 | | mA |
| OUTPUT OVERVOLTAGE SECTION | | | | | | | |
| OVP Triggering Current | 2 | I_{OVP} | | 30 | 40 | 50 | μA |
| Static OVP Threshold | | | | 2.25 | 2.4 | 2.55 | V |
| RESTART TIMER | | | | | | | |
| Start Timer | | t_{START} | | 70 | 130 | 300 | μs |

Note: 1. Parameter guaranteed by design, not tested in production.

■ TYPICAL APPLICATION CIRCUIT

(150W, Wide-range Mains)



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