D2942, OCTOBER 1986—REVISED JUNE 1990

- **2-A Output Current Capability per Full-H Driver**
- **Wide Range of Output Supply Voltage . . . 5 V to 46 V**
- **Separate Input-Logic Supply Voltage**
- **Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **Functional Replacement for SGS L298**

description

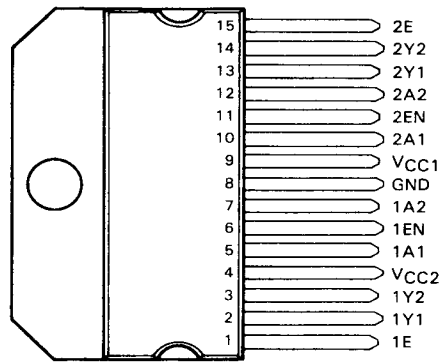
The L298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

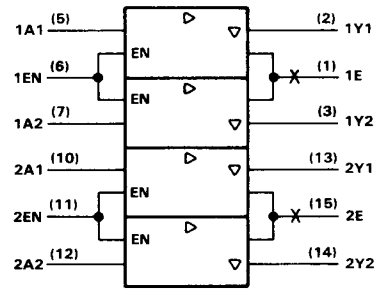
The L298 is designed for operation from 0°C to 70°C.

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8.

logic symbol†



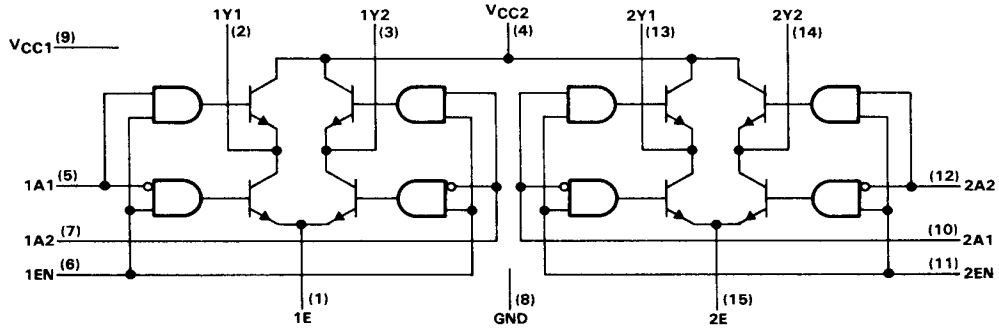
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH CHANNEL)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

‡ In the thermal shutdown mode, the outputs are in the high-impedance state regardless of the input levels.
H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1}, (see Note 1)	7 V
Output supply voltage, V_{CC2}	50 V
Input voltage range at A or EN, V_I	−0.3 to 7 V
Output voltage range, V_O	−2 V to V_{CC2}+2 V
Emitter terminal (1E and 2E) voltage range	−0.5 to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50\ \mu s$)	−1 V
Peak output current, I_{OM}, (nonrepetitive, $t_w \leq 0.1$ ms)	±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%)	±2.5 A
Continuous output current, I_O	±2 A
Peak combined output current for each full-H driver (see Note 2)	
(nonrepetitive, $t_w \leq 0.1$ ms)	±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%)	±2.5 A
Continuous combined output current for each full-H driver (see Note 2)	3.575 W
Continuous dissipation at (or below) 25°C free-air temperature (see Note 3)	3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 3)	25 W
Operating free-air, case, or virtual junction temperature range	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
2. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 4)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 4)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency, f_c			40	kHz
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 4: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower then V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_J = 25 °C (unless otherwise noted)

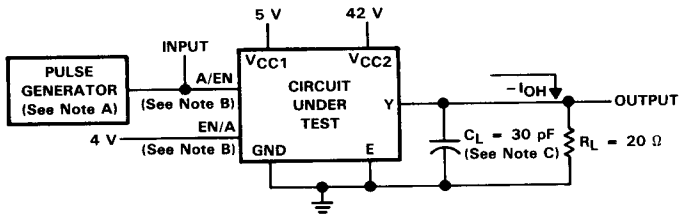
PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A			$V_{CC2}-1.8$	$V_{CC2}-1.2$		V
			I_{OH} = −2 A			$V_{CC2}-2.8$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		I_{OL} = 1 A				$V_E+1.2$	$V_E+1.8$	V
			I_{OL} = 2 A				$V_E+1.7$	$V_E+2.6$	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A		See Note 5		2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 2 A				3.5	5.2	
I_{IH}	High-level input current	A	$V_I = V_{IH}$				30	100	μA
		EN	$V_I = V_{IH} \le V_{CC1}-0.6$ V				30	100	
I_{IL}	Low-level input current		V_I = 0 to 1.5 V					−10	μA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level			7	12	mA
				All outputs at low level			24	32	
				All outputs at high impedance			4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level			38	50	mA
				All outputs at low level			13	20	
				All outputs at high impedance				2	

NOTE 5. The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels.
$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$

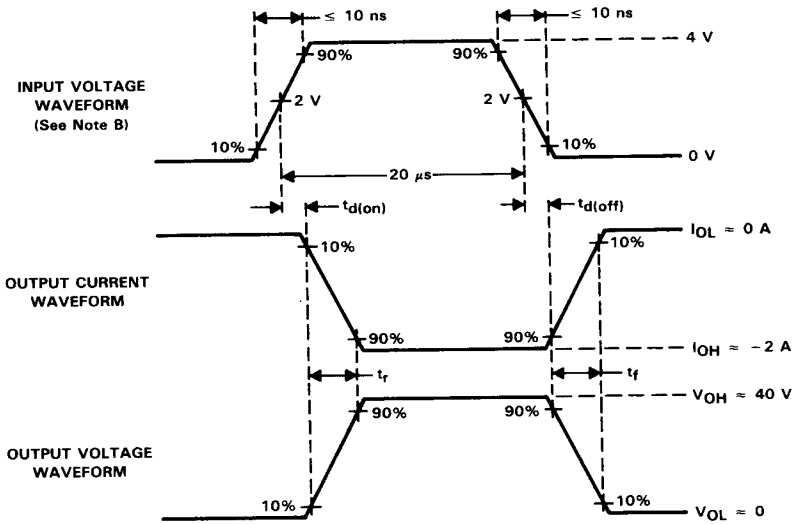
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Source current turn-on delay time from A input	C_L = 30 pF, See Figure 1		2.5		μs
$t_{d(off)}$	Source current turn-off delay time from A input			1.7		μs
t_r	Source current rise time (turning on)			0.4		μs
t_f	Source current fall time (turning off)			0.2		μs
$t_{d(on)}$	Source current turn-on delay time from EN input			2.5		μs
$t_{d(off)}$	Source current turn-off delay time from EN input			1.7		μs
$t_{d(on)}$	Sink current turn-on delay time from A input	C_L = 30 pF, See Figure 2		1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from A input			0.7		μs
t_r	Sink current rise time (turning on)			0.2		μs
t_f	Sink current fall time (turning off)			0.2		μs
$t_{d(on)}$	Sink current turn-on delay time from EN input			1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from EN input			0.7		μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

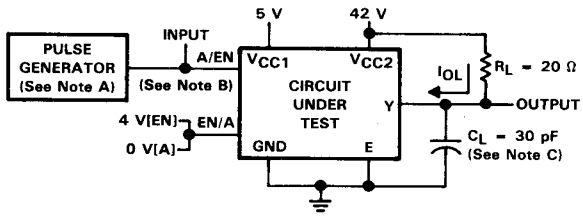


VOLTAGE AND CURRENT WAVEFORMS

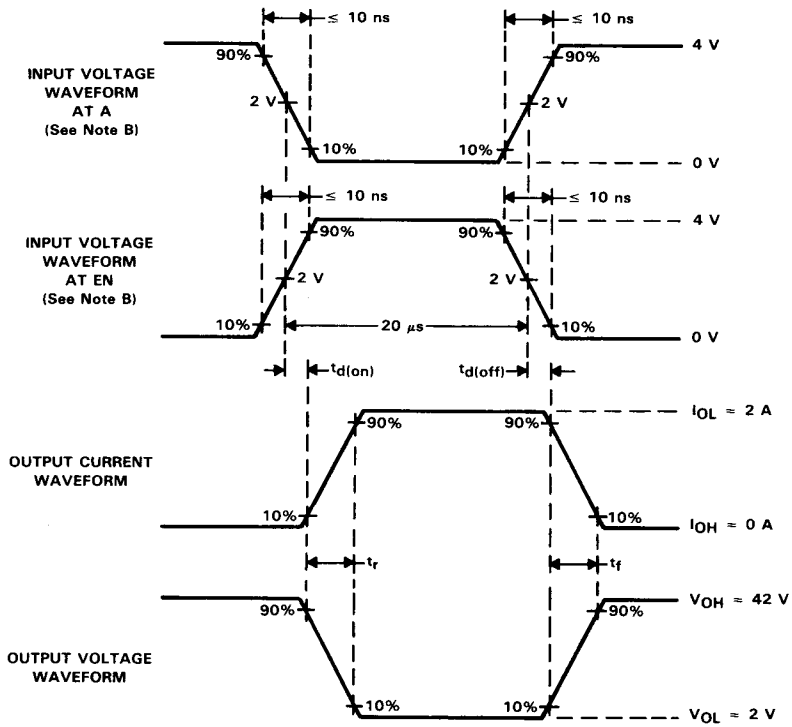
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

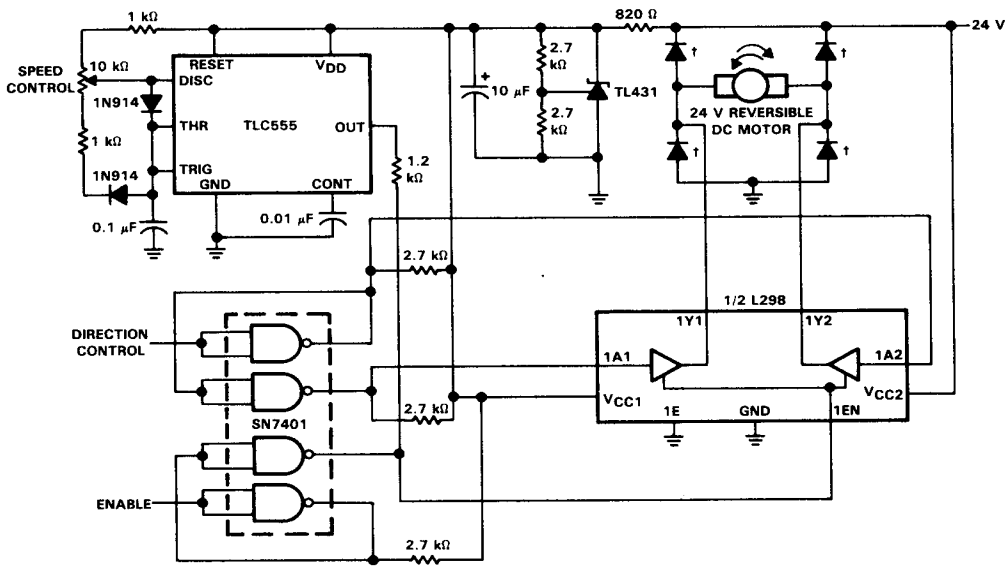
APPLICATION INFORMATION

This circuit shows one half of an L298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the L298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	X	disabled	disabled

X = don't care H = high level L = low level



†Diodes are 1N4934 or equivalent.

FIGURE 3. L298 AS BIDIRECTIONAL DC MOTOR DRIVER