

FEATURES

Latch-up proof
3 pF off source capacitance
5 pF off drain capacitance
0.07 pC charge injection
Low leakage: 0.2 nA maximum at 85°C
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
 V_{SS} to V_{DD} analog signal range

APPLICATIONS

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

GENERAL DESCRIPTION

The ADG5212/ADG5213 contain four independent single-pole/single-throw (SPST) switches. The ADG5212 switches turn on with Logic 1. The ADG5213 has two switches with digital control logic similar to that of the ADG5212; however, the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG5212 and ADG5213 do not have a V_L pin. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed together with high signal bandwidth make the parts suitable for video signal switching.

FUNCTIONAL BLOCK DIAGRAMS

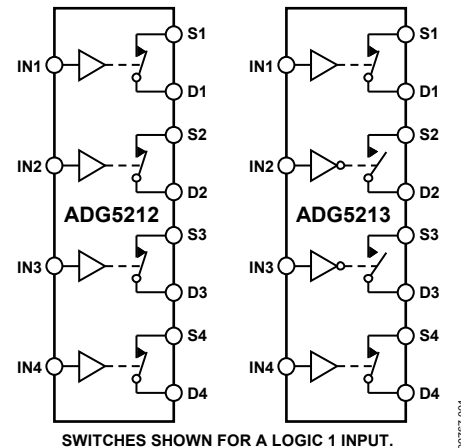


Figure 1.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
A dielectric trench separates the P and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Ultralow Capacitance and <1 pC Charge Injection.
3. Dual-Supply Operation.
For applications where the analog signal is bipolar, the ADG5212/ADG5213 can be operated from dual supplies of up to ±22 V.
4. Single-Supply Operation.
For applications where the analog signal is unipolar, the ADG5212/ADG5213 can be operated from a single rail power supply of up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.
 $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L Logic Power Supply Required.

Rev. 0

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REVISION HISTORY

4/11—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	160			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$, see Figure 24
On-Resistance Match Between Channels, ΔR_{ON}	200	250	280	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
	2			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	8	9	10	Ω max	
	38			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
	50	65	70	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 23
Drain Off Leakage, I_D (Off)	0.1	0.2	0.4	nA max	
	0.01			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 23
Channel On Leakage, I_D (On), I_S (On)	0.1	0.2	0.4	nA max	
	0.02			nA typ	$V_S = V_D = \pm 10\text{ V}$, see Figure 26
	0.2	0.25	0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	175			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	210	255	280	ns max	$V_S = 10\text{ V}$, see Figure 30
t_{OFF}	140			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	170	195	215	ns max	$V_S = 10\text{ V}$, see Figure 30
Break-Before-Make Time Delay, t_D (ADG5213 Only)	40			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection, Q_{INJ}			20	ns min	$V_{S1} = V_{S2} = 10\text{ V}$, see Figure 29
	0.07			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 31
Off Isolation	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 25
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 27
-3 dB Bandwidth	435			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 28
Insertion Loss	-6.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 28
C_S (Off)	3			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	5			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	8			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	45			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	$GND = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

ADG5212/ADG5213

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	140			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$, see Figure 24
On-Resistance Match Between Channels, ΔR_{ON}	160 1.5	200	230	Ω max Ω typ	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$ $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	8 33 45	9	10 60	Ω max Ω typ Ω max	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 23
Drain Off Leakage, I_D (Off)	0.1 0.01	0.2	0.4	nA max nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 23
Channel On Leakage, I_D (On), I_S (On)	0.1 0.02 0.2	0.2	0.4 0.9	nA max nA typ nA max	$V_S = V_D = \pm 15\text{ V}$, see Figure 26
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	155 195	235	255	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 30
t_{OFF}	145 165	185	210	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 30
Break-Before-Make Time Delay, t_D (ADG5213 Only)	35		20	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection, Q_{INJ}	-0.5			ns min pC typ	$V_{S1} = V_{S2} = 10\text{ V}$, see Figure 29 $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 31
Off Isolation	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 25
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 27
-3 dB Bandwidth	460			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 28
Insertion Loss	-6			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 28
C_S (Off)	2.8			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	4.8			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	8			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
I_{DD}	50			$\mu\text{A typ}$	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ Digital inputs = 0 V or V_{DD}
I_{SS}	70		110	$\mu\text{A max}$	
	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}			1	$\mu\text{A max}$	
			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V max	
On Resistance, R_{ON}	350			$\Omega\text{ typ}$	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$, see Figure 24
On-Resistance Match Between Channels, ΔR_{ON}	500	610	700	$\Omega\text{ max}$	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
	4			$\Omega\text{ typ}$	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	20	21	22	$\Omega\text{ max}$	
	160			$\Omega\text{ typ}$	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$
	280	335	370	$\Omega\text{ max}$	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 23
Drain Off Leakage, I_D (Off)	0.1	0.2	0.4	nA max	
	0.01			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 23
Channel On Leakage, I_D (On), I_S (On)	0.1	0.2	0.4	nA max	
	0.02			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$, see Figure 26
	0.2	0.25	0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	235			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	290	360	410	ns max	$V_S = 8\text{ V}$, see Figure 30
t_{OFF}	165			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	205	235	260	ns max	$V_S = 8\text{ V}$, see Figure 30
Break-Before-Make Time Delay, t_D (ADG5213 Only)	85			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			50	ns min	$V_{S1} = V_{S2} = 8\text{ V}$, see Figure 29
Charge Injection, Q_{INU}	-0.5			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 31
Off Isolation	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 25
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 27
-3 dB Bandwidth	340			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 28

ADG5212/ADG5213

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Insertion Loss	-11			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 28
C_S (Off)	3.5			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)	5.5			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (On), C_S (On)	9			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	40		65	μA typ μA max	$V_{DD} = 13.2 \text{ V}$ Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{SS} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V max	
On Resistance, R_{ON}	150			Ω typ	$V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$, see Figure 24
	170	215	245	Ω max	$V_{DD} = 32.4 \text{ V}$, $V_{SS} = 0 \text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	1.6			Ω typ	$V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	35			Ω typ	$V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$
	50	60	65	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = 39.6 \text{ V}$, $V_{SS} = 0 \text{ V}$ $V_S = 1 \text{ V}/30 \text{ V}$, $V_D = 30 \text{ V}/1 \text{ V}$, see Figure 23
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	$V_S = 1 \text{ V}/30 \text{ V}$, $V_D = 30 \text{ V}/1 \text{ V}$, see Figure 23
	0.1	0.2	0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	0.02			nA typ	$V_S = V_D = 1 \text{ V}/30 \text{ V}$, see Figure 26
	0.2	0.25	0.9	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	190			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	230	255	265	ns max	$V_S = 18 \text{ V}$, see Figure 30
t_{OFF}	175			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	215	230	245	ns max	$V_S = 18 \text{ V}$, see Figure 30
Break-Before-Make Time Delay, t_D (ADG5213 Only)	45			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
			25	ns min	$V_{S1} = V_{S2} = 18 \text{ V}$, see Figure 29
Charge Injection, Q_{INJ}	-0.5			pC typ	$V_S = 18 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$, see Figure 31
Off Isolation	-105			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 25
Channel-to-Channel Crosstalk	-105			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, Figure 27

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
-3 dB Bandwidth	410			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, see Figure 28
Insertion Loss	-6.8			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 28
C_S (Off)	3			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)	5			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
C_D (On), C_S (On)	8			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = 39.6 \text{ V}$
I_{DD}	80		130	μA typ	Digital inputs = 0 V or V_{DD}
	100		9/40	μA max	
V_{DD}				V min/V max	GND = 0 V, $V_{SS} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx or Dx				
$V_{DD} = +15 \text{ V}$, $V_{SS} = -15 \text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	18	10	5	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	32	15	6	mA maximum
$V_{DD} = +20 \text{ V}$, $V_{SS} = -20 \text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	29	16	8	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	50	22	9	mA maximum
$V_{DD} = 12 \text{ V}$, $V_{SS} = 0 \text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	18	12	7	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	32	17	8	mA maximum
$V_{DD} = 36 \text{ V}$, $V_{SS} = 0 \text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	34	18	8	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	59	24	9	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V _{DD} to V _{SS}	48 V
V _{DD} to GND	−0.3 V to +48 V
V _{SS} to GND	+0.3 V to −48 V
Analog Inputs ¹	V _{SS} − 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs ¹	V _{SS} − 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pin	60 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx ²	Data + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Thermal Impedance, θ _{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSOP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes.
Limit current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

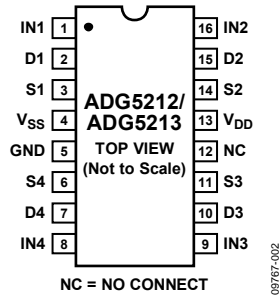
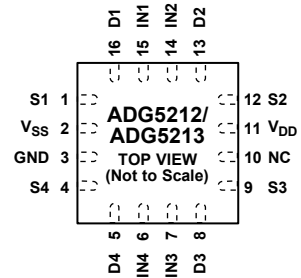


Figure 2. TSSOP Pin Configuration



NOTES
 1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .
 2. NC = NO CONNECT.

Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. This pin can be an input or an output.
3	1	S1	Source Terminal. This pin can be an input or an output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. This pin can be an input or an output.
7	5	D4	Drain Terminal. This pin can be an input or an output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin can be an input or an output.
11	9	S3	Source Terminal. This pin can be an input or an output.
12	10	NC	No Connect. These pins are open.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin can be an input or an output.
15	13	D2	Drain Terminal. This pin can be an input or an output.
16	14	IN2	Logic Control Input.
N/A ¹	EP	Exposed pad	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS} .

¹ N/A means not applicable.

Table 8. ADG5212 Truth Table

ADG5212 INx	Switch Condition
1	On
0	Off

Table 9. ADG5213 Truth Table

ADG5213 INx	S1, S4	S2, S3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

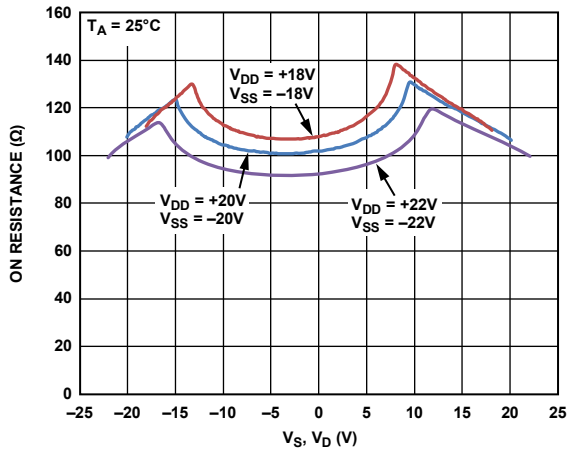


Figure 4. R_{ON} as a Function of V_S, V_D (Dual Supply)

09767-104

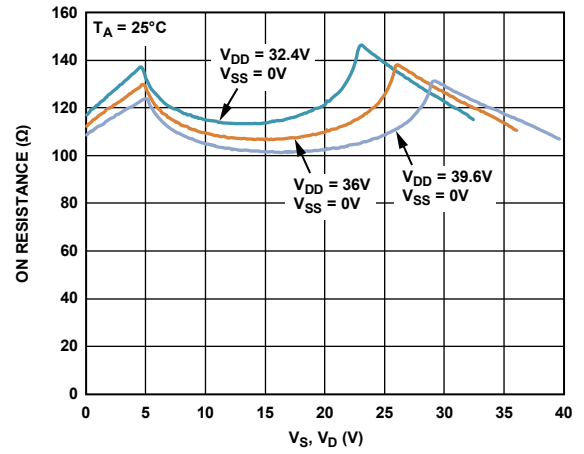


Figure 7. R_{ON} as a Function of V_S, V_D (Single Supply)

09767-107

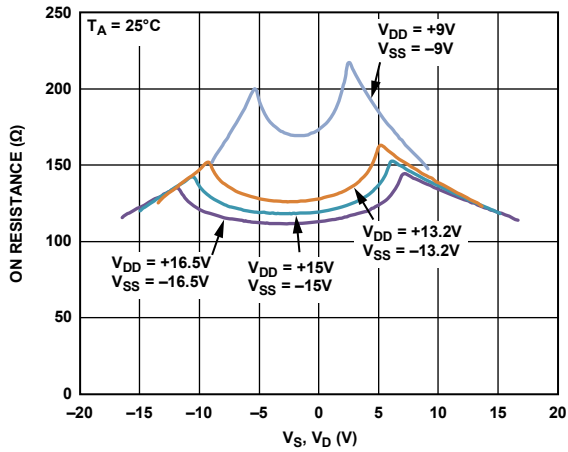


Figure 5. R_{ON} as a Function of V_S, V_D (Dual Supply)

09767-105

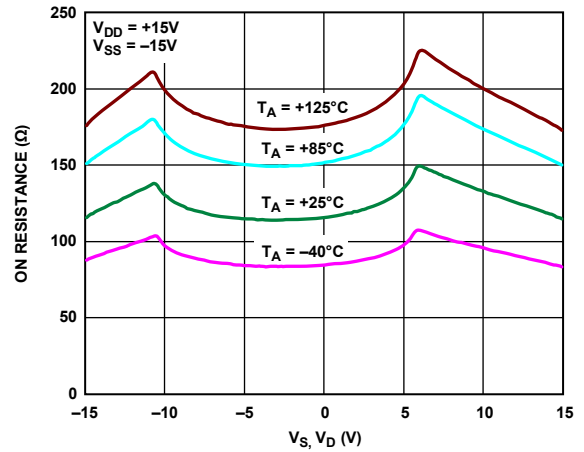


Figure 8. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 15 V Dual Supply

09767-108

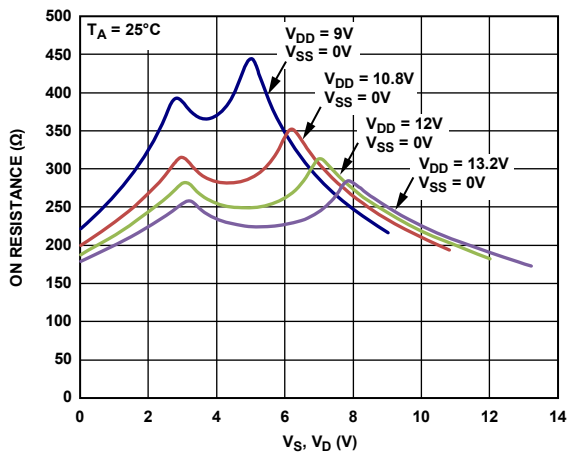


Figure 6. R_{ON} as a Function of V_S, V_D (Single Supply)

09767-106

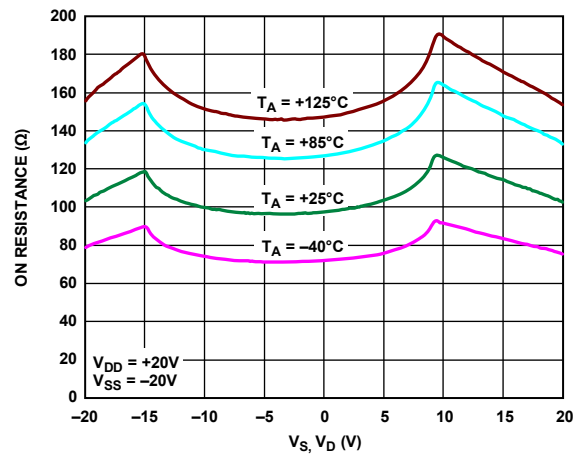


Figure 9. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 20 V Dual Supply

09767-109

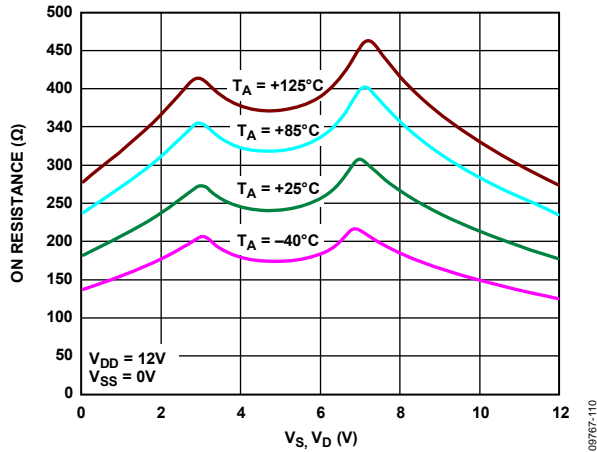


Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

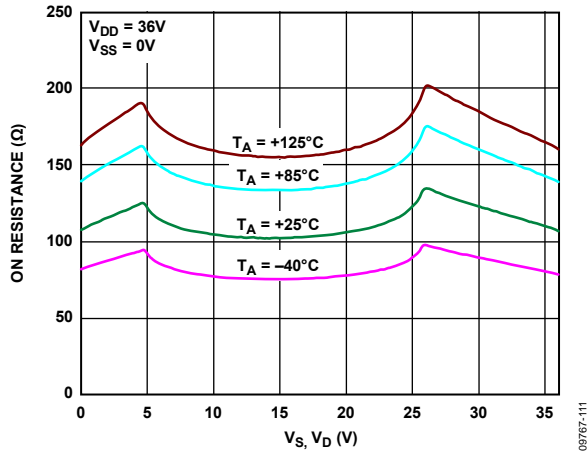


Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

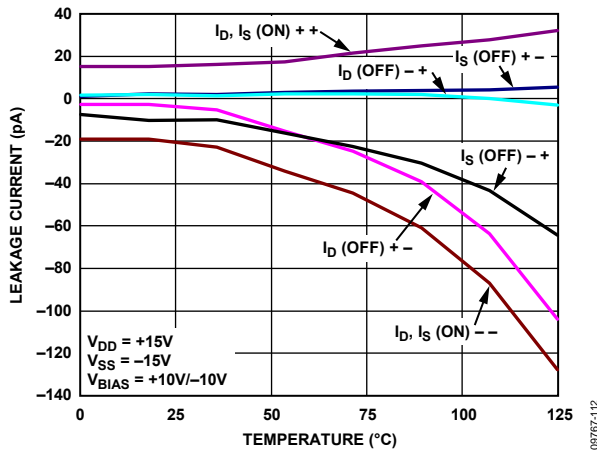


Figure 12. Leakage Currents vs. Temperature, ± 15 V Dual Supply

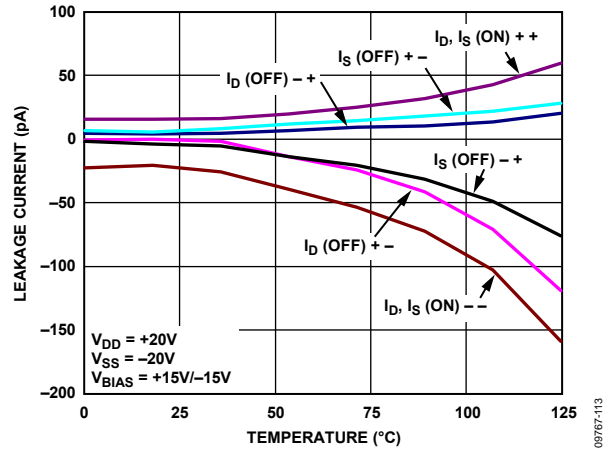


Figure 13. Leakage Currents vs. Temperature, ± 20 V Dual Supply

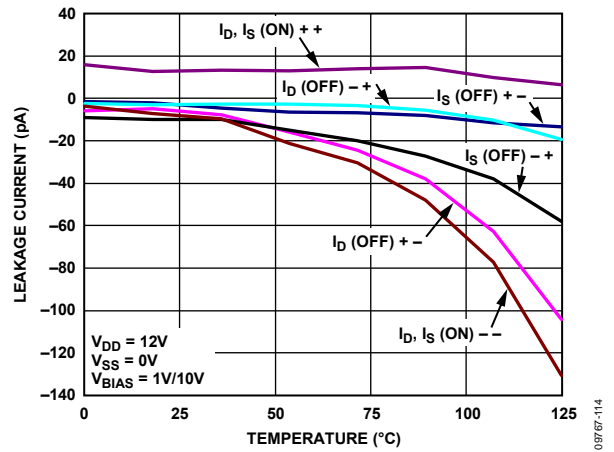


Figure 14. Leakage Currents vs. Temperature, 12 V Single Supply

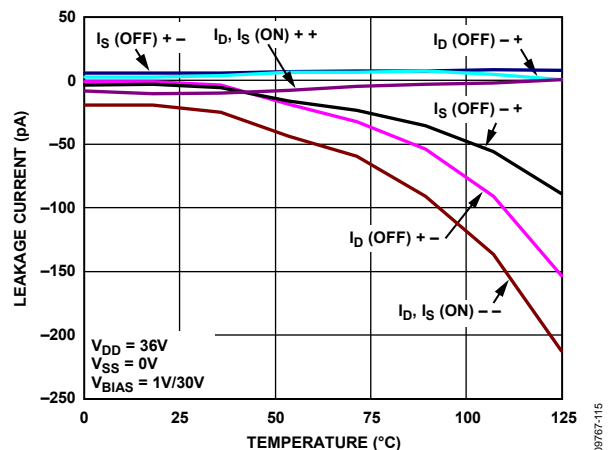


Figure 15. Leakage Currents vs. Temperature, 36 V Single Supply

ADG5212/ADG5213

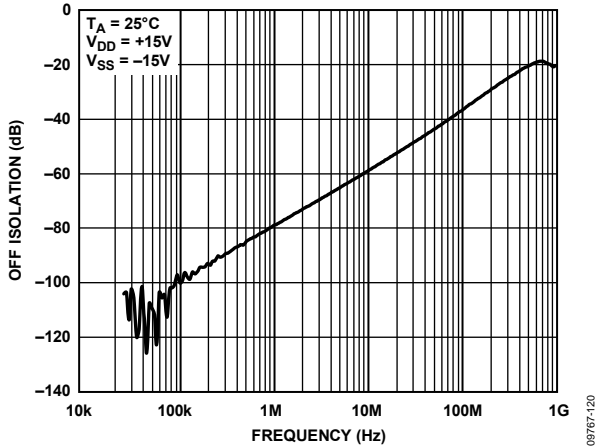


Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

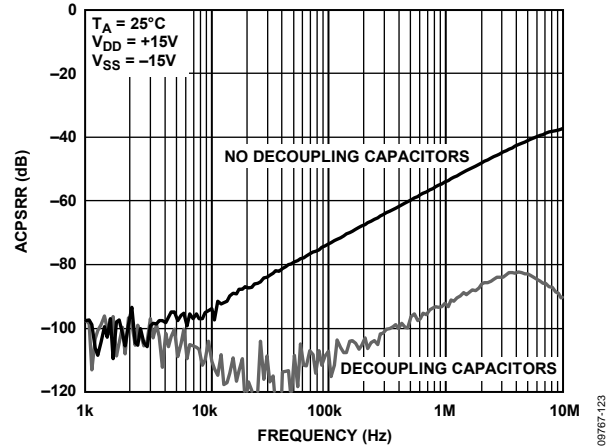


Figure 19. ACPSRR vs. Frequency, ±15 V Dual Supply

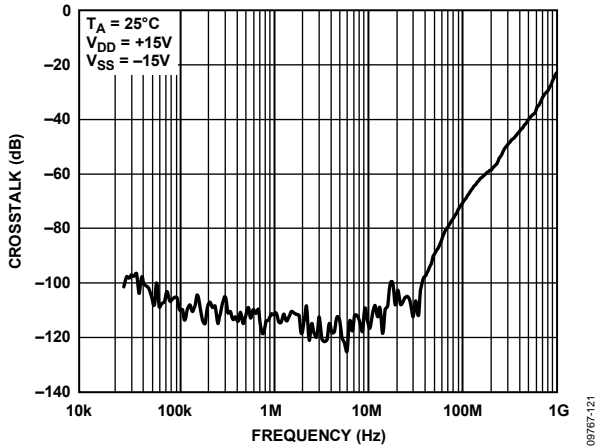


Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

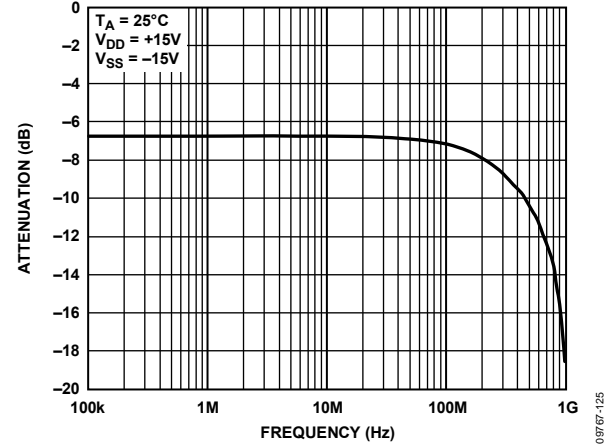


Figure 20. Bandwidth

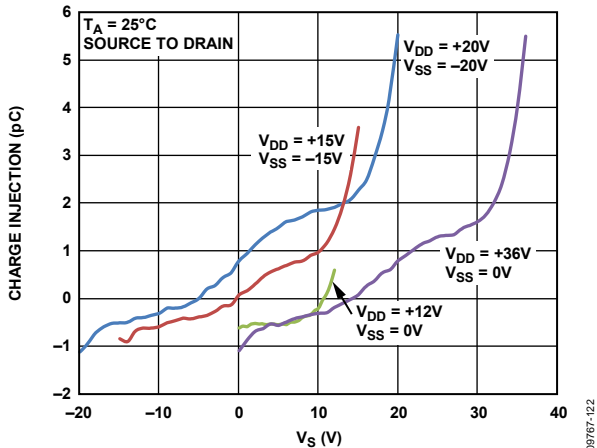


Figure 18. Charge Injection vs. Source Voltage

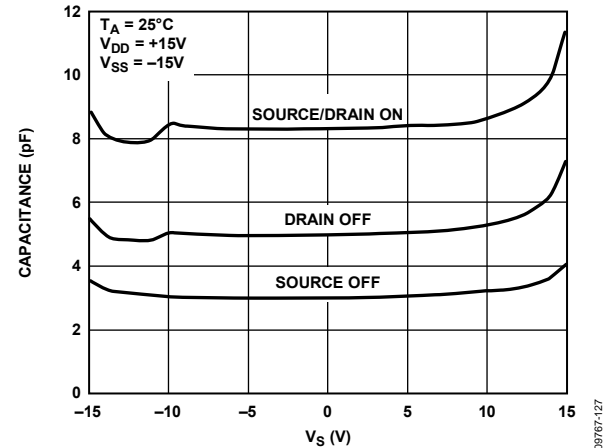


Figure 21. Capacitance

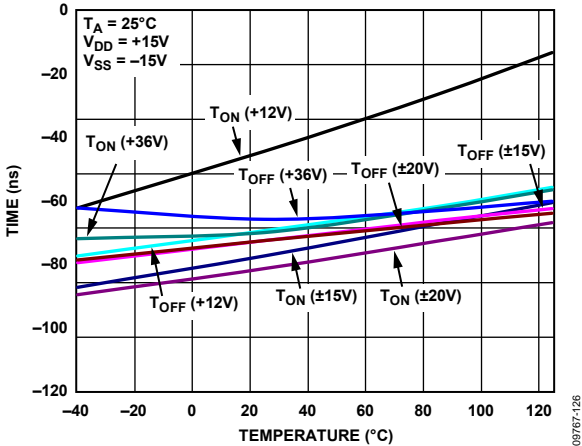


Figure 22. t_{ON} , t_{OFF} Times vs. Temperature

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TEST CIRCUITS

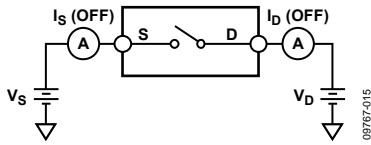


Figure 23. Off Leakage

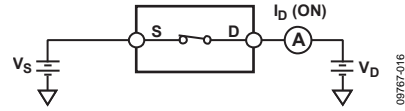


Figure 26. On Leakage

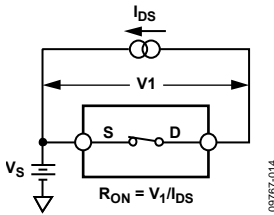


Figure 24. On Resistance

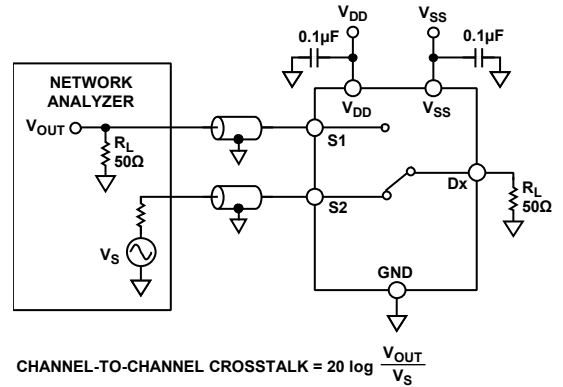


Figure 27. Channel-to-Channel Crosstalk

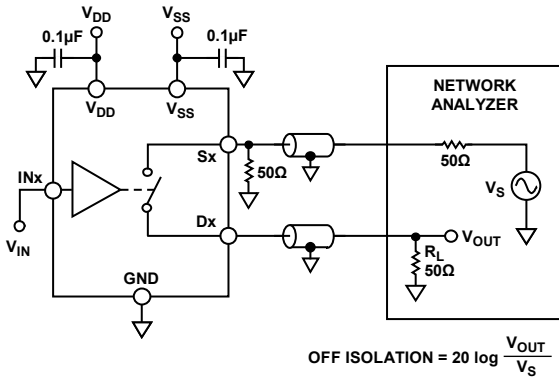


Figure 25. Off Isolation

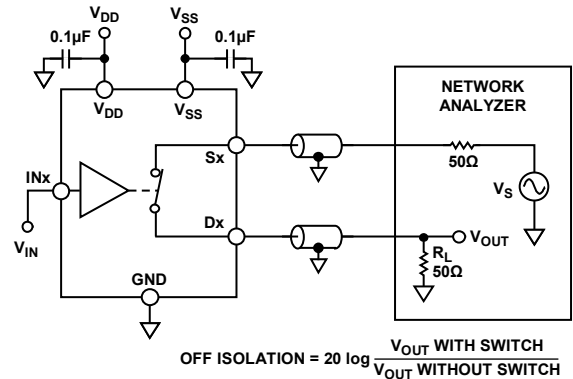


Figure 28. Bandwidth

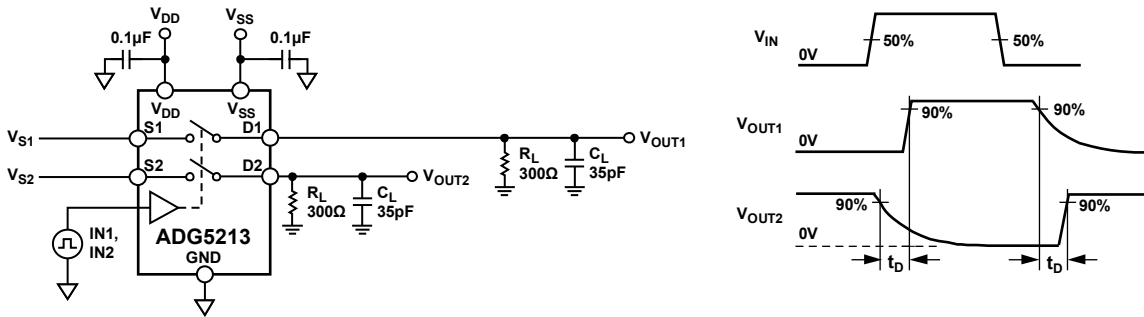


Figure 29. Break-Before-Make Time Delay, t_D

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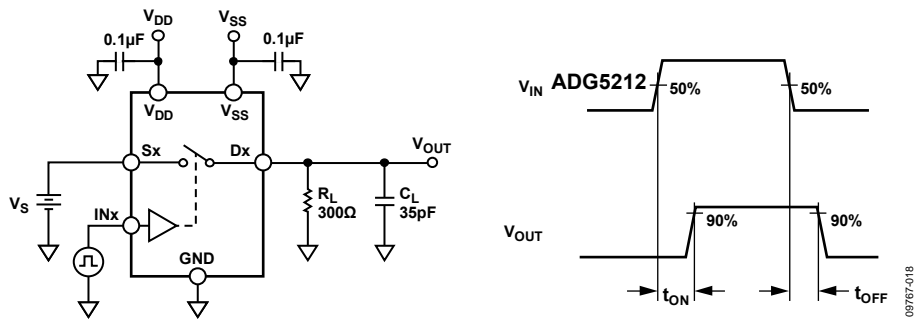


Figure 30. Switching Times

09767-018

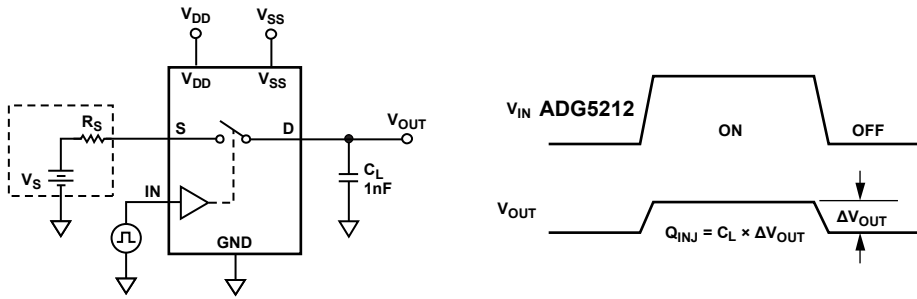


Figure 31. Charge Injection

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TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

R_{FLAT(ON)}

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by R_{FLAT(ON)}.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON}

t_{ON} represents the delay between applying the digital control input and the output switching on (see Figure 30).

t_{OFF}

t_{OFF} represents the delay between applying the digital control input and the output switching off (see Figure 30).

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

AC Power Supply Rejection Ratio (ACPSRR)

AC power supply rejection ratio (ACPSRR) is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the ADG5212 and ADG5213, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed and the result is a latch-up proof switch.

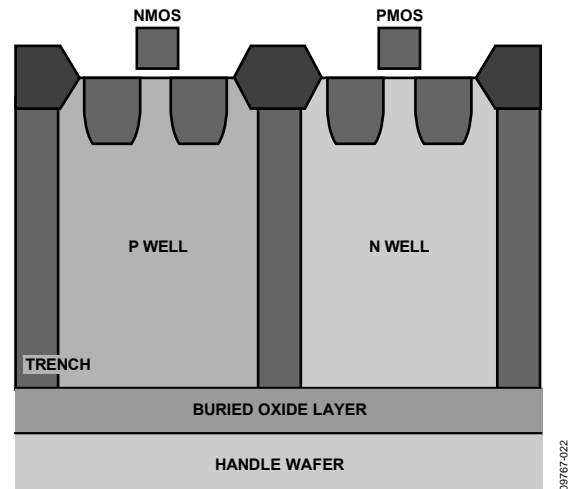


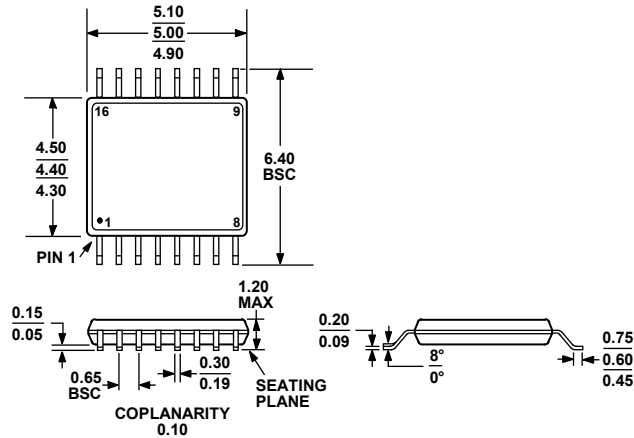
Figure 32. Trench Isolation

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APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provides a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5212/ADG5213 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ± 9 V to ± 22 V.

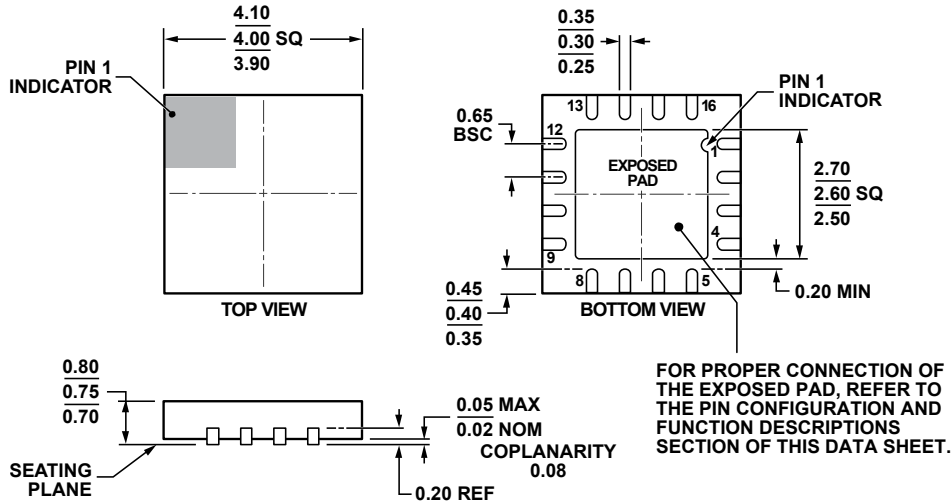
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ] 4 mm x 4 mm Body, Very Very Thin Quad (CP-16-17)

Dimensions shown in millimeters

08-16-2010-C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5212BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5212BRUZ-RL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5212BCPZ-RL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-17
ADG5213BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5213BRUZ-RL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5213BCPZ-RL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-17

¹ Z = RoHS Compliant Part.

NOTES