MTC-20172

Advanced 'S' Interface Circuit for ISDN

Data Sheet

Preliminary

Application Specific Standard Products

Features

- **Single Chip 4 wire S0-interface for ISDN**
- **Basic Access at 144 kbits/s with 2B+D**
- **Complying with CCITT I.430**
- **Applicable in all ISDN S0-interface Configurations:**
  - **NT: Network Termination**
  - **TE: Terminal Equipment**
  - **LTS: Line Termination Subscriber**
  - **LTT: Line Termination Trunk**
- **Switching of Test Loops**
- **S-bus Drivers with High Impedance in Power-off**
- **Balanced S-bus Receivers**
- **Line Length up to 2 km in Point to Point**
- **Handles V*, IOM1 (1), IOM2 (2) and GCI Digital Interfaces**
- **Supports Multiframing**
- **Includes a Maintenance M-channel**
- **Absorption of Clock Wander in LTT Mode**
- **Operating Power < 50 mW Stand-by Power < 3 mW**

Description

"The MTC-20172" is an enchanced version of the MTC-2072 SIC.
In addition to the basic line interface functions, the MTC-20172 offers digital interfaces compatible with most commonly used standards (V*, IOMI (1), IOM2 (2), GCI), as well as extended monitor channel functions and multi-framing.
The use of leading edge process technologies and restructuring of the analog functions results in greatly enhanced analog performance."

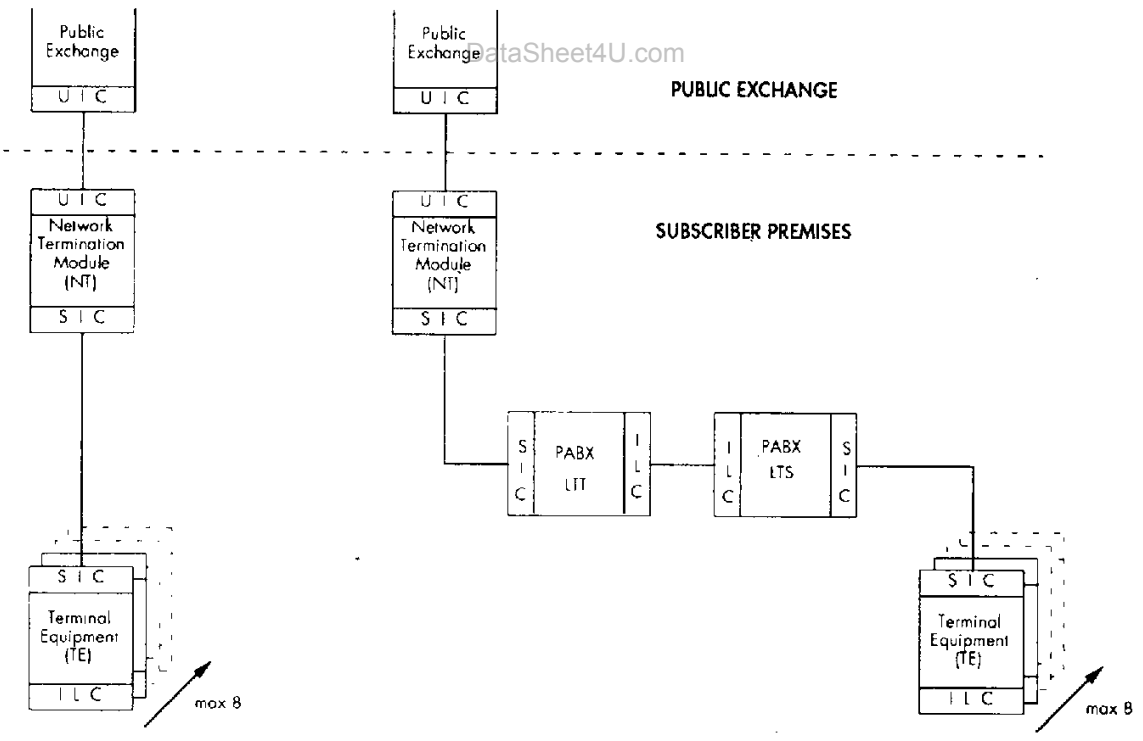

Fig.1: General ISDN Structure

The 22 pin DIL MTC-20172 is pin-to-pin compatible with the SBC 2080, and is a functional super-set of this device.
The S0-interface circuit (SIC) enables full duplex digital data transmission (2B+1D) over the S0-interface.
The SIC can be used as a 'Network Termination' (NT), providing transparent data transmission from the digital interface to the S0-interface and vice versa.
As a 'terminal equipment' device (TE), the SIC is connected to a "layer 2" device (e.g. ISDN Link Controller; MTC-2074 ILC).
To connect an ISDN PABX unit to the public network a SIC can be used as a 'Line Termination Trunk side'-device (LTT).
Furthermore, a 'Line Termination Subscriber side' (LTS) mode is available (fig. 1), which is similar to NT, but offers less complicated activate/deactivate procedures.
A digital serial interface provides a link between SIC, U-Interface, ILC and other communication devices. The digital serial interface supports V*, IOM1 (1), IOM2 (2) and GCI.
The SIC contains all necessary functions for direct connection to the S0-interface, especially transmitter and receiver stages.

The Digital Interface

Each ISDN configuration (NT, TE, LTS, LTT) is supported in either V*/IOM1 (1) or in IOM2 (2)/GCI.
The serial interface is made up of frames of 125 µs. Each frame can have from 32 to 512 bit positions and is divided into channels of 32 bits.
Each bit takes 2 cycles of the dataclock DCLK (With a frequency from 512 kHz to 8192 kHz). The start of a 125 µs frame is synchronized with a DFR signal of 8 kHz.
In TE modes the SIC is master of the digital interface, in NT, LTS and LTT the SIC is slave.

Depending on the strapped mode several frame formats are possible:

Normal Mode (fig. 2)
DCLK can go from 512 kHz to 8192 kHz with intervals of 16 kHz (32 to 512 bits/frame).
The rising edge of DFR marks the start of the frame and should be high for at least 2 DCLK periods.

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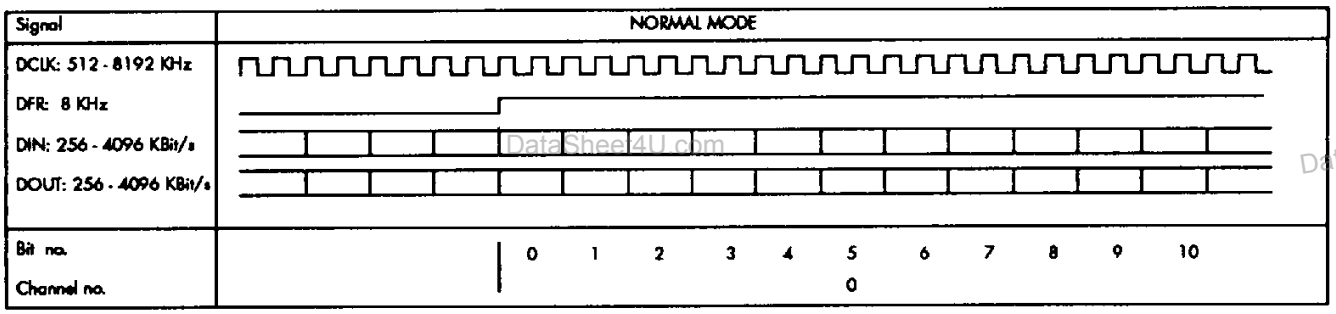


Fig.2: Timing in Normal Mode

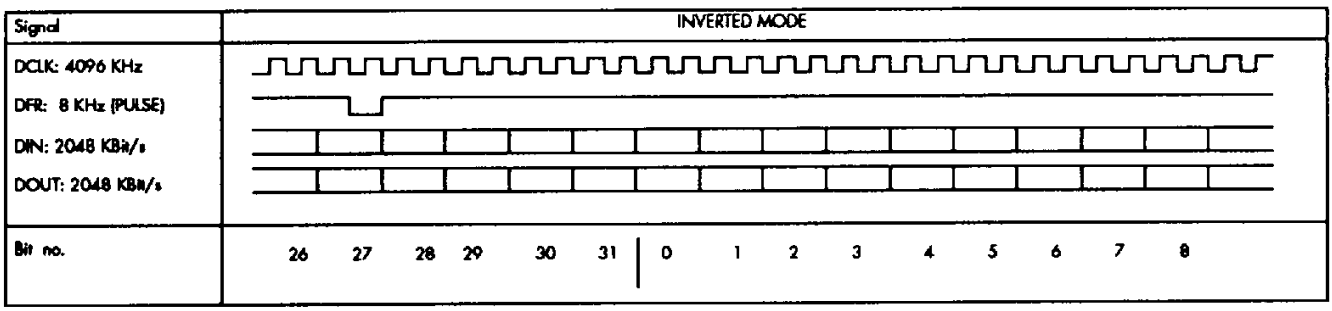


Fig.3: Timing in V* Inverted Mode

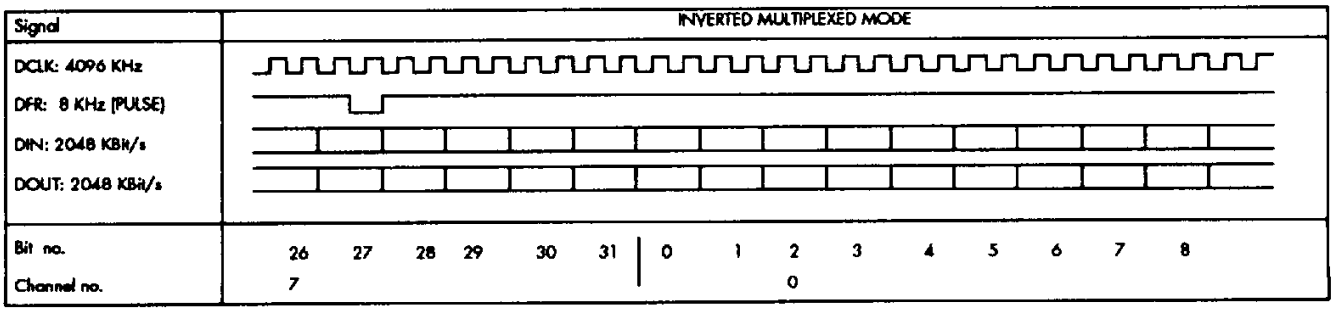


Fig.4: Timing in V* Inverted Multiplexed Mode

Depending on the DCLK frequency a maximum of 8 channels are available. The bits of higher channels are unused.
This mode is applicable in all configurations.

V* Inverted Mode (fig. 3)
Inverted frame and dataclock.
DCLK = 512 kHz (32 bits/frame)
DFR goes low for 1 clock cycle at the end of position 27.
Only 1 channel is available.
This mode is applicable in TE mode.

V* Inverted Multiplexed Mode (fig. 4)
Inverted frame and dataclock.
DCLK = 4096 kHz (256 bits/frame)
DFR goes low for 1 clock cycle at the end of position 251.
8 channels are available.
This mode is applicable in LTT and LTS mode.

Remark: In LTS and LTT there is an automatic recognition between inverted multiplexed and normal modes.

A channel of 32 bits is divided in 4 bytes (fig. 5):
1st byte B1:
First transparent data channel of 64 kBits/s.
2nd byte B2:
Second transparent data channel of 64 kBits/s.
3rd byte B2*:
Monitor channel with in TE and LTT the D-channel status in the 5th position.
4th byte B1*:
D1, D2: Two transparent D-channel bits at 16 kBits/s.
C/I: Four Command/Indication channel bits. Used for activation or deactivation and test modes. The interpretation of the received command codes and the transmitted Indications follow the V*/IOM1 (1) or the IOM2 (2)/GCI C/I code tables.
MR, MX: Two handshaking bits to control the monitor channel access.

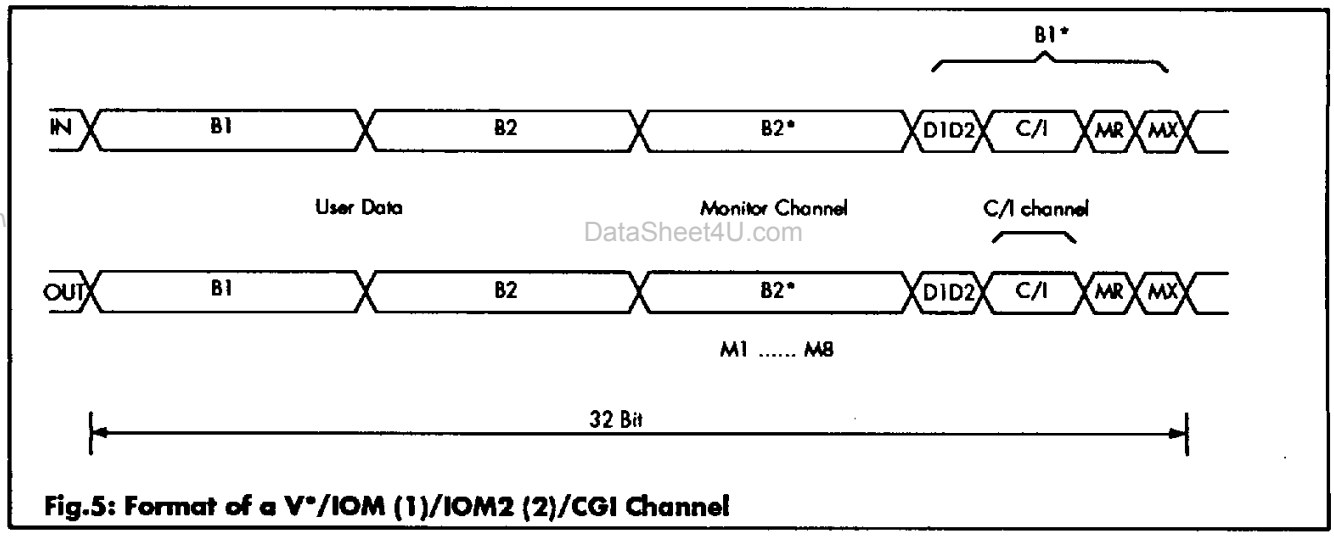


Fig.5: Format of a V*/IOM (1)/IOM2 (2)/CGI Channel

The possible combinations of ISDN configurations, frame format and activation/deactivation procedures are presented in table 1.

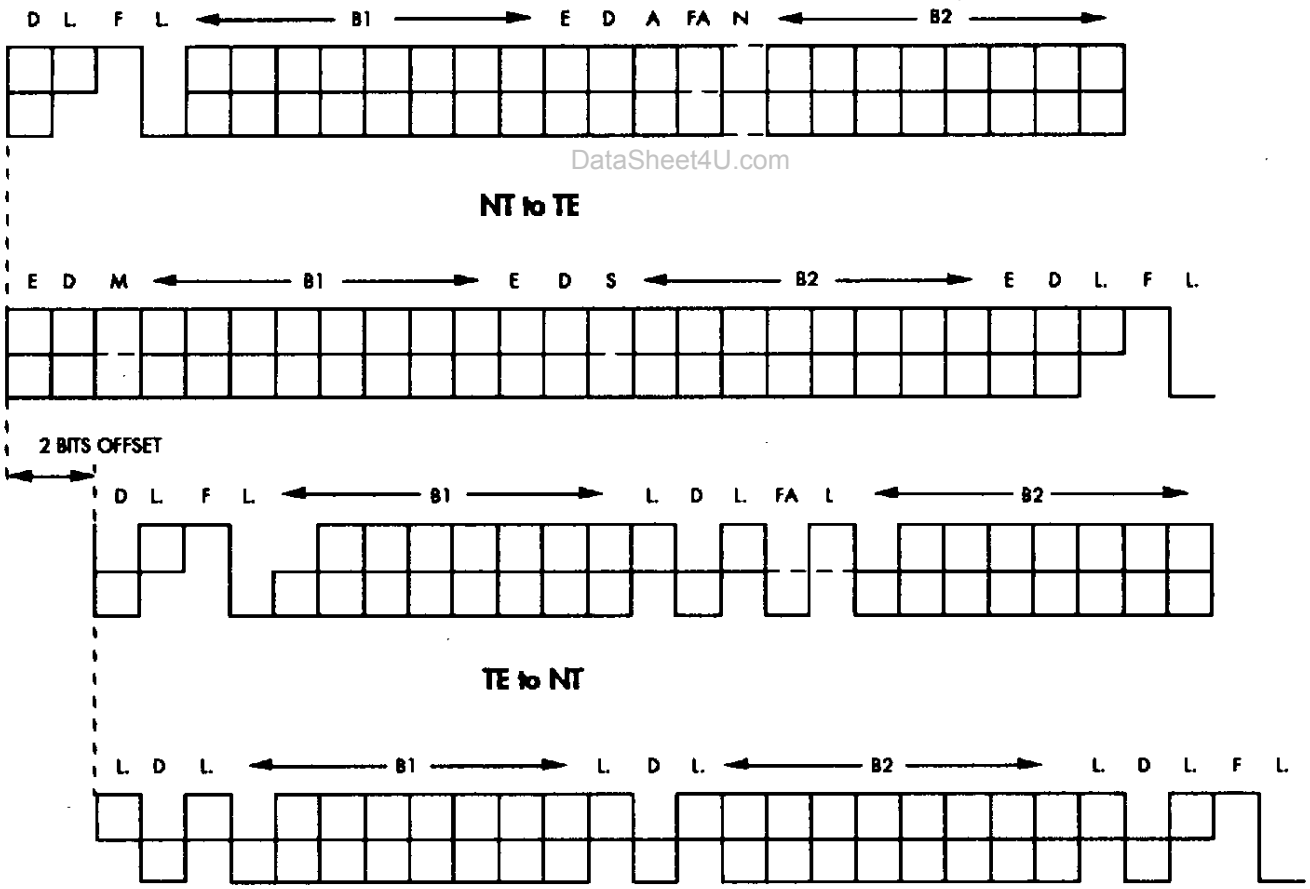
Table 1: Possible Mode Combinations

ISDN configuration	Frame format	DCLK frequency (kHz)	Available channel	Activation/ Deactivation according to
TE(*)	Inverted	512	1	V*/IOM1 (1)
TE(*)	Normal	512	1	V*/IOM1 (1)
LTS/LTT(*)	Inverted multiplexed	4096	1-8	V*/IOM1 (1)
LTS/LTT	Normal	512-8192	1-8	V*/IOM1 (1)
LTS/LTT(*)	Normal	512-8192	1	V*/IOM1 (1)
NT(*)	Normal	512-8192	1	V*/IOM1 (1)
TE	Normal	1536	1	IOM2 (2)/GCI
LTS/LTT	Normal	512-8192	1-8	IOM2 (2)/GCI
NT	Normal	512-8192	1	IOM2 (2)/GCI

(*) Compatible with the SIC-MTC-2072.

The S0-interface

For transmission of data over the subscriber premises the SIC is provided with an S0-interface. This interface enables full duplex transmission of data (2B + 1 D-channel) over 4 wires at a nominal data rate of 192 kBits/s. An Alternating Mark Invert (AMI) code is used for the line transmission via the S0-interface. The transmission of data over the S0-interface consists of frames of 250 µs. Each frame is 48 bits wide and contains 4 data bytes (2B1, 2B2) and 4 D-bits.
The frame structures are shown in fig.6. A frame start is marked using a first code violation (no mark inversion). To allow secure synchronization of the receiver a second code violation is generated before the 14th bit of the frame. To guarantee this second violation an auxiliary framing bit pair FA and N (from NT to TE) or the framing bit FA with associated balance bit (from TE to NT) are introduced.
The first bit of the transmitted frame from TE to NT shall be delayed for 2 bit periods with respect to the frame received from the NT. Furthermore an echo bit (E-bit) for the D-channel and an activation bit (A-bit) are provided, DC-balancing is done by L-bits.
The SIC supports multi-framing according to the CCITT I.430 recommendation, the capability of transmitting an S-channel from NT to TE and a Q-channel from TE to NT of 800 baud is provided. The S and Q data can be accessed via the monitor channel.



F : FRAMING BIT
L : DC BALANCING BIT
D : D-CHANNEL BIT
E : D-CHANNEL ECHO-BIT
FA : AUXILIARY FRAMING BIT

N : = $\overline{FA}$
B1 : BIT OF CHANNEL B1
B2 : BIT OF CHANNEL B2
A : ACTIVATION BIT
S : S-BIT
M : MULTIFRAMING BIT

Fig.6: S0-Frame Format

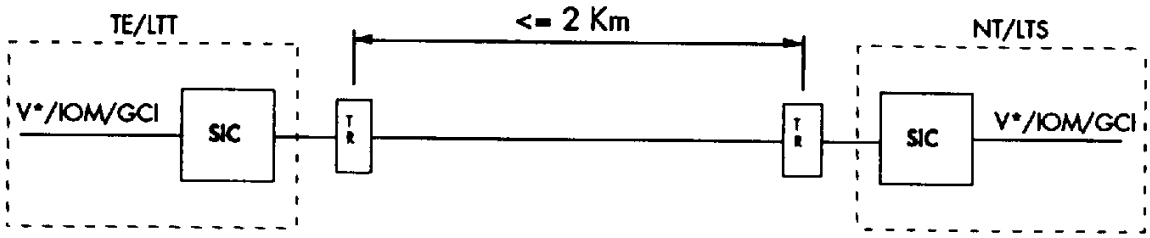


Fig.7: Point to Point Configuration

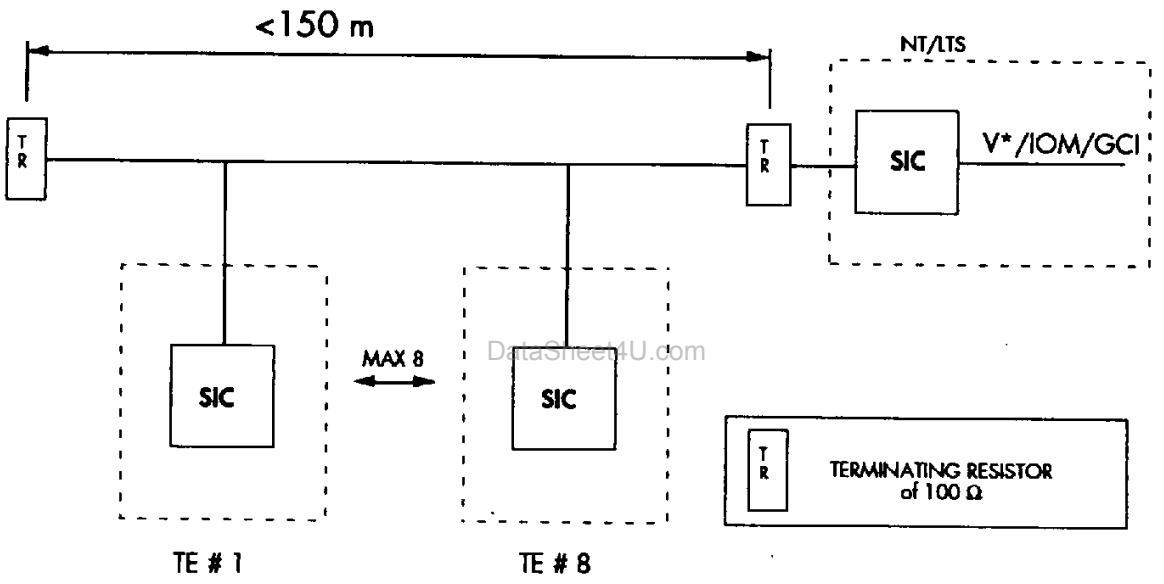


Fig.8: Point to Multipoint Configuration

The SIC can be used in a point to point and in a point to multipoint configuration (including extended passive bus). In the first configuration the length of the cable is limited to 2 km (see fig.7). In bus configuration (point to multipoint) up to 8 terminals may be connected to the S0-interface (fig.8) where the terminals must be connected in a range of 150 m. For the extended passive bus the terminals must be clustered within a 25m range with a cable length of maximum 1.5 km.
To avoid bus mismatching when multiple TEs are connected the driver stages are high impedant when they are unpowered.

Controlled access to the shared data channels is realized within the SIC by a D-channel access procedure. Each terminal can be given a certain priority for D access. Via the echo bit which is the reflection of the received D channel at the NT it is possible for the terminal to detect the status of the D-channel. In order to try to gain access over the D-channel a terminal has to see 8 to 11 consecutive ones in the echo-channel. The exact number depends on the priority given to the terminal. When several terminals try to gain access at the same time collisions occur on the S-bus. The terminal that transmitted the "one" does detect the collision in the echo channel and loses the D-channel access. The terminal that transmitted the "zero" gains the access. When a successful D-channel message is transmitted the priority is decreased by 1 in order to guarantee fairness with the other terminals. The status of the D-channel of the TE/LTT is available at a pin or at the 5th position of the monitor byte. This enables the control of the D-channel by an external HDLC controller.
At the NT/LTS side the echo bits of several NTs can be combined in an external common echo bus (wired AND) in an NT-star configuration. At the LTS side the same external common echo bus can be used to share an external HDLC controller between several LTS SICs.

SIC Operation

The block diagram is shown in fig.9. The data of the S0-interface is received by the SIC receiver which has a balanced input, an AGC stage, a filter and comparators with dynamically adapted thresholds. The timing of the received S0-frame can either be a fixed (Only NT/LTS) or adaptive timing.
In the first case the timing is locked to the transmitted frame and the tolerable phase delay on the received S0-frame is limited.
In adaptive timing mode, delays up to 48 µs can be tolerated. The start of the received frame is detected in the FL-detection unit. An adaptive algorithm is used for compensation of the slope of the FL transition. A digital PLL recovers the received bit clock (192 kHz). A second digital PLL generates the transmit bit clock (192 kHz) which is locked to the IOM (3) frame in case of NT/LTS or is locked to the received S0-frame in case of TE/LTT. It is possible to compensate external circuits (e.g. filters) by adjusting the internal phase of the bit clocks by means of a pin or a register accessible by the monitor channel. These circuits work with a 7680 kHz ±100 ppm clock. This clock can be delivered to the SIC by an external generator, a UIC for NT modes or can be generated by an on-chip oscillator.
The serial B and D data from the V*/IOM (3)/GCI digital interface is stored into a buffer with a dynamic pointer structure and presented at the s_transmitter where the S0-frame formatting is done.
In the other direction the s_receiver unit deassembles the received S0-frame. The B and D data are stored in the buffer and multiplexed together with M, C/I, MX and MR into a digital V*/IOM (3)/GCI frame.
The pointer structure of the buffer guarantees a minimum round-trip delay in NT, LTS and TE modes and is able to compensate the clock wander in LTT mode. If the clock wander becomes too big a warning is given in the C/I channel, the internal pointers are reinitialized.
Activation/deactivation procedures are handled in the status controller.
Two basic modes are available: A V*/IOM1 (1) mode, compatible with the SIC-MTC-2072 and an IOM2 (2)/GCI compatible mode.
The S/Q control module handles the multiframing on the S and the Q channel of the S0-interface.
Multiframing is enabled in NT/LTS by a width modulation of the frame synchronization signal DFR every 40th IOM (3)/GCI frame, a monitor programmable register or an auxiliary pin.
The M control unit interprets and responds to messages on the monitor channel. Via this channel access is possible to the S/Q bits and configuration registers. Observation of some inputs is also possible.
In order to reduce the power consumption of the components connected to the subscriber line, the SIC

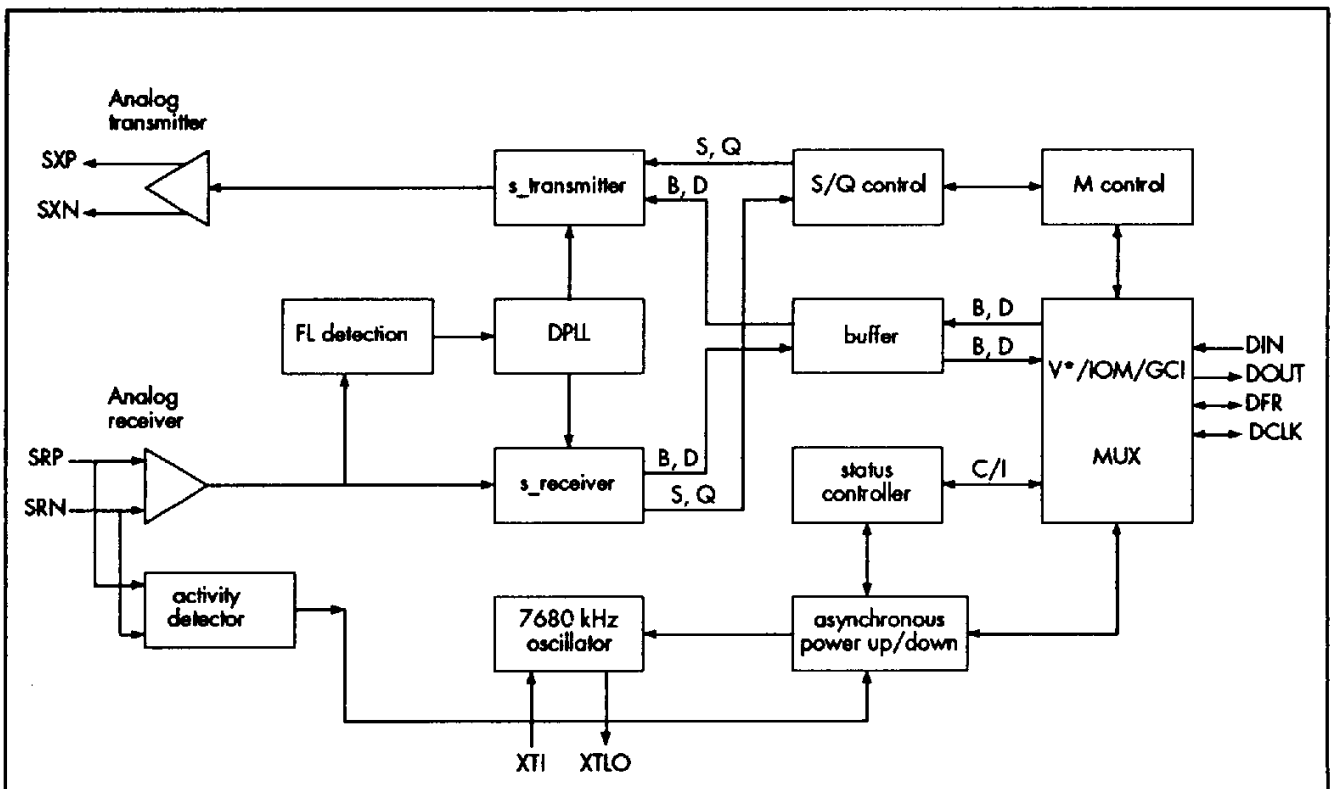


Fig.9: Block Diagram

may be switched to a power down mode during idle periods. In NT and TE modes the internal clock distribution and the oscillator are turned off and the power consumption is less than 3 mW. The component is powered up again during the line activation procedure. The power consumption when activated, with an applied DCLK clock of 512 kHz is less than 50 mW (excluding the power of the S0-bus).

Test Modes

Two test loops may be closed in the SIC, which depend on the selected mode of operation. In both modes all three channels (B1, B2 and D) are looped back as close as possible to the S0-interface.
Loop 2 (NT, LTS) is a transparent loop (fig.10a) where the transmitted S0-frame is also switched on the S-bus. Activation from the S0-interface is not possible.
Loop 3 (TE, LTT) is a non transparent loop (fig.10b) where the transmitted S0-frame is not switched on the S-bus in order not to activate the NT/LTS. Activation from the S-bus is possible and is indicated by a special code in the C/I channel.
Both loops are initiated over the C/I-channel and under control of a layer 2 component.
For further testing of the subscriber line two test signals can be transmitted over the S0-interface, a 96 kHz test sequence sending continuous AMI marks and a 2 kHz test sequence sending single AMI marks. Both test modes are under control of the C/I channel and in NT mode by a pin.

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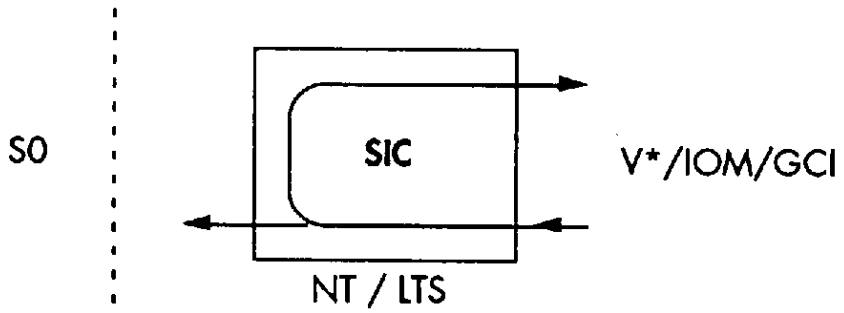
(1) IOM1 is a trademark of Siemens AG
(2) IOM2 is a trademark of Siemens AG
(3) IOM is a trademark of Siemens AG

a) LOOP2



b) LOOP3

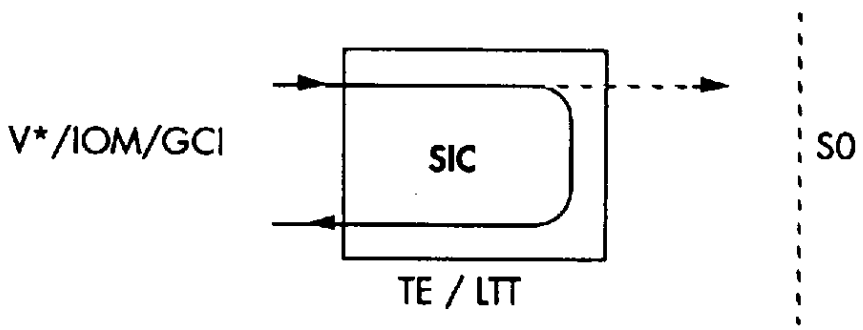


Fig.10: Test Loops

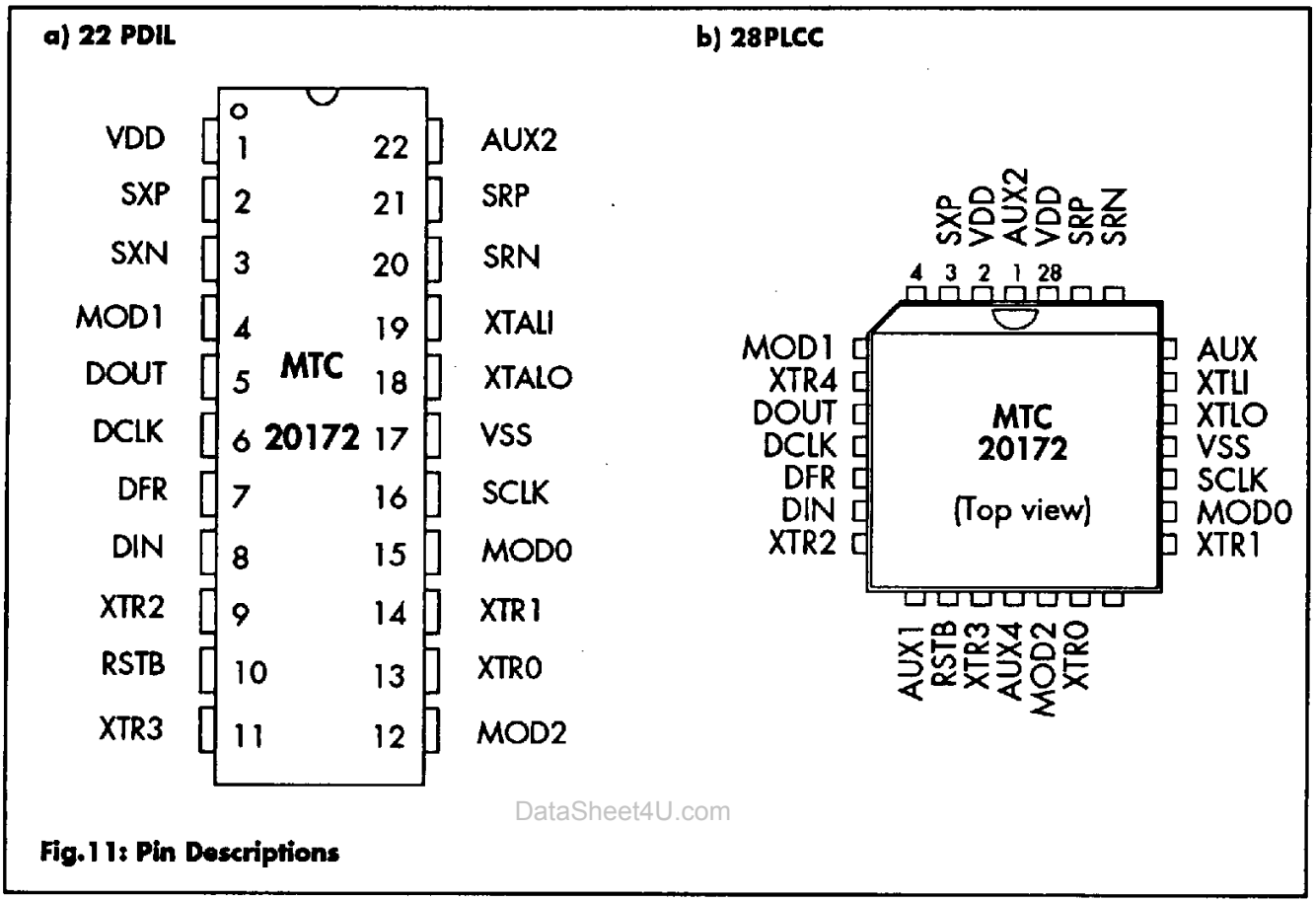


Fig.11: Pin Descriptions

Package

The SIC will be delivered in a 400 mil 22 DIL package and in a rectangular 28 PLCC package. The pin-outs are given in fig.11a and fig.11b. The 22 DIL pin-out is compatible with the SIC-MTC-2072.

For more detailed information, please contact your Alcatel Mietec representative for the MTC-20172 (SIC) Reference Manual.