Intrduction to STD80/STDM80 1

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LIBRARY DESCRIPTION

STD80 and STDM80 are 5V and 3.3V 0.5μm CMOS standard cell libraries supporting triple- and double-layer metal interconnections provided by Samsung Electronics.

Every types of internal macrocells and input/output buffers are contained in these cell libraries.

With the regard to the current increase of power mixture, 5V-to-3.3V and 3.3V-to-5V convertible cells having a level shifter inside are included in these libraries. In addition, the other interface (CMOS, TTL and Schmitt trigger) cells are fully equipped for your wide selection.

Various kinds of macrofunctions, megafunctions, memory and datapath compilers may satisfy the complicated design requirements. Moreover, core & megafunction cells such as MPU and DSP, and analog cells are under development.

We ensure the product reliability by preventing any possible noise, ESD and latch-up efficiently.

Every work operation in a design flow has been systematized and automated, and each stage is designed to go through enough reviews and verifications. It makes the design work easier and faster, and also prevents any errors or mistakes possible through a design flow.

FEATURES

- ❑ STD80: 5volt standard cell library
  STDM80: 3.3volt standard cell library
- ❑ Mixed 5V/3.3V I/O interface
- ❑ 0.5μm 5V HCMOS technology
  – Double and Triple layer metal options
- ❑ High basic cell usages
  – Up to 700,000 total number of gates
  – Maximum usage: 70% for triple layer metal
  – Maximum usage: 40% for double layer metal
- ❑ High speed
  – 0.2 ns (for STD80) and 0.3ns (for STDM80) delay of 2-input NAND with fanout = 2
- ❑ Fully configurable RAM, ROM and DPRAM
  – Up to 512K-bit ROM available
  – Up to 128K-bit RAM available
  – Up to 64K-bit DPRAM available
- ❑ Configurable Datapath elements available
  – 4 ~ 128-bit bus width
- ❑ Operating Temperature (T_A)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- ❑ ESD and latch-up protection
  – ESD: 2000V (Min.)
  – Latch-up: 300mA (Min.)
- ❑ Selectable output current drive capability
  – 1/2/4/8/12/16/20/24mA available for 5V
  – 1/2/4/6/8/10/12/16mA available for 3.3V
- ❑ TTL, CMOS, LVTTL, LVCMOS and Schmitt trigger I/Os
- ❑ X-tal oscillators
- ❑ PCI, PCMCIA buffers
- ❑ GTL, NTL, CardBus, SCSI, PECL, USB under-developed
- ❑ Various package options
- ❑ Fully integrated CAD software support
  – Verilog, Viewlogic, Mentor and Synopsys

CAE SUPPORT

STD80/STDM80 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor and Synopsys for front-end logic design capture and simulation, and ArcCell for back-end placement and routing.

For a high simulation accuracy, STD80/STDM80 uses a proprietary delay calculator. Cell delay calculations are based on a matrix of delay parameters for each macrocell, and signal interconnection delay is based on the RC tree analysis.

PRODUCT FAMILY

STD80/STDM80 library include the following design elements:

(a) Internal Macrocells
(b) Input/Output Cells
(c) Macrofunctions
(d) Megafunctions
(e) Memory Compilers
(f) Datapath Compilers
(g) JTAG Boundary Scans.

< Internal Macrocells >

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 300 different types of internal macrocells. They usually come in two levels of drive strength (1X and 2X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

< Macrofunctions >

Macrofunctions are netlists of logic function which have the complexity of a standard MSI circuit. Macrofunctions are logic building blocks. There are 44 kinds of 74XX (TTL) compatible functions in this library.

< Megafunctions >

Megafunctions are also netlists of logic function, but with a high logic complexity of a standard LSI circuit. Multipliers, barrel shifters, 82XX Intel functions, etc. are supported in this library.

< Memory Compilers>

Memory compilers of STDL80 consist of two ROMs (synchronous contact programmable and synchronous diffusion programmable), three single-port RAMs (synchronous and asynchronous) and three dual-port RAMs (synchronous and asynchronous).

In addition, a Register File and a FIFO are under-developed.

< Datapath Compilers >

Datapath compilers of STD80/STDM80 consist of 16 macro cells (Adder, ALU, Multiplier, etc.) and 14 primitive cells (NAND, NOR, DFF, LATCH, MUX, etc.)

< Input/Output Cells >

There are about one thousand different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 24mA for 5V drive and 1mA to 16mA for 3.3V drive.Two levels of slew rate controls are provided for each buffer type (except 1mA and 2mA buffers) to reduce output power/ground bus noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STD80/STDM80 library provides with three options of pull-down and pull-up resistances respectively. They are 50KΩ, 100KΩ, and 200KΩ (The default value is 100KΩ).

I/O Cell Drive Options

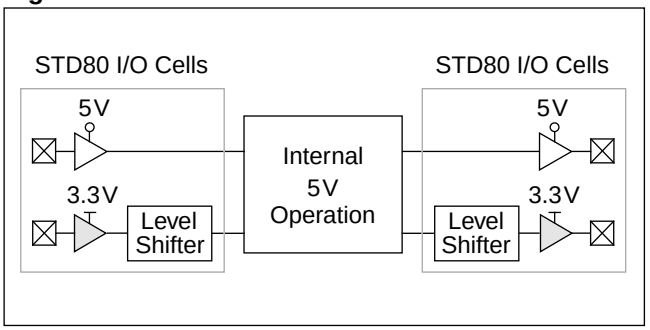
To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA, ..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. STD80/STDM80 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

5V/3.3V Mixed I/O Cells

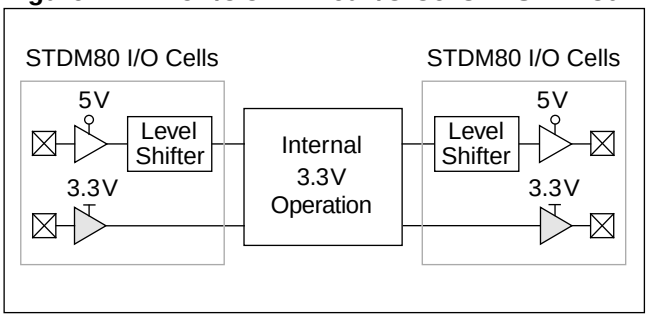
When designers intend to make transitions from 5V supplies to low voltage system, STD80 offers a solution of interfacing problems encountered in mixed 5V/3V environment. This solution provides great flexibility to different devices communicating each other. PCI and PCMCIA buffers are also available in this solution. You can see this in the following figure.

Figure 1-1. 5V/3.3V Mixed I/O Cells in STD80



In STDM80, level shifters are available to provide internal 3V core with great flexibility when it interfaces with a 5V device. Refer to the figure below.

Figure 1-2. 5V/3.3V Mixed I/O Cells in STDM80



PCI Buffers

In addition to input, output, bi-directional, slew rate controlled and Schmitt trigger I/O buffers, SEC ASIC now offers PCI (Peripheral Component Interconnect) I/O buffers. PCI is expected to be better suited to the more complex and feature-rich design than the existing local bus standards. 5V, 3.3V and Universal PCI buffers are included in the library.

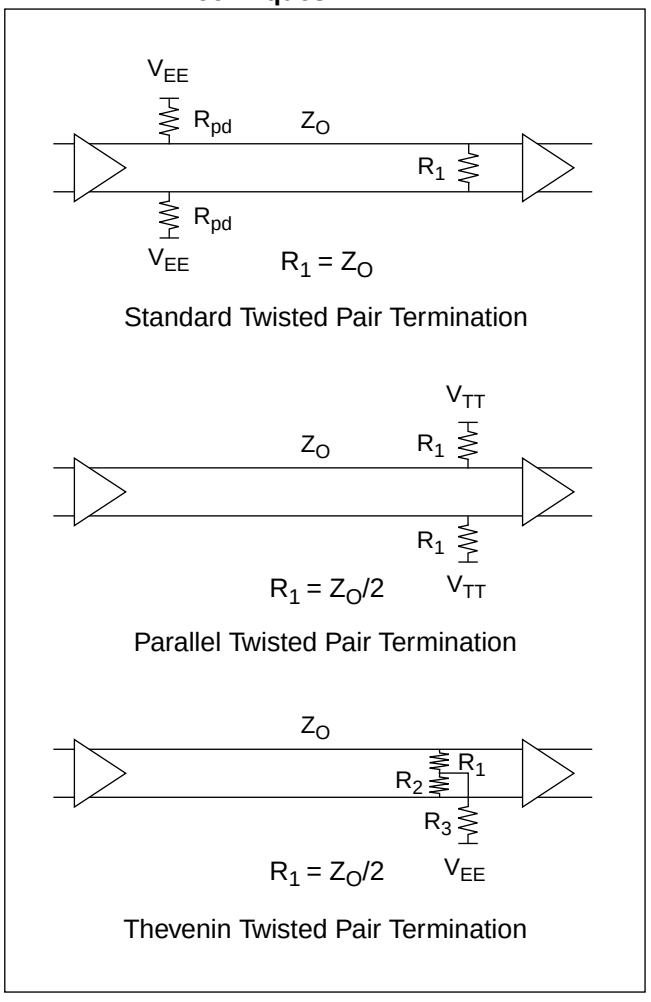
PECL

SEC ASIC's PECL (Positive Emitter Coupled Logic) buffer having 155MHz operating frequency is suited to ATM interface. It supports two voltage source modes; 5V and 3.3V.

The voltage swing level is about 0.8V, being similar to that of ECL, and the external terminator is needed. Its main features are the same as ECL; low noise, high speed and single ended/differential function.

In case of differential transmission, the external terminator is shown in the following figure.

Figure 1-3. Twisted Pair Termination Techniques

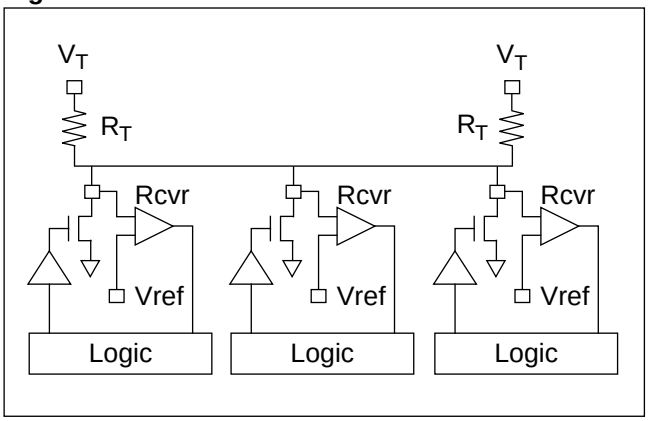


GTL (Gunning Transceiver Logic)

GTL and GTL+ interface I/Os are useful for implementing highly reliable system, satisfying fast and low-powered signal transfers and reducing noise in a switching circuitry.

In all 0.5μm cell libraries in SEC ASIC, GTL interface is fully supported.

Figure 1-4. GTL Interface

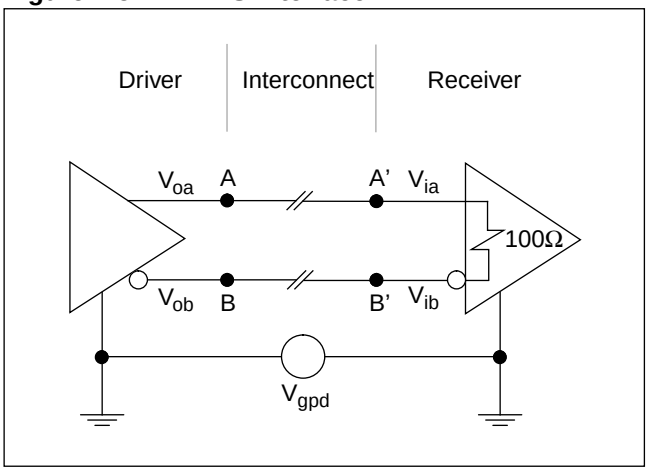


LVDS

LVDS (Low Voltage Differential Signals) buffer for SCI (Scalable Coherent Interface) system, shown in the following figure, enables high speed I/O interface with SEC ASIC's high frequency PLL.

This structure is designed for high speed point-to-point unidirectional interface. Its main characteristics are much the same as ECL's differential mode; low noise generation, high noise immunity and low level signalling.

Figure 1-5. LVDS Interface



USB (Universal Serial Bus)

Various kinds of peripheral equipments such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. SEC ASIC offers USB interfaced buffers in the 0.5μm technology.

USB is applicable only in STD cells.

Figure 1-6. Full Speed Device Cable and Resistor Connections

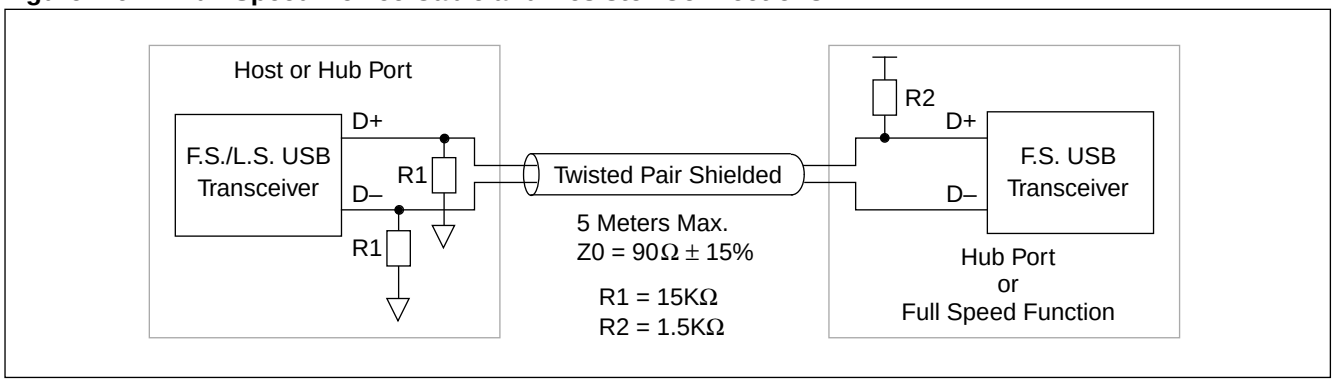
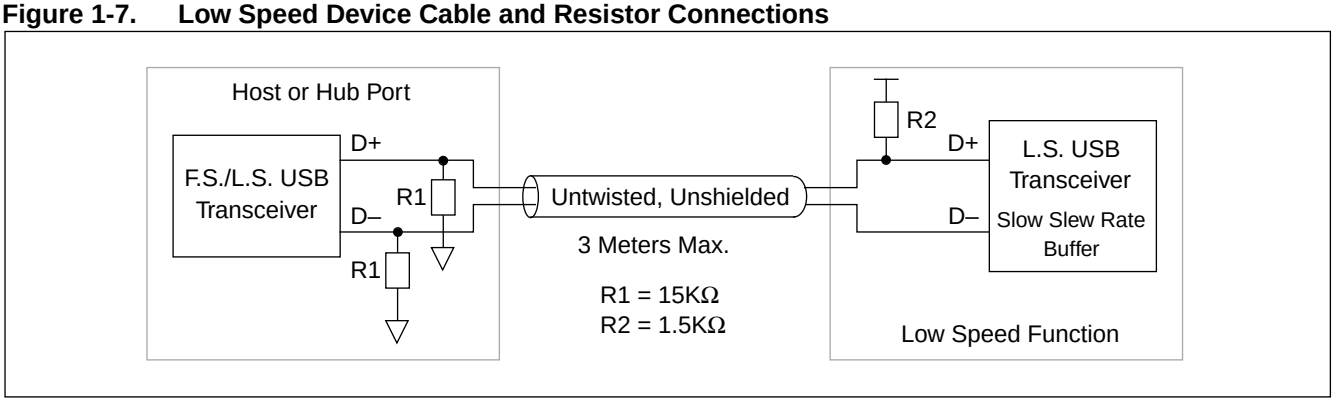


Figure 1-7. Low Speed Device Cable and Resistor Connections



LVTTL/LVCMOS

Low Voltage TTL and Low Voltage CMOS I/O buffers have various kinds of applications as normal TTL and CMOS I/O sets. Their key features are low voltage swing and low noise. Input voltage level is 5V compatible. Output high voltage is 2.4V ~ 3.5V in LVTTL and VDD–0.2V in LVCMOS.

SCSI

SCSI is widely used to extend peripherals, requires external terminator. SEC ASIC supports SCSI-3 fast-20 parallel interface and SCSI-3 parallel interface only in STD80. Both of them have fail-safe function. SCSI buffer is two times as big as normal buffers.

PCMCIA

PCMCIA (Personnel Computer Memory Card Industry Association) buffers guarantees an accurate logic level even when the internal or external voltage source level of a chip changes between 5V and 3.3V.

This buffers are designed for 16-bit external extension card of notebook PC.

CardBus Buffers

CardBus I/O buffers have 3.3V 32-bit bus width and 33MHz of transmission speed. They are for external CardBus type of extension card of notebook PC.

V_{DD}/V_{SS} RULES AND GUIDELINES

There are three types of V_{DD} and V_{SS} in STD80/STDM80, each with its related bus and pad cells. To support the use of mixed voltage, two different V_{DD} types are needed for 5V and 3.3V respectively.

(1) Core logic
– VSSI, VDD5I (for 5V)
(2) Input buffers (usable when requested)
– VSSP, VDD5P (for 5V), VDD3P (for 3.3V)
(3) Output buffers
– VSSO, VDD5O (for 5V), VDD3O (for 3.3V)

The number of V_{DD} and V_{SS} pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching inputs
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency of the design.

Core Logic V_{SS} Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that V_{DD}/V_{SS} bounce caused by a simultaneous gate switching is kept to minimum. The voltage bounce on the power bus can have a negative impact on a gate-switching speed and even on the functionality of macrocells like flip-flops and latches in an extreme case.

Because of variations in package inductance, the number of V_{DD}/V_{SS} pads required for a specific design is the function of the operating frequency of a chip, i.e., designs operating at high frequency should use more V_{DD}/V_{SS} pads.

- V_{DD} bus width and pad requirements are half of V_{SS}.
- V_{DD}/V_{SS} buses and pads should be distributed evenly in the core and on all sides of the chip.
- Whenever possible, at least one VSSI pad should be used on each side of the chip.
- The total number of core logic V_{DD} pads required is half of VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

G x S x F x 2.00e–5

,where
G = Total number of used gates,
S = % of simultaneous switching gates,
F = Switching frequency in MHz.

Input Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

- One VSSP is required to support 32 input buffers, and one input buffer V_{DD} can support up to 64 inputs.
- For simultaneous switching inputs, one VSSP pad is required for every 20 inputs, and one input buffer V_{DD} pad for every 40 inputs.
- Input buffer V_{SS}/V_{DD} pads should be placed in such a way that they equally divide the input buffers on either side.

Output Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

The number of VSSO pads required for a device can be calculated from the following expressions.

In 5V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 40 + \Sigma (I_{OL\ Normal\ outputs}) / 64$$

In 3.3V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 50 + \Sigma (I_{OL\ Normal\ outputs}) / 80$$

- The total number of output buffer V_{DD} pads required is half of VSSO.
- Output buffer V_{SS}/V_{DD} pads should be placed in such a way that output buffers are equally divided on either side.

POWER DISSIPATION

Estimation of Power Dissipation in CMOS Circuit

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, a switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and a reliability of the device also depend on the power dissipation which determines the temperature at which the die operates. To obtain a high speed and a reliability, designers must estimate the power dissipation of the device accurately and determine the appropriate environments including packages and system cooling methods.

This section describes the concept of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating them in the SEC STD80/STDM80 library, and finally their relationship with a temperature.

Static (DC) Power Dissipation

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor included in the input buffers is about 50μA typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of TTL output and bi-directional buffers is determined by the following formula:

$$P_{DC\_TTL\_OUTPUT} = \Sigma(V_{OL} \times I_{OL} \times t_L) + \Sigma((V_{DD} - V_{OH}) \times I_{OH} \times t_H)$$

,where

$t_H = T_{HIGH} / T$,

$t_L + t_H = 1$.

Dynamic (AC) Power Dissipation

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging of a node capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$$1 / 2 \times (C_L \times V_{DD}^2)$$

,where V_{DD} is a power supply voltage.

The switching occurs twice per cycle for periodic signals: once for charging a capacitance and once for discharging it. Hence, the dynamic power dissipation due to the switching current is the energy divided by the clock period and multiplied by the factor of two, or

$$C_L \times V_{DD} \times V_{DD} / T$$

,where T is a clock period.

As shown above, it is quite straight forward to calculate the dynamic power dissipation for a single gate. The dynamic power dissipation for an entire chip is, however, much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 20% on the average and recommends to use this number to estimate the total dynamic power dissipation.

Power Dissipation in STD80/STDM80

This section describes the equations on how to estimate the power dissipation in STD80/STDM80. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{DC} + P_{AC}$$

Since only output buffers contribute to the static power dissipation,

$$P_{DC} = P_{DC\_OUTPUT}$$

,where P_{DC} output is the static power dissipated when output buffers source or sink.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), and internal cells ($P_{AC\_INTERNAL}$).

$$P_{AC} = P_{AC\_INPUT} + P_{AC\_OUTPUT} + P_{AC\_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

In STD80,

$P_{DC\_OUTPUT} = 150 \times I_{OL} \times N\_output$ [µW]
$P_{AC\_INPUT} = 23 \times N\_input \times F \times S$ [µW]
$P_{AC\_OUTPUT} = 25 \times N\_output \times F \times S \times C$ [µW]
$P_{AC\_INTERNAL} = 2.3 \times N\_internal \times F \times S$ [µW]

In STDM80,

$P_{DC\_OUTPUT} = 150 \times I_{OL} \times N\_output$ [µW]
$P_{AC\_INPUT} = 9.8 \times N\_input \times F \times S$ [µW]
$P_{AC\_OUTPUT} = 25 \times N\_output \times F \times S \times C$ [µW]
$P_{AC\_INTERNAL} = 1.2 \times N\_internal \times F \times S$ [µW]

,where
I_{OL} is source and sink current of output buffers in mA,
N_output is the number of output buffers used,
N_input is the number of input buffers used,
N_internal is the number of internal cells used,
F is the maximum operation frequency in MHz,
S is the estimated degree of a switching activity (typically 0.2),
C is the output load capacitance in pF.

Temperature and Power Dissipation

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

,where
θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-1. Thermal Impedances of SEC Packages

	QFP						
Pin Number	**64**	**80**	**100**	**120**	**160**	**208**	**240**
θ_{JA} [°C/W]	60	60	60	50	50	40	40

Maximum Junction Temperature (T_J)

The allowable maximum junction temperatures for plastic and ceramic packages are as follows:

Junction temperature for plastic package ≤ 125°C
Junction temperature for ceramic package ≤ 150°C.

PROPAGATION DELAYS

Interconnection wire length, temperature and supply voltage are the chief factors affecting propagation delays.

Wire Length Load

The loading due to interconnection wire length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{FO} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

,where

C_{FO} = Number of fanouts in a standard load,

A = Area of block size in mm^2,

C_{WL} = Number of equivalent standard loads due to an interconnection,

e.g.,

C_{FO} = 7 (standard load),

A = 25mm^2,

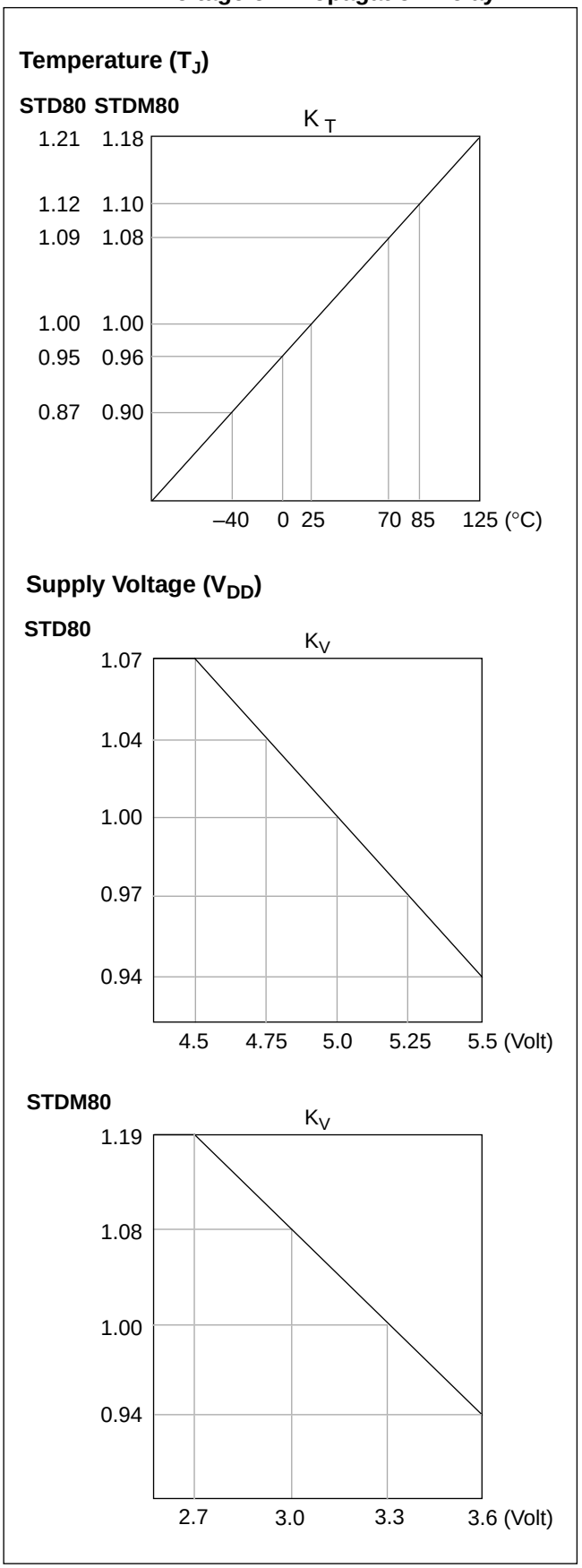
C_{WL} = 5.8 (standard load).

Temperature and Supply Voltage

The next figure describes propagation delay correction factors (K_T, K_V) as a function of on-chip junction temperature (T_J) as well as supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same.

The temperature of the die inside the package (junction temperature, T_J), is calculated using chip power dissipation and the thermal resistance to ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from SEC application engineers.

Figure 1-8. Effect of Temperature and Supply Voltage on Propagation Delay



Best and Worst Case Conditions

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case:

$T_{BC} = K_{PBC} \times K_T \times K_V \times T_{NOM} = K_{BC} \times T_{NOM}$

Worst case:

$T_{WC} = K_{PWC} \times K_T \times K_V \times T_{NOM} = K_{WC} \times T_{NOM}$

,where

T_{BC} = Best case propagation delay

T_{WC} = Worst case propagation delay

T_{NOM} = Normal propagation delay

($T_J = 25^oC$, $V_{DD} = 5V$ and typical process)

K_{PWC} = Worst case process correction factor

K_{PBC} = Best case process correction factor

With above equations, we can calculate the multipliers of K_{WC} and K_{BC} as follows.

Table 1-2. STD80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	5.5V	–40 °C	Min.	0.51
Commercial	5.25V	0 °C	Min.	0.56

Table 1-3. STD80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	4.5V	125 °C	Max.	1.77
Commercial	4.75V	115 °C	Max.	1.69

Table 1-4. STDM80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	3.6V	–40 °C	Min.	0.49
Commercial	3.6V	0 °C	Max.	0.52

Table 1-5. STDM80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	2.7V	125 °C	Max.	1.97
Commercial	3.0V	115 °C	Max.	1.77

Derating factors of STD80/STDM80

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of $V_{DD} = 5V$, $T_A = 25°C$ and typical process.

The derating factors of STD80/STDM80 are as follows.

Table 1-6. STD80/STDM80 process derating factor

Process Factor (K_P)	Slow	Typ.	Fast
	1.40	1.00	0.60

Table 1-7. STD80 temperature derating factor

Temp. (°C)	125	85	70	25	0	–40
K_T	1.21	1.12	1.09	1.00	0.95	0.87

Table 1-8. STDM80 temperature derating factor

Temp. (°C)	125	85	70	25	0	–40
K_T	1.18	1.10	1.08	1.00	0.96	0.90

Table 1-9. STD80 voltage derating factor (K_V)

Voltage (V)	5.5	5.25	5	4.75	4.5
K_V	0.94	0.97	1.00	1.04	1.07

Table 1-10. STDM80 voltage derating factor (K_V)

Voltage (V)	3.6	3.3	3.0	2.7
K_V	0.94	1.00	1.08	1.19

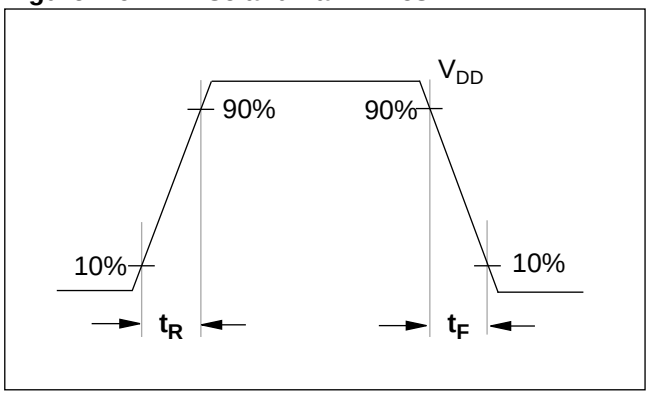
Timing Parameters

This section discusses issues involving timing parameters for primitive cells.

RISE / FALL TIMES

The definition of rise time (t_R) and fall time (t_F) is shown in the following figure.

Figure 1-9. Rise and Fall Times

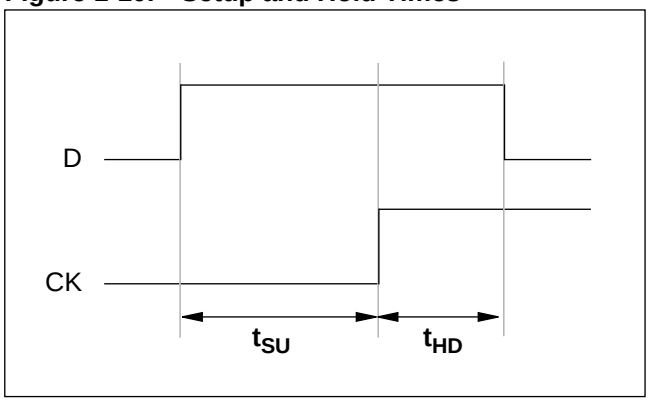


SETUP / HOLD TIMES

Setup time (t_{SU}) is a minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs. Hold time (t_{HD}) is a minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred.

The next figure shows the relationship between setup and hold times for a standard flip-flop triggered on the rising edge of the clock.

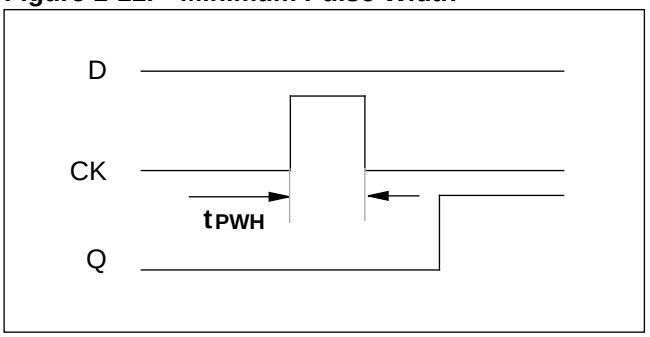
Figure 1-10. Setup and Hold Times



MINIMUM PULSE WIDTHS

Minimum clock pulse widths (t_{PWH}, t_{PWL}) are the time intervals during a clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch.

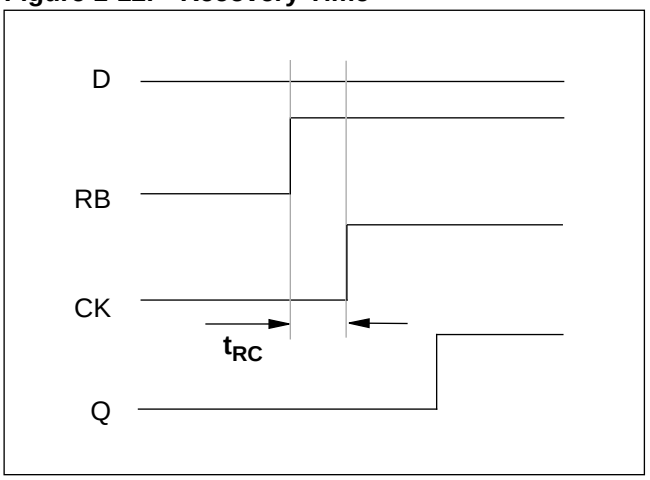
Figure 1-11. Minimum Pulse Width



RECOVERY TIMES

Recovery time (t_{RC}) is the minimum time after an asynchronous pin is disabled that an active clock edge will propagate data from input to output. If the active edge or clock occurs before the specified recovery time, the input data will not propagate.

Figure 1-12. Recovery Time

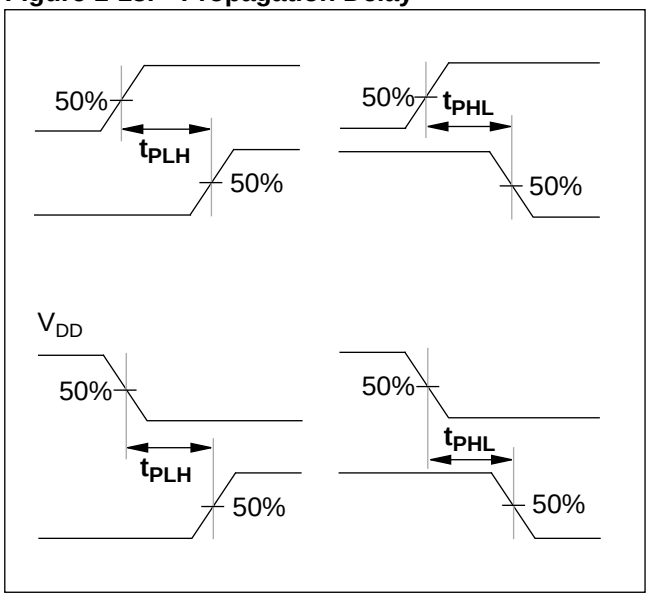


PROPAGATION DELAYS

A delay for a macrocell is considered to be a rising delay (t_{PLH}) if the signal on the output pin is rising. For a rising input and a rising output, the rising delay is the interval between the times the input becomes 50% of supply voltage (V_{DD}) and the output becomes 50% of V_{DD}.

If the input is falling and the output is rising, the rising delay is the interval between the times the input falls to 50% of V_{DD} and the output rises to 50% of V_{DD}. The converse is true for a falling delay (t_{PHL}).

Figure 1-13. Propagation Delay

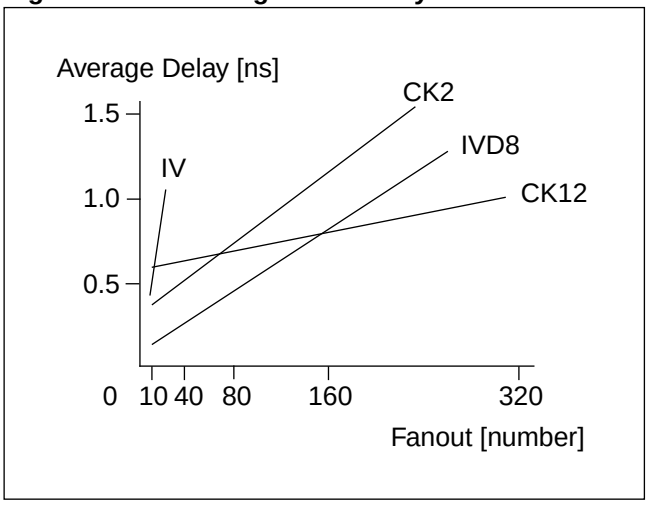


Proper Use of Buffers

Figure 1-14. Average Gate Delay in STD80 shows the average propagation delays of an internal inverter (IV), an 8X inverter (IVD8), a normal clock driver (CK2), and a high clock driver (CK12) in STD80.

Note that transistors uses in I/O slots are larger and have ON channel resistance about one order of magnitude lower than those of the N and P channel transistors in primitive cells. This makes them likely candidates for use as buffers for high fanout signals. For example, CK2 and CK12 buffers require one I/O slot location. Both can be used as high fanout internal buffers.

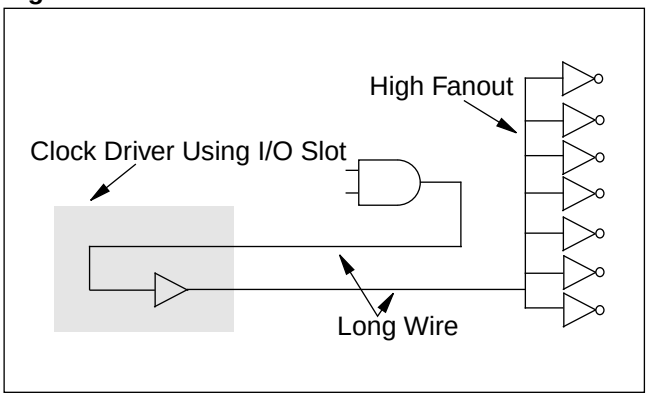
Figure 1-14. Average Gate Delay in STD80



One caution, emphasized in Figure 1-15. Use of I/O Slot for an Internal Buffer, shows that if you route to a buffer that uses an I/O slot from an internal element and back into internal logic, the additional wiring needed could increase propagation delays materially. Higher drive strength internal cells may be more appropriate than I/O slot buffers.

Realize also that using I/O slot cells for internal buffering removes those locations for use as external I/Os and uses two wiring channels, thereby increasing routability congestion on masterslice products.

Figure 1-15. Use of I/O Slot for an Internal Buffer



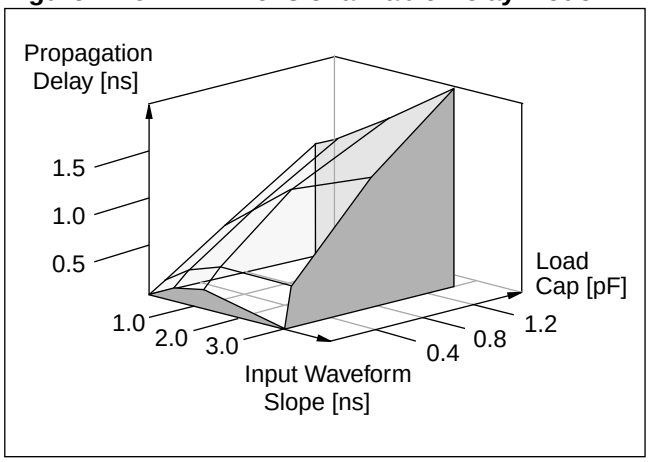
DELAY MODEL

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STD80/STDM80 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.5μm cell-based products.

Figure 1-16. 2-Dimensional Table Delay Model



The Table 1-11. Table Delay Model Example shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-11. Table Delay Model Example

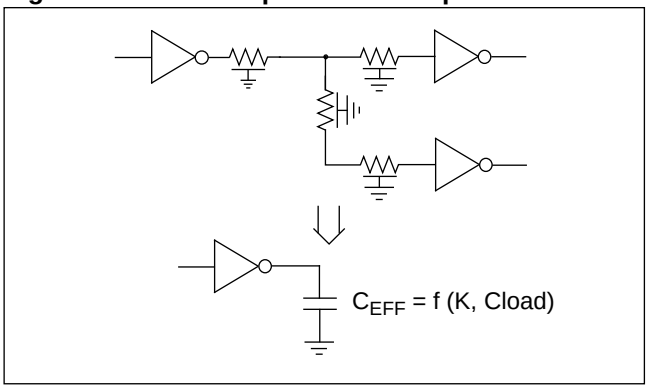
Slope \ Cap.	0.03	0.13	0.53	1.32
0.10	0.07	0.14	0.42	0.97
0.30	0.08	0.17	0.45	1.02
0.80	0.06	0.18	0.51	1.07
1.60	0.01	0.18	0.60	1.18

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The delay time due to the interconnection wire can be separated into two components. One is the signal propagation delay time across the metal lines. This delay time component is computed through conventional RC analysis based on ∏-model. The other is an additional delay on the driving cell due to the wire load. The traditional way to compute this is based on the lumped capacitance model, ignoring wire resistance.

For sub-micron technology, this approximation cannot be accepted any more. The wire resistance has a shielding effect on the driving cell from load capacitances. An effective capacitance C_{EFF}, a single capacitance approximating distributed interconnection wire resistance and capacitance, is derived, as illustrated in the following figure. The compensation factor K, extracted for each cell, is a function of the length of interconnection wires and the layout topology. All these effects are merged to determine the effective capacitance and this value is used as an index of the table delay model.

Figure 1-17. Concept of Effect Capacitance



The figure below summarizes the features of SEC ASIC's delay model.

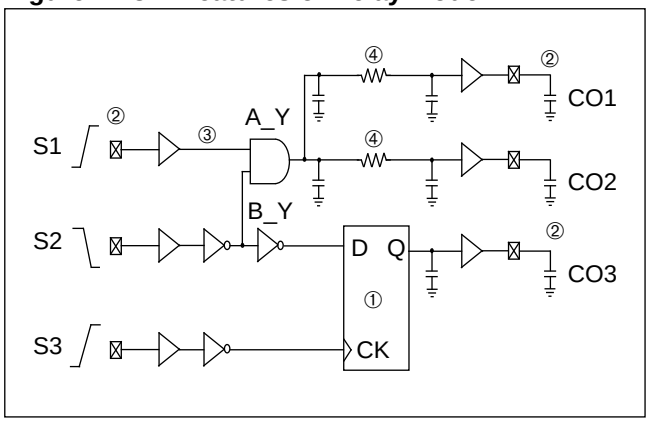
① 2-dimensional table delay model for output loading and input waveform slope effects is used. The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-18. Features of Delay Model



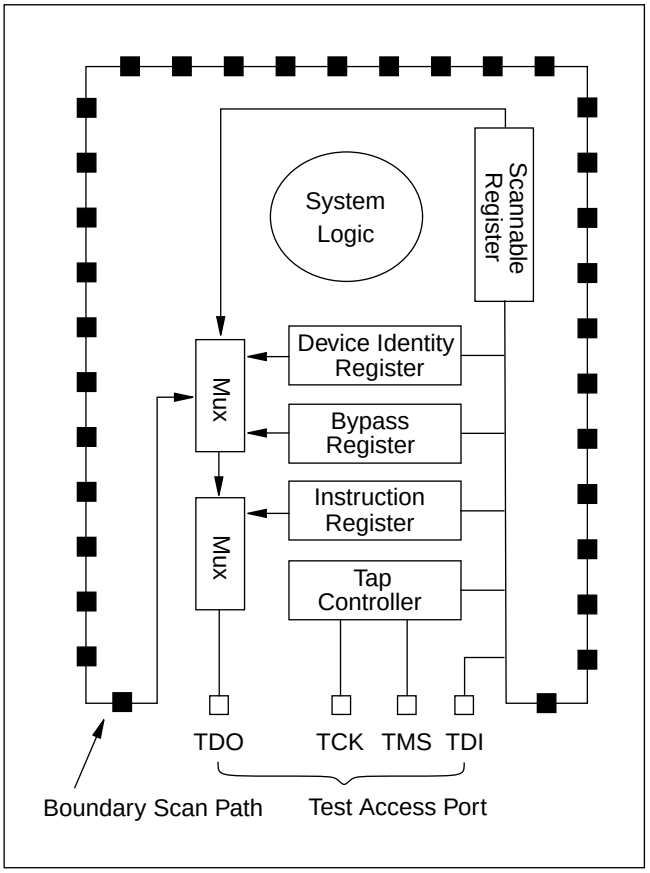
TESTABILITY DESIGN METHODOLOGY

Scan Design

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

Boundary-Scan

- IEEE Std 1149.1
- 5 types of JTAG boundary-scan cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design



MAXIMUM FANOUTS

Internal Macrocells

The maximum fanouts for STD80/STDM80 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.44ns (STD80)/0.39ns (STDM80). Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STD80/STDM80 internal macrocells are listed.

Table 1-12. Maximum Fanouts of Internal Macrocells (When t_R/t_F = 0.44ns (STD80)/0.39ns (STDM80))

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
Logic Cells			
AD2	Y	49	28
AD2D2	Y	106	59
AD3	Y	49	28
AD3D3	Y	161	84
AD4	Y	49	28
AD4D2	Y	105	58
AD5	Y	38	17
AD5D2	Y	78	34
ND2	Y	45	23
ND2D2	Y	95	48
ND3	Y	30	15
ND3D2	Y	63	30
ND4	Y	23	11
ND4D2	Y	47	22
ND5	Y	18	7
ND5D2	Y	36	16
ND6	Y	49	28
ND6D2	Y	104	55
ND8	Y	49	28
ND8D2	Y	105	56
NR2	Y	40	17
NR2D2	Y	87	37
NR3	Y	25	11
NR3D2	Y	54	23
NR4	Y	18	7
NR4D2	Y	38	15
NR5	Y	49	28
NR5D2	Y	104	59
NR6	Y	49	28
NR6D2	Y	104	58
NR8	Y	49	28
NR8D2	Y	104	58
OR2	Y	49	28
OR2D2	Y	104	55
OR3	Y	49	26
OR3D3	Y	147	71
OR4	Y	43	22
OR4D2	Y	89	44
OR5	Y	40	21
OR5D2	Y	89	45
XN2	Y	49	27
XN2D2	Y	103	54
XN3	Y	47	25
XN3D3	Y	134	65
XO2	Y	49	28
XO2D2	Y	102	55
XO3	Y	47	25
XO3D3	Y	134	65
AO21	Y	30	15
AO21D2	Y	64	31
AO211	Y	22	9
AO211D2	Y	44	18
AO22	Y	28	13
AO22D2	Y	57	27
AO22A	Y	27	13
AO22D2A	Y	55	27
AO222	Y	21	8
AO222D2	Y	105	59
AO222A	Y	26	10
AO222D2A	Y	52	21
AO33	Y	18	7
AO33D2	Y	106	58
AO333	Y	15	4
AO333D2	Y	107	60
OA21	Y	29	15
OA21D2	Y	61	31
OA211	Y	20	9
OA211D2	Y	40	19
OA22	Y	28	14
OA22D2	Y	59	29

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
OA22A	Y	29	15
OA22D2A	Y	59	31
OA2222	Y	49	28
OA2222D2	Y	104	55
DL1D2	Y	105	60
DL1D4	Y	222	113
DL2D2	Y	108	60
DL2D4	Y	219	114
DL3D2	Y	109	61
DL3D4	Y	226	111
DL4D2	Y	110	61
DL4D4	Y	228	110
DL5D2	Y	110	60
DL5D4	Y	228	109
DL10D2	Y	105	53
DL10D4	Y	207	97
IV	Y	53	29
IVD2	Y	114	65
IVD3	Y	175	101
IVD4	Y	231	144
IVD6	Y	324	190
IVD8	Y	403	234
IVA	Y	53	29
IVD2A	Y	114	65
IVD3A	Y	175	101
IVD4A	Y	231	144
IVCD11	Y	51	27
	YN	53	29
IVCD13	Y	47	24
	YN	175	100
IVCD22	Y	117	62
	YN	114	65
IVCD26	Y	101	53
	YN	324	190
IVCD44	Y	259	162
	YN	231	144
IVT	Y	43	23
IVTD2	Y	93	48
IVTD4	Y	177	90
IVTD8	Y	323	179
IVTN	Y	43	22
IVTND2	Y	87	46
IVTND4	Y	173	85

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
IVTND8	Y	336	158
NID	Y	49	28
NID2	Y	106	59
NID3	Y	161	90
NID4	Y	222	121
NID6	Y	331	163
NID8	Y	438	209
NIT	Y	43	23
NITD2	Y	91	47
NITD4	Y	180	96
NITD8	Y	323	203
NITN	Y	43	23
NITND2	Y	88	46
NITND4	Y	176	88
NITND8	Y	324	158
Flip-Flops			
FD1	All Pins	49	28
FD1D2	Q	105	58
	QN	107	60
FD1CS	Q	49	28
	QN	49	27
FD1CSD2	Q	105	58
	QN	104	55
FD1S	All Pins	49	28
FD1SD2	Q	105	58
	QN	106	60
FD1Q	Q	49	28
FD1QD2	Q	107	59
FD1X2	All Pins	49	28
FD1X4	All Pins	49	28
YFD1	Q	49	26
	QN	43	24
YFD1D2	Q	105	53
	QN	90	49
FD2	All Pins	49	28
FD2D2	Q	106	58
	QN	109	60
FD2CS	All Pins	49	27
FD2CSD2	Q	105	58
	QN	106	55
FD2S	All Pins	49	28
FD2SD2	Q	106	58
	QN	108	60

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FD2Q	Q	49	28
FD2QD2	Q	107	58
FD2X2	All Pins	49	28
FD2X4	All Pins	49	28
YFD2	Q	48	26
	QN	40	21
YFD2D2	Q	103	51
	QN	80	42
FD2T	Q	49	27
	Z	28	15
FD2TD2	Q	106	58
	Z	52	26
FD2TCS	Q	48	27
	Z	28	12
FD2TCSD2	Q	104	57
	Z	52	26
FD2TS	Q	49	27
	Z	28	12
FD2TSD2	Q	106	58
	Z	52	26
FD3	All Pins	49	28
FD3D2	Q	107	58
	QN	107	59
FD3CS	Q	49	28
	QN	49	27
FD3CSD2	Q	106	59
	QN	105	55
FD3S	All Pins	49	28
FD3SD2	Q	106	59
	QN	106	58
FD3Q	Q	49	28
FD3QD2	Q	106	59
FD3X2	All Pins	49	28
FD3X4	All Pins	49	28
YFD3	Q	43	22
	QN	43	24
YFD3D2	Q	89	42
	QN	89	49
FD4	Q	49	27
	QN	49	28
FD4D2	All Pins	106	58
FD4CS	All Pins	49	27

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FD4CSD2	Q	106	58
	QN	106	55
FD4S	All Pins	49	28
FD4SD2	All Pins	106	58
FD4Q	Q	49	28
FD4QD2	Q	106	59
FD4X2	All Pins	49	28
FD4X4	Qn	49	27
	QNn	49	28
YFD4	Q	43	22
	QN	39	20
YFD4D2	Q	88	41
	QN	80	42
FD5	All Pins	49	28
FD5D2	Q	105	60
	QN	106	59
FD5S	All Pins	49	28
FD5SD2	Q	105	58
	QN	106	59
FD5X4	All Pins	49	28
FD6	All Pins	49	28
FD6D2	Q	105	58
	QN	106	61
FD6S	All Pins	49	28
FD6SD2	Q	106	58
	QN	108	60
FD7	All Pins	49	28
FD7D2	Q	106	59
	QN	106	58
FD7S	All Pins	49	28
FD7SD2	All Pins	106	58
FD8	Q	49	27
	QN	49	28
FD8D2	Q	106	58
	QN	105	58
FD8S	All Pins	49	28
FD8SD2	Q	106	59
	QN	106	58
FDS2	All Pins	59	28
FDS2D2	Q	105	58
	QN	106	60
FDS2CS	Q	49	28
	QN	49	27

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FDS2CSD2	Q	105	58
	QN	105	55
FDS2S	All Pins	49	28
FDS2SD2	Q	106	60
	QN	105	59
FDS3	All Pins	49	28
FDS3D2	Q	106	60
	QN	105	59
FG1	All Pins	49	28
FG1X4	All Pins	49	28
FG2	All Pins	49	28
FG2X4	All Pins	49	28
FJ1	All Pins	49	28
FJ1D2	Q	105	56
FJ1D2	QN	104	58
FJ1S	Q	50	28
	QN	49	28
FJ1SD2	Q	105	56
	QN	107	59
FJ2	Q	50	28
	QN	49	28
FJ2D2	Q	105	57
	QN	106	59
FJ2S	Q	50	28
	QN	49	28
FJ2SD2	Q	106	56
	QN	109	61
FJ4	Q	50	28
	QN	49	27
FJ4D2	Q	105	56
	QN	106	58
FJ4S	Q	50	28
	QN	49	28
FJ4SD2	Q	106	56
	QN	106	58
FT2	All Pins	49	28
FT2D2	Q	106	57
	QN	108	60
FT3	All Pins	49	28
FT3D2	Q	107	59
	QN	106	58
Latches			
LD1	All Pins	49	28

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
LD1D2	Q	106	60
	QN	105	58
LD1S	All Pins	49	28
LD1SD2	Q	106	60
	QN	106	58
LD1Q	Q	49	28
LD1QD2	Q	104	59
LD1X4	All Pins	49	28
LD1X4D2	Qn	106	59
	QNn	106	58
YLD1	Q	43	24
	QN	51	28
YLD1D2	Q	89	50
	QN	114	61
LD1A	Q	43	23
LD1B	QN	15	5
	ZN	43	23
LD2	All Pins	49	28
LD2D2	Q	105	58
	QN	108	60
LD2Q	Q	49	28
LD2QD2	Q	107	59
YLD2	Q	42	22
	QN	44	22
YLD2D2	Q	44	23
	QN	96	47
LD3	All Pins	49	28
LD3D2	Q	108	60
	QN	106	58
LD4	Q	49	28
	QN	49	27
LD4D2	Q	107	58
	QN	105	58
LD5	All Pins	49	28
LD5D2	Q	106	59
	QN	105	58
LD5S	All Pins	49	28
LD5SD2	Q	106	59
	QN	105	58
LD5X4	All Pins	49	28
LD5X4D2	Qn	106	59
	QNn	106	58
LD6	All Pins	49	28

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
LD6D2	Q	106	58
	QN	108	60
LD7	All Pins	49	28
LD7D2	Q	108	60
	QN	106	58
LD8	Q	49	28
	QN	49	27
LD8D2	Q	107	58
	QN	105	58
LDS2	All Pins	49	28
LDS6	All Pins	49	28
LS0	All Pins	39	20
LS0D2	All Pins	78	40
LS1	All Pins	18	8
LS2	All Pins	39	20
Bus Holder			
BUSHOLDER	Y	10,000	10,000
Internal Clock Drivers			
CK2	Y	Fig 1-19 (a)	Fig 1-20 (a)
CK4	Y	Fig 1-19 (b)	Fig 1-20 (b)
CK6	Y	–	Fig 1-20 (c)
CK8	Y	Fig 1-19 (c)	Fig 1-20 (d)
CK12	Y	Fig 1-19 (d)	–
Decoders			
DC4	All Pins	49	28
DC4I	YN(0/2)	43	23
	YN(1/3)	45	23
DC8I	All Pins	30	15
Adders			
FA	S	49	28
	CO	49	27
FAD2	S	103	55
	CO	103	54
HA	S	49	27
	CO	49	28
HAD2	S	103	54
	CO	106	59
Multiplexers			
MX2	Y	49	28
MX2D3	Y	152	76
MX2X4	All Pins	49	28
YMX2	Y	49	28
YMX2D2	Y	102	59

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
MX2I	YN	28	13
MX2ID2	YN	104	59
MX2IA	YN	28	13
MX2ID2A	YN	104	59
MX2IX4	All Pins	28	13
MX3I	YN	49	28
MX3ID2	YN	104	59
MX4	Y	48	26
MX4D2	Y	96	48
YMX4	Y	49	27
YMX4D2	Y	102	33
MX5	Y	49	27
MX5D2	Y	102	55
MX8	Y	45	22
MX8D2	Y	86	41
YMX8	Y	49	27
YMX8D2	Y	102	53

I/O Cells

The maximum fanouts for 5V and 3.3V I/O cells are as follows when the rise and fall times of the input signal is 0.40ns.

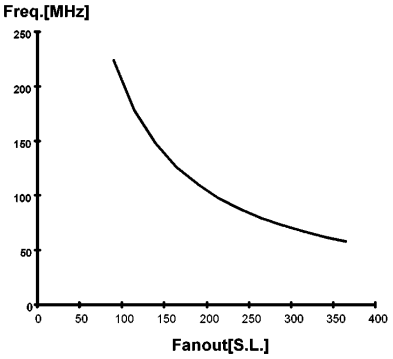
The graphs for fanout vs. frequency curve of STD80/STDM80 internal/input clock drivers are shown in the next page.

Table 1-13. Maximum Fanouts of I/O Cells (When t_R/t_F = 0.40ns)

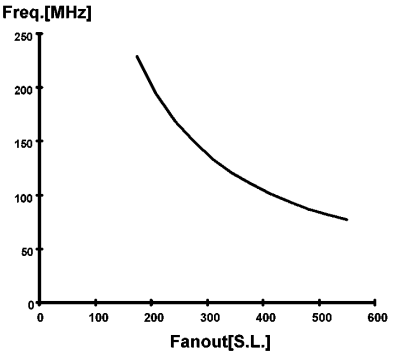
Cell Name	Output Pin	Maximum Fanouts	
		STD80	STDM80
PIC	PO	91	42
	Y	231	137
PICD	PO	92	42
	Y	237	141
PICU	PO	91	42
	Y	240	130
PIL PILD	PO	91	–
	Y	277	–
PILU	PO	91	–
	Y	281	–
PIS	PO	91	42
	Y	182	181
PISD	PO	91	42
	Y	179	150
PISU	PO	91	42
	Y	179	206
PITb	PO	91	–
	Y	180	–
PLIC	PO	69	–
	Y	293	–
PLICD	PO	69	–
	Y	317	–
PLICU	PO	69	–
	Y	302	–
PLIS	PO	69	–
	Y	348	–
PLISD	PO	69	–
	Y	361	–
PLISU	PO	69	–
	Y	246	–
PHIC	PO	–	34
	Y	–	141
PHICD	PO	–	34
	Y	–	143
PHICU	PO	–	34
	Y	–	137
PHIL	PO	–	34
	Y	–	136
PHILD	PO	–	34
	Y	–	156
PHILU	PO	–	34
	Y	–	135
PHIS	PO	–	34
	Y	–	131
PHISD	PO	–	34
	Y	–	144
PHISU	PO	–	34
	Y	–	145
PHIT PHITD	PO	–	34
	Y	–	144
PHITU	PO	–	34
	Y	–	148
PSCKDab2	Y	Fig 1-19 (a)	Fig 1-20 (a)
PSCKDab4	Y	Fig 1-19 (b)	Fig 1-20 (b)
PSCKDab6	Y	–	Fig 1-20 (c)
PSCKDab8	Y	Fig 1-19 (c)	Fig 1-20 (d)
PSCKDab12	Y	Fig 1-19 (d)	–
PSOSCK1 PSOSCK16	PADY	9	6
	YN	36	25
PSOSCK2 PSOSCK26	PADY	94	62
	YN	319	225
PSOSCM1 PSOSCM16	PADY	1097	778
	YN	888	633
PSOSCM2 PSOSCM26	PADY	1097	778
	YN	888	633
PSOSCM3 PSOSCM36	PADY	2194	1548
	YN	1596	1136
PSOSCM4 PSOSCM46	PADY	4356	3010
	YN	2389	1699
PSOSCM5 PSOSCM56	PADY	6592	4508
	YN	1257	894
PSOSCM6 PSOSCM66	PADY	8923	6054
	YN	4750	3369

Figure 1-19. Fanout (SL) vs. Frequency Curve of STD80 Clock Drivers

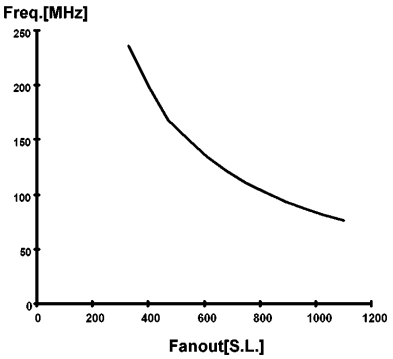
(a) CK2 PSCKDab2



(b) CK4 PSCKDab4



(c) CK8 PSCKDab8



(d) CK12 PSCKDab12

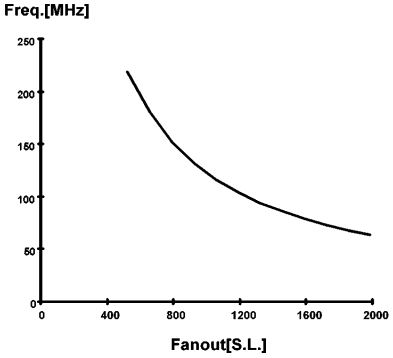
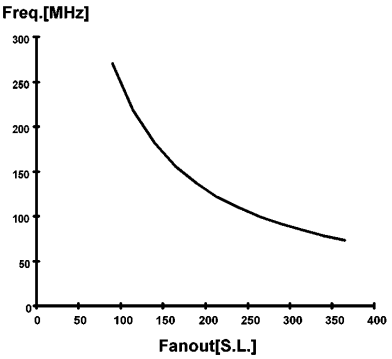
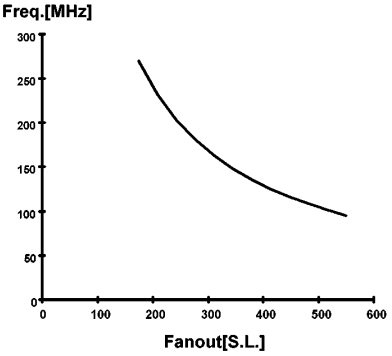


Figure 1-20. Fanout (SL) vs. Frequency Curve of STDM80 Clock Drivers

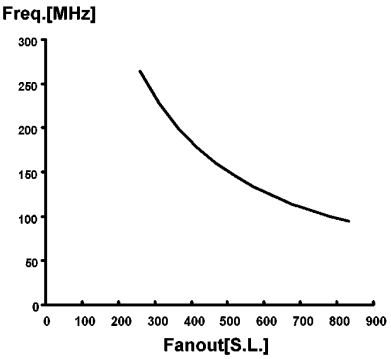
(a) CK2 PSCKDab2



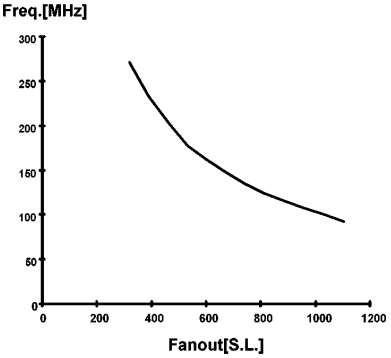
(b) CK4 PSCKDab4



(c) CK6 PSCKDab6



(d) CK8 PSCKDab8



PRODUCT LINE-UP

Table 1-14. Optimum Gates vs. Pad Numbers on STD80/STDM80

Ref. No	Estimated Gates	Total Pads		Maximum I/O Pads	
		TLM (70%)	DLM (40%)	TLM	DLM
01	10,000	57	75	41	59
02	15,000	70	93	54	77
03	20,000	81	107	65	91
04	30,000	99	131	83	115
05	40,000	114	151	98	135
06	50,000	128	169	112	153
07	60,000	140	186	124	170
08	70,000	151	201	135	185
09	80,000	162	214	146	198
10	90,000	172	227	156	211
11	100,000	181	240	175	224
12	120,000	198	263	182	247
13	140,000	214	284	198	268
14	160,000	229	303	213	287
15	180,000	243	322	227	306
16	200,000	256	339	240	323
17	250,000	287	379	271	363
18	300,000	314	416	298	400
19	350,000	339	449	323	433
20	400,000	363	480	347	464
21	450,000	385	509	369	493
22	500,000	406	537	390	521

NOTE: Chip size can be changed depending on the circuit design.

PACKAGES

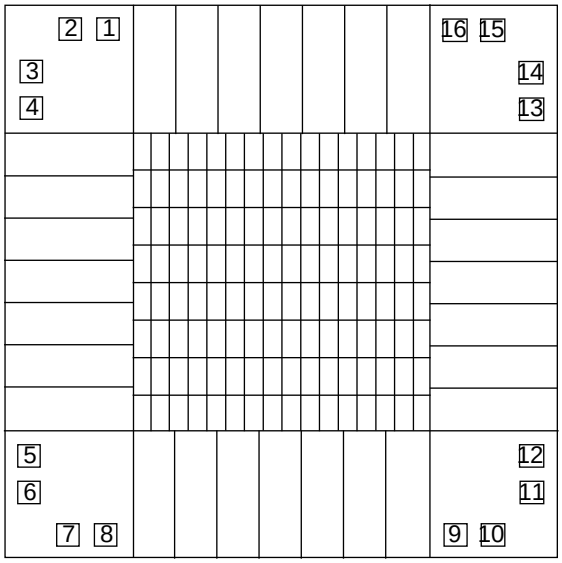
Type	DIP	SDIP	SOP	PLCC	QFP
Pin Count	24	24	28	28	44
	28	28	32	32	48
	40	30		44	60
	42	32		68	64
		40		84	80
		42			100
		48			128
		54			132
		56			160
		64			208
					240

NOTE: The selection of a package type and pin count is dependent on the size of a chip.

DEDICATED CORNER V_{DD}/V_{SS} PADS

The corner pads shown in the following figure are well-suited for double bonding purposes. Pad 1 and pad 2 can be bonded to the same package pin. Unlike normal I/O pads, these pads can only be used for V_{DD}/V_{SS} listed in Table 1-15. Use of Corner Pads.

Figure 1-21. V_{DD}/V_{SS} Corner Pads



NOTES:

1. There is no dedicated corner VSSI pad. Therefore, internal V_{SS} must be supplied using I/O pad type cell.
2. Corner pads are used to reduce the power/ground noise when some parts of the design cause noise problem especially while the other parts keep quiet.

Table 1-15. Use of Corner Pads

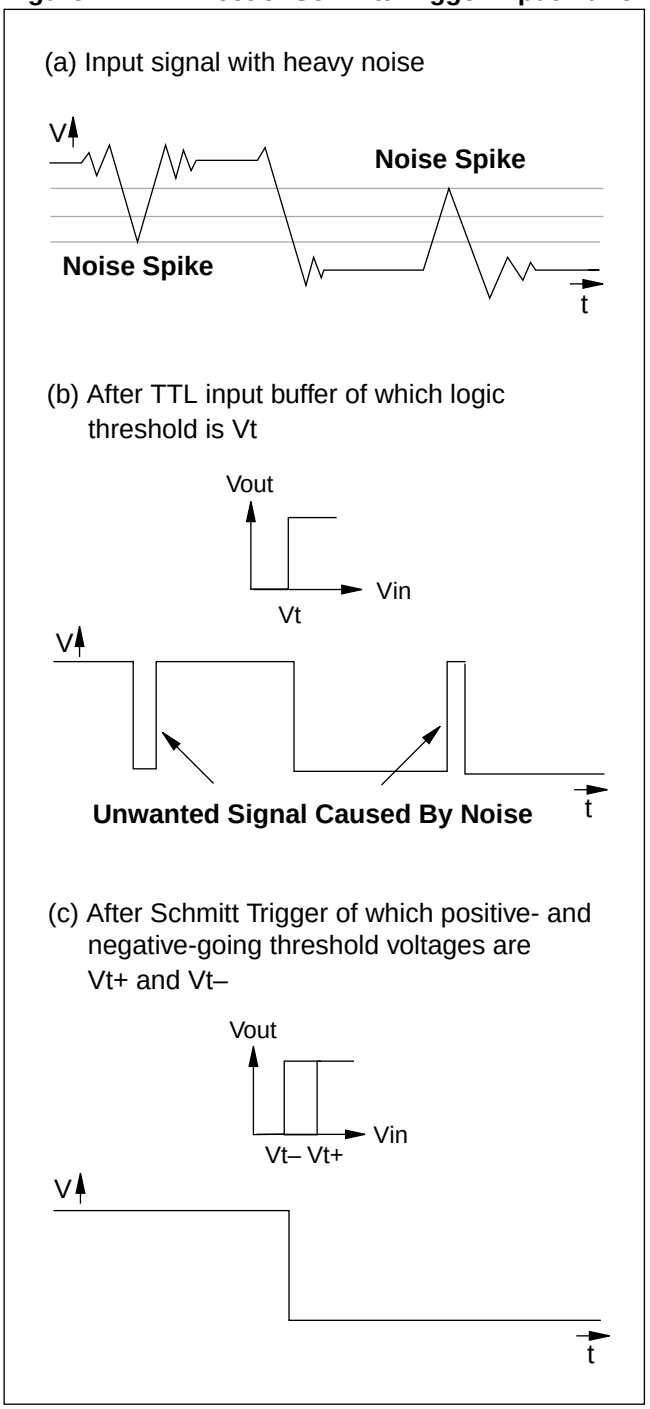
1	VSSO	9	VDD3O
2	VSSO	10	VDD3O
3	VSSI	11	VSSI
4	VSSI	12	VSSI
5	VDDI	13	VDDI
6	VDDI	14	VDDI
7	VDD5O	15	VSSO
8	VDD5O	16	VSSO

EXTERNAL DESIGN INTERFACE CONSIDERATIONS

This section briefly describes what you should consider when chips interface with outside world especially for a noise protection.

Input Buffer

Figure 1-22. Effect of Schmitt Trigger Input Buffer



Usually there are three types of input receivers in ASIC libraries; TTL input buffer, CMOS input buffer, and various Schmitt trigger input buffers.

TTL input buffer has relatively poor noise characteristics because of its shifted logic threshold voltage. CMOS input buffer is better than TTL against a noise because the logic threshold voltage is near 2.5volt. If an input signal has relatively large noise spikes, it could cause an unwanted input signal.

When an input signal is very noisy, the noise can be filtered by using a Schmitt trigger input buffer. As shown in Figure 1-22. Effect of Schmitt Trigger Input Buffer, Schmitt trigger input buffers have two different input thresholds for positive- and negative-going signals. This hysteresis between positive- and negative-going voltage signals can filter a noisy signal to a wanted one.

According to applications, the most suitable one can be chosen among the various Schmitt trigger input buffers having different levels of threshold voltage.

Output Pad Cell

As incoming signals to a chip have a noise, the noise can also be induced by the operation of the chip itself. There are several sources of a noise, but the greatest singular source of a noise is the switching of an output with high capacitive load.

Figure 1-23. Simple Model of Output Pad Cell

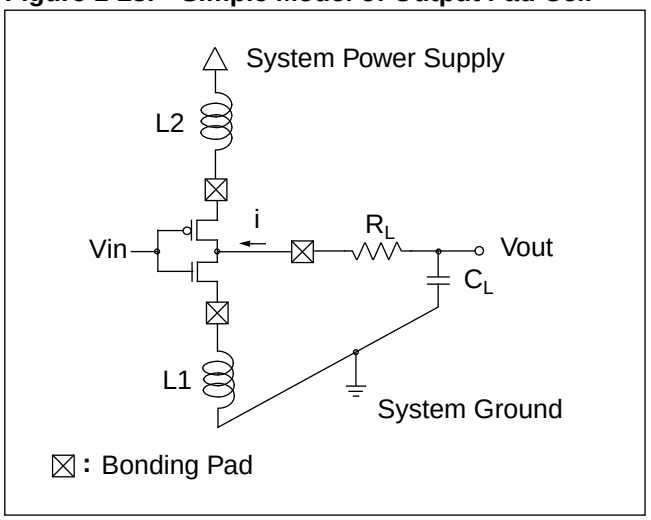


Figure 1-23. Simple Model of Output Pad Cell shows the simple model of an output driver considering the external interface. L1 and L2 are parasitic inductances of the package and C_L is an output load. Vout will fall as Vin rises and the current i flows through n-transistor discharging the loaded charge ($V_{DD} \times C_L$).

The details of this operations are described in Figure 1-24. Ground Bounce Phenomenon.

The important phenomenon which can be observed in this figure is that the voltage level Vn shifts relative to the system ground. Vn is the ground of the chip.

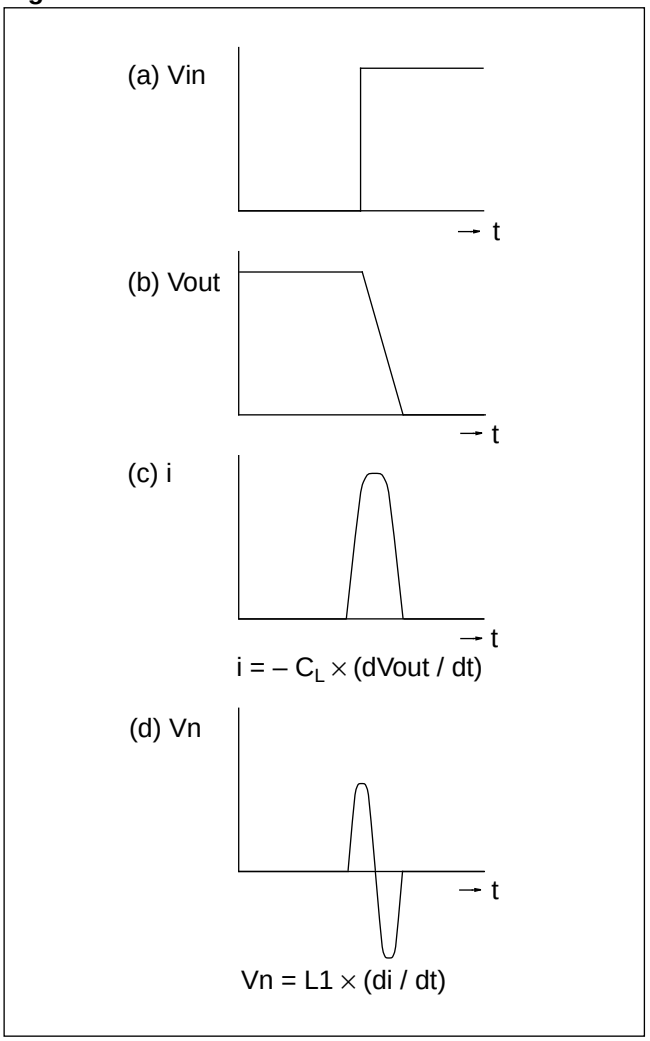
This phenomenon is called as a “ground bounce” that is the chip reference shift caused by the external inductance and the transient current flow to the ground.

The amount of voltage level shifted by the ground bounce is

$$Vn = -L \times (di / dt)$$

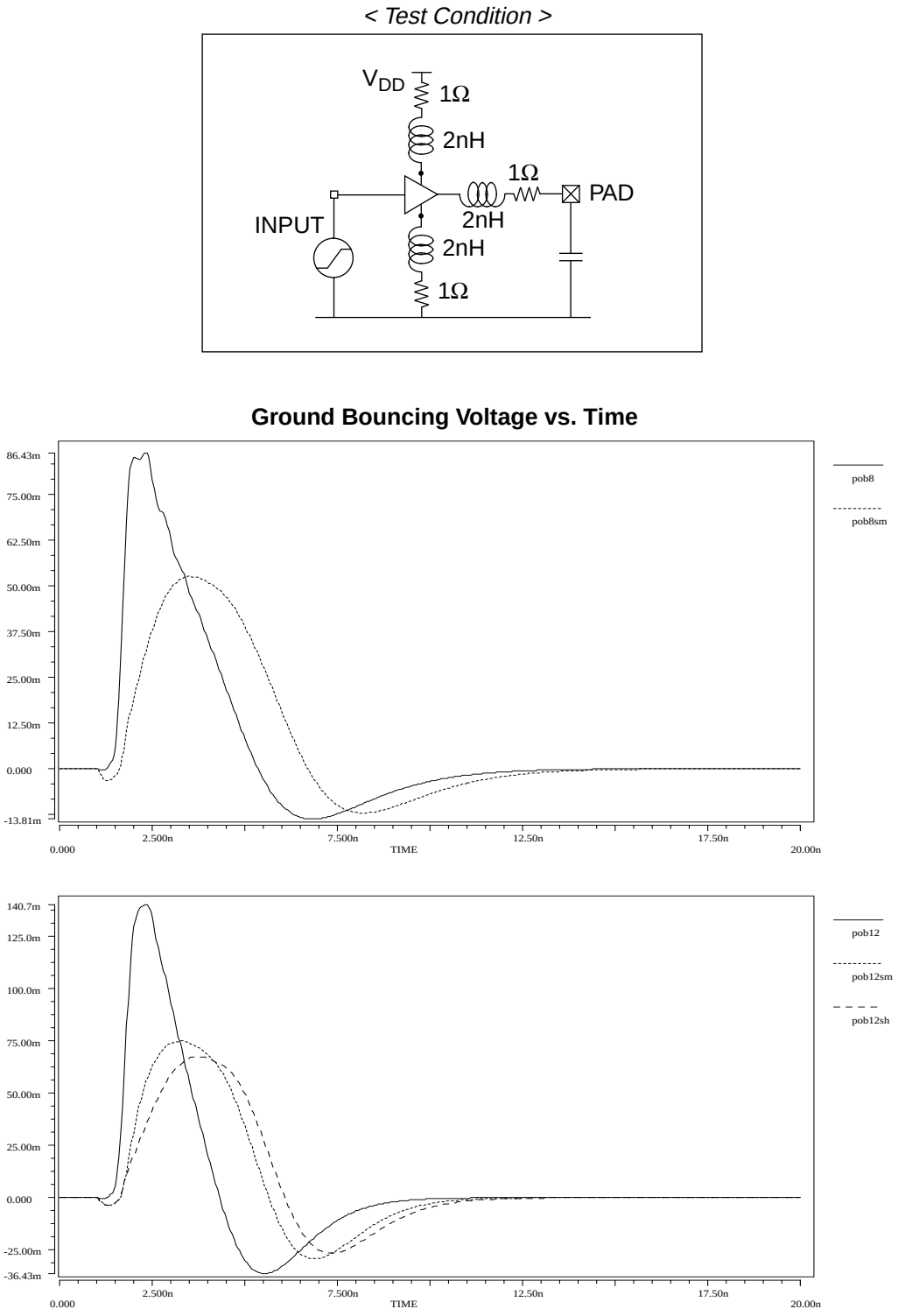
When the output driver makes a low-to-high transition, the similar noise problem is generated on the power.

Figure 1-24. Ground Bounce Phenomenon

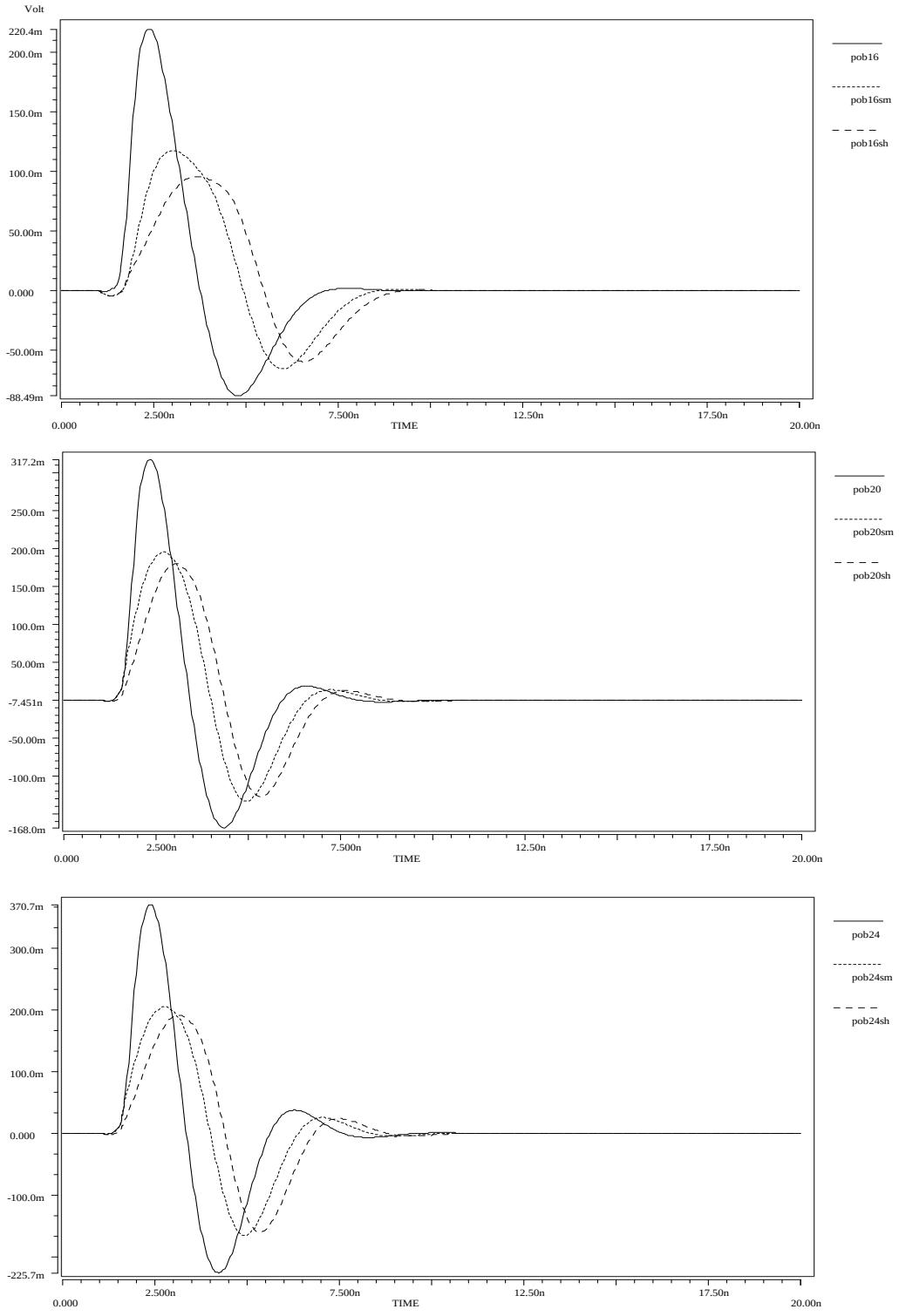


The following graphs show typical AC characteristics of non-slew and slew-rate output drives in STD80/STDM80. Using the slew-rate control, you can reduce the switching noise.

Figure 1-25. AC Characteristics of Non-Slew and Slew Rate Output Drives



Ground Bouncing Voltage vs. Time



Simultaneous Switching Outputs (SSOs)

If several output drivers switch from high to low simultaneously, the ground bouncing level becomes quite large because the current flowing through the inductance L is the total sum of the transient current of each output driver. The amount of total current and the level of ground bounce are proportional to the number of SSOs.

This ground bounce can cause two types of problems, a noise margin reduction and a generation of noise spike on the output pad.

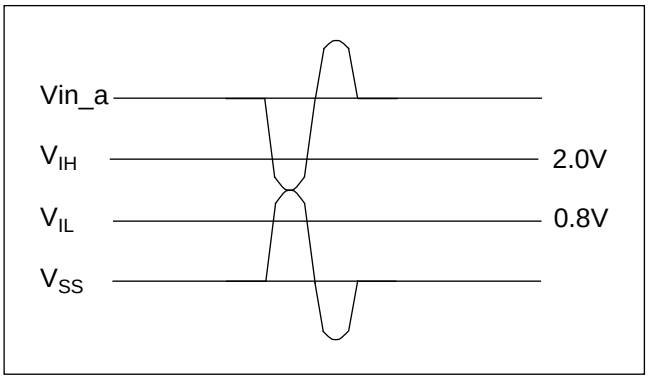
NOISE MARGIN REDUCTION

The ground bounce can cause a noise margin reduction when the same ground bus is used for both input buffers and output drivers as shown in Figure 1-27. The Figure of SSOs. The noise margin reduction can be explained using the circuit in the same figure.

As you can see, if outputs switch from high to low simultaneously, it results in a ground bounce or the rise of the chip ground level relative to system ground. The rise appears as the input voltage Vin_a is below V_{IH} causing false triggering of the input buffer. Vin is, in this case, not the same as Vin_a. Note that Vin is measured relative to the system ground, while Vin_a is measured relative to the local device ground.

This phenomenon is shown in Figure 1-26. Noise Margin Reduction due to SSOs. For a low-to-high transition, it is the low input levels (V_{IL}) that are affected.

Figure 1-26. Noise Margin Reduction due to SSOs

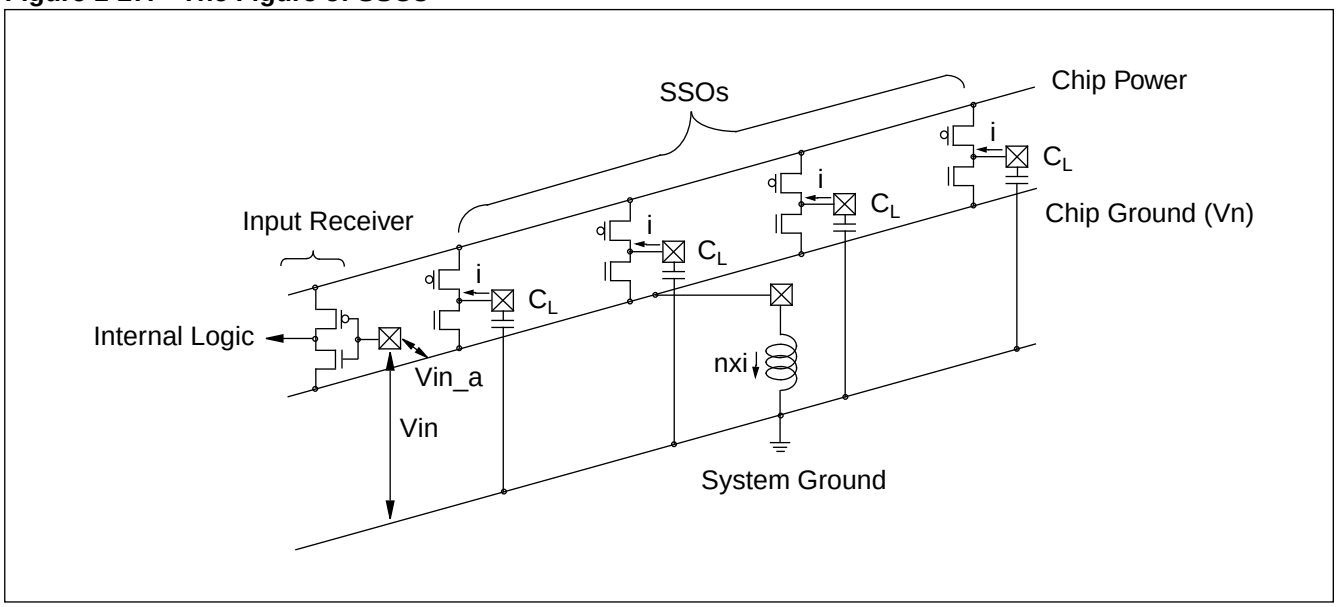


NOISE SPIKE GENERATION ON STABLE OUTPUT

If input and output power buses are separated, the problem of a noise margin reduction in the input buffer can be solved. However, ground bounce can cause another problem in spite of using separated power and ground bus.

The Figure 1-28. Noise Spike Induced by Ground Bounce shows a common octal driver application where ground bounce spikes will be observable on the one stable output. If the spike is considered as high by another chip, this ground bounce may upset that operation of interfacing device or cause system logic errors.

Figure 1-27. The Figure of SSOs



For example, suppose C_L = 100pF, V_{DD} = 3.3Volt, t_F = 5ns. From Figure 1-24. Ground Bounce Phenomenon, the maximum current flow occurs at time $0.5 \times t_F$. Then approximately,

$i = C_L \times (dv / dt) \cong C_L \times (\Delta V / \Delta t)$,
and

$i\ (max) = 100 \times 10^{-12} \times \{5 / (2.5 \times 10^{-9})\} = 200$ [mA].

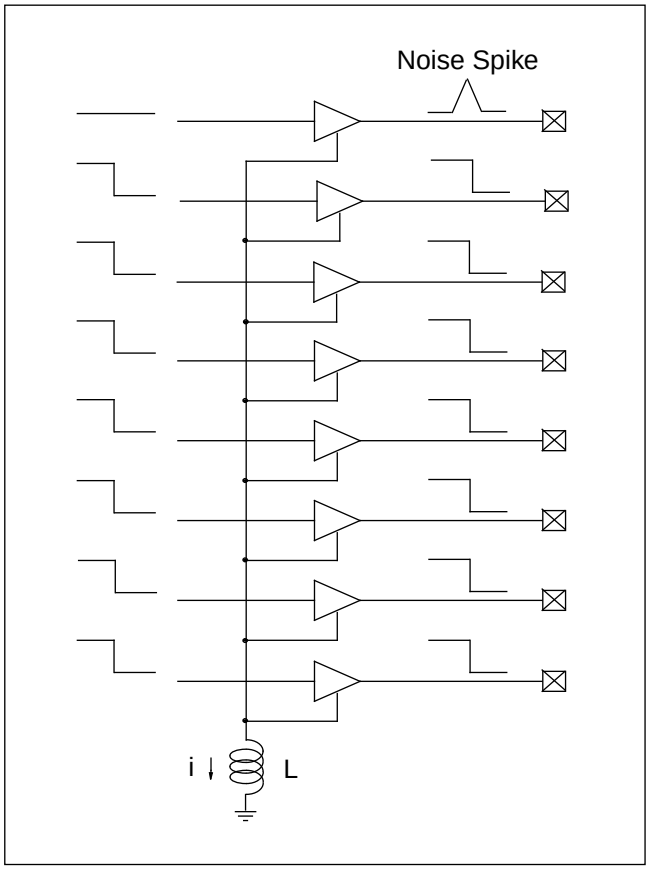
If the number of SSOs is 5, and L is 4nH,

$Vn = L \times (di / dt) \times N \cong L \times (\Delta i / \Delta t) \times N$ by approximation,

$Vn\ (max) = 4 \times 10^{-9} \times \{0.200 / (2.5 \times 10^{-9})\} \times 5 = 1.60$ [Volt].

From this calculation, 1.60V of noise spike is expected. This is about logic threshold voltage of TTL. This numerical estimate clearly shows that power bus noise control is one of the fundamental problems in a high-speed CMOS VLSI design. It is an important design consideration to prevent the noise from affecting the integrity of the logic operation of a chip.

Figure 1-28. Noise Spike Induced by Ground Bounce



How to Protect Ground Bounce?

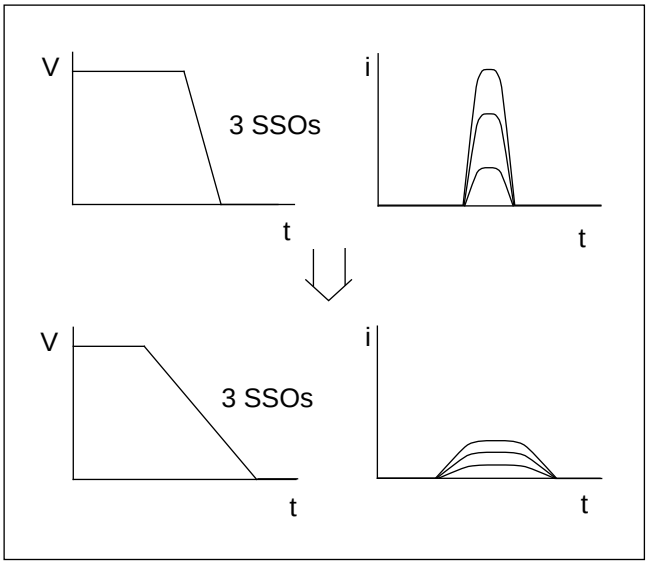
The fundamental solution to the ground bounce problem is to reduce the inductance of the package. However, in the boundary of a given packaging technology, the following guidelines can be used for reducing ground bounce:

(1) If possible, use separate power and ground buses for input buffers and output drivers.

(2) The number of ground and power pads should not be less than the required number of pads.

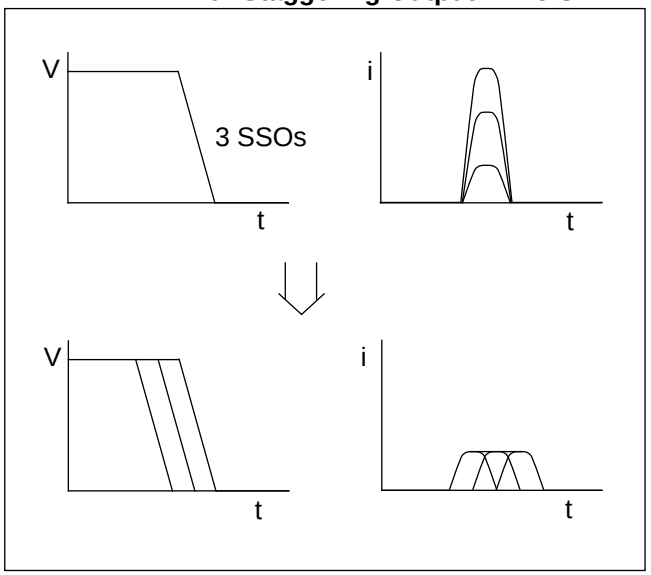
(3) If the design is not so much sensitive to speed, use slew rate control, i.e., increase switching time, to reduce the value of di / dt of an output driver. SEC supports two levels of slew rate controlled output buffers, SM and SH. You can see this effect in the following figure.

Figure 1-29. Effect on Reducing Peak Current with Slew-Rate Control



(4) If you cannot use a slew rate cell because of the speed requirement, you can stagger the output driver as shown in Figure 1-30. Effect on Reducing Peak Current with Staggering Output Drivers. This is not a general-purpose solution. It makes sense only when special relief in timing requirements exists from a system architecture.

Figure 1-30. Effect on Reducing Peak Current with Staggering Output Drivers



(5) High-drive outputs should be close to V_{SS} pins. SSOs should be placed particularly close to V_{SS} pins.

(6) SSOs should be appropriately placed in groups belonging to given V_{SS} pins.

(7) Noise-sensitive signals such as clock, asynchronous clear and preset should be located away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near V_{SS}, if one is available away from SSOs or high-drive outputs.

(8) Place SSOs on low inductance pins, such as those located on the inner rows or middle positions of PGAs.

(9) Clock, preset and clear inputs must not be placed on the corners of a package, especially when the array is packaged in DIP.

(10) Output signals to be used as clock, preset or clear for other devices must be kept away from SSOs and close to V_{SS} pin.

These guidelines assist you in choosing the best package(s) for the application. Furthermore, the recommendations about pinout results in reliable and predictable devices that minimizes harmful DC and AC effects on the system.

CRYSTAL OSCILLATOR CONSIDERATIONS

Overview

STD80/STDM80 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, anymore than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that SEC will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

Oscillator Design Considerations

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

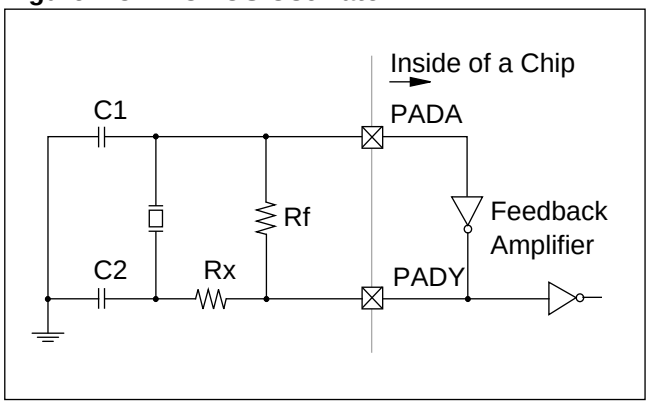
The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

ON-CHIP OSCILLATOR

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-31. CMOS Oscillator



CRYSTAL SPECIFICATIONS

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can’t be compensated for by appropriate selection of the capacitances, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking “ppm” tolerances with radio engineers and simply won’t take your order until you’ve filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don’t pay for 0.003% crystals if your actual frequency tolerance is 1%.

OSCILLATION FREQUENCY

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7 pF each.

Internal phase deviations capacitance of 25 to 30 pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

C1 / C2 SELECTION

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 20pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 20 and 100pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

RF / RX SELECTION

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-31. CMOS Oscillator.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

PIN CAPACITANCE

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a "pin capacitance", but more like an "equivalent output capacitance" of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

PLACEMENT OF COMPONENTS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

Troubleshooting Oscillator Problems

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.