IS82C600

TRAILBLAZER

High-Speed SRAM with Address Decoding and Ready Logic

PRELIMINARY
JANUARY 1999

FEATURES

- Zero wait-state performance on the Primary Bus
  - — Point-to-point interface between the SRAM and the high-speed processor
- Seamless interface to Texas Instruments' TMS320LC54x high-speed processor
- Integrates the single-ported SRAM with a dual-ported interface and handshake
  - — 9 ns access time to the SRAM
  - — Can also be used as a standalone, high-speed SRAM
- Integrates the port-to-port bridge function
  - — Broadcasts all processor cycles from Primary Bus to the Secondary Bus
  - — Programmability to only broadcast non-SRAM cycles to the Secondary Bus
  - — Supports older, slower peripheral devices on the Secondary Bus
  - — Allows the processor transparent access to the devices on the Secondary Bus through $\overline{XCVR}$ pin
  - — Supports a Boot ROM on the Secondary Bus
- Features Address Decoding and Ready Logic
  - — A total of six Chip Selects
  - — Supports "Ready" logic signal generation for memory and I/O
  - — Eliminates PALs for address decoding and ready logic
  - — No "glue logic" interface for local peripherals on the Secondary Bus processor
- Allows dynamic re-allocation of memory spaces for transparent block moves
  - — Programmable memory decoding allows memory blocks to be accessed as either Program Space ($\overline{PS}$) or Data Space ($\overline{DS}$)
  - — Programmable registers to map the internal SRAM memory and external secondary port devices into Data Space ($\overline{DS}$), Program Space ($\overline{PS}$) and I/O Space ($\overline{IS}$)
- Can also be used as a standalone, high-speed SRAM
- Allows the shadowing of the ROM on the Secondary Bus into the on-board SRAM

GENERAL DESCRIPTION

The IS82C600 TrailBlazer simplifies high-speed system design and layout, providing an SRAM with zero wait-state performance up to 90 MHz, address coding, and "Ready" logic. In many cases, TrailBlazer allows existing system designs to be easily upgraded, enabling the re-use of already available ASICs and glue logic.

A key benefit of the TrailBlazer device is its ability to relieve high-performance processors from a necessity to drive heavily loaded multidrop buses by providing a point-to-point, low-load interconnect to the high-speed memory and buffering of the slower speed devices. This could allow the processors to operate at a maximum frequency with zero wait-states. Also, it eases PCB timing and layout-related considerations, often allowing a reduction in the number of PC board layers and the lowering of noise. Programmable decodes and "Ready" generation logic built into the TrailBlazer eliminates the need for expensive PALs, other glue logic, and additional board space.

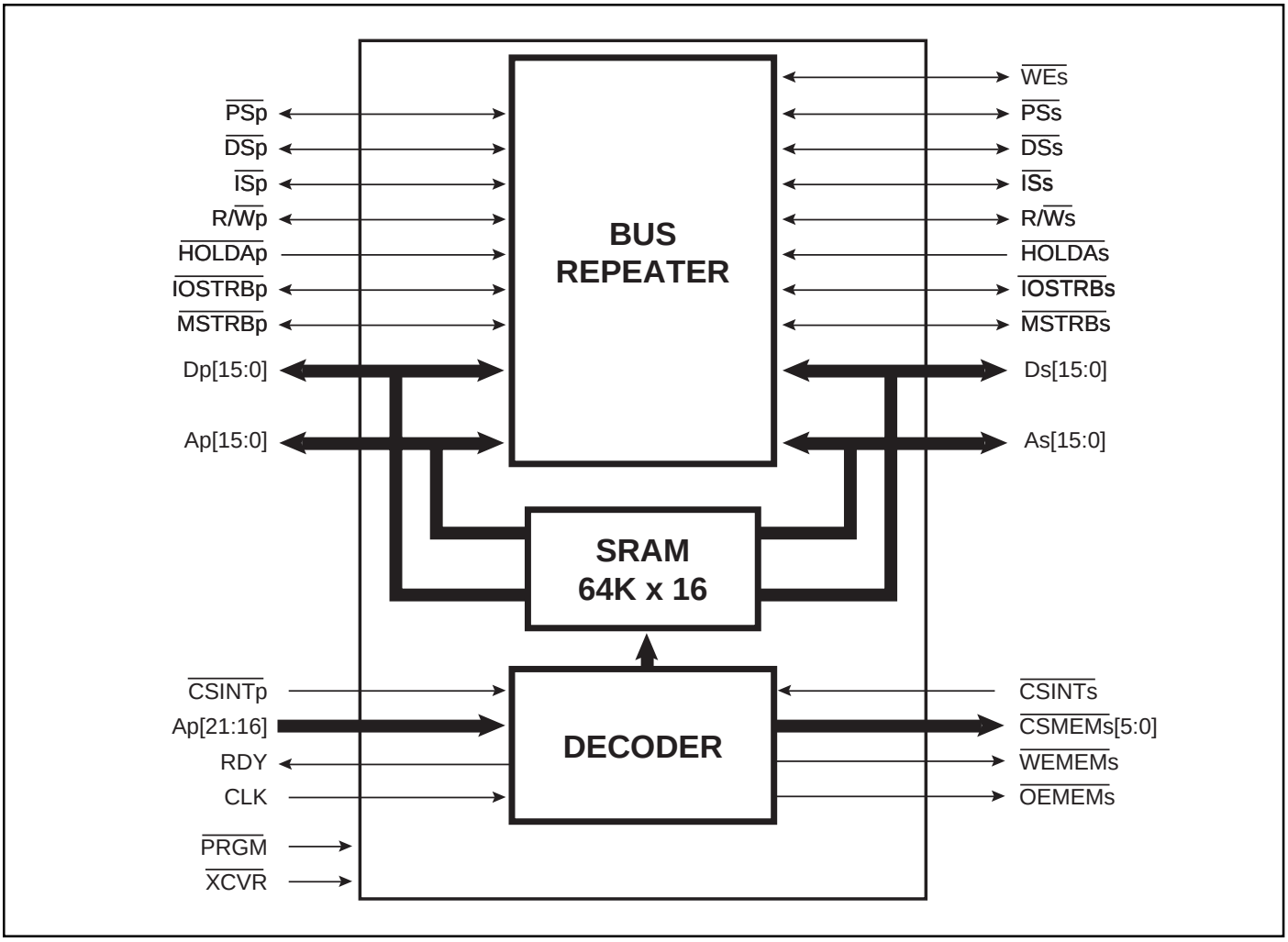


Figure 1. TrailBlazer Functional Block Diagram

PRODUCT OVERVIEW

The IS82C600 TrailBlazer integrates a high-speed 64K x 16 SRAM with a processor port-to-processor port bridge function. This simplifies any high-speed designs by providing a fast access time for the processor on the Primary Port and enabling for a low-cost implementation of a high-frequency system.

TrailBlazer combines a high-performance memory array, programmable decodes, and "Ready" logic to achieve maximum performance and flexibility, while keeping costs at a minimum. In order to simplify system development, TrailBlazer duplicates the Primary Bus signals on its Secondary Bus to permit the use of existing system components and ASICs together with a new generation of high-performance processors.

On its Primary Bus, the TrailBlazer provides a high-speed SRAM interface and then broadcasts the Primary Bus cycles to its Secondary Bus, allowing the processor on its Primary Bus to access peripherals on its Secondary Bus. In many cases, since the peripherals are accessed by the same signals, existing ASICs can be re-used.

TrailBlazer provides an optimized, seamless interface to TI TMS320LC54x high-speed processor without the need for any glue logic interfaces for local peripherals on the Secondary Bus. TrailBlazer can also be used as shared Local or Global Memory for a dual processor-based system where the Chip Select logic on each bus allows for the same data to be accessed at different locations in memory, if so desired.

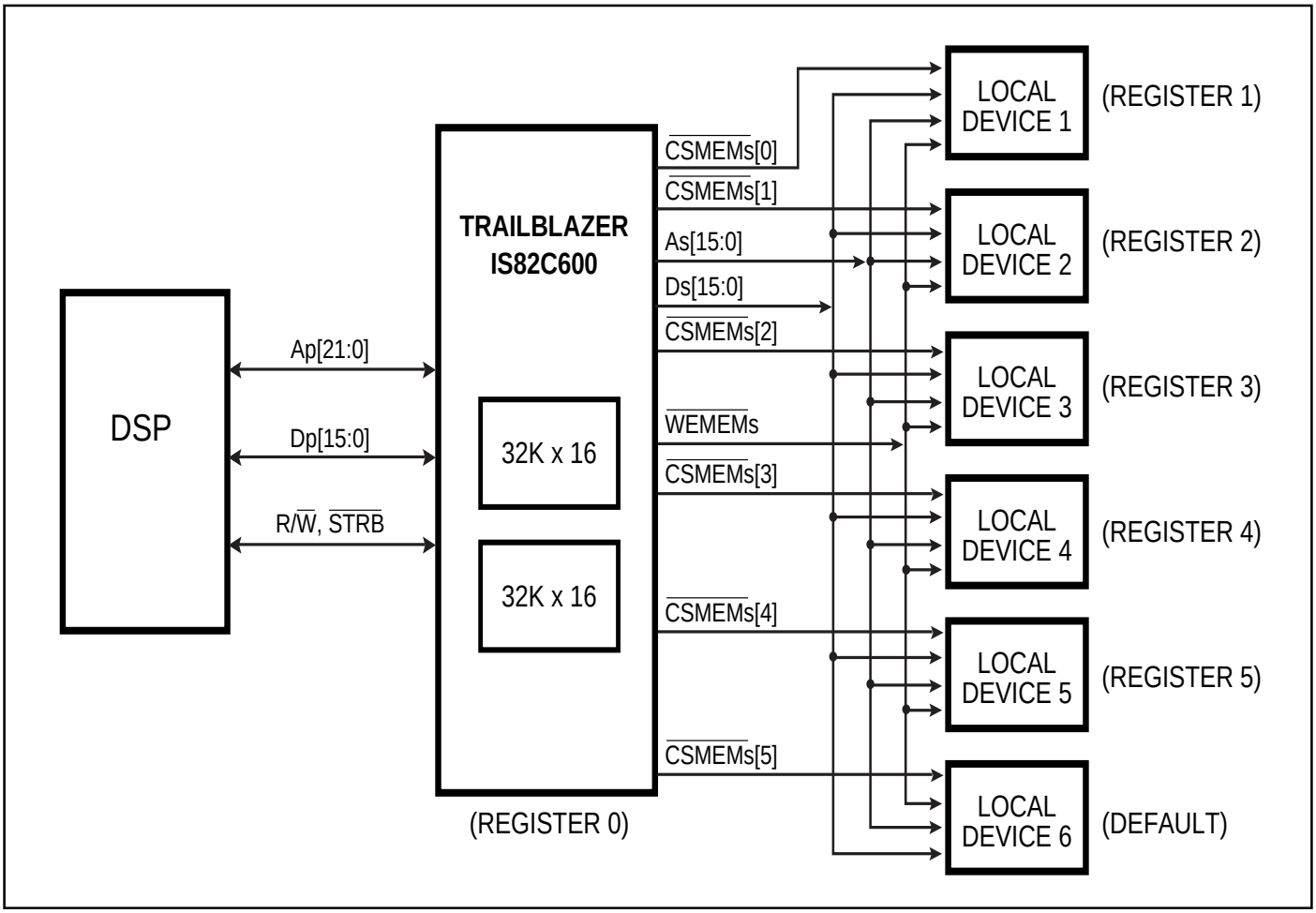


Figure 2. TrailBlazer System Block Diagram with High-Speed DSP on the Primary Bus and the Slower Existing DSP System Components on the Secondary Bus

PIN INFORMATION

Complete pin information on the device is organized as follows:

- Overview
- Conventions
- Pin Diagram
- Pin Assignment Table—Arranged by Pin Number
- Pin Assignment Table—Arranged by Ball Location
- Detailed Pin Descriptions

Overview

The R/$\overline{W}$ signal determines the direction of the bus transaction.

Some processors, including TI TMS320LC54X, have three major memory spaces. Program Space ($\overline{PS}$); Data Space ($\overline{DS}$); and I/O Space ($\overline{IS}$). The Memory Space signals ($\overline{DS}$, $\overline{PS}$, and $\overline{IS}$) select the memory address space being accessed (Data, Program, or I/O). No more than one of the Memory Space signals can be asserted at the same time. Data or Program spaces (or any part of these spaces) can be mapped into either internal SRAM of the TrailBlazer or any external devices. I/O space can only be mapped to external devices. The TrailBlazer's internal SRAM has two 32KB regions that are restricted to either $\overline{DS}$ or $\overline{PS}$ space.

Register 0 controls the decoding for the internal SRAM. Registers 1 through 5 control the address decoding for the external devices on the Secondary Bus. For processors that have A15 as the MSB, the three memory spaces are restricted to 64KB each. However, the registers do allow for programmable address ranges in 8KB blocks. For processors with A[21:16] as the MSB, there is a 4MB maximum address space that can be partitioned by programming Registers 1 to 5.

Chip Selects ($\overline{CSMEM}$x) are used to select external devices on the Secondary Bus. These signals are generated by combinations of the Memory Space signals and Addresses Ap[13:21].

Strobes ($\overline{MSTRB}$ and $\overline{IOSTRB}$) validate Memory Space selections. $\overline{PS}$ and $\overline{DS}$ have to be validated by the assertion of $\overline{MSTRB}$ and $\overline{IS}$ has to be validated by the assertion of $\overline{IOSTRB}$.

The following provides detailed technical information related to the pins on the device. For ease of reference, the pin information is presented in a table format arranged both by pin numbers and by pin names. A pin diagram has also been included to be used as a visual point of reference.

Conventions

Table 1 details conventions that are used to present information on the pins.

Table 1. Pin Conventions

Convention	Meaning
NC	This pin is reserved for ISSI, Inc. and must be left as a 'No Connect'
I	Input-only
O	Output-only
I/O	Input or Output (Bi-directional)
Power	Power pin
Ground	Ground pin
$\overline{SIGNAL}$	Active (or asserted) state occurs when pin is at a low voltage
/	Multiplexed or Dual functionality

Pin Diagram

Refer to Figure 3 and Table 2 for the pin diagram for the TrailBlazer device. It depicts the pin names and the corresponding ball location. Pins marked as 'NC' are not available and are defined as 'No Connect' pins. For more detailed information on the pins refer to Table 5.

Table 2. Pin Configuration: 119-pin PBGA

	1	2	3	4	5	6	7
A	Ap18	Ap16	Ap4	Ap5	Ap11	$\overline{\text{XCVR}}$	$\overline{\text{ISp}}$
B	Ap19	Ap17	Ap3	Ap6	Ap12	$\overline{\text{PSp}}$	$\overline{\text{DSp}}$
C	Ap21	Ap20	Ap2	Ap7	Ap13	Dp0	Dp1
D	Ds1	Ds0	Ap1	Ap8	Ap14	Dp2	Dp3
E	Ds3	Ds2	Ap0	Ap9	Ap15	Dp4	Dp5
F	Ds4	GND	GND_Q	Ap10	GND_Q	V_{CC}	Dp6
G	Ds7	Ds6	Ds5	Dp7	$\overline{\text{HOLDAp}}$	$\overline{\text{CSINTp}}$	R/$\overline{\text{W}}$p
H	CLK	GND_Q	RDY	V_{CCQ}	$\overline{\text{RDp}}$	GND_Q	$\overline{\text{IOSTRBp}}$
J	Ds8	$\overline{\text{OEMEMs}}$	V_{CCQ}	V_{CCQ}	$\overline{\text{WEs}}$	$\overline{\text{WEp}}$	$\overline{\text{MSTRBp}}$
K	Ds9	GND_Q	$\overline{\text{WEMEMs}}$	V_{CCQ}	$\overline{\text{IOSTRBs}}$	GND_Q	$\overline{\text{MSTRBs}}$
L	Ds10	Ds11	As1	As7	$\overline{\text{CSINTs}}$	R/$\overline{\text{W}}$s	$\overline{\text{RDs}}$
M	Ds12	Vcc	GND_Q	As8	GND_Q	GND	$\overline{\text{HOLDAs}}$
N	Ds13	Ds14	As2	As9	Dp10	Dp9	Dp8
P	Ds15	$\overline{\text{CSMEMs0}}$	As3	As10	Dp13	Dp12	Dp11
R	$\overline{\text{CSMEMs1}}$	$\overline{\text{CSMEMs2}}$	As4	As11	$\overline{\text{PRGM}}$	$\overline{\text{DSs}}$	Dp14
T	$\overline{\text{CSMEMs3}}$	$\overline{\text{CSMEMs5}}$	As5	As12	As15	$\overline{\text{ISs}}$	Dp15
U	$\overline{\text{CSMEMs4}}$	As0	As6	As13	As14	$\overline{\text{PSs}}$	NC

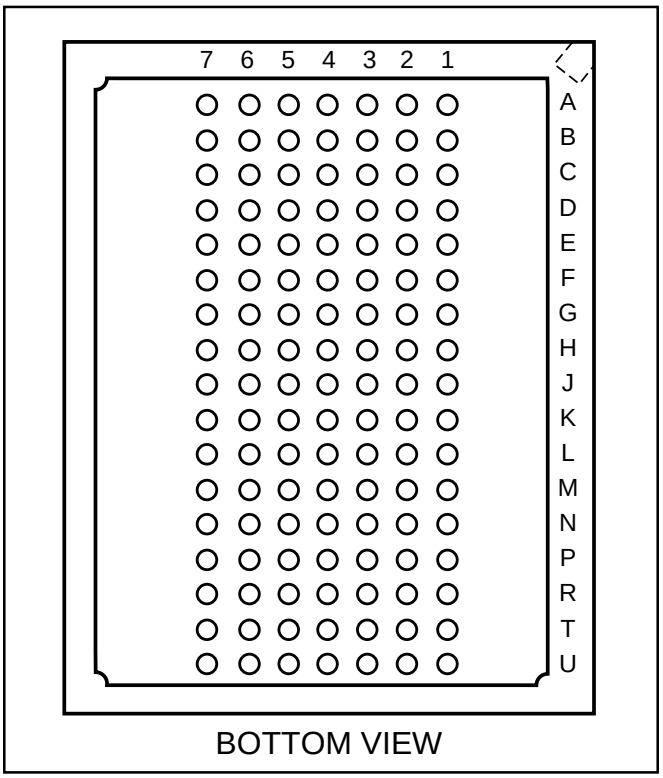


Figure 3. TrailBlazer Pin Diagram

Table 3. Pin Assignment Table—Arranged by Pin Name in Alphabetical Order

Pin Name	Ball Location	Pin Type
Ap0	E3	I/O
Ap1	D3	I/O
Ap2	C3	I/O
Ap3	B3	I/O
Ap4	A3	I/O
Ap5	A4	I/O
Ap6	B4	I/O
Ap7	C4	I/O
Ap8	D4	I/O
Ap9	E4	I/O
Ap10	F4	I/O
Ap11	A5	I/O
Ap12	B5	I/O
Ap13	C5	I/O
Ap14	D5	I/O
Ap15	E5	I/O
Ap16	A2	I
Ap17	B2	I
Ap18	A1	I
Ap19	B1	I
Ap20	C2	I
Ap21	C1	I
As0	U2	I/O
As1	L3	I/O
As2	N3	I/O
As3	P3	I/O
As4	R3	I/O
As5	T3	I/O
As6	U3	I/O
As7	L4	I/O
As8	M4	I/O
As9	N4	I/O
As10	P4	I/O
As11	R4	I/O
As12	T4	I/O
As13	U4	I/O
As14	U5	I/O
As15	T5	I/O
CLK	H1	I
$\overline{\text{CSINTp}}$	G6	I

Pin Name	Ball Location	Pin Type
$\overline{\text{CSINTs}}$	L5	I
$\overline{\text{CSMEMs0}}$	P2	O
$\overline{\text{CSMEMs1}}$	R1	O
$\overline{\text{CSMEMs2}}$	R2	O
$\overline{\text{CSMEMs3}}$	T1	O
$\overline{\text{CSMEMs4}}$	U1	O
$\overline{\text{CSMEMs5}}$	T2	O
Dp0	C6	I/O
Dp1	C7	I/O
Dp2	D6	I/O
Dp3	D7	I/O
Dp4	E6	I/O
Dp5	E7	I/O
Dp6	F7	I/O
Dp7	G4	I/O
Dp8	N7	I/O
Dp9	N6	I/O
Dp10	N5	I/O
Dp11	P7	I/O
Dp12	P6	I/O
Dp13	P5	I/O
Dp14	R7	I/O
Dp15	T7	I/O
Ds0	D2	I/O
Ds1	D1	I/O
Ds2	E2	I/O
Ds3	E1	I/O
Ds4	F1	I/O
Ds5	G3	I/O
Ds6	G2	I/O
Ds7	G1	I/O
Ds8	J1	I/O
Ds9	K1	I/O
Ds10	L1	I/O
Ds11	L2	I/O
Ds12	M1	I/O
Ds13	N1	I/O
Ds14	N2	I/O
Ds15	P1	I/O
$\overline{\text{DSp}}$	B7	I/O

Table 3. Pin Assignment Table—Arranged by Pin Name in Alphabetical Order *(continued)*

Pin Name	Ball Location	Pin Type
$\overline{DSs}$	R6	I/O
GND	F2	Ground
GND	M6	Ground
GND_Q	F3	Ground
GND_Q	F5	Ground
GND_Q	H2	Ground
GND_Q	H6	Ground
GND_Q	K2	Ground
GND_Q	K6	Ground
GND_Q	M3	Ground
GND_Q	M5	Ground
$\overline{HOLDAp}$	G5	I
$\overline{HOLDAs}$	M7	I
$\overline{IOSTRBp}$	H7	I/O
$\overline{IOSTRBs}$	K5	I/O
$\overline{ISp}$	A7	I/O
$\overline{ISs}$	T6	I/O
$\overline{MSTRBp}$	J7	I/O
$\overline{MSTRBs}$	K7	I/O
NC	U7	
$\overline{OEMEMs}$	J2	O
$\overline{PRGM}$	R5	I
$\overline{PSp}$	B6	I/O
$\overline{PSs}$	U6	I/O
$\overline{RDp}$	H5	I/O
$\overline{RDs}$	L7	I/O
R/$\overline{W}$p	G7	I/O
R/$\overline{W}$s	L6	I/O
RDY	H3	O
V_{CC}	F6	Power
V_{CC}	M2	Power
V_{CCQ}	H4	Power
V_{CCQ}	J3	Power
V_{CCQ}	J4	Power
V_{CCQ}	K4	Power
$\overline{WEMEMs}$	K3	O
$\overline{WEp}$	J6	I/O
$\overline{WEs}$	J5	I/O
$\overline{XCVR}$	A6	I

Table 4. Pin Assignment Table—Arranged by Ball Location in Alphabeltical Order

Pin Name	Ball Location	Pin Type
Ap18	A1	I
Ap16	A2	I
Ap4	A3	I/O
Ap5	A4	I/O
Ap11	A5	I/O
$\overline{XCVR}$	A6	I
$\overline{ISp}$	A7	I/O
Ap19	B1	I
Ap17	B2	I
Ap3	B3	I/O
Ap6	B4	I/O
Ap12	B5	I/O
$\overline{PSp}$	B6	I/O
$\overline{DSp}$	B7	I/O
Ap21	C1	I
Ap20	C2	I
Ap2	C3	I/O
Ap7	C4	I/O
Ap13	C5	I/O
Dp0	C6	I/O
Dp1	C7	I/O
Ds1	D1	I/O
Ds0	D2	I/O
Ap1	D3	I/O
Ap8	D4	I/O
Ap14	D5	I/O
Dp2	D6	I/O
Dp3	D7	I/O
Ds3	E1	I/O
Ds2	E2	I/O
Ap0	E3	I/O
Ap9	E4	I/O
Ap15	E5	I/O
Dp4	E6	I/O
Dp5	E7	I/O
Ds4	F1	I/O
GND	F2	Ground
GND_Q	F3	Ground
Ap10	F4	I/O

Table 4. Pin Assignment Table—Arranged by Ball Location in Alphabeltical Order *(continued)*

Pin Name	Ball Location	Pin Type
GND_Q	F5	Ground
V_{CC}	F6	Power
Dp6	F7	I/O
Ds7	G1	I/O
Ds6	G2	I/O
Ds5	G3	I/O
Dp7	G4	I/O
$\overline{HOLDAp}$	G5	I
$\overline{CSINTp}$	G6	I
R/$\overline{W}$p	G7	I/O
CLK	H1	I
GND_Q	H2	Ground
RDY	H3	O
V_{CCQ}	H4	Power
$\overline{RDp}$	H5	I/O
GND_Q	H6	Ground
$\overline{IOSTRBp}$	H7	I/O
Ds8	J1	I/O
$\overline{OEMEMs}$	J2	O
V_{CCQ}	J3	Power
V_{CCQ}	J4	Power
$\overline{WEs}$	J5	I/O
$\overline{WEp}$	J6	I/O
$\overline{MSTRBp}$	J7	I/O
Ds9	K1	I/O
GND_Q	K2	Ground
$\overline{WEMEMs}$	K3	O
V_{CCQ}	K4	Power
$\overline{IOSTRBs}$	K5	I/O
GND_Q	K6	Ground
$\overline{MSTRBs}$	K7	I/O
Ds10	L1	I/O
Ds11	L2	I/O
As1	L3	I/O
As7	L4	I/O
$\overline{CSINTs}$	L5	I
R/$\overline{W}$s	L6	I/O
$\overline{RDs}$	L7	I/O
Ds12	M1	I/O
V_{CC}	M2	Power

Pin Name	Ball Location	Pin Type
GND_Q	M3	Ground
As8	M4	I/O
GND_Q	M5	Ground
GND	M6	Ground
$\overline{HOLDAs}$	M7	I
Ds13	N1	I/O
Ds14	N2	I/O
As2	N3	I/O
As9	N4	I/O
Dp10	N5	I/O
Dp9	N6	I/O
Dp8	N7	I/O
Ds15	P1	I/O
$\overline{CSMEMs0}$	P2	O
As3	P3	I/O
As10	P4	I/O
Dp13	P5	I/O
Dp12	P6	I/O
Dp11	P7	I/O
$\overline{CSMEMs1}$	R1	O
$\overline{CSMEMs2}$	R2	O
As4	R3	I/O
As11	R4	I/O
$\overline{PRGM}$	R5	I
$\overline{DSs}$	R6	I/O
Dp14	R7	I/O
$\overline{CSMEMs3}$	T1	O
$\overline{CSMEMs5}$	T2	O
As5	T3	I/O
As12	T4	I/O
As15	T5	I/O
$\overline{ISs}$	T6	I/O
Dp15	T7	I/O
$\overline{CSMEMs4}$	U1	O
As0	U2	I/O
As6	U3	I/O
As13	U4	I/O
As14	U5	I/O
$\overline{PSs}$	U6	I/O
NC	U7	—

Table 5. Primary Bus Pins

Pin Name	Pin Type	Pin Description
Ap[15:0]	I/O	**ADDRESS:** Primary Bus address pins. The Ap[21] is the MSB and Ap[0] is the LSB.
Ap[21:16]	I	
CLK	I	**CLOCK SIGNAL (Primary):** This is the high-speed clock from the processor. Used for generation of RDY signal.
$\overline{\text{CSINTp}}$	I	**INTERNAL SRAM CHIP SELECT SIGNAL (Primary):** When asserted, the SRAM access is guaranteed from the Primary Bus, irrespective of the configuration mode.
Dp[15:0]	I/O	**DATA:** Data pins Dp[15] (MSB) through Dp[0] (LSB) connected to the processor on the Primary Bus.
$\overline{\text{DSp}}$	I/O	**DATA SPACE SIGNAL (Primary):** When asserted, indicates processor is accessing the Data Space ($\overline{\text{DS}}$) memory. It also validates address information on Ap[21:0].
$\overline{\text{HOLDAp}}$	I	**HOLD ACKNOWLEDGE SIGNAL (Primary):** $\overline{\text{HOLDAp}}$, when asserted, indicates that the processor or MPU on the Primary Bus is in a Hold state. This also indicates that Ap[21:0] and Dp[15:0] are tri-stated. Typically, this signal is used in dual-processor configurations where access to the internal SRAM is guaranteed for the processor on the Secondary Bus.
$\overline{\text{IOSTRBp}}$	I/O	**I/O STROBE (Primary):** When asserted, indicates a Primary Bus access to I/O devices.
$\overline{\text{ISp}}$	I/O	**I/O SPACE SIGNAL (Primary):** When asserted, indicates that processor is accessing the I/O Space ($\overline{\text{IS}}$). It also validates the address.
$\overline{\text{MSTRBp}}$	I/O	**MEMORY STROBE (Primary):** When asserted, indicates bus access to data or program memory.
$\overline{\text{PSp}}$	I/O	**PROGRAM SPACE SIGNAL (Primary):** When asserted, indicates processor is communicating with Program Space ($\overline{\text{PS}}$) memory. It also validates the address.
$\overline{\text{RDp}}$	I/O	This pin should be pulled HIGH.
R/$\overline{\text{W}}$p	I/O	**READ/WRITE SIGNAL (Primary):** R/$\overline{\text{W}}$ indicates transfer direction during access from Primary Bus. Set HIGH for a Read and LOW for a Write access.
$\overline{\text{WEp}}$	I/O	This pin should be pulled HIGH.

Table 6. Secondary Bus Pins

Pin Name	Pin Type	Pin Description
As[15:0]	I/O	**ADDRESS:** Secondary Bus address pins. As[15] is the MSB and As[0] is the LSB.
$\overline{\text{CSINTs}}$	I	**INTERNAL SRAM CHIP SELECT SIGNAL (Secondary):** When asserted, the SRAM access is guaranteed from the Secondary Bus (if $\overline{\text{HOLDAp}}$ = 0), irrespective of the configuration mode.
$\overline{\text{CSMEMs[5:0]}}$	O	**EXTERNAL MEMORY CHIP SELECTS (Secondary):** Selects devices on the Secondary Bus. Refer to the Register Definition Section for more details.
$\overline{\text{DSs}}$	I/O	**DATA SPACE SIGNAL (Secondary):** When asserted, indicates processor is accessing the Data Space ($\overline{\text{DS}}$) memory. It also validates address information on As[15:0].
$\overline{\text{HOLDAs}}$	I	**HOLD ACKNOWLEDGE SIGNAL (Secondary):** $\overline{\text{HOLDAs}}$, when asserted, indicates that the processor or MPU on the Secondary Bus is in a Hold state. This also indicates that As[15:0] and Ds[15:0] are tri-stated. Typically, this signal is used in dual-processor configurations where access to the internal SRAM is guaranteed for the processor on the Secondary Bus.
$\overline{\text{IOSTRBs}}$	I/O	**I/O STROBE (Secondary):** When asserted, indicates a Secondary Bus access to I/O devices.
$\overline{\text{ISs}}$	I/O	**I/O SPACE SIGNAL (Secondary):** When asserted, indicates that processor is accessing the I/O space ($\overline{\text{IS}}$). It also validates the address.
$\overline{\text{MSTRBs}}$	I/O	**MEMORY STROBE (Secondary):** When asserted, indicates bus access to data or program memory.
$\overline{\text{PSs}}$	I/O	**PROGRAM SPACE SIGNAL (Secondary):** When asserted, indicates processor is communicating with Program Space ($\overline{\text{PS}}$) memory. It also validates the address.
$\overline{\text{RDs}}$	I/O	This pin should be pulled HIGH.
R/$\overline{\text{Ws}}$	I/O	**READ/WRITE SIGNAL (Secondary):** R/$\overline{\text{W}}$ indicates transfer direction during access from Secondary Bus. Set HIGH for a Read access and LOW for a Write access.
$\overline{\text{WEs}}$	I/O	This should be pulled HIGH.
$\overline{\text{WEMEMs}}$	O	**EXTERNAL MEMORY WRITE ENABLE:** This is the memory Write Enable signal for external memory or peripherals on the Secondary Bus.

Table 7. Miscellaneous Pins

Pin Name	Pin Type	Pin Description
$\overline{\text{PRGM}}$	I	**PROGRAM ENABLE:** This signal latches the Secondary Address Bus, As[15:0], on its rising edge. Typically, the $\overline{\text{PRGM}}$ is derived from $\overline{\text{RESET}}$ so that upon power-up, the state of As[15:0] is latched. As[15:8] determine the mode of internal SRAM decode and external memory decoding for the Secondary Bus. (See Register Descriptions for more detail.)
RDY	O	RDY is asserted whenever a Secondary Bus device is able to communicate with the TrailBlazer. RDY is programmed in Register 6 for various $\overline{\text{DS}}$, $\overline{\text{IS}}$, and $\overline{\text{PS}}$ memory address spaces.
$\overline{\text{XCVR}}$	I	**TRANSCEIVER MODE:** This pin puts the TrailBlazer into a transceiver-like mode to support the processor's DMA through the TrailBlazer, e.g., when a Primary Bus wants to read the data on the Secondary Bus. In this mode, the $\overline{\text{XCVR}}$ is asserted, and the $\overline{\text{HOLDAs}}$ pin must be LOW, indicating no processors are on the Secondary Bus and the Primary Bus processor can read from the peripheral (or memory) from the Secondary Bus. (See Table 8, Bus Logic Truth Table for every possible combination.)
V_{CCQ}	Power	Power pins for I/O buffers of TrailBlazer.
GND_Q	Ground	Ground pins for I/O buffers of TrailBlazer.
V_{CC}	Power	Power pins for core of TrailBlazer.
GND	Ground	Ground pins for core of TrailBlazer

Note: 1. Typically, V_{CC} and V_{CCQ} are at 3.3 Volts.

Table 8. Bus Logic Truth Table

XCVR	HOLDAp	HOLDAs	CSINTp	CSINTs	Action	CSMEMs[5:0]
0	0	X	X	X	Transceiver R/W of Primary Bus by Secondary Bus (DMA).	CSMEMs[5:0] are not asserted. .
0	1	X	X	X	Transceiver R/W of Secondary Bus by Primary Bus (DMA).	CSMEMs[5:0] are not asserted.
1	0	X	X	0	R/W of Internal SRAM by the Secondary Bus only.	CSMEMs[5:0] are not asserted
1	1	0	0	X	R/W of Internal SRAM by the Primary Bus only.	CSMEMs[5:0] are not asserted
1	1	0	1	X	Primary Bus is in control. R/W from external or internal memory by Primary Bus. Control signals are forward to the Secondary Bus.	One of CSMEMs[5:0] asserted, depending on Ap[21:13] and PSp, DSp and ISp.
1	1	1	0	X	R/W of Internal SRAM by the Primary Bus only. Control signals are not forwarded to the Secondary Bus. Secondary Bus access to internal memory denied.	CSMEMs[5:0] are not asserted
1	1	1	1	X	R/W of internal SRAM by Primary Bus. Control signals are not forwarded to the Secondary Bus. Secondary Bus access to internal memory denied.	CSMEMs[5:0] are not asserted Internal SRAM selection is based on Ap[21:13], PSp and DSp

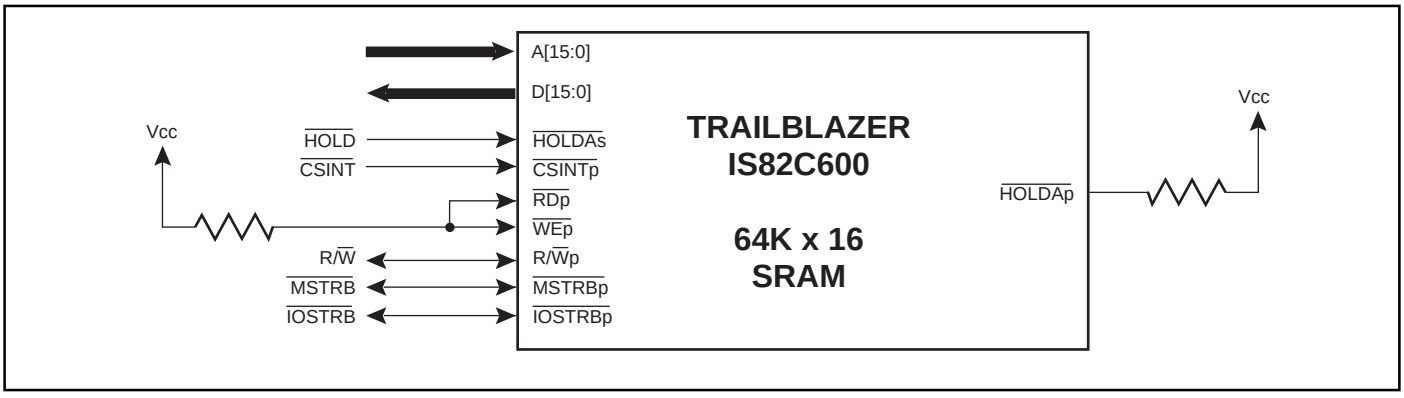


Figure 4. TrailBlazer Interface with TMS320LC54x DSP.

REGISTER DEFINITIONS

A set of I/O addresses is reserved in the system and is used for TrailBlazer registers. As[15:8], when sampled by the rising edge of PRGM, determine the displacement of the starting address for the registers from location 00. A block of 256 addresses from the starting address is not available for the system. For example, if As[15:8] are sampled as 80 (i.e., As[15] pulled HIGH and As[14:8] pulled LOW) the starting I/O address is 8000h and I/O address 8000h to(80+255)h are reserved. Register 0 of TrailBlazer maps to 80 and Register 1 maps to 81, and so on. Currently, eight registers are defined and the remaining registers are reserved.

All these registers will come up in their predetermined default states during power-up.

Upon power-up, the mode registers are loaded by sampling the As[15:0] (Secondary Address Bus). These bits are sampled on the rising edge of the PRGM. The PRGM pin can be controlled in several different ways. The simpliest method is to tie the pin to the RESET pulse of the processor. When PRGM is asserted, the entire chip will be tri-stated and, therefore, normal functionality cannot be maintained while this pin is active. If the system requires a “dynamic” decoding of the address bits, the XF pin from the processor can be used as a gate to the decoding latch.

Register 0

TrailBlazer SRAM Decode Register (default FFFF)

This register is used to set the base address for each of the two 32K x 16 blocks of TrailBlazer SRAM. Register 0 bits 6:0 are used for setting the starting address of a 32K block of SRAM and bit 7 determines if this block corresponds for PS or DS. When the DS/PS bit is 0, the block is in DS space and if 1, the block is in PS space. Similarly, bits 15:8 programs the other 32K block.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DS/PS	A21	A20	A19	A18	A17	A16	A15	DS/PS	A21	A20	A19	A18	A17	A16	A15

Register 1

CSMEMs0 Pin Select Register (default 0008)

This register is used to select the decoding for CSMEMs0. The decoding is on an 8K boundary and can be programmed to respond to PS, DS, or IS address space or a combination thereof. The CSMEMs0 can be used as a chip select pin for external memory or I/O device.

Register 1 bits D[14:6] are used to set the base address for which the decode occurs, bits 5:3 determine the space, PS, DS, or IS, and bits 2:0 determine the size of the decode. Bit 15 is a reserved bit. On power-up, the register will reset at the default state of 0008.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	A21	A20	A19	A18	A17	A16	A15	A14	A13	PS	DS	IS	SZ2	SZ1	SZ0

Bits 14 to 6 correspond to address bits A21 to A13 and sets the starting address for which CSMEMs0 is active.
Bits 5 to 3 determine the space for which the pin will be active which are encoded as follows:

Bits 2 to 0 determine the size for which CSMEMs0 will be active starting from address as determined by bits 14 to 6. RSRVD bit should always be programmed to ZERO.

$\overline{PS}$	$\overline{DS}$	$\overline{IS}$	Space for which $\overline{CSMEMs0}$ will be active
0	0	0	$\overline{CSMEMs0}$ will not respond to any space, i.e., disabled.
0	0	1	$\overline{CSMEMs0}$ will be asserted for I/O space (when $\overline{IS}$ asserted) as determined by the starting address and size bits.
0	1	0	$\overline{CSMEMs0}$ will be asserted for DATA space (when $\overline{DS}$ asserted) as determined by the starting address and size bits.
0	1	1	$\overline{CSMEMs0}$ will be asserted for I/O or DATA space (when $\overline{IS}$ or $\overline{DS}$ asserted) as determined by the starting address and size bits.
1	0	0	$\overline{CSMEMs0}$ will be asserted for PROGRAM space (when $\overline{PS}$ asserted) as determined by the starting address and size bits.
1	0	1	$\overline{CSMEMs0}$ will be asserted for PROGRAM or I/O space (when $\overline{PS}$ or $\overline{IS}$ asserted) as determined by the starting address and size bits.
1	1	0	$\overline{CSMEMs0}$ will be asserted for PROGRAM or DATA space (when $\overline{PS}$ or $\overline{DS}$ asserted) as determined by the starting address and size bits.
1	1	1	$\overline{CSMEMs0}$ will be asserted for any space as determined by the starting address and size bits.

SZ2	SZ1	SZ0	Size for which $\overline{CSMEMs0}$ will be active starting from the programmed starting address. The sizes are in the increments of 8K Words.
0	0	0	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 8K
0	0	1	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 16K
0	1	0	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 32K
0	1	1	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 64K
1	0	0	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 128K
1	0	1	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 256K
1	1	0	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 512K
1	1	1	$\overline{CSMEMs0}$ will be asserted for starting address to starting address + 1024K

Register 2

$\overline{CSMEMs1}$ Pin Select Register (default 0048):

This register is used to select the decoding for $\overline{CSMEMs1}$. The decoding is on an 8K boundary and can be programmed to respond to $\overline{PS}$, $\overline{DS}$, or $\overline{IS}$ address space or a combination thereof. The $\overline{CSMEMs0}$ can be used as chip select pin for external memory or I/O device. The bit descriptions and programmability are identical to Register 1, except that the default is 0048. Refer to $\overline{CSMEMs0}$ bit descriptions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	A21	A20	A19	A18	A17	A16	A15	A14	A13	$\overline{PS}$	$\overline{DS}$	$\overline{IS}$	SZ2	SZ1	SZ0

Register 3

$\overline{\text{CSMEMs2}}$ Pin Select Register (default 0088):

This register is used to select the decoding for $\overline{\text{CSMEM}}$s2. The decoding is on an 8K boundary and can be programmed to respond to $\overline{\text{PS}}$, $\overline{\text{DS}}$, or $\overline{\text{IS}}$ address space or a combination thereof. The $\overline{\text{CSMEM}}$s2 can be used as a chip select pin for external memory or I/O device. The bit descriptions and programmability are identical to Register 1, except that the default is 0088. Refer to $\overline{\text{CSMEM}}$s0 bit descriptions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	A21	A20	A19	A18	A17	A16	A15	A14	A13	$\overline{\text{PS}}$	$\overline{\text{DS}}$	$\overline{\text{IS}}$	SZ2	SZ1	SZ0

Register 4

$\overline{\text{CSMEMs3}}$ Pin Select Register (default 00C8):

This register is used to select the decoding for $\overline{\text{CSMEM}}$s3. The decoding is on an 8K boundary and can be programmed to respond to $\overline{\text{PS}}$, $\overline{\text{DS}}$, or $\overline{\text{IS}}$ address space or a combination thereof. The $\overline{\text{CSMEM}}$s3 can be used as a chip select pin for external memory or I/O device The bit descriptions and programmability are identical to Register 1, except that the default is 00C8. Refer to $\overline{\text{CSMEM}}$s0 bit descriptions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	A21	A20	A19	A18	A17	A16	A15	A14	A13	$\overline{\text{PS}}$	$\overline{\text{DS}}$	$\overline{\text{IS}}$	SZ2	SZ1	SZ0

Register 5

$\overline{\text{CSMEMs4}}$ Pin Select Register (default 0112):

This register is used to select the decoding for $\overline{\text{CSMEM}}$s4. The decoding is on an 8K boundary and can be programmed to respond to $\overline{\text{DS}}$ or $\overline{\text{IS}}$ address space or a combination thereof. The $\overline{\text{CSMEM}}$s4 can be used as a chip select pin for external memory or I/O device. The bit descriptions and programmability are identical to Register 1, except that the default is 0112. Refer to $\overline{\text{CSMEM}}$s0 bit descriptions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	A15	A14	A13	RSVD	$\overline{\text{DS}}$	$\overline{\text{IS}}$	RSVD	SZ1	SZ0

$\overline{\text{DS}}$	$\overline{\text{IS}}$	Space for which $\overline{\text{CSMEMs4}}$ will be active
0	0	$\overline{\text{CSMEMs0}}$ will not respond to any space, i.e., disabled.
0	1	$\overline{\text{CSMEMs0}}$ will go active for I/O space (when $\overline{\text{IS}}$ is active) as determined by the starting address and size bits.
1	0	$\overline{\text{CSMEMs0}}$ will go active for DATA space (when $\overline{\text{DS}}$ is active) as determined by the starting address and size bits.
1	1	$\overline{\text{CSMEMs0}}$ will go active for I/O or DATA space (when $\overline{\text{IS}}$ or $\overline{\text{DS}}$ is active) as determined by the starting address and size bits.

SZ1	SZ0	Size for which $\overline{\text{CSMEMs4}}$ will be active starting from the programmed starting address. The sizes are in the increments of 8K Words.
0	0	$\overline{\text{CSMEMs0}}$ will be active for starting address to starting address + 8K
0	1	$\overline{\text{CSMEMs0}}$ will be active for starting address to starting address + 16K
1	0	$\overline{\text{CSMEMs0}}$ will be active for starting address to starting address + 32K
1	1	$\overline{\text{CSMEMs0}}$ will be active for starting address to starting address + 64K

$\overline{\text{CSMEMs5}}$ Pin Select Register

This is a negative decode of the other chip selects, i.e., it is active when $\overline{\text{CSMEM}}$s[4:0] are HIGH.

\

Register 6

RDY Generation Logic and Write Control Register (default FFFF):

Register 6 is the signal RDY generation register for $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ space. $\overline{PS}$[4:0] (bits 4:0) determine the number of clocks after which the RDY is generated whenever $\overline{PS}$ goes active. Similarly, $\overline{DS}$[4:0] are used to program the RDY generation in number of clocks when $\overline{DS}$ is active and $\overline{IS}$[4:0] are used to generate the RDY for I/O cycles. The RDY signal could be used to delay an access to an external device on the Secondary Bus. Please note that if an external RDY has to be sampled by the processor, the processor's access should be programmed for at least two wait states.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$\overline{WE}$	IS4	IS3	IS2	IS1	IS0	DS4	DS3	DS2	DS1	DS0	PS4	PS3	PS2	PS1	PS0

Notes:
1. The above registers are read/writable.
2. No $\overline{CSMEMs}$ will be active if the I/O address of the registers matches with any $\overline{CSMEMs}$ decodes.

Table 9. Register Accessibility

Register Number	Register Address	Register Compare Data	Chip Select
0	Ap[15:8] = SA	Ap[21:15]; $\overline{DS}$p; $\overline{PS}$p	Internal SRAM
1	Ap[15:8] = SA+1	Ap[21:13]; $\overline{DS}$p; $\overline{PS}$p; Isp	$\overline{CSMEMs0}$
2	Ap[15:8] = SA+2	Ap[21:13]; $\overline{DS}$p; $\overline{PS}$p; $\overline{IS}$p	$\overline{CSMEMs1}$
3	Ap[15:8] = SA+3	Ap[21:13]; $\overline{DS}$p; $\overline{PS}$p; $\overline{IS}$p	$\overline{CSMEMs2}$
4	Ap[15:8] = SA+4	Ap[21:13]; $\overline{DS}$p; $\overline{PS}$p; $\overline{IS}$p	$\overline{CSMEMs3}$
5	Ap[15:8] = SA+5	Ap[15:13]; $\overline{DS}$p; $\overline{IS}$p	$\overline{CSMEMs4}$
6	Ap[15:8] = SA+6	$\overline{DS}$p; $\overline{PS}$p; $\overline{IS}$p	$\overline{CSMEMs5}$

Notes:
1. SA = Starting address as defined by As[15:8] on the rising edge of $\overline{PRGM}$.
2. Register write data: Dp[15:0].
3. Register write control: $\overline{IOSTRB}$p • (R/$\overline{W}$p) • $\overline{IS}$p. Some processors, including TI TMS320LC54X, have three major memory spaces. Program Space ($\overline{PS}$ signal); Data space ($\overline{DS}$ signal); and I/O space ($\overline{IS}$ signal). The TrailBlazer's internal SRAM has two 32KB regions that are restricted to either $\overline{DS}$ or $\overline{PS}$ space. Register 0 controls the decoding for the internal SRAM. Registers 1 through 5 control the address decoding for the external devices on the Secondary Bus. For processors that have A15 as the MSB, the three memory spaces are restricted to 64MB each. However, the registers do allow for programmable address ranges in 8KB blocks. For processors with A[21:16] as the MSB, there is a 4MB maximum address space that can be partitioned by programming Registers 1 to 5.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameters	Ratings	Units
V_{CC}	Supply Voltage	–0.4 to 4.1	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (Low)	20	mA

Note:
1. Stresses above the absolute maximum ratings can cause permanent damage to the device.

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.0V to 3.6V
Industrial	–40°C to +85°C	3.0V to 3.6V

DC Electrical Characteristics (Over Operating Range)

Symbol	Parameter	Test Conditona	Min	Max	Units
V_{OH}	Output High Voltage	Vcc = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output Low Voltage	Vcc = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input High Voltage		2.2	Vcc + 0.3	V
V_{IL}	Input Low Voltage(1)		0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–2	2	µA

Note:

1. V_{IL}(min) = –2.0V for pulse width less than 10 µs.

AC Specification: 25 pF Load
Internal SRAM Cycles Primary Bus Master

		-8		-9		-10		
T#	Parameter	Min	Max	Min	Max	Min	Max	Units
T1	Data Access Time from $\overline{RDp}$ LOW	—	5	—	5.5	—	6	ns
T2	Data Access Time from Address Valid (5X CPU)	—	8	—	9	—	10	ns
T3	Data Access Time from Address (54X CPU)	—	8	—	9	—	10	ns
T4	Data Access Time from $\overline{PS/DS/IS}$	—	8	—	9	—	10	ns
T5	Data Access Time from $\overline{MSTRBp}$	—	5	—	5.5	—	6	ns
T6	Data Access Time from $\overline{CSINTp}$	—	6	—	6.5	—	7	ns
T7	Address to $\overline{WEp}$ Valid	1	—	1	—	1	—	ns
T8	Write Data Setup Time before $\overline{WEp}$ HIGH	4	—	4	—	4	—	ns
T9	Write Data Hold Time after $\overline{WEp}$ HIGH	0	—	0	—	0	—	ns
T10	Write Data Setup Time before $\overline{MSTRB}$ HIGH	4	—	4	—	4	—	ns
T11	Write Data Hold Time after $\overline{MSTRB}$ HIGH	0	—	0	—	0	—	ns

Primary Bus Master Local Mode

T#	Parameter	Min	Max	Min	Max	Min	Max	Units
T12	$\overline{MSTRBp}$ / $\overline{IOSTRBp}$ Active to $\overline{OEMEMp}$ Active Delay	0	5	0	5.5	0	6	ns
T13	$\overline{WEp}$ Active to $\overline{WMEMp}$ Active Delay	0	5	0	5.5	0	6	ns
T14	$\overline{MSTRBp}$ / $\overline{IOSTRBp}$ Active to $\overline{WEMEMp}$ Delay	0	5	0	5.5	0	6	ns
T15	$\overline{PSp}$ / $\overline{DSp}$ / $\overline{ISp}$ Active to $\overline{CSMEMp}$[5:0] Delay	0	5	0	5.5	0	6	ns

Primary Bus Master Remote Mode (Non-$\overline{XCVR}$ Mode)

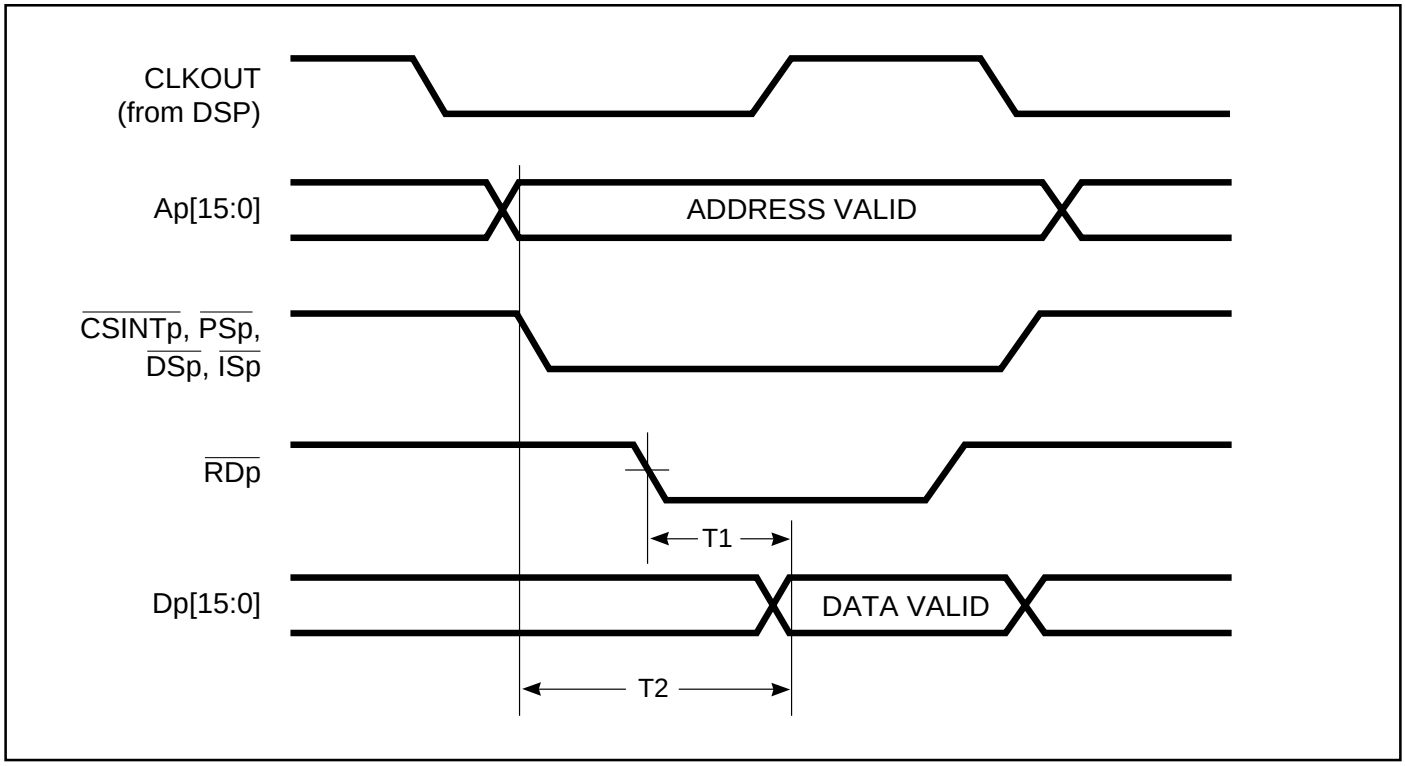
T#	Parameter	Min	Max	Min	Max	Min	Max	Units
T16	R/$\overline{W}$p, $\overline{PSp}$, $\overline{DSp}$, $\overline{ISp}$, $\overline{MSTRBp}$, $\overline{IOSTRBp}$, $\overline{RDp}$, $\overline{WEp}$ Delay to corresponding control signals on Secondary Bus	0	5	0	5.5	0	6	ns
T17	Dp to Ds Write Mode (R/$\overline{W}$=0)	0	5	0	5.5	0	6	ns
T18	Ds to Dp Read Mode (R/$\overline{W}$=1)	0	5	0	5.5	0	6	ns
T19	$\overline{MSTRBp}$ / $\overline{IOSTRBp}$ Active to $\overline{OEMEMs}$ Active Delay	0	5	0	5.5	0	6	ns
T20	$\overline{WEp}$ Active to $\overline{WEMEMs}$ Active Delay	0	5	0	5.5	0	6	ns
T21	$\overline{MSTRB}$ / $\overline{IOSTRBp}$ Active to $\overline{WEMEMs}$ Delay	0	5	0	5.5	0	6	ns
T22	$\overline{PSp}$ / $\overline{DSp}$ / $\overline{ISp}$ Active to $\overline{CSMEMs}$[5:0] Delay	0	5	0	5.5	0	6	ns

Primary Bus Master $\overline{XCVR}$ Mode

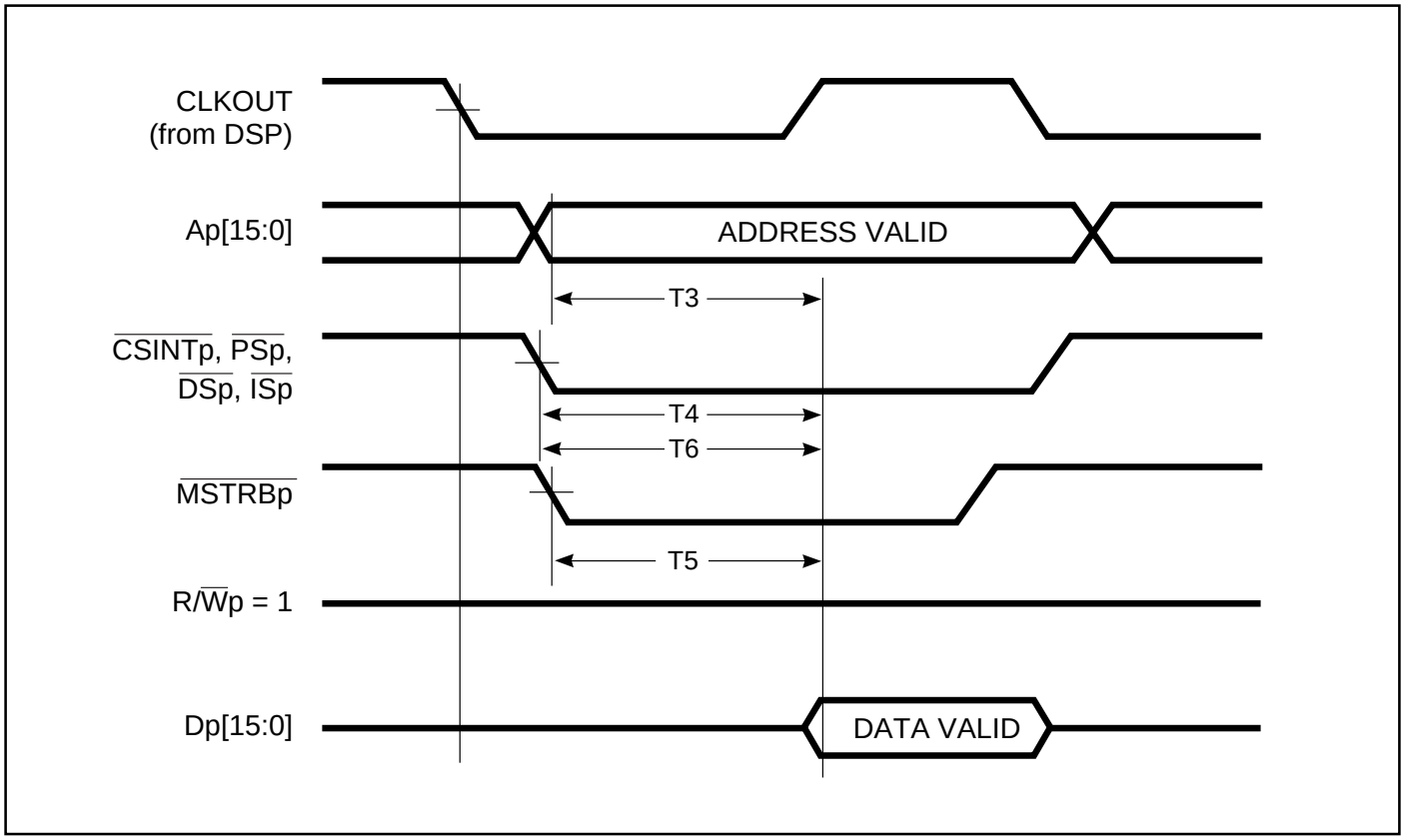
T#	Parameter	Min	Max	Min	Max	Min	Max	Units
T23	R/$\overline{W}$p, $\overline{PSp}$, $\overline{DSp}$, $\overline{ISp}$, $\overline{MSTRBp}$, $\overline{IOSTRBp}$, $\overline{RDp}$, $\overline{WEp}$ Delay to corresponding control signals on Secondary Bus	0	3	0	3	0	3	ns
T24	Ds to Dp Delay (R/$\overline{W}$=HIGH) Read from Secondary Bus	0	5	0	5.5	0	6	ns
T25	Dp to Ds Delay (R/$\overline{W}$=0) Write to Secondary Bus	0	5	0	5.5	0	6	ns

Note:
1. In the above list, the timing parameters are specified with the Primary Bus Master as the basis.

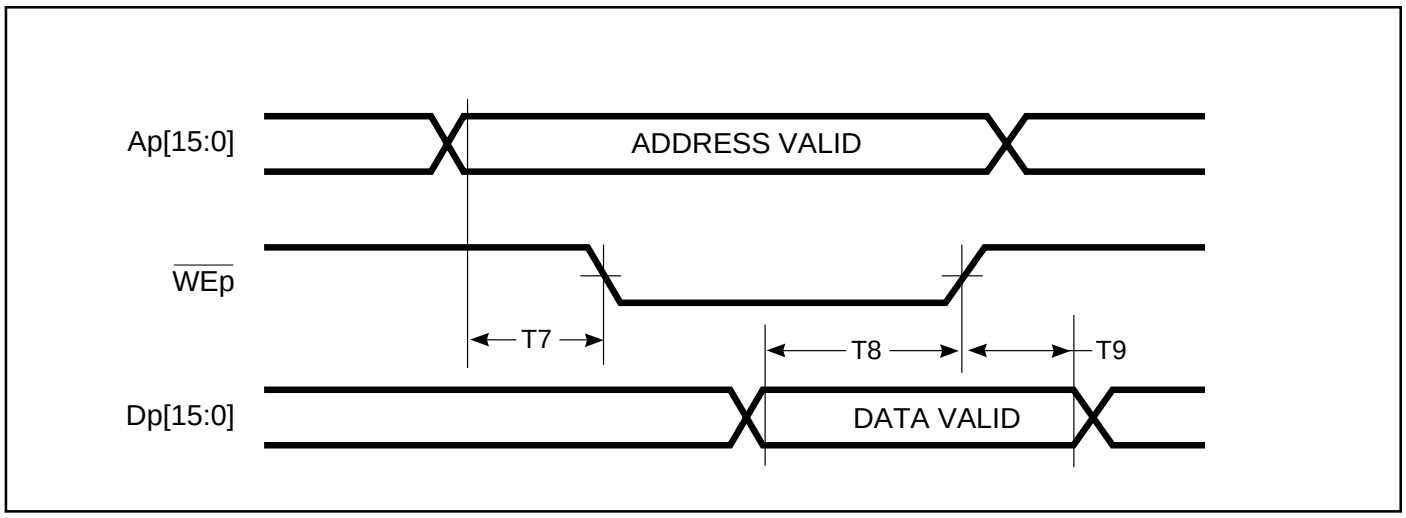
READ CYCLE 1: Primary Bus Internal SRAM READ Cycle Timing (TI TMS320LC5x/C5x DSP)



READ CYCLE 2: Primary Bus Internal SRAM READ Cycle Timing (TI TMS320LC54x/C54x DSP)

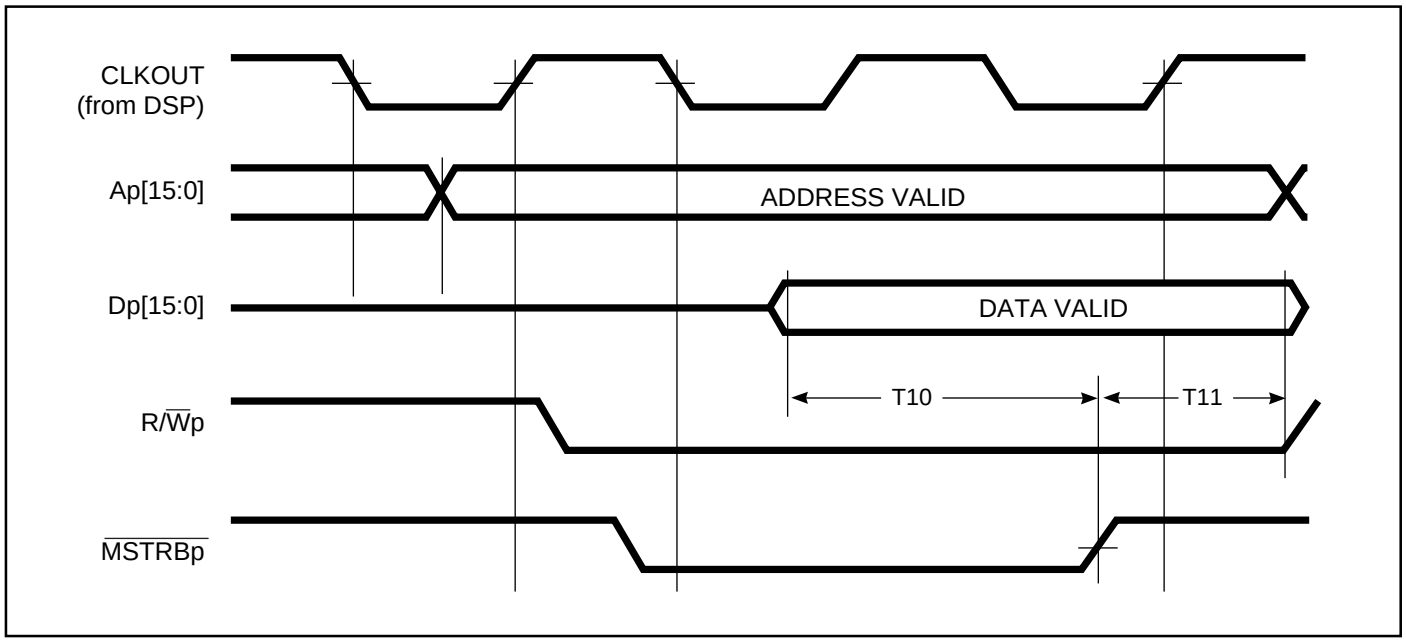


WRITE CYCLE 1: Primary Bus Internal SRAM WRITE Cycle Timing (TI TMS320LC5x/C5x DSP)



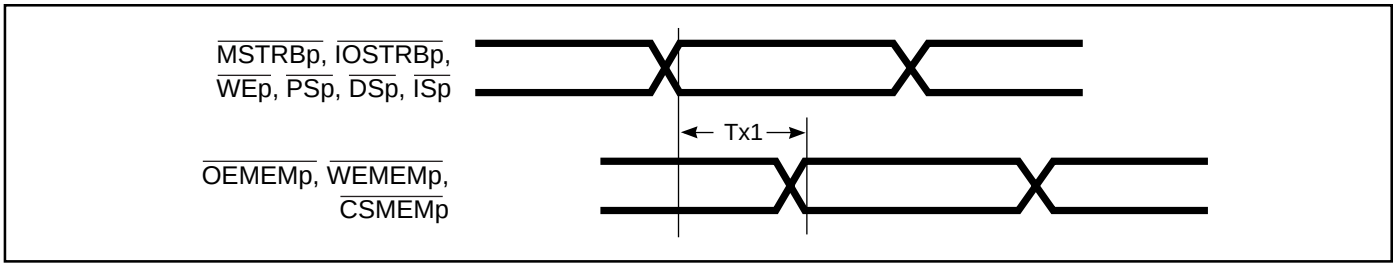
Note:
1. All timings are at zero wait state. However, external Writes require two cycles to prevent external bus conflicts. (Refer to the TI TMS320LC54x/C54x Databook.)

WRITE CYCLE 2: Primary Bus Internal SRAM WRITE Cycle Timing (TI TMS320LC54x/C54x DSP)



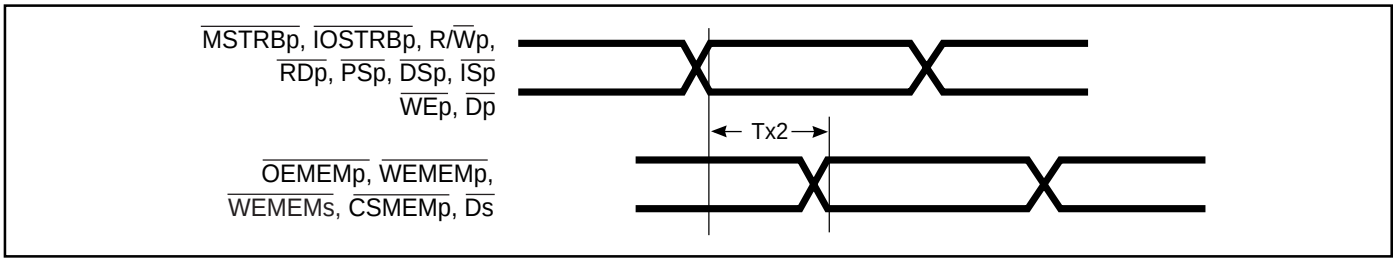
Note:
1. All timings are at zero wait state. However, external Writes require two cycles to prevent external bus conflicts. (Refer to the TI TMS320LC54x/C54x Databook.)

Primary Bus Control Signals for $\overline{\text{OEMEMp}}$, $\overline{\text{WEMEMp}}$, and $\overline{\text{CSMEMp}}$[5:0]



Note:
1. Tx1 = Timings from T12 through T15.

Primary Bus to Secondary Bus Delay



Note:
1. Tx2 = Timings from T16 through T25.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
8	IS82C600-8B	PBGA
9	IS82C600-9B	PBGA
10	IS82C600-10B	PBGA

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part Number	Package
8	IS82C600-8BI	PBGA
9	IS82C600-9BI	PBGA
10	IS82C600-10BI	PBGA

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