SIEMENS

ICs for Communications

PCI Interface for Telephony/Data Applications
PITA

PSB 4600 Version 1.2

Preliminary Data Sheet 12.98

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Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
all	all	New release in Information Mapping®

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Organization of this Data Sheet

This Preliminary Data Sheet is divided into 13 chapters:

- **Chapter 1, Features**
  Describes the compliants, interfaces and the compatibilities of the PITA.

- **Chapter 2, Applications realized with the PITA**
  Describes the applications realized with the PITA.

- **Chapter 3, Construction of the PITA**
  Shows a block diagram and describes the interfaces and their functions.

- **Chapter 4, Communication with the PITA**
  Describes the different controllers, registers and the power management of the PITA.

- **Chapter 5, Communication with external Components**
  Gives a general description of the interfaces and modes of the PITA.

- **Chapter 6, Configuration of the PITA**
  Describes the pinstrapping and pins used for pinstrapping during system reset.

- **Chapter 7, Pinning**
  Describes the pins, types of pins and the characteristics of the interfaces.

- **Chapter 8, Package Outlines**
  Describes the package outlines.

- **Chapter 9, Precaution**s
  Describes electrical maximum ratings and electrical characteristics.

- **Chapter 10, Configuration Space Register of the PITA**
  Contains maps and descriptions of the PCI Configuration Space Registers of the PITA.

- **Chapter 11, Internal Register of the PITA**
  Contains maps and descriptions of the Internal Registers of the PITA.

- **Chapter 12, Abbreviations**
  Describes abbreviations occuring in this data sheet.

- **Chapter 13, Index**

Important Notes about this Data Sheet

What's New?

The organization of the structure follows the guidelines of *Information Mapping*®.

What is *Information Mapping*®?

This is a research based method for the

- analysis
- structure
- presentation

of user-orientated manuals.

Major Changes

Instead of the used chapters with mono causal descriptions you now get

- all information
- for a scope
- under the corresponding heading.

The Intention

This Data Sheet is intended to be

- easily surveyed
- increasingly readable
- customized applicable
- practice-orientated
- offering the quickest possible way to the required information.

1 **Features** 1-1

2 **Applications realized with the PITA** 2-1

3 **Construction of the PITA** 3-1

4 **Communication with the PITA** 4-1
4.1 PCI Configuration Space 4-2
4.1.1 Information about the PCI Configuration Space 4-3
4.1.2 Access to the PCI Configuration Space 4-6
4.1.3 Base Address Register 4-7
4.1.4 Other Registers of the PCI Configuration Space 4-11
4.2 PCI Master Target Controller 4-13
4.2.1 Supported PCI Commands 4-14
4.2.2 Transaction Type Single Data Read 4-16
4.2.3 Transaction Type Single Data Write 4-17
4.2.4 Transaction Type Burst Read 4-18
4.2.5 Transaction Type Burst Write 4-20
4.2.6 Transaction Type Fast Back to Back 4-22
4.3 Power Management 4-24
4.3.1 Information about the Power Management States 4-25
4.3.2 Configuration Space Registers of the Power Management 4-28
4.4 Interrupt Control Register - Retry Counter 4-35

5 **Communication with external Components** 5-1
5.1 Serial DMA Interface 5-2
5.1.1 DMA Controller 5-4
5.1.2 IOM-2 Mode 1 5-15
5.1.3 IOM-2 Mode 2 5-18
5.1.4 IOM-2 Mode 3 5-21
5.1.5 IOM-2 Modes - Supplementary Description 5-24
5.1.6 Single Modem Mode V2.1 5-29
5.1.7 Single Modem Mode ALIS V3.X 5-33
5.1.8 Dual Modem/Modem+Voice Mode 5-42
5.1.9 Loop Back Mode 5-45
5.2 Parallel Interface 5-47
5.2.1 ALE after System Reset 5-50
5.2.2 ALE after internal Software Reset 5-51
5.2.3 ALE after setting the Parallel Interface Mode Bit 5-52
5.2.4 Non Multiplexed Mode (Write Transaction) 5-53
5.2.5 Non Multiplexed Mode (Read Transaction) 5-54
5.2.6 Multiplexed Mode (Write Transaction) 5-55
5.2.7 Multiplexed Mode (Read Transaction) 5-56
5.2.8 Transaction Disconnect with Target Abort 5-57
5.2.9 Transaction Termination with Retry 5-60

5.2.10 Timing of the Parallel Interface 5-62
5.3 General Purpose I/O Interface 5-65
5.3.1 Information about the GP I/O Interface 5-66
5.3.2 Timing of the GP I/O Interface 5-68
5.3.3 Internal Registers of the GP I/O Interface 5-69
5.3.4 Input Mode 5-76
5.3.5 Output Mode 5-78
5.3.6 Interrupt Mode 5-80
5.3.7 Usage of the GP I/O Interface as ALIS V2.1 Control Interface 5-82
5.4 SPI EEPROM Interface 5-84
5.4.1 Information about the SPI EEPROM Interface 5-85
5.4.2 Timing of the SPI EEPROM Interface 5-88
5.4.3 Internal Registers for the SPI EEPROM Interface 5-90

6 **Configuration of the PITA** 6-1

7 **Pinning** 7-1

8 **Package Outlines** 8-1

9 **Precaution** 9-1
9.1 Absolute Maximum Ratings 9-2
9.2 DC Characteristics 9-3
9.3 AC Characteristics 9-5
9.4 Capacitances 9-6

10 **Configuration Space Register of the PITA** 10-1
10.1 Description of the Register Types 10-2
10.2 Configuration Space Register 10-3
10.3 Registers which do not occur elsewhere in the Data Sheet 10-13

11 **Internal Register of the PITA** 11-1
11.1 Description of the Register Types 11-2
11.2 Internal Register 11-3
11.3 Registers which do not occur elsewhere in the Data Sheet 11-10

12 **Abbreviations** 13

13 **Index** 13-1

Introduction

What is the PITA?

The PITA is a cost-effective PCI bridge for industrial and communication applications.

The PITA can be used in

- PCI ISDN cards.
- PCI hardware modems.
- PCI software modems.
- Industrial PCI bridge applications.

Interfaces of the PITA

The PITA offers the following interfaces:

Interfaces	to find in
PCI Master Target Controller	see chapter “4.2” on page 4-13
Serial DMA Interface	see chapter “5.1” on page 5-2
Parallel Interface	see chapter “5.2” on page 5-47

The PITA offers the following interfaces:

Interfaces	**to find in**
General Purpose I/O Interface	see chapter “5.3” on page 5-65
SPI EEPROM Interface	see chapter “5.4” on page 5-84

1 Features

Compliant with

- PC98
- PCI Bus Specification Version 2.2
- PCI Power Management Specification Version 1.0

Interfaces

- PCI Master Target Interface
  - PCI 2.2 compliant
  - 32 bit
  - 33 MHz
- Serial Interface
  - Supports IOM-2 Modes
  - Supports serial interface to the ALIS chip-set family
  - DMA Controller for serial communication
  - 16 word FIFOs for each direction
- Parallel Interface
  With chip select logic supporting up to three external components
- General Purpose I/O Interface
  With interrupt capability
- SPI^{TM} Interface
  for optional EEPROM

Compatibility

- ALIS V2.1 PSB 4596
- ALIS V3.X PSB 4596
- ISDN IOM-2 Components, e.g.:
  - IEC-Q family
  - SBCX
- Components consisting of a parallel multiplexed or non multiplexed Intel Interface, e.g:
  - IPAC
  - ISAC
  - ISAR

2 Applications realized with the PITA

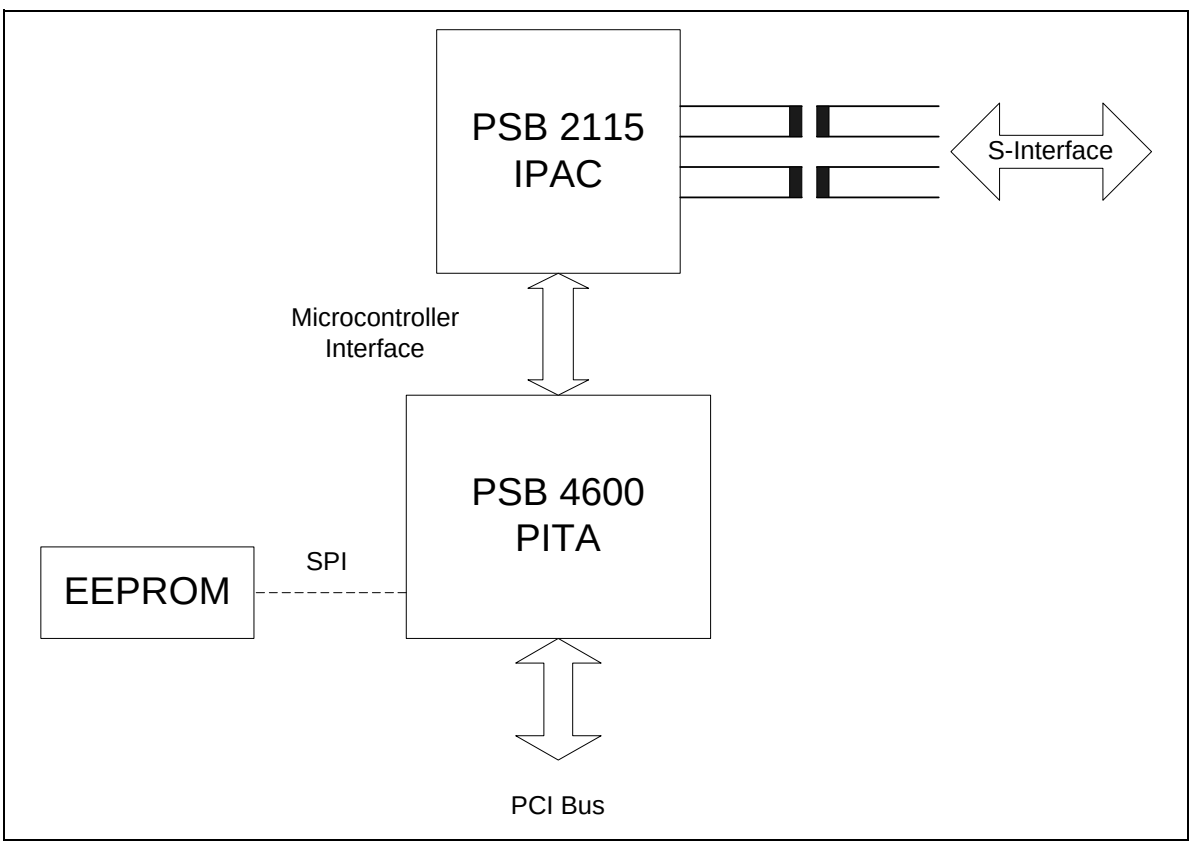
Overview

The PITA provides a PCI interface supporting a serial and parallel interface, including communication applications such as analog software modems and hardware ISDN modems.

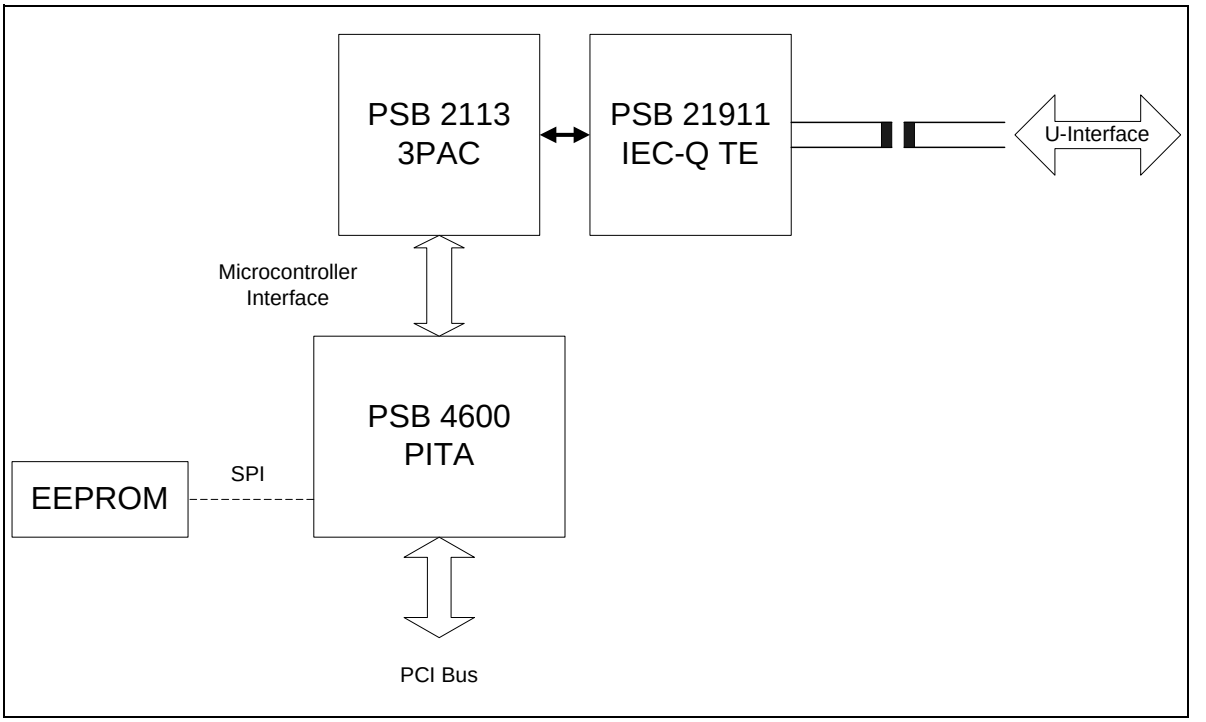
Note

The name ALIS referes to the ALIS chip-set (Analog Line Interface Solution), consting of ALIS-A (PSB4595) and ALIS-D (PSB4596).

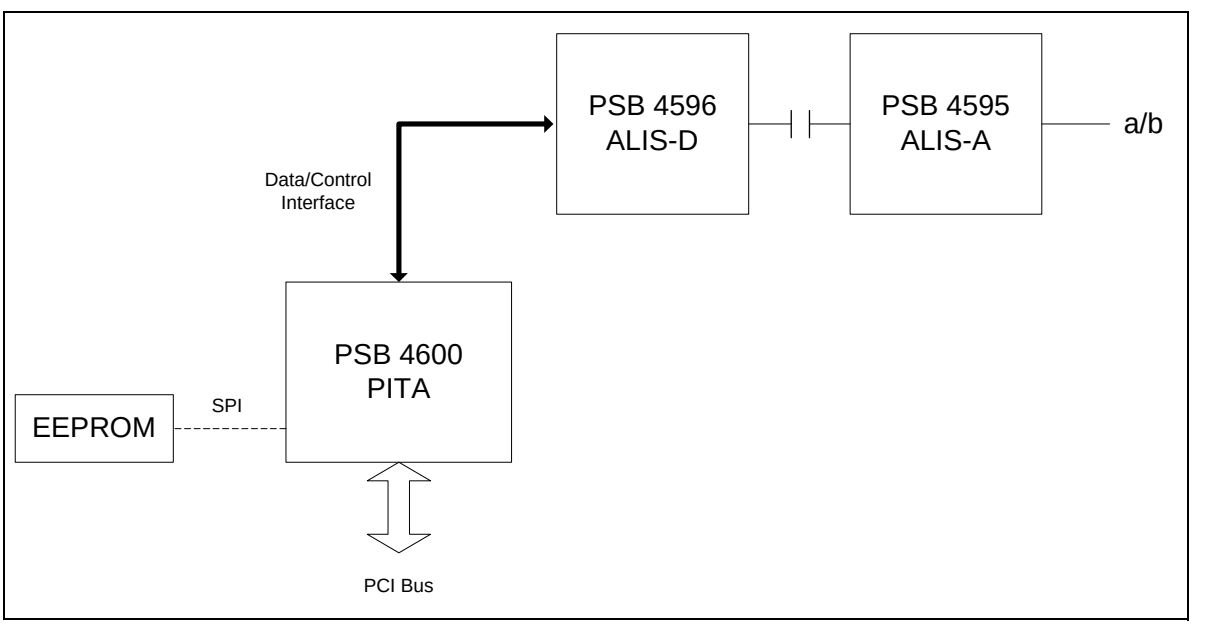
ISDN-S Interface Application with the IPAC



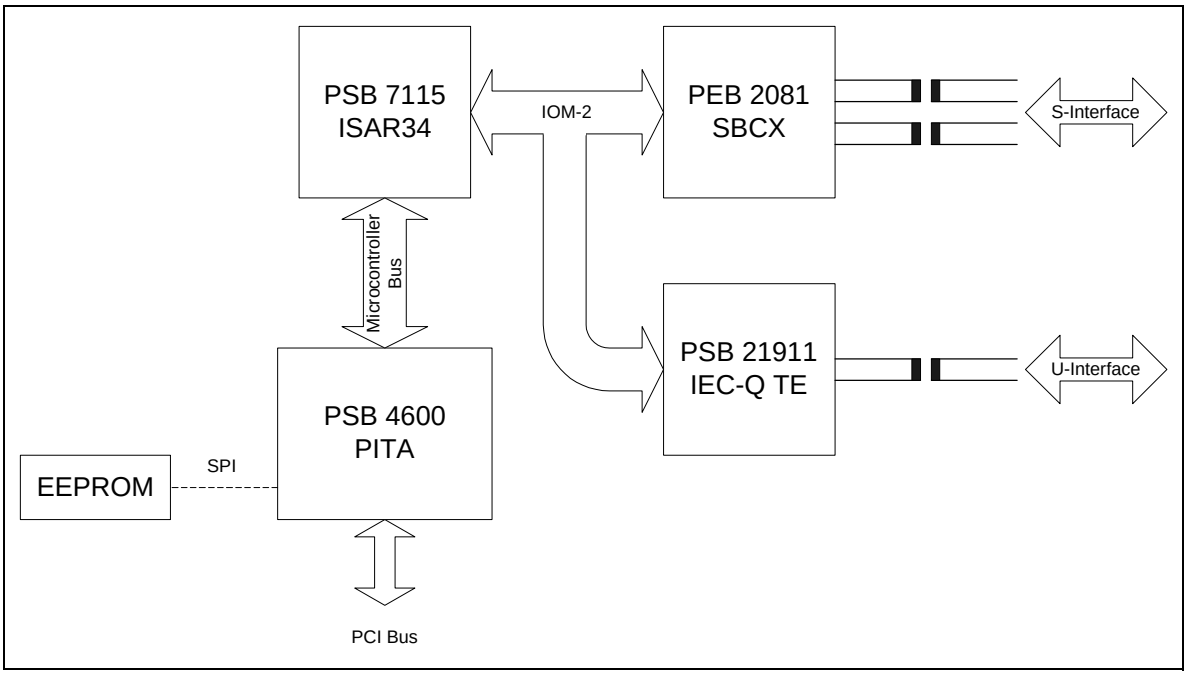
ISDN-U Interface Application with the 3PAC and IEC-Q TE



Software Modem using the ALIS-A and ALIS-D with PCI Interface



ISDN Modem using the ISAR 34 with two Interfaces



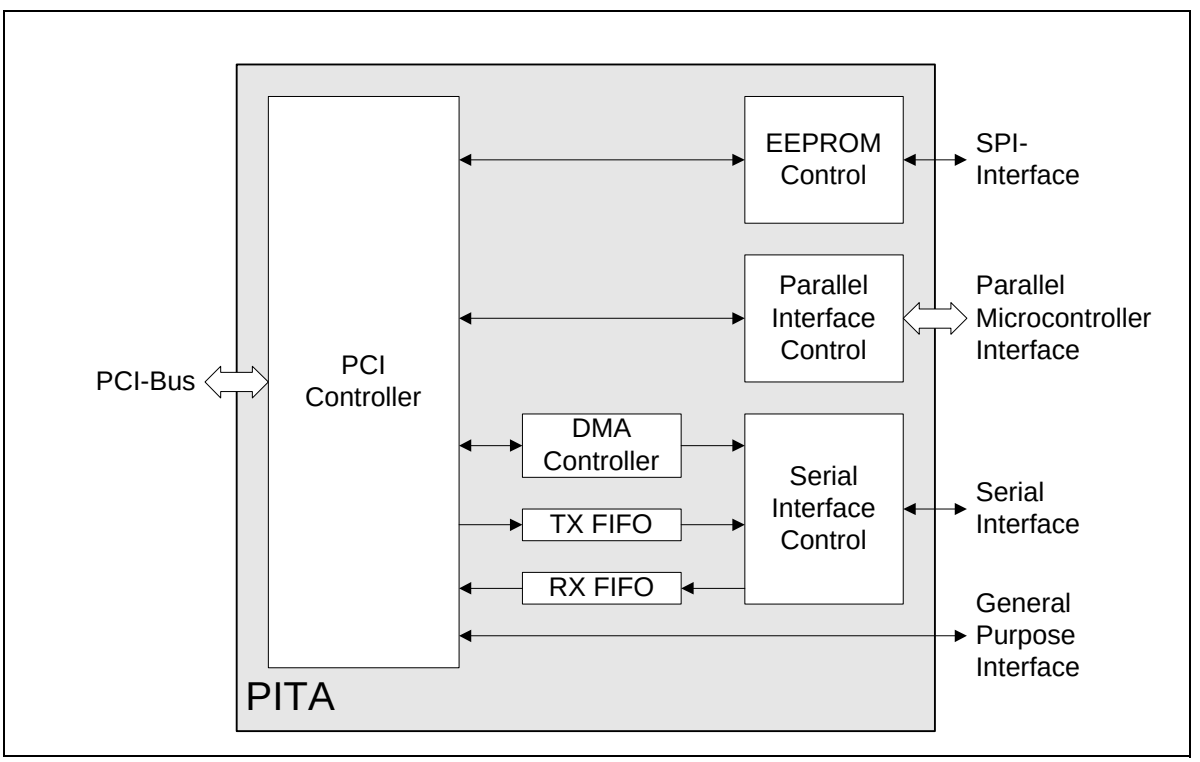
3 Construction of the PITA

Overview

The PITA provides a Peripheral Component Interconnect (PCI) bus interface which acts as a bridge between the PCI bus and the different controllers and interfaces:

- The Parallel Interface Control supports up to three external devices.
- The Serial Interface is controlled by the internal DMA Controller; serial communications use transmit and receive FIFOs.
- The EEPROM for configuration of the PITA and customer specific data storage.
- The General Purpose I/O Interface.

Block Diagram of the PITA



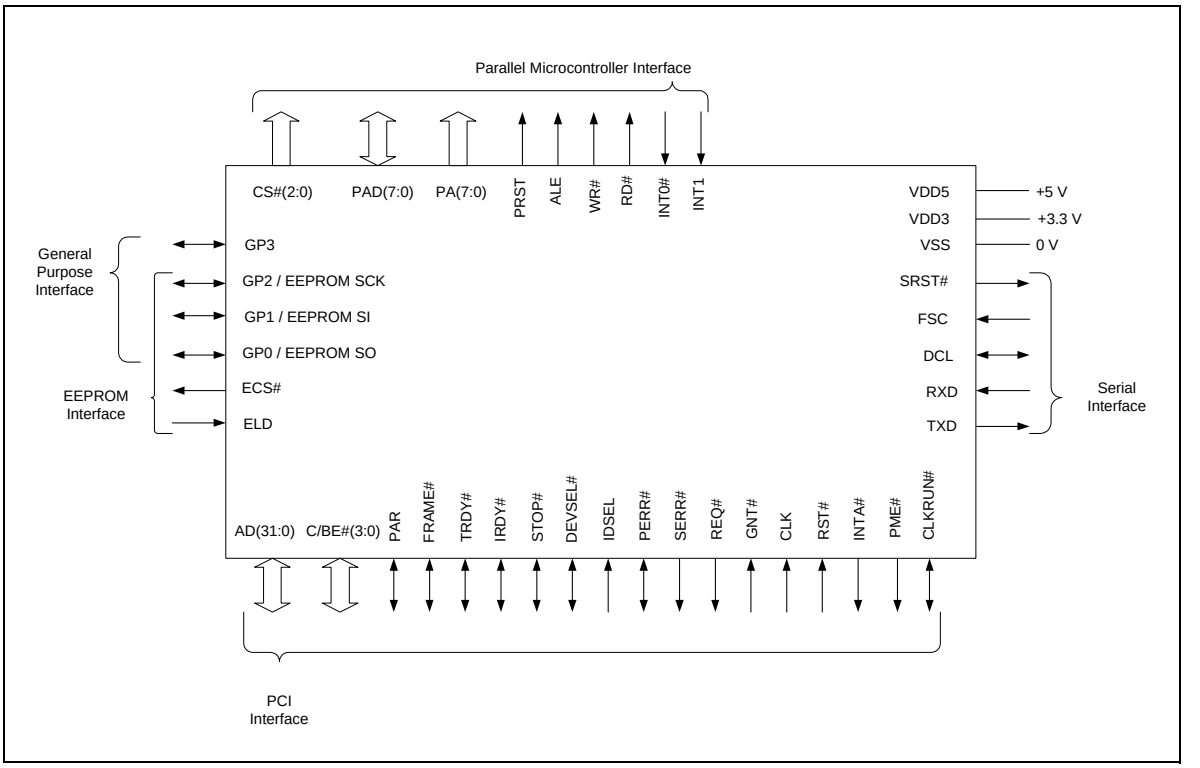
Description of the single Blocks

Name	provides	supports	Notes
PCI Bus Control	• a 32 bit interface at speeds up to 33 MHz • Bus Master DMA capability for data passing through the Serial Interface • Target capability for data passing through the Parallel Interface	the Power Management States: default • D0 • D1 • D3 configurable • D2	
Parallel Interface Control		Chips with a SIEMENS/Intel standard parallel Interface, including: • ISDN devices • Modems DSPs • Industrial devices	
Serial Interface Control		Chips with a serial interface, including: • Analog voice codecs • Analog modem codecs • IOM-2 devices.	Transmit and receive data are held in separate 16-word FIFOs.

Description of the single Blocks

Name	provides	supports	Notes
EEPROM Control	• additional information, such as – the Subsystem ID – the Subsystem Vendor ID – enabling of the D2 Power Management state		This is an optional feature that can be used to customize the PITA configuration at start-up.
General Purpose I/O Interface	• GP outputs • GP inputs • GP interrupt inputs		It can be configured to act as • Input pins • Output pins • Interrupt pins. At start-up these pins are used for the EEPROM interface.

Logical Symbol of the PITA



4 Communication with the PITA

For communication with the PITA following blocks are used:

Components	Page
PCI Configuration Space	4-2
PCI Master Target Controller	4-13
Power Management	4-13
Interrupt Control Register - Retry Counter	4-35

4.1 PCI Configuration Space

Overview

Overview	Page
Information about the PCI Configuration Space	4-3
Access to the PCI Configuration Space	4-6
Base Address Register	4-7
Other Registers of the PCI Configuration Space	4-11

4.1.1 Information about the PCI Configuration Space

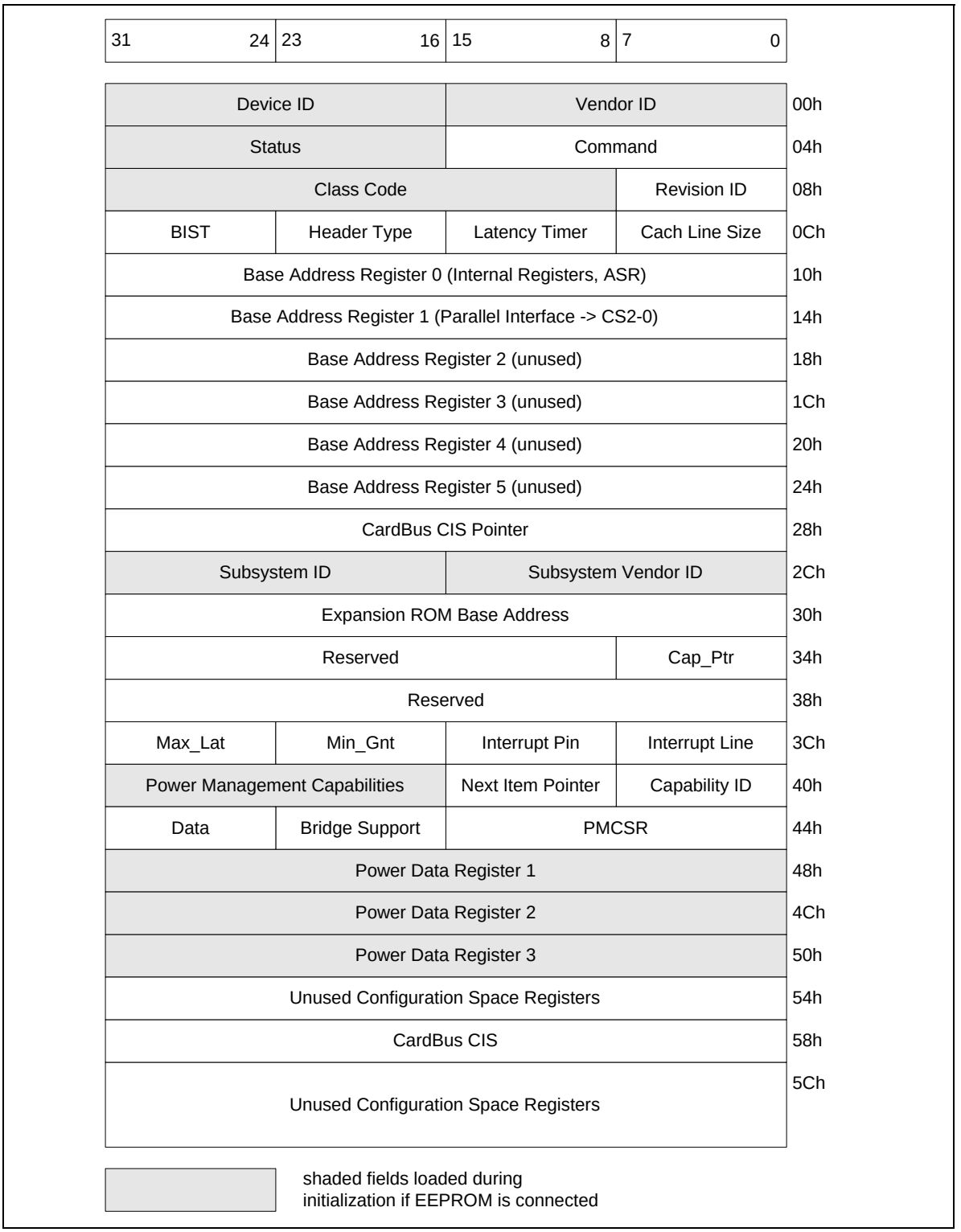
Description

The PCI Configuration Space contains information about

- the PCI device
- the requested address space in the memory space of the PCI system.

The address space includes 64 32-bit registers where as the first 16 registers build the configuration space header (00h-3Ch, refer to “Configuration Space Register of the PITA” on page 10-1)

Construction of the PCI Configuration Space



Description of Register Types

Type	Description
R	• read only • these bits are initialized by pinstrapping during PCI reset
H	• read only • hardwired
RC	• read clear • these bits are set by the internal logic • these bits can be read out and reset by writing logical “1” to them • writing logical “0” doesn’t influence the states of these bits
RW	• read write • these bits can be read out and written via the PCI bus
EW	• EEPROM write • these bits can be set by an external EEPROM after a system reset

4.1.2 Access to the PCI Configuration Space

Description

The PITA supports single 32 bit data transactions for the access to the PCI Configuration Space.

Special Qualities

Name	Description
Subsystem ID	• during System reset: – as well as part of the Subsystem Vendor ID – can be set via pinstrapping if no EEPROM is used • with external EEPROM the complete 16 bit value can be loaded for the Subsystem ID
Subsystem Vendor ID	• 16 bit ID of the card manufacturer • default value: 110Ah (Vendor ID of SIEMENS AG) • identifies the card of the card manufacturer • has to be applied for at the PCI Special Interest Group • during system reset part of the Subsystem ID
CardBus CIS Pointer	is not supported by the PITA, although it is implemented in the PCI Configuration Space

4.1.3 Base Address Register

Base Address Registers 0 - 5

Base Address Register	Description
Base Address Register 0	• the lower 12 bits are connected to logical “0” • occupies an address space of 4K
Base Address Register 1	• the lower 12 bits are connected to logical “0” • allows continuous read and write operations for access to the parallel interface • occupies an address space of 4K – address space is segmented in 4x1K address blocks
Base Address Register 2 - 5	not used

Structure of the Address Space of Base Address Register 1

Address Space	Access to
3FFh - 000h	device 1 on the parallel interface ($\overline{CS0}$)
7FFh - 400h	device 2 on the parallel interface ($\overline{CS1}$)
BFFh - 800h	device 3 on the parallel interface ($\overline{CS2}$)
FFFh - C00h	not used

Configuration Space Register: 04h

Bit 1	Memory_Access_Enable
Type	RW
Default Value	0b
Description	Only if this bit is set to ‘1’, the PCI interface will react on transactions to the base address registers BAR (all Base Address Registers are defined as memory mapped).

Configuration Space Register: 10h

Bit 31:12	Base Address Register 0
Type	RW
Default Value	0000h
Bit 11:00	Base Address Register 0
Type	H
Default Value	000h
Description	Bar 0 contains the base address of an address space in the PCI main memory through which the internal registers of the PITA can be accessed.

Configuration Space Register: 14h

Bit 31:12	Base Address Register 1
Type	RW
Default Value	0000h
Bit 11:00	Base Address Register 0
Type	H
Default Value	000h
Description	Bar 1 contains the base address of a 4-kbyte address space in the PCI main memory through which the internal registers of the PITA can be accessed.

Configuration Space Register: 18h

Bit 31:0	Base Address Register 2
Type	H
Default Value	0000 0000h
Description	Base Address Register 2 is not supported.

Configuration Space Register: 1Ch

Bit 31:0	Base Address Register 3
Type	H
Default Value	0000 0000h
Description	Base Address Register 3 is not supported.

Configuration Space Register: 20h

Bit 31:0	Base Address Register 4
Type	H
Default Value	0000 0000h
Description	Base Address Register 4 is not supported.

Configuration Space Register: 24h

Bit 31:0	Base Address Register 5
Type	H
Default Value	0000 0000h
Description	Base Address Register 5 is not supported.

4.1.4 Other Registers of the PCI Configuration Space

Configuration Space Register: 28h

Bit 31:0	CardBus CIS Pointer
Type	H
Default Value	0000 02C0h
Description	

Bit 31:28	ROM_Image_Number
Type	H
Default Value	0000b
Description	

Bit 27:3	Address_Space_Offset
Type	H
Default Value	000058h
Description	Points to the first CIS register in the Configuration Space.

Bit 2:0	Address_Space_Indicator
Type	H
Default Value	000b
Description	CIS in the device specific Configuration Space.

Note

The CardBus function is not supported in this version of the PITA.

Configuration Space Register: 2Ch

Bit 31:20	Subsystem ID
Type	H/EW
Default Value	000h
Bit 19:16	Subsystem ID
Type	R/EW
Default Value	pinstrap value or EEPROM value
Description	Identifies a specific board of a manufacturer on which the PITA is used. The 4 LSBs will be set by pinstrapping during PCI reset if no EEPROM is used and the complete 16 bit register can be configured by a connected EEPROM.

Bit 15:0	Subsystem Vendor ID
Type	R/EW
Default Value	pinstrap value or EEPROM value
Description	Marks of the Vendor of the board on which the PITA is used. This register will be set by pinstrapping during PCI reset if no EEPROM is used or configured from a connected EEPROM. This ID is allocated by the PCI SIG.

4.2 PCI Master Target Controller

Introduction

The interface of the PCI bus is represented by the PCI Master/Target Controller. This Controller is part of the PITA.

The PCI Master/Target Controller supports

- several types of transactions,
- two of the six Base Address Registers.

The PCI Master Target Controller

- has a “Medium Device Select” behavior,
- truncates burst transactions at the end of the first dataphase.

4.2.1 Supported PCI Commands

PCI Master Controller:

PCI Command	Transaction Type
Memory Read	single transfer
Memory Write	single transfer

PCI Target Controller:

PCI Command	Transaction Type
Memory Read	single transfer
Memory Read Multiple	single transfer, mapped on Memory Read
Memory Read Line	single transfer, mapped on Memory Read
Memory Write	single transfer
Memory Write and Invalidate	single transfer, mapped on Memory Write
Configuration Read	single transfer
Configuration Write	single transfer

Overview

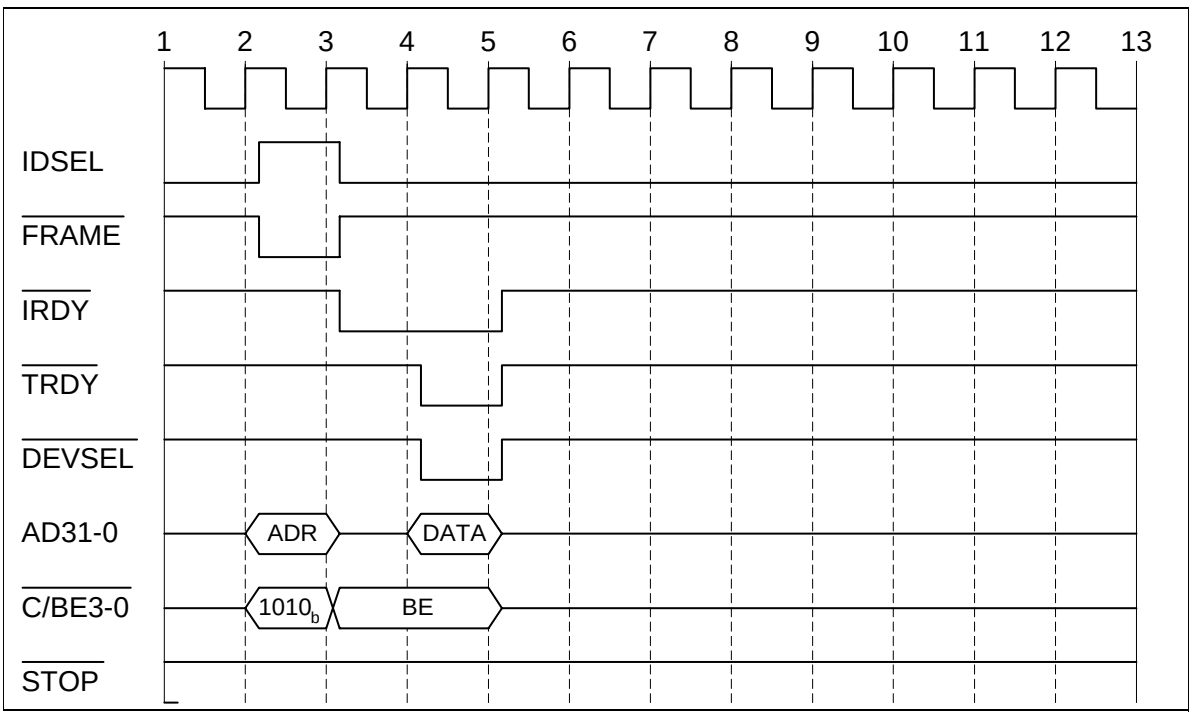
Overview	Page
Transaction Type Single Data Read	4-16
Transaction Type Single Data Write	4-17
Transaction Type Burst Read	4-18
Transaction Type Burst Write	4-20
Transaction Type Fast Back to Back	4-22

Note

The following timing diagrams are meant as an example and show the transactions to and from the PCI configuration space.

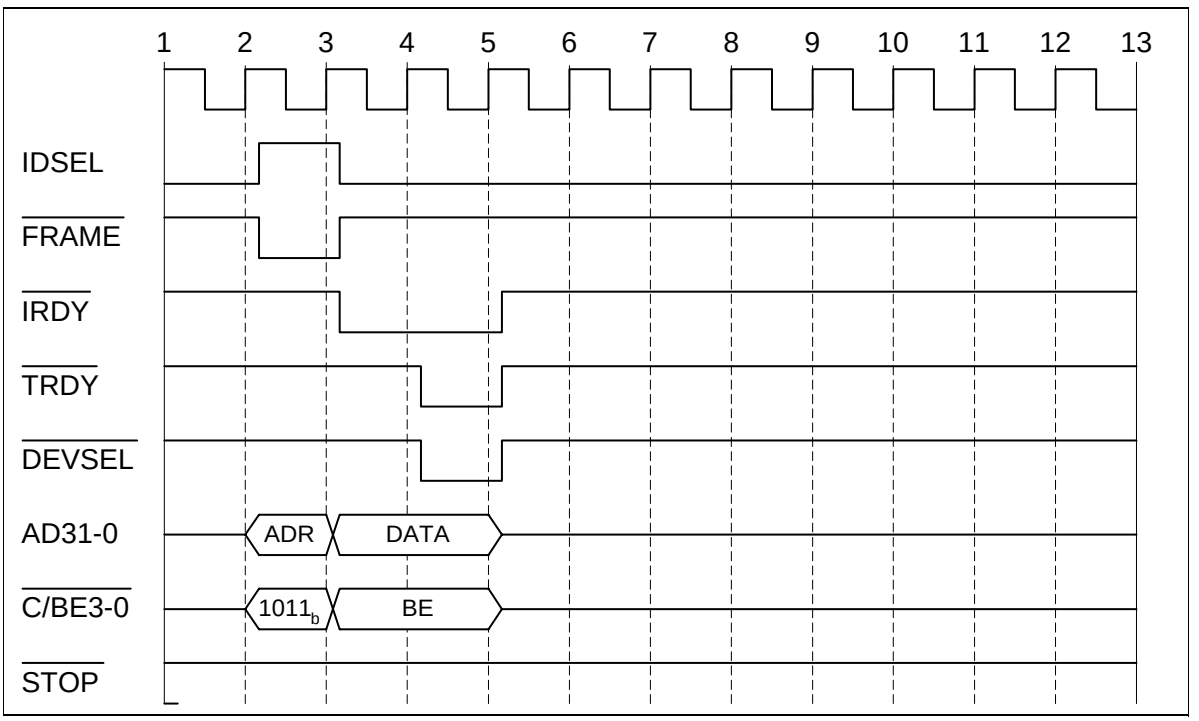
4.2.2 Transaction Type Single Data Read

Timing Diagram



4.2.3 Transaction Type Single Data Write

Timing Diagram

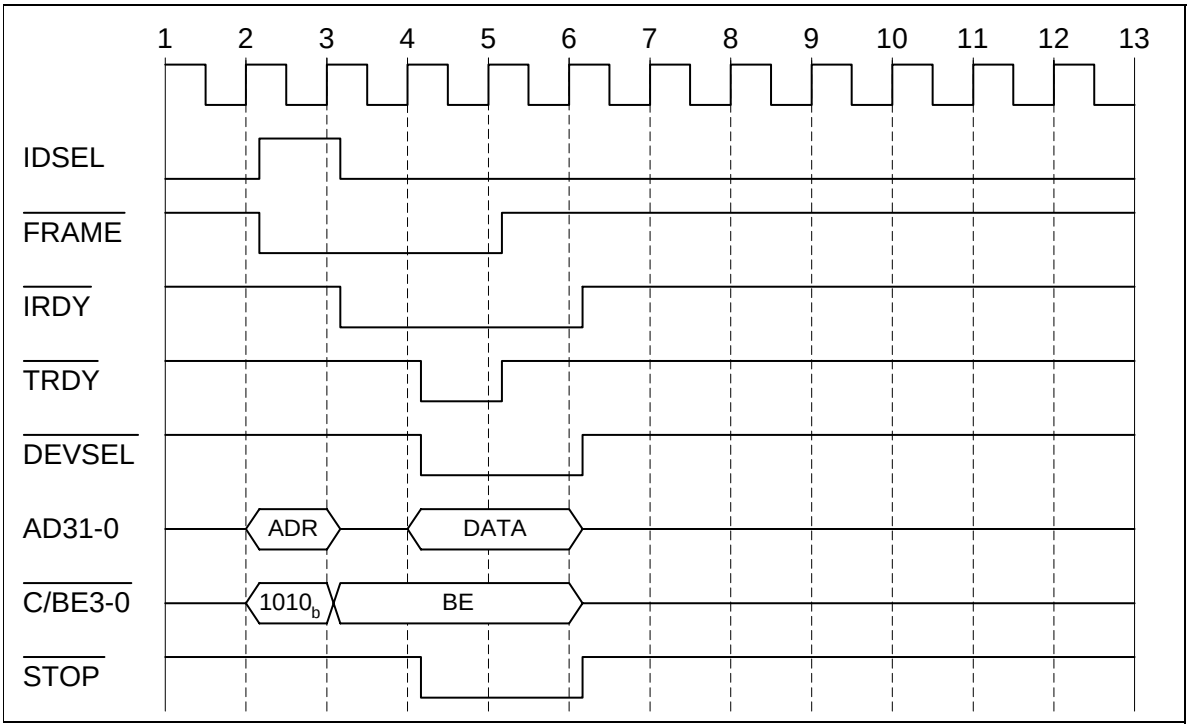


4.2.4 Transaction Type Burst Read

Description

- Asserting $\overline{\text{IRDY}}$ and $\overline{\text{STOP}}$ at the first dataphase leads to the disconnection (Disconnect-B) of the burst read transaction by the PITA.
- $\overline{\text{STOP}}$ is asserted until $\overline{\text{FRAME}}$ is deasserted.
- Deassertion of $\overline{\text{FRAME}}$ means that $\overline{\text{STOP}}$ and $\overline{\text{DEVSEL}}$ together are deasserted.

Timing Diagram



Configuration Space Register: 04h

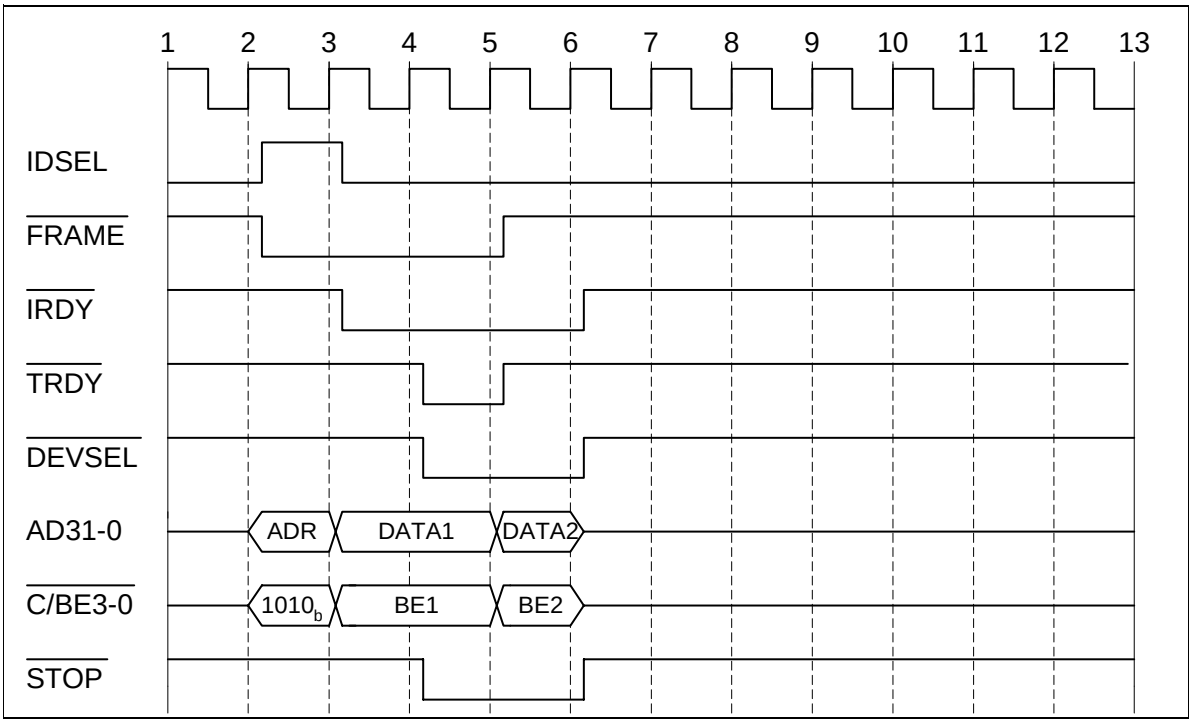
Bit 26:25	DEVSEL_Timing
Type	H
Default Value	01b
Description	‘01’ = medium timing, i.e. the DEVSEL signal will be asserted from the PCI interface with the second positive PCI clock edge after $\overline{\text{FRAME}}$ was asserted on the PCI bus by a master.

4.2.5 Transaction Type Burst Write

Description

- Asserting $\overline{\text{IRDY}}$ and $\overline{\text{STOP}}$ at the first dataphase leads to the disconnection (Disconnect-B) of the burst write transaction by the PITA.
- $\overline{\text{STOP}}$ is asserted until $\overline{\text{FRAME}}$ is deasserted.
- Deassertion of $\overline{\text{FRAME}}$ means that $\overline{\text{STOP}}$ and $\overline{\text{DEVSEL}}$ together are deasserted.

Timing Diagram



Configuration Space Register: 04h

Bit 26:25	DEVSEL_Timing
Type	H
Default Value	01b
Description	‘01’ = medium timing, i.e. the DEVSEL signal will be asserted from the PCI interface with the second positive PCI clock edge after $\overline{\text{FRAME}}$ was asserted on the PCI bus by a master.

4.2.6 Transaction Type Fast Back to Back

Description

With the fast back to back transaction a PCI Master Controller can perform

- several write transactions
- a read transaction as last transaction

without setting the PCI bus to IDLE state in between or releasing the bus to another master.

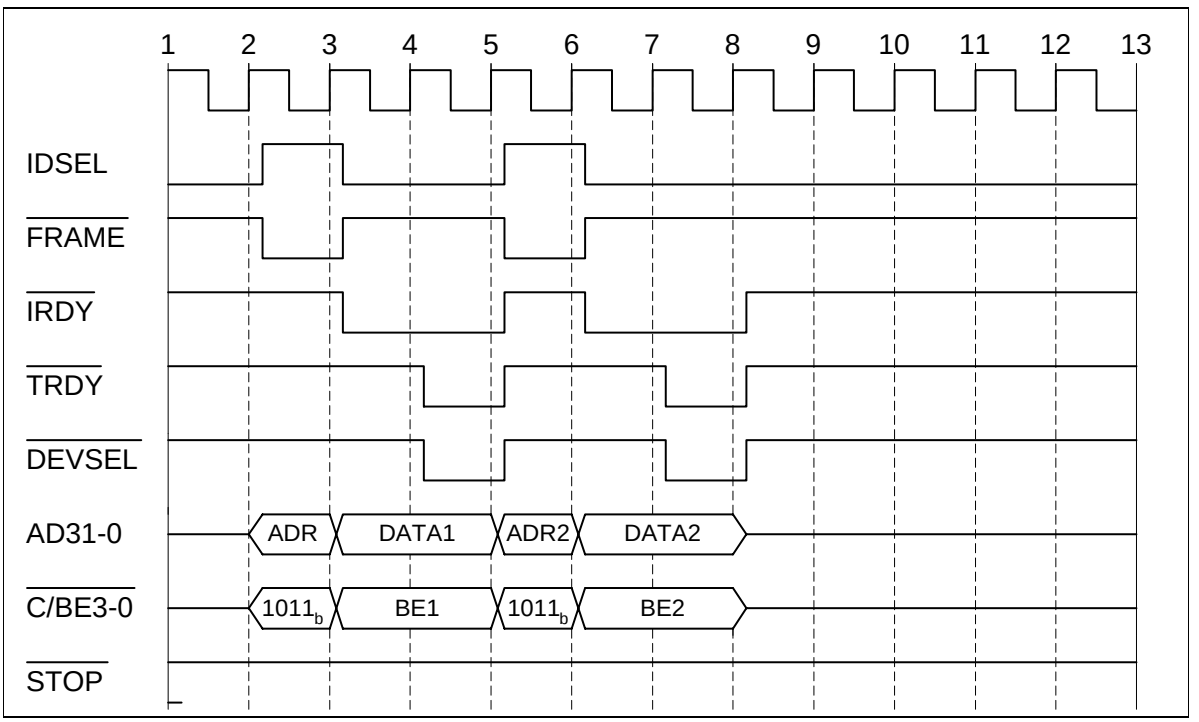
At the end of a transaction:

- The Master asserts the $\overline{\text{FRAME}}$ signal and at the same time the $\overline{\text{TRDY}}$ signal is deasserted.

The transaction is answered with a RETRY signal by the PITA

- if the parallel interface is included in the fast back to back transaction
- and the parallel interface is still busy.

Timing Diagram



Configuration Space Register: 04h

Bit 23	Fast_Back_To_Back_Capability
Type	H
Default Value	1b
Description	The PITA supports fast back-to-back.

Bit 9	Fast_Back_To_Back_Enable
Type	H
Default Value	0b
Description	The PITA itself generates no Fast back-to-back transactions.

4.3 Power Management

Overview

Overview	Page
Information about the Power Management	4-25
Configuration Space Registers of the Power Management	4-28

4.3.1 Information about the Power Management States

Description

The PITA supports the Power Management states D0, D1, D2, D3, $D3_{hot}$ and $D3_{cold}$.

D0

- The D0 state represents the default state of the internal logic after a system reset.
- After a system reset the PCI interface is in the D0 state and has to be initialized before being used.
- The PITA responds only to configuration accesses while not completely initialized.
- The PCI Master Target controller is disabled while not completely initialized.

D1

- D1 is a light sleep rate.
- The PITA supports the D1 state by default if this state is not disabled by an EEPROM configuration.
- The PITA PCI function can be set to the D1 state by software.
- The PITA PCI function only responds to PCI configuration accesses.
- All accesses to the memory spaces defined by the Base Address Registers are disabled.
- The only PCI bus operation the PCI interface is allowed to initiate is the assertion of the $\overline{PME}$ signal.

D2

- By default the support of the D2 state is disabled in the PITA.
- D2 can be enabled by configuration by an EEPROM.
- Same state behavior as described for the state D1.

D3

- Same state behavior as described for the state D1.
- The only legal state transitions from D3 to D0 are:
  - by software reset; the software has to perform a fully reinitialization of the PCI function including the PCI Configuration Space.
  - by system reset

$D3_{hot}$

- Power and clock are still available to the PITA.
- Power and clock can be returned to D0 by software.
- State behavior as described for the state D3.

$D3_{cold}$ (POWER OFF)

- $D3_{cold}$ is a “power off” state.
- The PCI bus power V_{cc} has been disconnected.
- If V_{cc} is removed from the device.
- PME generation is not possible in that state.

Electrical Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min	max		
Power supply current	I_{CC}		0	mA	$D3_{cold}$ state - power off (power is removed)
			19	mA	$D3_{hot}$ state - power down
			19	mA	D2 state - deep sleep mode
			19	mA	D1 state - light sleep mode
			19	mA	D0 state - operational mode

4.3.2 Configuration Space Registers of the Power Management

Configuration Space Register: 34h

Bit 31:8	Reserved
Type	H
Default Value	000000h
Description	Reserved

Bit 7:0	Cap_Ptr
Type	H
Default Value	40h
Description	The Capabilities Pointer points to the first Power Management Register in the PCI Configuration Space.

Configuration Space Register: 40h

Bit 31:0	Power Management Capabilities (PMC)

Bit 31	PME_Support_D3$_{cold}$
Type	H
Default Value	0b
Description	Bit 31=PME_Support_D3$_{cold}$=’0’; not supported

Configuration Space Register: 40h (cont'd)

Bit 30	PME_Support_D3$_{hot}$
Type	H
Default Value	0b
Description	Bit 30=PME_Support_D3$_{hot}$='0'; PME supports D3$_{hot}$

Bit 29	PME_Support_D2
Type	H or EW
Default Value	0b
Description	Bit 29=PME_Support_D2='0'; not supported; can be enabled by EEPROM

Bit 28	PME_Support_D1
Type	H or EW
Default Value	1b
Description	Bit 28=PME_Support_D1='0'; not supported; can be enabled by EEPROM

Bit 27	PME_Support_D0
Type	H
Default Value	0b
Description	Bit 27=PME_Support_D0='0'; not supported

Configuration Space Register: 40h (cont'd)

Bit 26	D2_Support
Type	H or EW
Default Value	0b
Description	• Not supported from the PITA by default. • Support can be enabled by EEPROM. Board with the PITA must be able to assert the $\overline{\text{PME}}$ signal. • D2 state is fully enabled when – assertion of PME_Clock – assertion of the PME_Support_2 bit is required.

Bit 25	D1_Support
Type	H or EW
Default Value	1b
Description	• The PITA supports the D1 Power state by default. • Can be disabled by EEPROM.

Bit 24:22	Reserved
Type	H
Default Value	000b
Description	Reserved

Bit 21	DSI (Device Specific Initialization)
Type	H
Default Value	1b
Description	Indicates that the PITA requires a specific initialization sequence following the transition to D0 state (uninitialized).

Configuration Space Register: 40h (cont'd)

Bit 20	Reserved
Type	H
Default Value	0b
Description	Reserved

Bit 19	PME_Clock
Type	H or EW
Default Value	1b
Description	The PME_Clock bit is by default ='1', because only $\overline{\text{PME}}$ assertion is supported if the PCI clock is present. If also $\overline{\text{PME}}$ assertion out of D2 (no clock running) is supported, the PME_Clock bit must be set to '0' by EEPROM.

Bit 18:16	Version
Type	H
Default Value	001b
Description	The value 01b indicates that the device complies with the Revision 1.0 of the PCI Power Management Interface Specification.

Bit 15:8	Next_Item_Ptr
Type	H
Default Value	00h
Description	No next item

Configuration Space Register: 40h (cont'd)

Bit 7:0	Capabiltity_ID
Type	H
Default Value	01h
Description	'Indicates that the data structure is currently pointed to the PCI Power Management data structure.

Configuration Space Register: 44h

Bit 31:24	DATA_Register
Type	H
Default Value	00h
Description	Depending on the Data_Select field (Bit 12:9) parts of the Power Data register (48h) are mapped to this register.

Bit 23:16	PMCSR_BSE (Bride support extension)
Type	H
Default Value	00h
Description	not used

Bit 15	PME_Status
Type	RC
Default Value	0b
Description	This bit is set when the PCI interface asserts the $\overline{\text{PME}}$ signal independent of the state of the PME_EN bit.

Configuration Space Register: 44h (cont'd)

Bit 15:8	Power Management Control/Status Register
Type	H
Default Value	00h

Bit 14:13	Data_Scale
Type	H
Default Value	00b
Description	Depending on the Data_Select field (Bit 12:9) parts of the Power_Data register are mapped to this register.

Bit 12:9	Data_Select
Type	RW
Default Value	0h
Description	• Values from 0 - 7 are supported: Parts of the Power_Data register are mapped to the DATA register and the Data_Scale field. • Values from 8 - 15: Zero values are mapped to the DATA register and the Data_Select field.

Bit 8	PME_En
Type	RW
Default Value	0b
Description	Enables ar disables the PITA to assert the $\overline{\text{PME}}$ signal. PME_En='0': Assertion of the $\overline{\text{PME}}$ signal is disabled. PME_En='1': The device is enabled to assert the $\overline{\text{PME}}$ signal.

Configuration Space Register: 44h (cont'd)

Bit 8	PME_En
Type	RW
Default Value	000000b
Description	Reserved

Bit 7:2	Reserved
Type	H
Default Value	00h
Description	Reserved

Bit 1:0	Power_State
Type	RW
Default Value	00b
Description	Power_State='00': D0 state (supported by the PITA) Power_State='01': D1 state (supported by the PITA) Power_State='10': D2 state (not supported by default) Power_State='11': D3 state (supported by the PITA).

4.4 Interrupt Control Register - Retry Counter

Description

- Part of the PCI Master Target Controller
- Functionality:

1. Disconnection of the PCI Master transaction with Retry by the addressed PCI Slave.
2. Decrement of the counter.
3. The Retry_Counter_Int bit is set.
4. An interrupt will be generated if the Retry_Counter_Enable bit is set.
5. The PCI Master starts the transaction again.

Internal Register: 00h

Bit 27	RETRY_Counter_Down_Int_En
Type	RW
Default Value	0b
Description	Enable for the Retry_Counter_Down interrupt bit

Bit 11	Retry_Counter_Int
Type	RC
Default Value	0b
Description	If a PCI Master initiated transaction is retried from a PCI Slave with the number of retries defined in the Retry_Counter register, this interrupt bit is set by the PCI interface.

Internal Register:1Ch

Bit 23:16	Retry Count Register
Type	RW
Default Value	00h
Description	• Part of the PCI Master Target Controller • Functionality: 1. Disconnection of the PCI Master transaction with Retry by the addressed PCI Slave. 2. Decrement of the counter. 3. The Retry_Counter_Int bit is set. 4. If the Retry_Counter_Enable an interrupt will be generated. 5. The PCI Master starts the transaction again.

5 Communication with external Components

Interfaces

Interfaces	Page
Serial DMA Interface	5-2
Parallel Interface	5-47
General Purpose I/O Interface	5-65
SPI EEPROM Interface	5-84

5.1 Serial DMA Interface

Introduction

The serial DMA interface is used in different modes to transmit and receive 16 bit/ 32 bit data frames. These data frames have different structures:

- Data/Voice and Command
- Data/Voice and Command for two codecs
- Different time slots on IOM-2.

Usage of the Serial DMA Interface

The serial DMA interface is clocked by default with the internally generated clock (PCI clock divided by 40).

The Ser_Clock_Set bit must be set in the Serial Clock Select register to ’1’ when the interface works in ALIS V3.X or IOM-2 mode

- after a system reset
- before starting the DMA controller.

The reset of this bit can result in an unknown behavior of the FIFOs and the serial controller.

The serial DMA interface is fully controlled by the DMA controller.

Overview

Overview	Page
DMA Controller	5-4
IOM-2 Mode 1	5-15
IOM-2 Mode 2	5-18
IOM-2 Mode 3	5-21
IOM-2 Modes - Supplementary Description	5-24
Single Modem Mode V2.1	5-29
Single Modem Mode ALIS V3.X	5-33
Dual Modem/Modem+Voice Mode	5-42
Loop Back Mode	5-45

5.1.1 DMA Controller

Overview

Overview	Page
Information about the DMA Controller	5-5
Interrupts	5-9
Internal Registers of the DMA Controller	5-10

5.1.1.1 Information about the DMA Controller

Description

For the control of the DMA Controller, three register are implemented in the internal registers:

- The Circular Buffer Start Address is a 4-kbyte aligned PCI address which points to a 4-kbyte circular buffer in the PCI main memory. All DMA read/write transactions between host and PITA will be processed via this 4-kbyte address space.
- The DMA Control register includes the 6-bit parameter DMA Select which is used to define the mode for the next DMA transfer. With the DMA_Start bit the DMA transfer can be started and stopped.
- The contents of the DMA Write Count Register is interpreted as a threshold for the write transfers from the DMA controller.

Function of the DMA Controller

Phase	Function
1	DMA_Start bit is set in the DMA Control Register and a DMA transfer is started as defined in the DMA Select Register.
2	The DMA controller loads the Circular Buffer Start Address to its Actual Circular Buffer Pointer.
3	The DMA controller fills the TX FIFO by reading 15 times through the PCI interface (PCI master mode) from the circular buffer.
4	The DMA controller signals the end of the initial sequence.
5	The DMA controller increments the Actual Circular Buffer Pointer by 4 each read transfer.
6	The DMA controller loads the contents of the 12 bit DMA Write Count Register to its internal 12 bit DMA write counter.
7	After the first 15 read transfers in the beginning of the 16th read transfer the DMA controller starts the normal DMA algorithm.

Function of the DMA Algorithm

Phase	Function
1	The DMA controller reads the 16th data word from the current address in the circular buffer (Actual Circular Buffer Pointer) to the internal TX FIFO.
2	The DMA controller writes the first received 16-bit data word from the RX FIFO to the same address in the circular buffer.
3	The DMA controller increments the Actual Buffer Pointer by 4.
4	The DMA controller reads the 17th data word from the current address in the circular buffer (Actual Circular Buffer Pointer) to the internal TX FIFO.
5	The DMA controller writes the second received 16-bit data word from the RX FIFO to the same address in the circular buffer.
6	The DMA controller increments the Actual Buffer Pointer by 4.
7	and so on

DMA Write Counter

After each write transaction from the RX FIFO to the buffer the internal DMA write counter is incremented by 1. If this counter reaches ’0’ an interrupt is generated and the counter is loaded again with the contents of the DMA Write Counter Register.

The internal DMA write counter is decremented every two write transactions as long as two 16 bit values per FSC frame are transferred in the following modes:

- 32 bit frame mode
- dual modem mode
- modem+voice mode
- IOM-2 mode 2 and 3.

DMA_Start bit

- The reset of the DMA_Start bit stops the DMA transfer immediately.
- The assertion of the DMA_Start bit resets the TX and RX FIFO's. This means that all FIFO data is lost when the DMA transfer is stopped.

Data in the Circular Buffer

Since no data is written from the RX FIFO to the circular buffer for the first 15 addresses, the first interrupt after the DMA_Start assertion means that the received data is available in the circular buffer on address

- 003Ch to 003Ch + [DMA Write Count]: 16 bit frame modes
- 003Ch to 0003Ch + 2 x [DMA Write Count]: 32 bit frame modes.

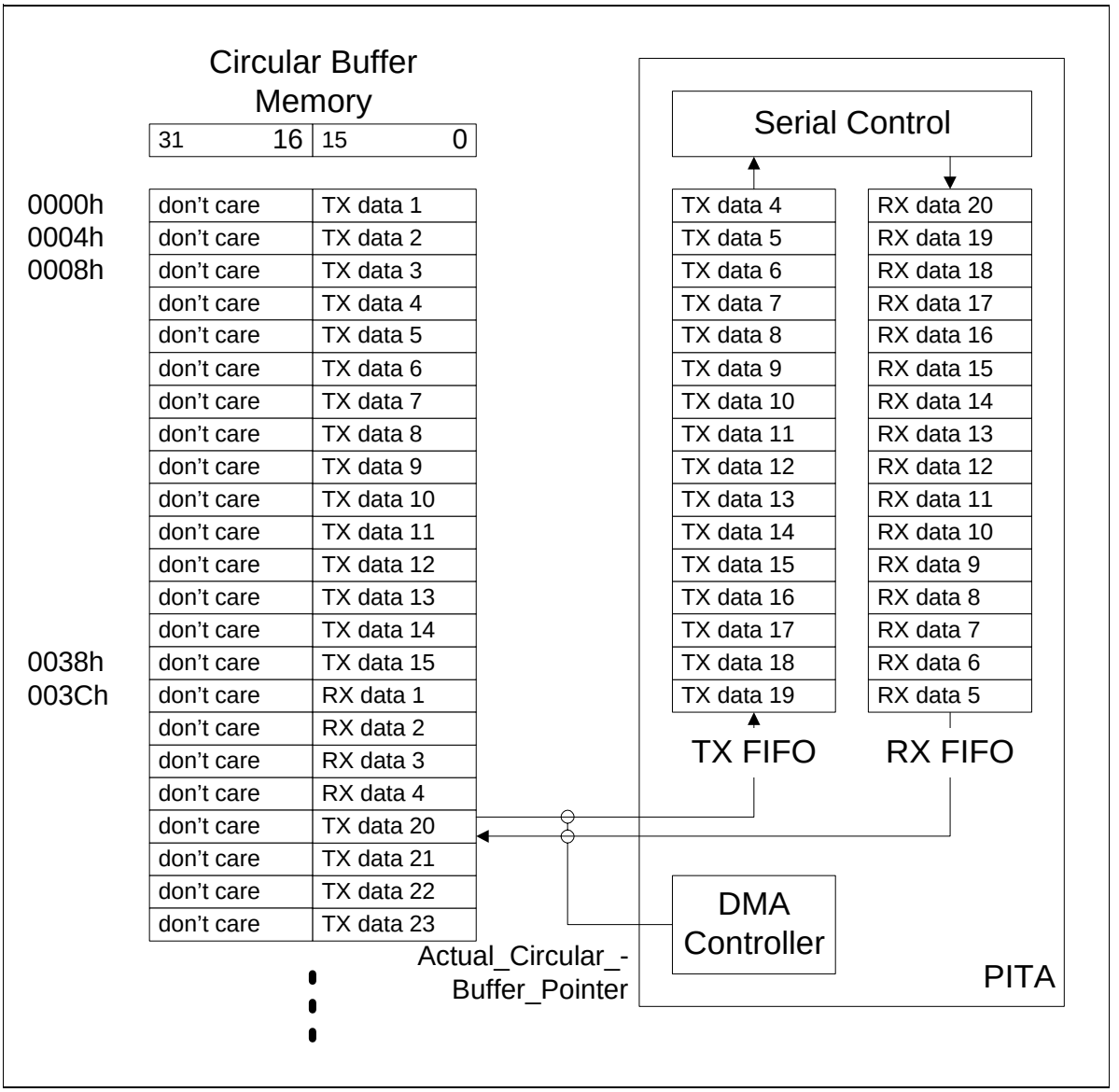
During normal data transfer every interrupt means that received data is available in the circular buffer on address

- [end address from last interrupt] to [end address from last interrupt] + [DMA Write Count]: 16 bit frame modes
- [end address from last interrupt] to [end address from last interrupt] + 2 x [DMA Write Count]: 32 bit frame modes

Example for DMA controlled Data Transfer via Circular Buffer

The status of the DMA controller:

16 bit frame access mode (ALIS V2.1 mode/IOM-2 mode 1) when three data frames are already written to the TX line.



5.1.1.2 Interrupts

FIFO Overflow/Empty Interrupt

- This interrupt bit is set by the serial controller during the active DMA if:
  - The selected serial protocol could not be generated because there was no data available in the TX FIFO.
  - A received data frame was lost because of FIFO Overflow.
- This bit is not set during the DMA start sequence by the serial controller.

Write Counter Interrupt

An interrupt by the write counter must be processed by the host in the following way:

- read out the new received data in the circular buffer
- fill in new transmit data in the circular buffer
- reset the DMA_Write_Counter bit in the Interrupt Control Register.

Note

This has to be done before the DMA Write Counter expires once again (e.g. interrupt latency), which would cause the generation of a DMA_Write_Counter_Overflow.

5.1.1.3 Internal Registers of the DMA Controller

Internal Registers: 00h

Bit 26	FIFO_Overflow_Empty_Int_En
Type	RW
Default Value	0b
Description	Enable for the FIFO_Overflow_Empty interrupt bit

Bit 25	DMA_Write_Counter_Overflow_Int_En
Type	RW
Default Value	0b
Description	Enable for the DMA_Write_Counter_Overflow interrupt bit.

Bit 24	DMA_Write_Counter_Int_En
Type	RW
Default Value	0b
Description	Enable for the DMA_Write_Counter interrupt bit.

Bit 10	FIFO_Overflow_Empty_Int
Type	RC
Default Value	0b
Description	During a DMA transfer the serial controller was unable to write received data to the RX FIFO because is was already full or the serial controller was unable to send data after the rising FSC edge because of empty TX FIFO.

Internal Registers: 00h (cont'd)

Bit 9	DMA_Write_Counter_Overflow_Int
Type	RC
Default Value	0b
Description	This bit is set if the internal DMA write counter is counted down while the DMA_Write_Counter_Int bit is still active. This means that the interrupt generated by the DMA_Write_Counter_Int bit is not yet processed.

Bit 8	DMA_Write_Counter_Int
Type	RC
Default Value	0b
Description	This bit is set if the number of data, defined in the DMA Write Count Register is written through the PCI interface. In the 32-bit modes (dual modem, modem+voice, IOM-2 mode 2, IOM-2 mode 3) this bit is set if the number of data pairs defined in the DMA Write Count Register is transferred through the PCI interface.

Internal Registers: 04h

Bit 31:0	DMA Control Register
Bit 31:9	Reserved
Type	H
Default Value	0000000h
Description	Reserved

Internal Registers: 04h (cont'd)

Bit 8	DMA_Start
Type	RW
Default Value	0b
Description	By asserting this bit a DMA transfer between the circular buffer and the serial DMA interface using internal RX/TX FIFOs is started. This bit is reset by the host if the DMA transfer is to be finished.

Bit 7:6	Reserved
Type	H
Default Value	00b
Description	Reserved

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	Used to define the mode for the next DMA transfer: – Mode 1 ('000001'): Single Modem Mode V2.1 – Mode 2 ('000010'): Single Modem Mode V3.X – Mode 3 ('000100'): Single Dual Modem/Modem+Voice Mode V3.X – Mode 4 ('001000'): IOM-2 Mode 1 – Mode 5 ('010000'): IOM-2 Mode 2 – Mode 6 ('100000'): IOM-2 Mode 3 With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Registers: 08h

Bit 31:12	Circular Buffer Start Address
Type	RW
Default Value	000000h
Bit 11:0	Circular Buffer Start Address
Type	H
Default Value	000h
Description	• 4-kbyte aligned PCI address which points to a 4-kbyte circular buffer in the PCI main memory. • All DMA read/write transactions between the host and the PITA are processed via this 4-kbyte address space.

Internal Register: 0Ch

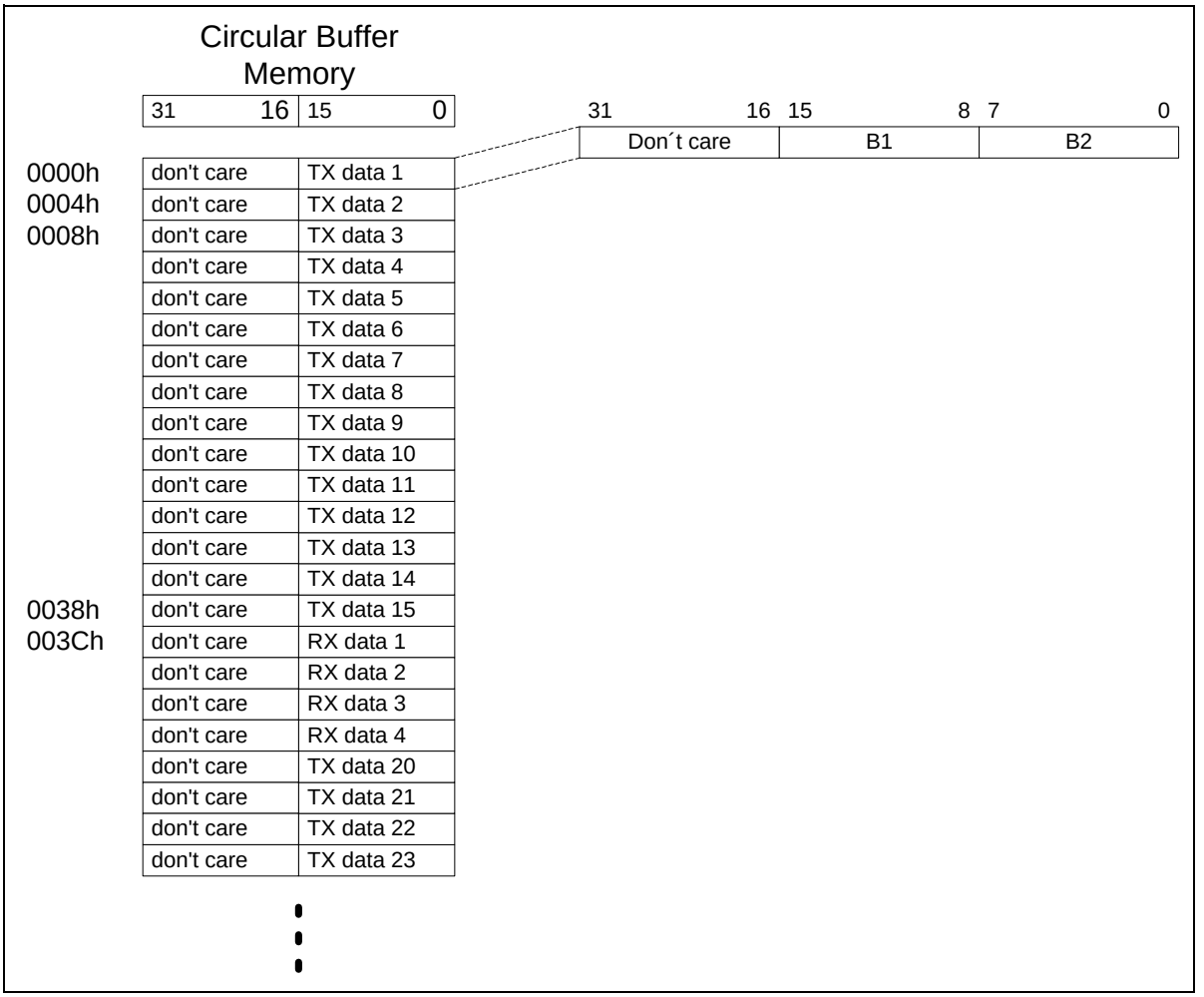
Bit 31:02	Actual Circular Buffer Pointer
Type	R
Default Value	0000 0000h
Bit 1:0	Actual Circular Buffer Pointer
Type	H
Default Value	00b
Description	By reading this register the software has access to the PCI address in the DMA circular buffer address pointer. The bits 31-12 are equal the contents of the Circular Buffer Start Address Register. The bits 11-0 represent the actual dword address in the circular buffer.

Internal Register: 1Ch

Bit 11:0	DMA Write Count Register
Type	RW
Default Value	000h
Description	

5.1.2 IOM-2 Mode 1

Transmission and Reception of Data in the Circular Buffer



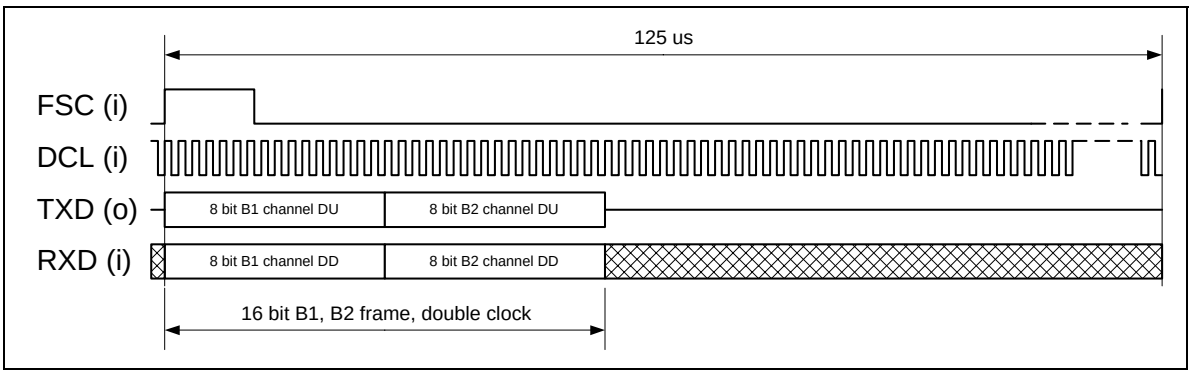
Data in Circular Buffer and on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Bits from circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Write to serial DMA interface: B1 [7:0] B2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Receive	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]

Timing Diagram



Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 4 ('001000'): IOM-2 Mode 1** With the DMA_Start bit the DMA transfer can be started or stopped.

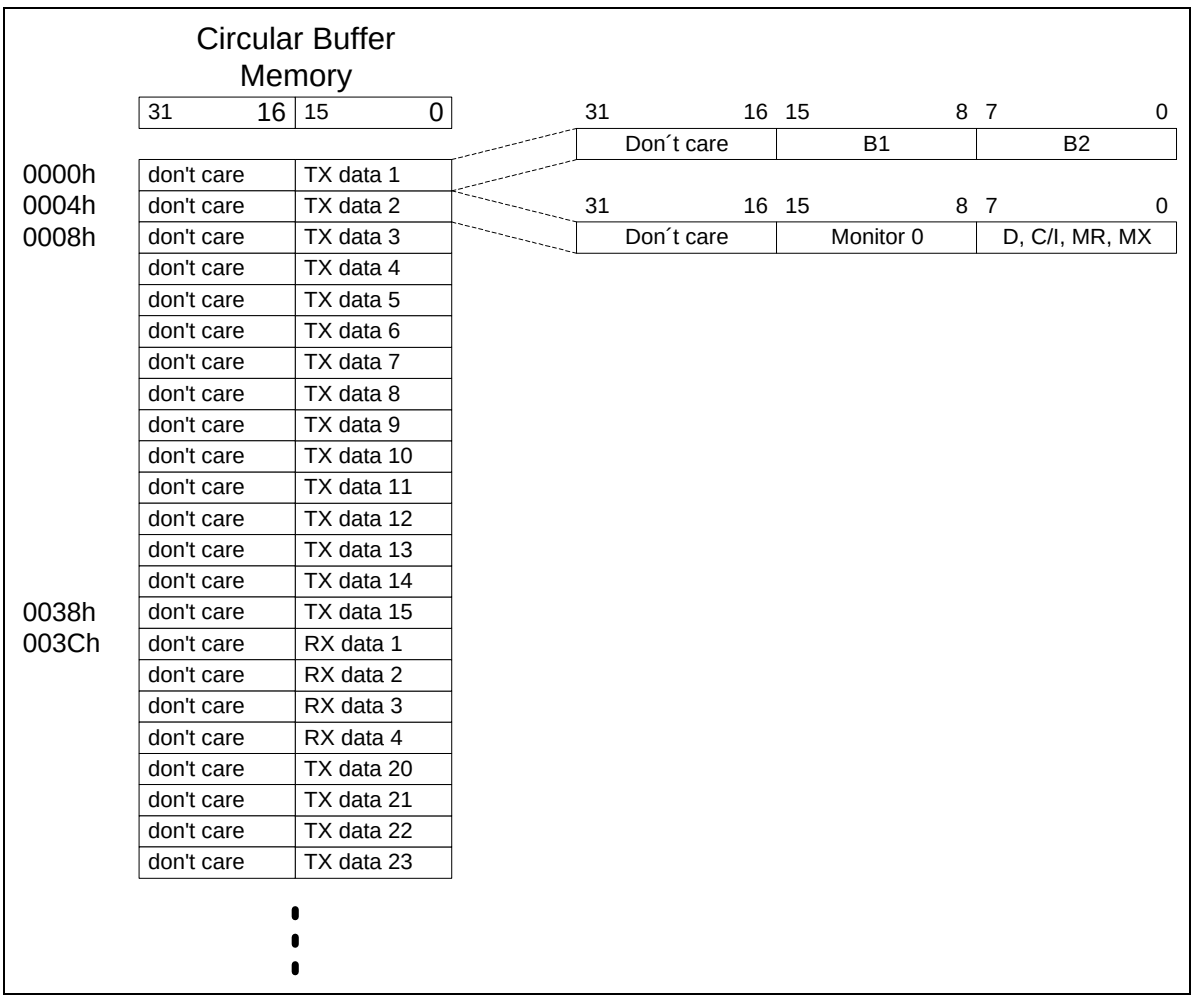
Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1=’0’: The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0=’1’: The serial controller is driven with the external DCL input clock.

5.1.3 IOM-2 Mode 2

Transmission and Reception of Data in the Circular Buffer



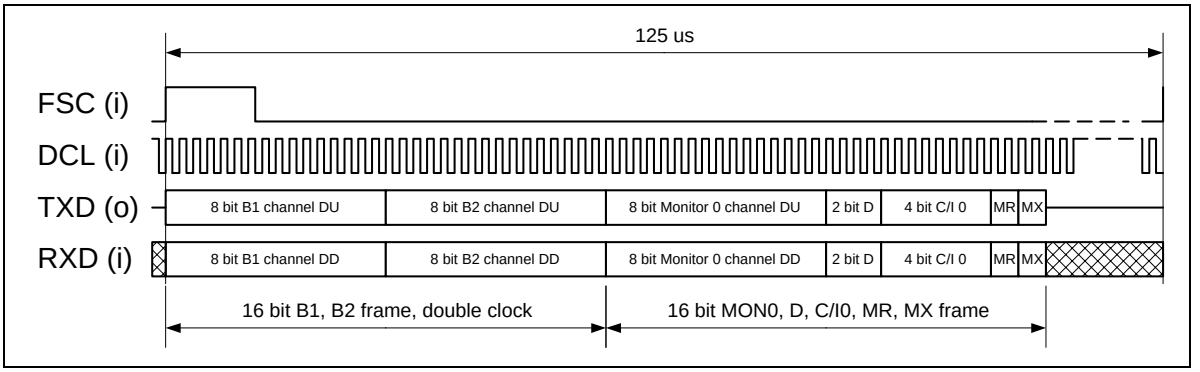
Data in Circular Buffer and on Serial DMA Interface

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	0, 2, 4, ...	Bits from circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Write to serial DMA interface: B1 [7:0] B2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	1, 3, 5, ...	Bits from circular buffer: [31:16] = don't care [15:8] = Monitor 0 [7:0] [7:0] = D,C/I0,MR,MX [7:0]	Write to serial DMA interface: Monitor 0 [7:0] D,C/I0,MR,MX [7:0]
Receive	0, 2, 4, ...	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]
	1, 3, 5, ...	Bits to circular buffer: [31:16] = don't care [15:8] = Monitor 0 [7:0] [7:0] = D,C/I0,MR,MX [7:0]	Read from serial DMA interface: Monitor 0 [7:0] D,C/I0,MR,MX [7:0]

Timing Diagram



Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 5 ('010000'): IOM-2 Mode 2** With the DMA_Start bit the DMA transfer can be started or stopped.

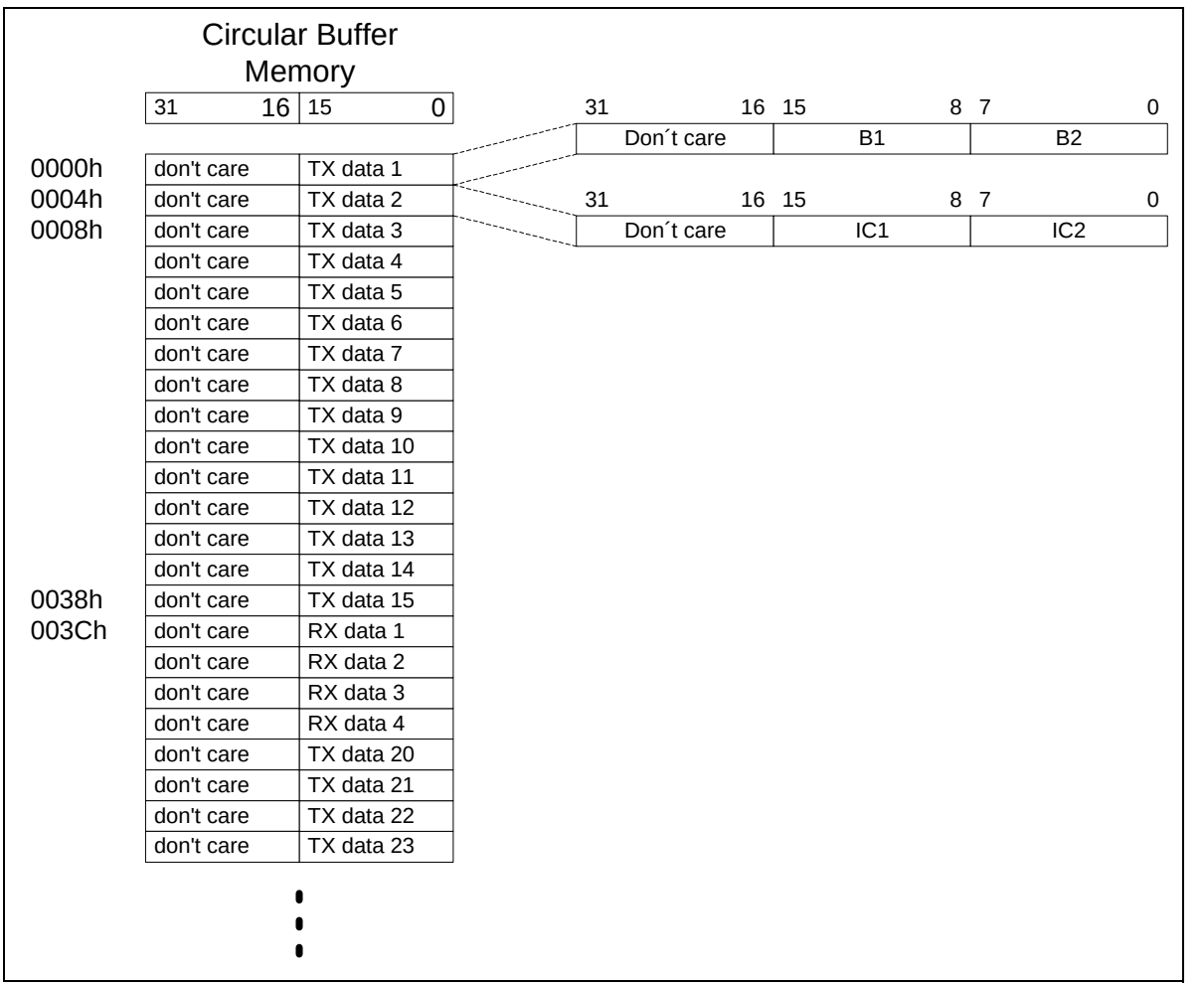
Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.4 IOM-2 Mode 3

Transmission and Reception of Data in the Circular Buffer



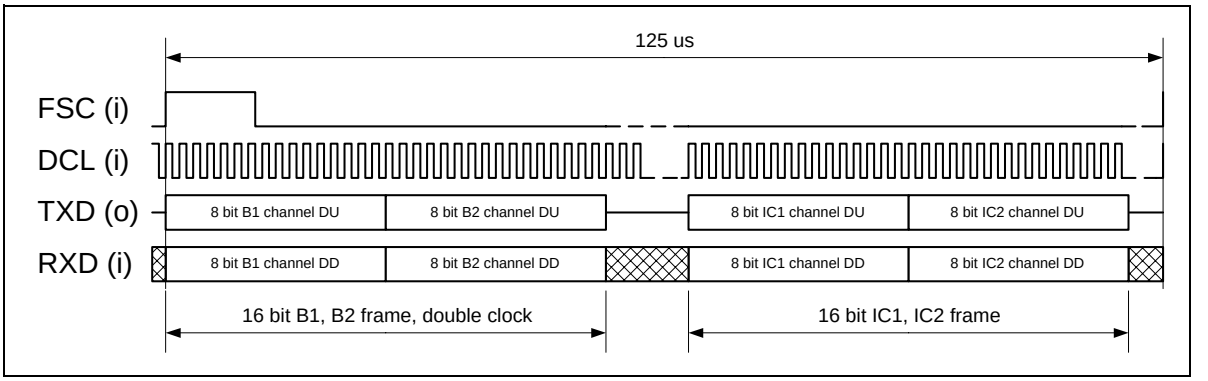
Data in Circular Buffer and on Serial DMA Interface

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	0, 2, 4, ...	Bits from circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Bits to serial DMA interface: B1 [7:0] B2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	1, 3, 5, ...	Bits from circular buffer: [31:16] = don't care [15:8] = IC1 [7:0] [7:0] = IC2 [7:0]	Write to serial DMA interface: IC1 [7:0] IC2 [7:0]
Receive	0, 2, 4, ...	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]
	1, 3, 5, ...	Write to circular buffer: [31:16] = don't care [15:8] = IC1 [7:0] [7:0] = IC2 [7:0]	Read from serial DMA interface: IC1 [7:0] IC2 [7:0]

Timing Diagram



Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 6 ('100000'): IOM-2 Mode 3** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.5 IOM-2 Modes - Supplementary Description

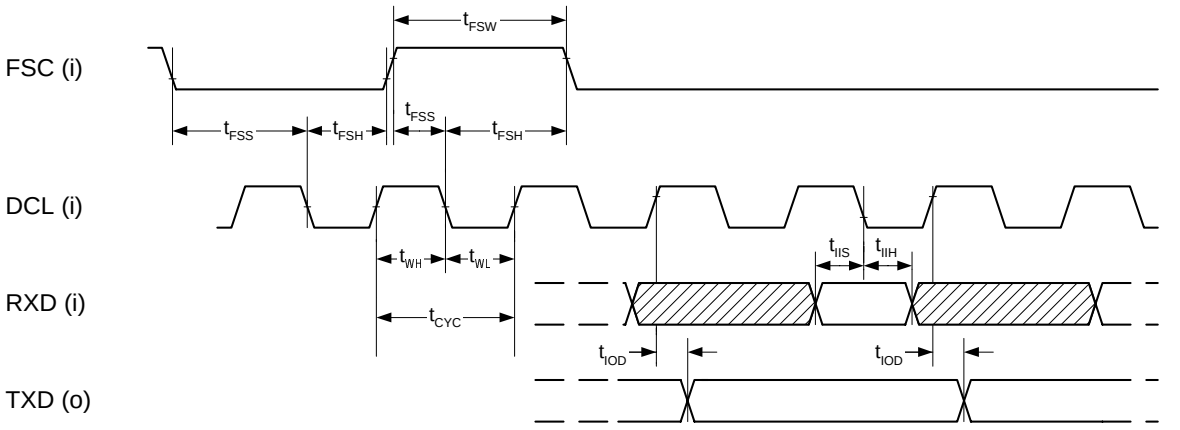
Selection of IOM-2 Time Slots

The MISC register contains four bits. They are used for masking the time slot on IOM-2.

If Bx_MSK (x := [1,4]) is set:

- The corresponding value from the TX FIFO is not written to the DU line.
- FFh is written to this time slot.
- In IOM-2 mode 1 the bits B3_MSK and B4_MSK have no effect.
- Data is always transferred from the IOM-2 time slot to the RX-FIFO.

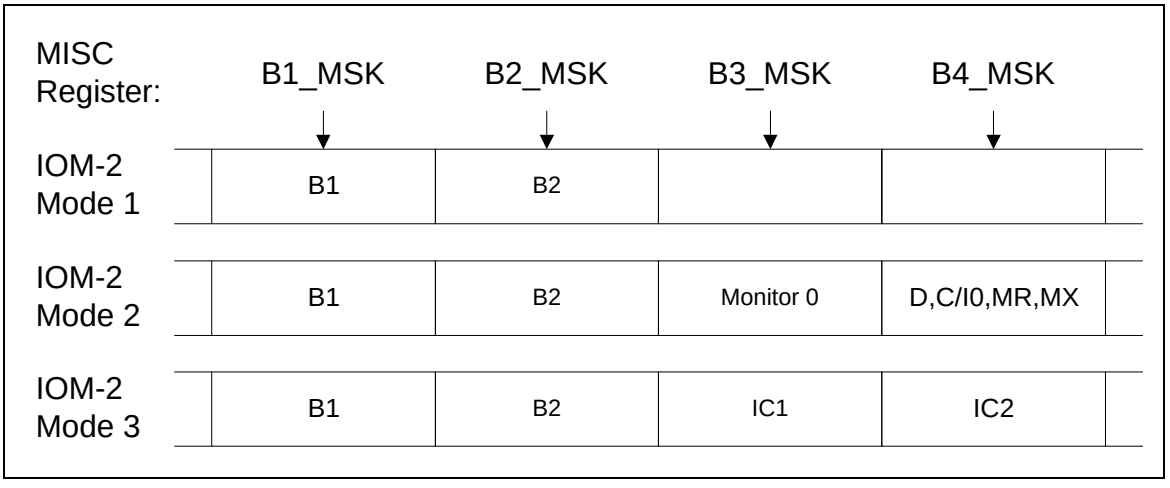
Timing Diagram for all IOM-2 Modes



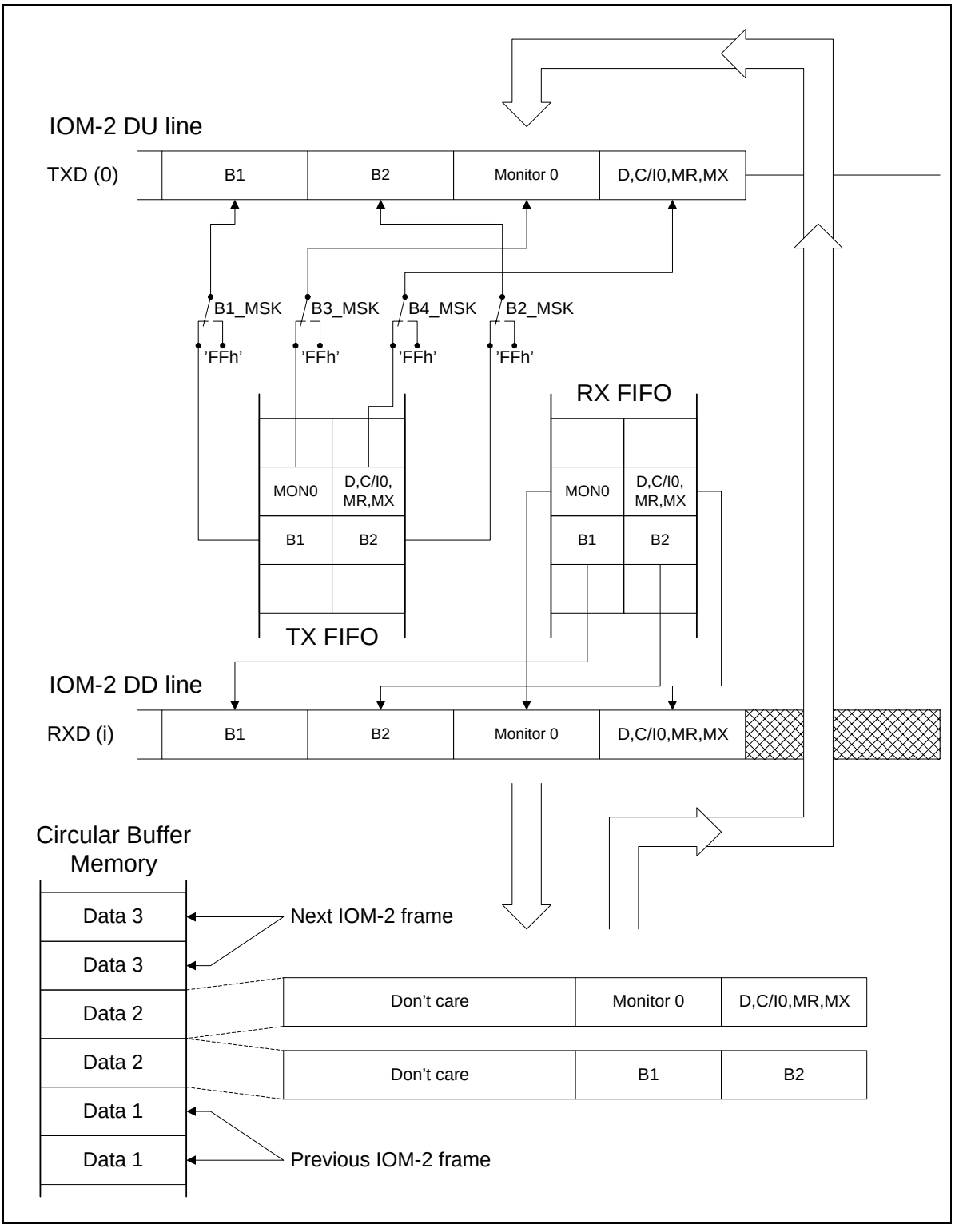
Abbreviations for the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC pulse width	t_{FSW}	40		ns
FSC setup time	t_{FSS}	40		ns
FSC hold time	t_{FSH}	40		ns
DCL cycle time	t_{CYC}	244		ns
DCL HIGH time	t_{WH}	100		ns
DCL LOW time	t_{WL}	100		ns
IOM output data delay	t_{IOD}		100	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	20		ns

Figure of the MISC Register B1 - B4 Mask Bits



Masking of IOM-2 Time slots (Example for IOM-2 Mode 2)



Internal Register: 1Ch

Bit 31:0	MISC (Miscellaneous Register)

Bit 31	IOM_B1_masking
Type	RW
Default Value	0b
Description	Bit 31=’0’: Byte B1 is generated out of the circular buffer. Bit 31=’1’: FFh is transmitted on the B1 time slot.

Bit 30	IOM_B3_masking
Type	RW
Default Value	0b
Description	Bit 30=’0’: Byte B1 is generated out of the circular buffer. Bit 30=’1’: FFh is transmitted on the B2 time slot.

Bit 29	IOM_Monitor_0 / IC1_masking
Type	RW
Default Value	0b
Description	Bit 29=’0’: Byte Monitor 0 or IC1 is generated out of the circular buffer. Bit 29=’1’: FFh is transmitted on the Monitor/IC1 time slot. Monitor is used in IOM-2 mode 2. IC1 is used in IOM-2 mode 3.

Internal Register: 1Ch (cont'd)

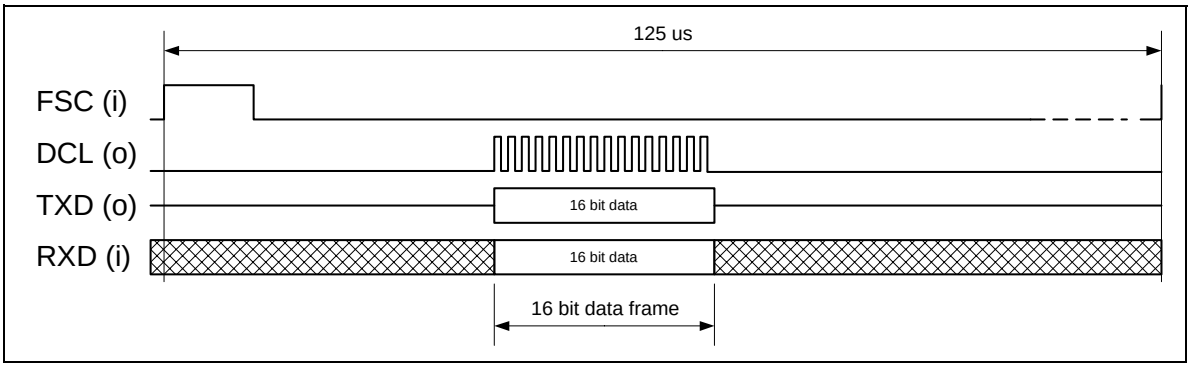
Bit 28	IOM_Supl_masking / IC2_masking
Type	RW
Default Value	0b
Description	Address:='0': Byte D, C/I0, MR, MX or IC2 is generated out of the circular buffer. Address:='1': FFh is transmitted on the D, C/I0, MR, MX or IC2 time slot. D, C/I0, MR, MX: Used in IOM-2 mode 2. IC2: Used in IOM-2 mode 3

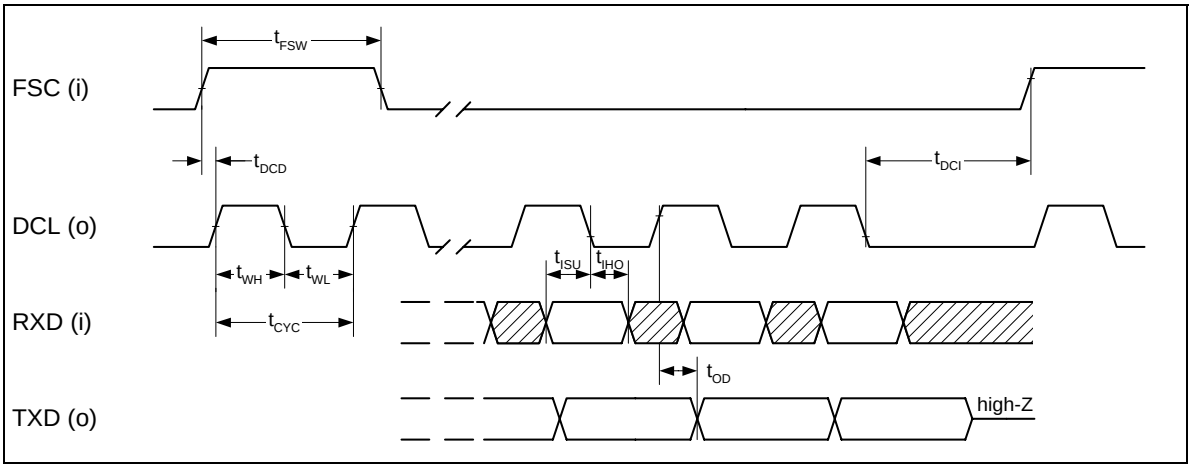
5.1.6 Single Modem Mode V2.1

Data in Circular Buffer and on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Bits from circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Write to serial DMA interface: data frame [15:0]
Receive	Bits to circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Read from serial DMA interface: data frame [15:0]

Timing diagrams





Abbreviations for the Timing Diagram

Parameter	Symbol	PCI Clock Cycles	Limit Values			Unit
			min.	typ.	max.	
FSC pulse width	t_{FSW}		40			ns
DCL delay	t_{DCD}	16	480			ns
DCL idle time	t_{DCI}			105		µs
DCL cycle time	t_{CYC}	40		1200		ns
DCL HIGH time	t_{WH}	20		600		ns
DCL LOW time	t_{WL}	20		600		ns
DCL duty cycle			45	50	55	%
Input data setup	t_{ISU}		10			ns
Input data hold	t_{IHO}		10			ns
Output data delay	t_{OD}				10	ns

Configuration of the Single Modem Mode V2.1 after a System/Soft Reset

- The configuration of the PSB4596 V2.1 in single modem mode is realized by software using the 4-bit General Purpose I/O Interface of the PITA (See “General Purpose I/O Interface” on page 5-65.).
- After a system/soft reset the FSC is an input pin both for
  – the PITA
  – the ALIS V2.1
- After a system reset the DCL_Out_En bit must be set to ’1’ by the host.

PITA Configuration for ALIS V2.1 after a System Reset

Serial DMA Interface Mode	Ser_Clock_Sel (clock input to Serial DMA interface)		DCL_Out_En (DCL Direction)	
ALIS V2.1	0	PCI clock/ 40	1	DCL output

Note

A Pull Down resistor is required on the board to avoid a floating FSC signal in this situation.

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 1 (’000001’): Single Modem Mode V2.1** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1=’1’: The DCL signal is output (open drain) and driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0=’0’: The serial controller is driven with the clock signal generated by the internal clock divider.

5.1.7 Single Modem Mode ALIS V3.X

Overview

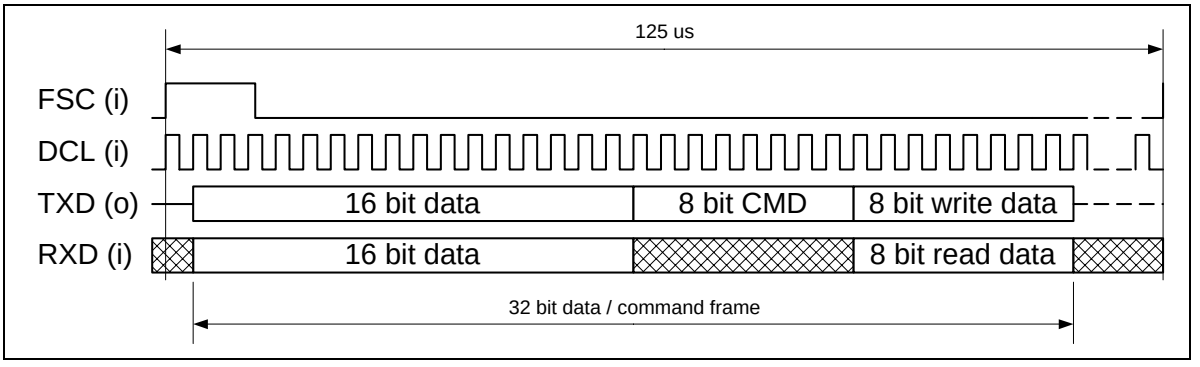
Overview	Page
Information about the Single Modem Mode ALIS V3.X	5-34
Internal Registers of the Single Modem Mode V3.X	5-36

5.1.7.1 Information about the Single Modem Mode ALIS V3.X

Data in Circular Buffers, on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Read from circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Write to serial DMA interface: data frame [15:0]
Receive	Write to circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Read from serial DMA interface: data frame [15:0]

Timing Diagram



Note

The timing characteristics of the serial DMA interface in Single modem mode V3.X mode are identical to the IOM-2 modes with the only difference that the DCL signal is not a double bit clock, but a single bit clock, similar to Single Modem mode V2.1.

Configuration of the Single Modem Mode V3.X after a System/Soft Reset

- Realized by starting the DMA transfer.
  - Separate from this transfer the command byte and command data byte are written to the ALIS Command Registers in the PITA on addresses 10h.
- After a system/soft reset the single modem mode V3.X is in the multiplexed mode because the non multiplexed mode is not supported.

PITA Configuration for ALIS V3.X after a System Reset

Serial DMA Interface Mode	Ser_Clock_Sel (clock input to Serial DMA interface		DCL_Out_En (DCL Direction)	
ALIS V3.X	1	DCL input clock	0	DCL_Out_En
2×ALIS V3.X	1		0	
ALIS V3.X + second codec	1		0	

5.1.7.2 Internal Registers of the Single Modem Mode V3.X

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 2 ('000010'): Single Modem Mode V3.X** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 10h

Bit 31:0	ALIS Command Register 1
Description	This command register is used for the first command structure in the FSC time slot by the serial controller.

Bit 31:25	Reserved
Type	H
Default Value	0b
Description	Reserved

Internal Register: 10h (cont'd)

Bit 24	New_ALIS_Command_1
Type	RW
Default Value	0b
Description	Bit 24='1': The host has written a new command to the ALIS Command Resister 1. Bit 24='0': Last command written to the ALIS Command Register 1 by the host is processed and the received data is available in the ALIS Received Data 1 register. This bit is set by software if there is a new command in the ALIS Command 1 Register. After the serial DMA interface has transmitted the new command and the received data is written to the ALIS_Received_Data_1 bits, this bit is reset by the serial DMA interface.

Bit 23:16	ALIS_Received_Data_1
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 2 or 3 every time a new command is transferred through the serial DMA interface, the received data is fetched and saved in this register. New command means: The command was written through the PCI interface to the ALIS command register. Transferring a NOP command (FFh or 00h) leads to skipping of the received data.

Internal Register: 10h (cont'd)

Bit 15:8	ALIS_Command_1
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 2 or 3 the contents of this register are transferred as command through the serial DMA interface. After transferring the new command through the serial DMA interface, the register is set to NOP (FFh).

Bit 7:0	ALIS_Transmit_Data_1
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 2 or 3 the contents of this register are transferred as data through the serial DMA interface.

Internal Register: 14h

Bit 31:0	ALIS Command Register 2
Default Value	00000000h

Bit 31:25	Reserved
Type	H
Default Value	000h
Description	Reserved

Bit 24	New_ALIS_Command_2
Type	RW
Default Value	0b
Description	Bit 24=’1’: The host has written a new command to the ALIS Command 2 Register. Bit 24=’0’: Last command written to the ALIS Command 2 Register by the host is processed and the received data is available in the ALIS Received Data 2 Register. This bit is set by software if there is a new command in the ALIS Command 2 Register. After the serial controller has transmitted the new command and the received data is written in the ALIS Received Data 2 Register, this bit is reset by the serial controller.

Internal Register: 14h (cont'd)

Bit 23:16	ALIS_Received_Data_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 every time a new command is transferred through the serial DMA interface, the received data is fetched and saved in this register. New command means: The command was written through the PCI interface to the ALIS V3.X command register. If only a NOP command (FFh or 00h) is transferred the received data is skipped.

Bit 15:8	ALIS_Command_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 the contents of this register are transferred as command through the serial DMA interface. After transferring the new command through the serial DMA interface, the register is set to NOP (FFh).

Bit 7:0	ALIS_Transmit_Data_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 the contents of this register are transferred as data through the serial interface.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1=’0’: The DCL signal is input and driven by the PITA.

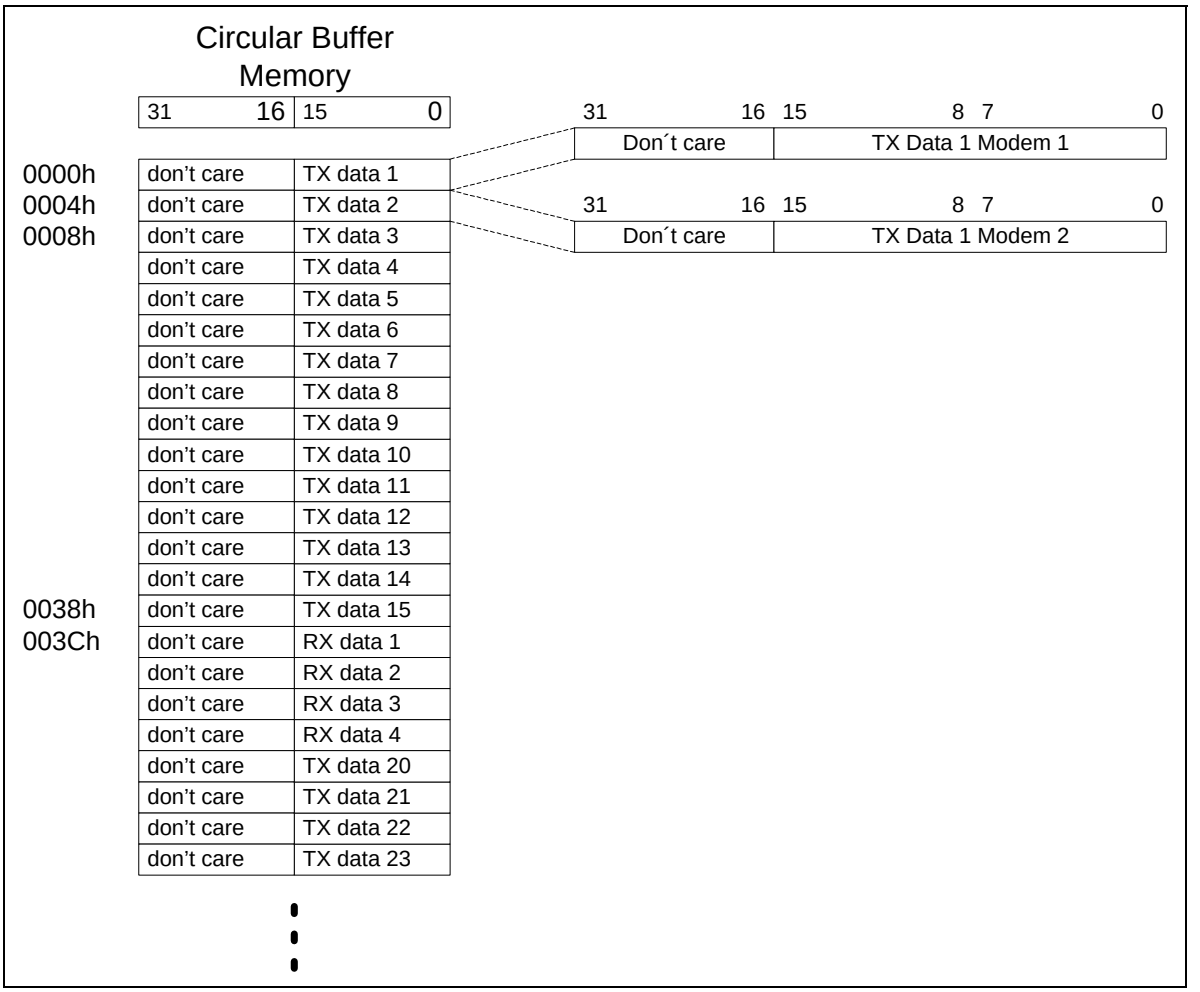
Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0=’1’: The serial controller is driven with the external DCL input clock.

5.1.8 Dual Modem/Modem+Voice Mode

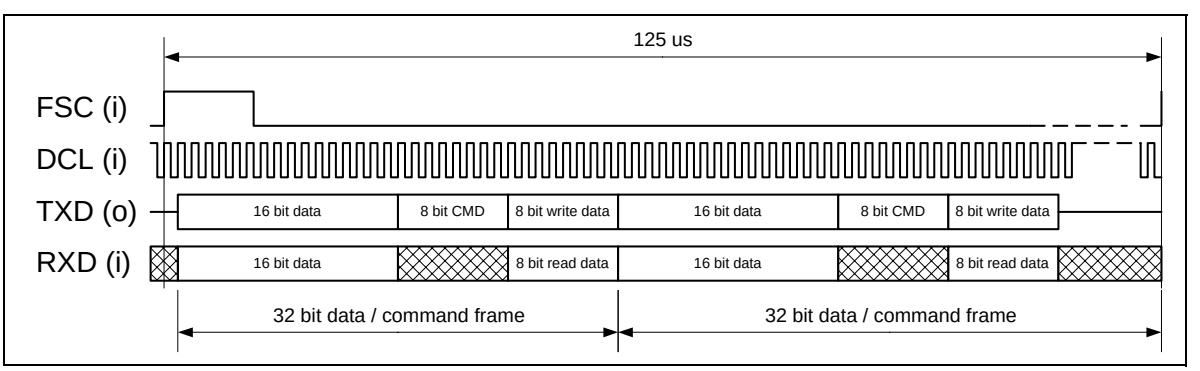
Description

- The PITA transmits and receives two 32 bit frames per FSC time slot.
- Each 32 bit frames consists of 16 bit data and 16 bit command/data information.
- For each of the 32 bit frames the 16 bit transmitted data is read out of the TX FIFO.
- The 16 bit transmitted data is written to the RX FIFO.
- The command read/write data for the first 32 bit frame is read out/written to the ALIS Command Register 1 (10h)
- The command read/write data for the second 32 bit frame is read out/written to the ALIS Command Register 2 (14h).
- The internal DMA write counter is incremented every second write transfer to the circular buffer.
- A new frame transmission starts if the FSC is sampled ’1’ at a negative edge of the DCL signal.
- The PITA starts driving the TXD line with the first bit of the transmitted data at the next positive DCL edge.
- During the transmission the rising DCL edge indicates the start of a bit on the TXD while the falling edge of the DCL is used to latch the RXD signal.
- The PITA stops driving the TXD signal with the positive DCL edge when bit 32 of the first or second transmitted frame is on the TXD line.

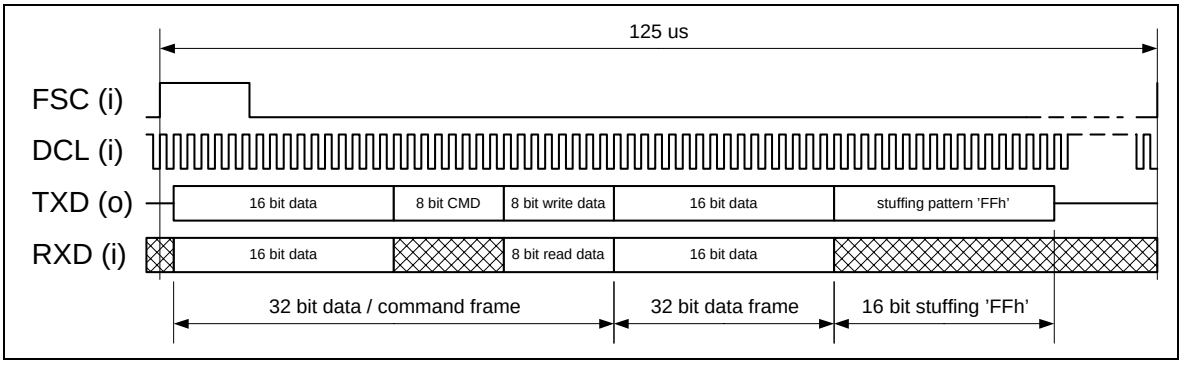
Data Organization in the Circular Buffer



Timing Diagram for the Dual Modem Mode



Timing Diagram for the Dual Modem+Voice Mode



Description of the Timing Diagram

- The second 32 bit frame only consists of the 16 bit voice data.
- The voice data is read out the TX FIFO.
- The voice data is transmitted through the serial DMA interface (MSB first).
- During this transmission the received 16 bit voice data (MSB first) is written to the RX FIFO.

Internal Registers: 04h

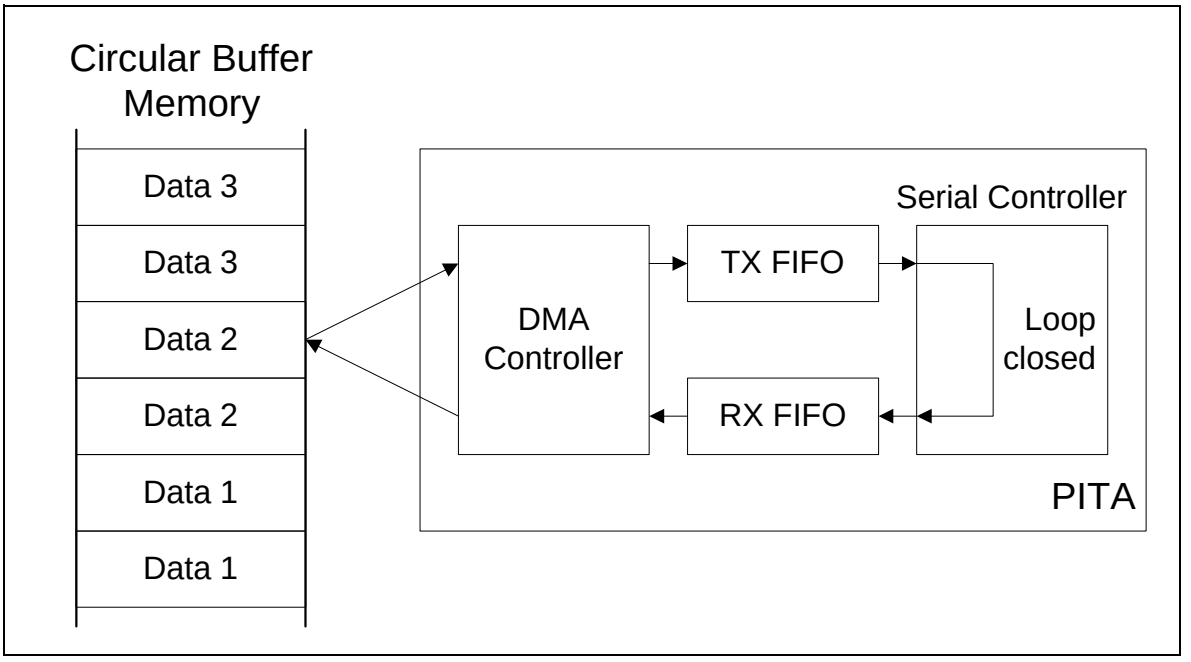
Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 3 ('000100'): Single Dual Modem/Modem + Voice Mode V3.X** With the DMA_Start bit the DMA transfer can be started or stopped.

5.1.9 Loop Back Mode

Description

If Loop_Back_Mode is set to ’1’ transmit data is transferred from the TX FIFO back to the RX FIFO.

Mode Diagram



Internal Register: 28h

Bit 0	Loop_Back_Mode
Type	RW
Default Value	0b
Description	• Bit 0=’0’: The serial controller transmits and receives data/ commands through the serial DMA interface (normal operation mode). • Bit 0=’1’: The serial controller is in loop back mode. – The serial DMA interface reads the data in the transmitting FIFO and writes them in the receiving FIFO. – No data/command transmission will take place on the serial DMA interface. – The serial DMA interface is clocked with the defined Ser_Clock_Sel bit.

5.2 Parallel Interface

Description

The PITA has an 8 bit parallel interface to support three external components.
This parallel interface is implemented in multiplexed and non multiplexed mode.
It works in Siemens/Intel bus mode.
The parallel interface is by default in the non multiplexed mode.

Internal Register: 1Ch

Bit 26	Parallel_ interface_mode
Type	RW
Default Value	0b
Description	Bit 26=’0’: non multiplexed mode Bit 26=’1’: multiplexed mode

Bit 24	Softreset_parallel_mode
Type	RW
Default Value	0b
Description	Bit 24=’0’: Deactivates the reset signal PRST to the application. Bit 24=’1’: Activates the high active reset signal PRST to the application.

Mapping between PCI Data and Parallel Interface Data

Data on the PCI bus AD31-0	PCI Byte Enables $\overline{\text{C/BE3-0}}$	Data on the Parallel Interface Data bus PAD7-0
AD[31-8] = Don't Care AD[7-0] = Parallel Interface Data	"XXX0"	PAD[7-0] = AD[7-0]
AD[31-8] = Don't Care AD[7-0] = Parallel Interface Data	"XXX1"	No transaction, PCI interface disconnects with Target Abort.

Address Mapping of the 4-kbyte PCI Address Space to the Parallel Interface

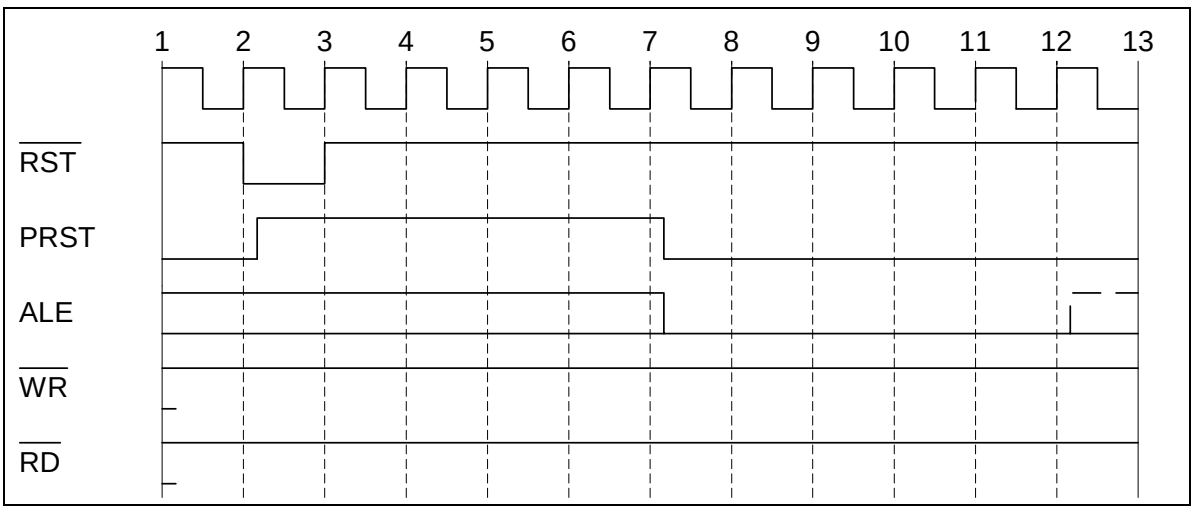
Address on the PCI address bus AD11-0	Chip Select on the parallel interface	Address on the parallel interface address bus PAD7-0 = AD9-2 (mux mode) PA7-0 = AD9-2 (non-mux mode)
3FFh - 000h	$\overline{\text{CS2-0}}$ = "110"	FFh - 00h
7FFh - 400h	$\overline{\text{CS2-0}}$ = "101"	FFh - 00h
BFFh - 800h	$\overline{\text{CS2-0}}$ = "011"	FFh - 00h
FFFh - C00h	$\overline{\text{CS2-0}}$ = "111"	(not used)

Modes and Timing of the Parallel Interface

Modes and Timing	Page
ALE after System Reset	5-50
ALE after internal Software Reset	5-51
ALE after setting the Parallel Interface Mode Bit	5-52
Non Multiplexed Mode (Write Transaction)	5-53
Non Multiplexed Mode (Read Transaction)	5-54
Multiplexed Mode (Write Transaction)	5-55
Multiplexed Mode (Read Transaction)	5-56
Transaction Disconnect with Target Abort	5-57
Transaction Termination with Retry	5-60
Timing of the Parallel Interface	5-62

5.2.1 ALE after System Reset

Timing Diagram

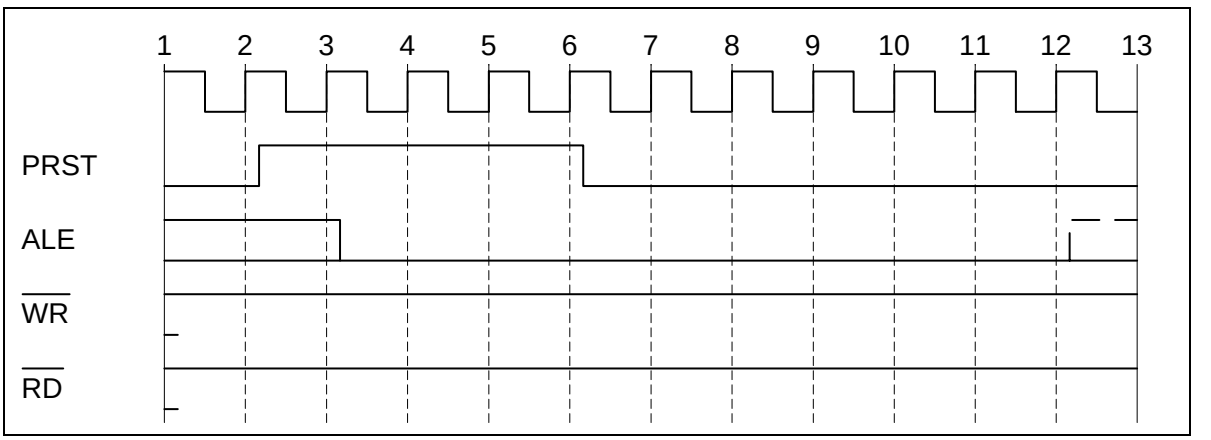


Description

Both ALE and PRST are high during $\overline{RST}$ and remain high for a maximum of 4 cycles after $\overline{RST}$ goes deasserted.

5.2.2 ALE after internal Software Reset

Timing Diagram

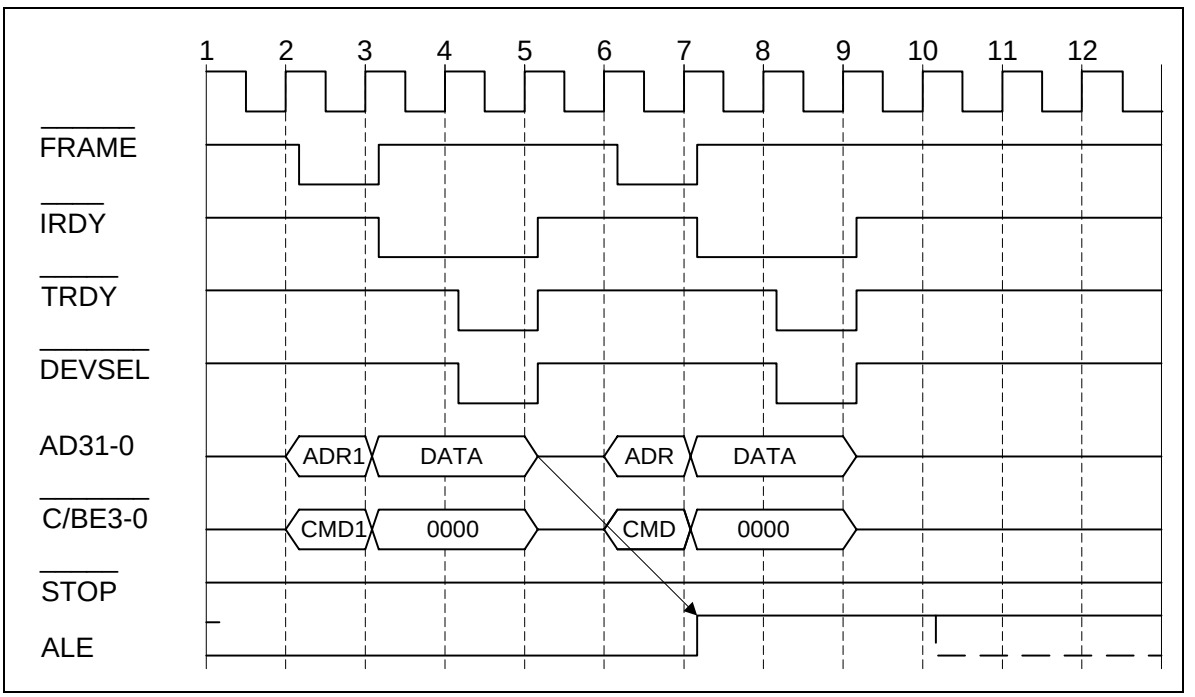


Description

- After the internal Soft Reset is deasserted the same behavior as in „ALE after System Reset“ generated.
- The soft reset bit in the internal registers can only be set or reset if the parallel interface is in idle state.
- If ALE is high before PAR_RST is asserted, it goes to low one cycle after PRST and takes the new value depending on the PAR_MOD bit in the 6th cycle after PRST is deasserted.

5.2.3 ALE after setting the Parallel Interface Mode Bit

Timing Diagram

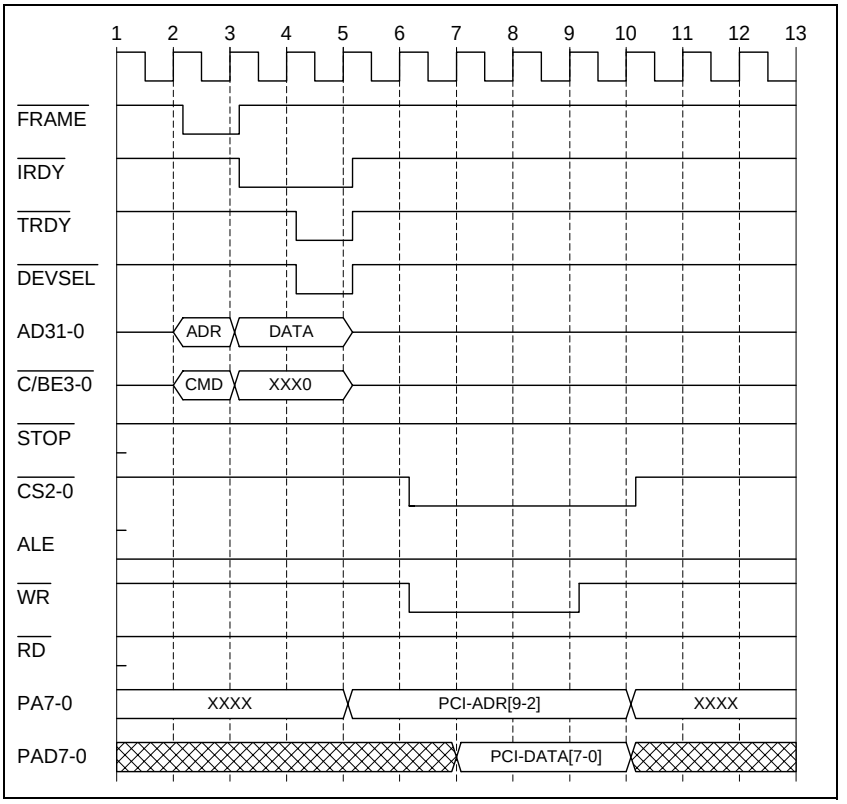


Description

- The parallel interface is in non multiplexed mode by default.
- To set the parallel interface into multiplexed mode:
  The Parallel_Interface_Mode bit has to be set to ’1’ after reset.
- Two PCI clocks after finishing this data phase the ALE signal is asserted.

5.2.4 Non Multiplexed Mode (Write Transaction)

Timing Diagram

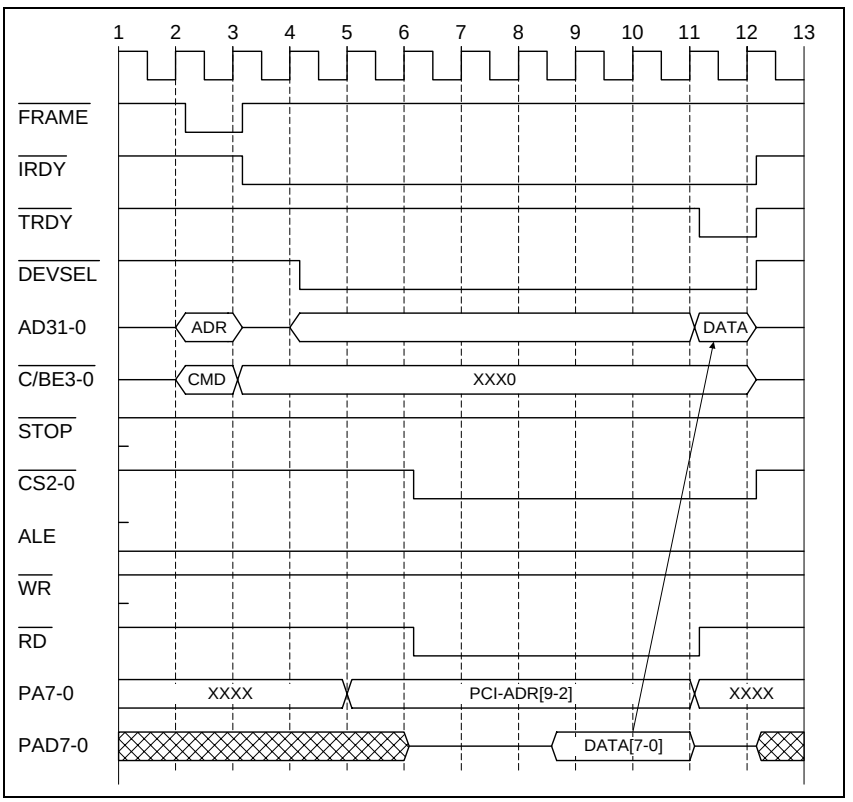


Description

- After the address phase on the PCI bus (clock3) and the $\overline{\text{C/BE0}}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0.
- One PCI clock after the PCI data phase is finished the data from the PCI bus is placed on the data bus PAD7-0 (clock 5) and the write transaction starts.
- The data is placed from the PCI bus on PAD7-0 asserting the $\overline{\text{WR}}$ signal and a $\overline{\text{CS2-0}}$ signal.
- A new access to the parallel interface could be accepted with an address phase at clock 9. Any access before would be cancelled with Retry because the PCI Interface is processing the last access.

5.2.5 Non Multiplexed Mode (Read Transaction)

Timing Diagram

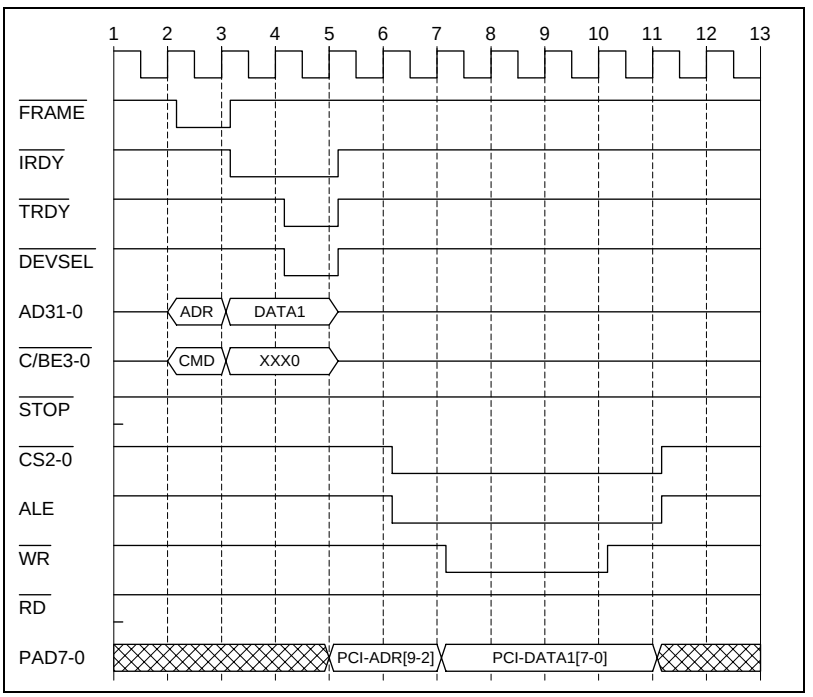


Description

- After the address phase on the PCI bus (clock3) and the $\overline{C/BE0}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0 (clock 5).
- The following PCI clock asserts the signals $\overline{RD}$ and $\overline{CS2\text{-}0}$.
- After 5 clocks the $\overline{RD}$ signal is deasserted.
- The data from PAD7-0 is fetched.
- With the next clock the data is placed on the PCI bus and the data phase is finished by deasserting the $\overline{TRDY}$ signal.
- The 8 bit data from the parallel interface is placed an the last significant byte of the PCI data bus AD7-0.

5.2.6 Multiplexed Mode (Write Transaction)

Timing Diagram

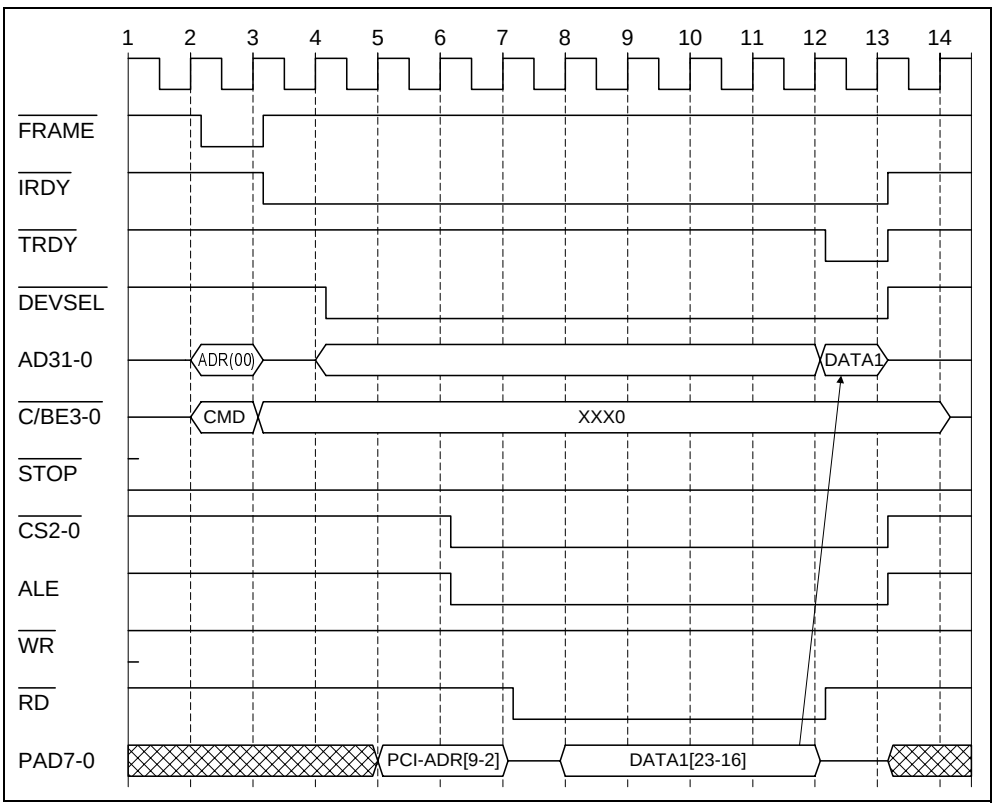


Description

- After the address phase on the PCI bus (clock 3) and the $\overline{C/BE0}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface address is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0.
- One PCI clock after the PCI data phase is finished the data from the PCI bus is placed on the data bus PAD7-0 (clock 5) and the write transaction starts.
- The data is placed from the PCI bus on PAD7-0 asserting the $\overline{CS2-0}$ signal.
- The ALE signal is deasserted.
- With the following PCI clock the data from the PCI bus is placed on PAD7-0 (clock5).
- The $\overline{WR}$ signal is asserted.
- A new access to the parallel interface could be accepted with an address phase at clock 11. Any access before would be cancelled with Retry because the PCI Interface is processing the last access.

5.2.7 Multiplexed Mode (Read Transaction)

Timing Diagram

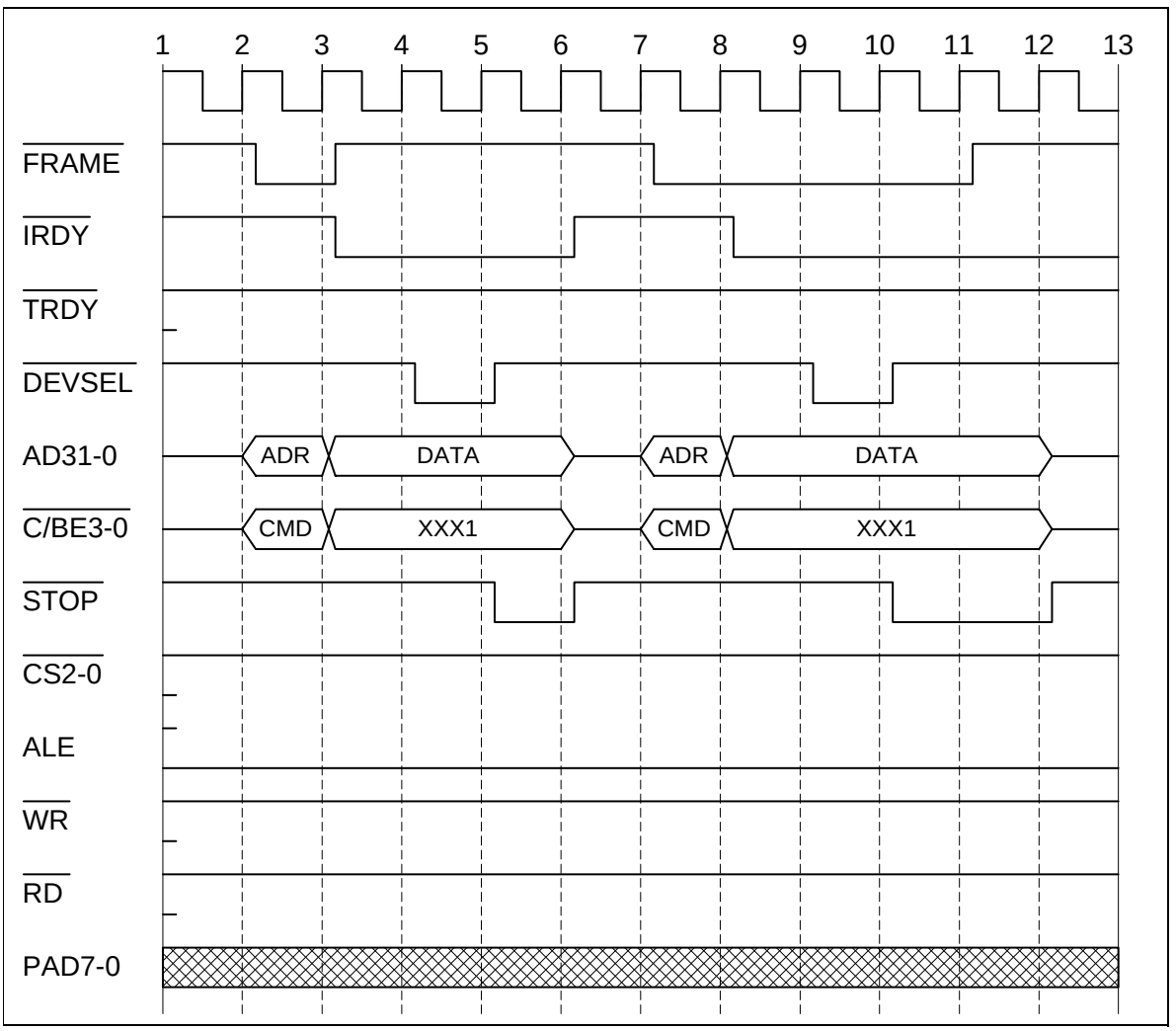


Description

- After the address phase on the PCI bus (clock 3) and the C/BE0=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0 (clock 5).
- The following PCI clock asserts the ALE signal.
- After 2 clocks the ALE signal is deasserted.
- The address is held for one more clock.
- After 5 clocks the RD signal is deasserted.
- At the same time the data is latched in die PCI output registers.
- TRDY is asserted on the PCI bus to finish the data phase.
- At the next clock the CS2-0 and ALE signals are deasserted.

5.2.8 Transaction Disconnect with Target Abort

Timing Diagram



Description

$\overline{C/BE0}$ = 1: No transaction is started on selected parallel interface, due to the wrong byte enable. The PCI Master Target Controller disconnects the transaction with target abort.

Configuration Space Register: 04h

Bit 30	System_Error_Signaled
Type	RC
Default Value	0b
Description	This bit is set by the PITA's PCI Master, if the master asserts the system error signal on the PCI bus. This occurs if a transaction initiated by the PITA is disconnected with target abort.

Bit 29	Master_Abort_Detected
Type	RC
Default Value	0b
Description	If no fast/medium/slow or subtractive slave reacts to a PCI transaction initiated by the PCI Master, the master will discard the transaction and set this bit.

Bit 28	Master_Abort_Detected
Type	RC
Default Value	0b
Description	If a PCI transaction initiated by the PCI Master is disconnected with Target Abort, the PCI master will set this bit. The PCI Master is not allowed to start a new PCI transaction, until this bit is deasserted.

Configuration Space Register: 04h (cont'd)

Bit 27	Target_Abort_Signaled
Type	RC
Default Value	0b
Description	This bit is set by the PCI interface if a transaction was disconnected with Target Abort. The PITA will disconnect transactions with Target Abort if illegal byte enables are detected.

Bit 8	System_Error_Enable
Type	RW
Default Value	0b
Description	If this bit is asserted, the PCI Master will assert the System Error Signal ($\overline{SERR}$) if it receives a target abort during a transaction initiated by itself.

Bit 2	Master_Enable
Type	RW
Default Value	0b
Description	If this bit is set to '0' the PCI Master is not allowed to start any transaction on the PCI Bus.

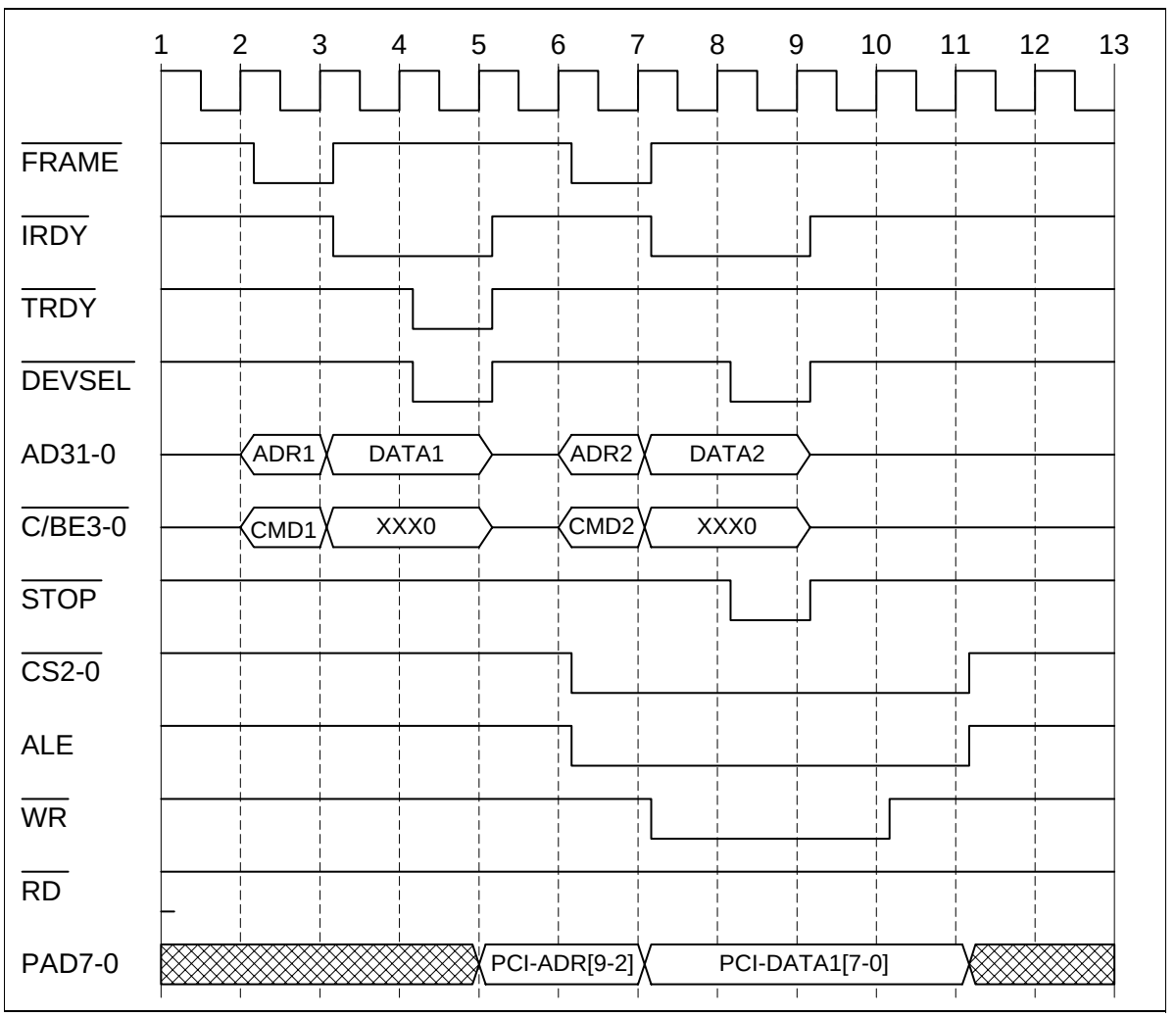
5.2.9 Transaction Termination with Retry

Description’

Retry means that the PITA finishes a transaction without a data transfer by asserting the signal $\overline{\text{STOP}}$, because the parallel interface processes another transaction.

The PCI Master Target Controller has to repeat the transaction until a slave accepts the transaction with data transfer or target abort. This sequence is invisible for the software.

Timing Diagram



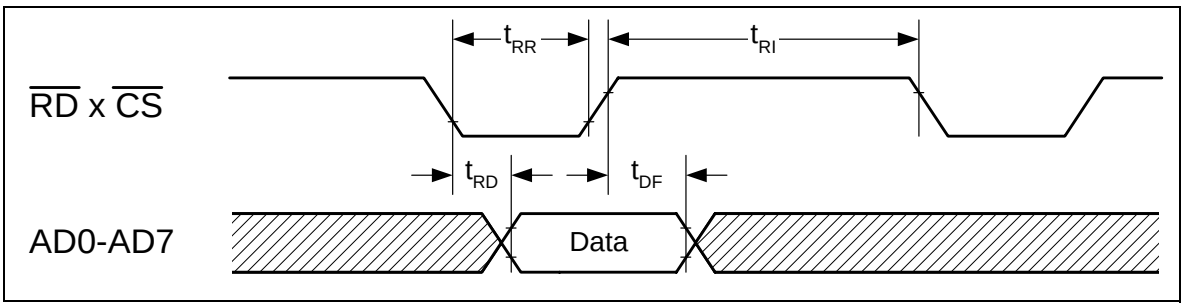
Explanation of ADR/CMD and ADR2/CMD2

ADR/CMD: The PCI Master Target Controller accepts the write transaction

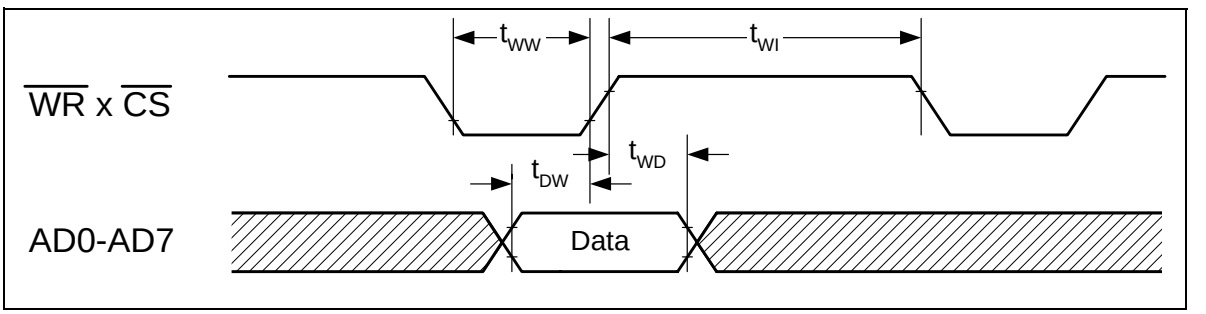
ADR2/CMD2: The second transaction is retried.

5.2.10 Timing of the Parallel Interface

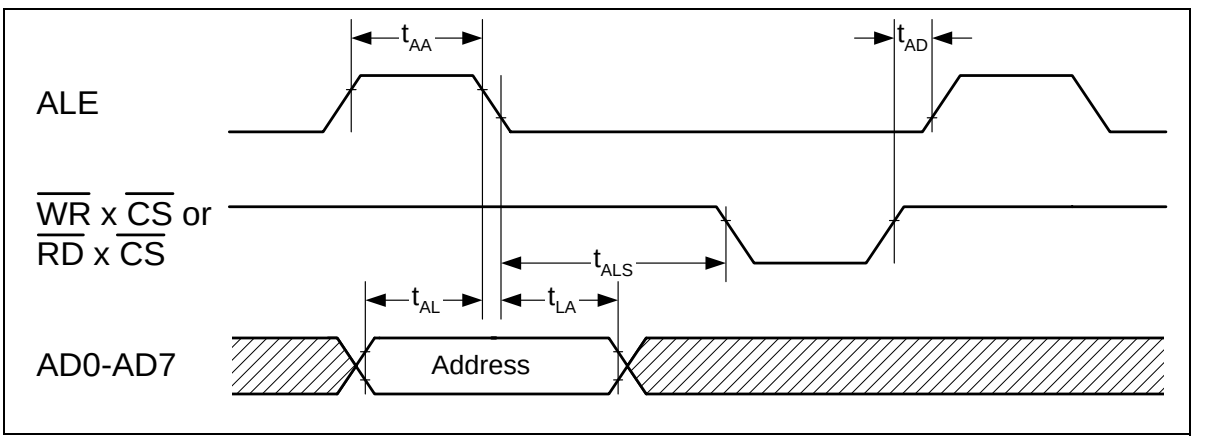
Read Timing



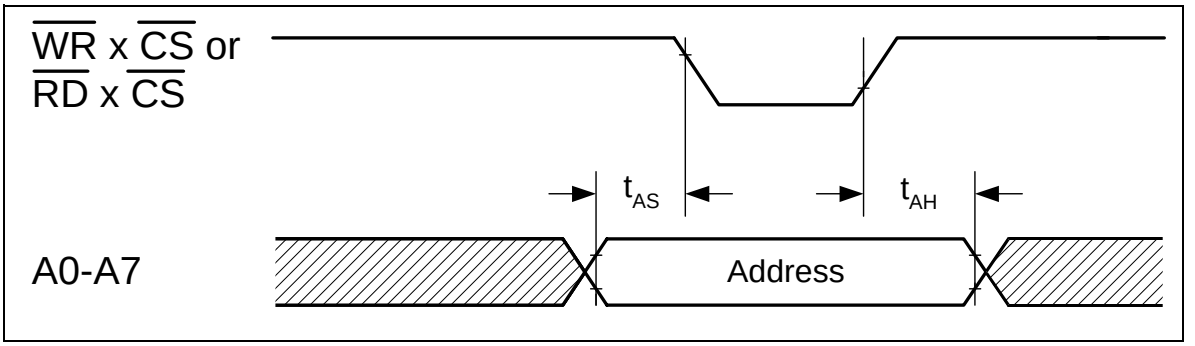
Write Timing



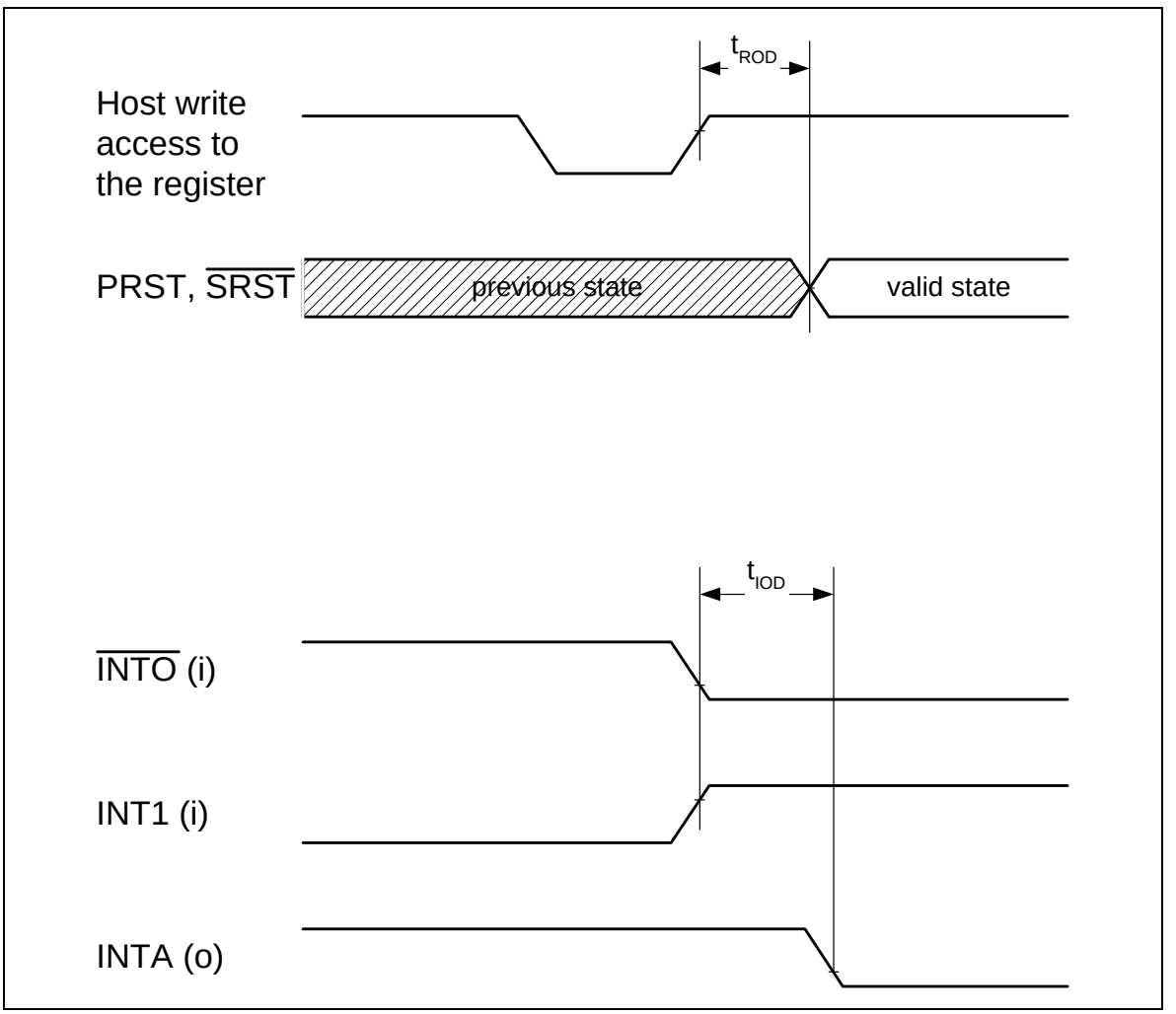
Multiplexed Address Timing



Non Multiplexed Address Timing



Application Reset and Interrupt Timing



Abbreviations of the Timing Diagrams

Parameter	Sym-bol	PCI Clock Cycles	Limit Values		Unit
			min.	max.	
ALE pulse width	t_{AA}	5	150		ns
Address setup time to ALE	t_{AL}	1	30		ns
Address hold time from ALE	t_{LA}	1	30		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	1	30		ns
Address setup time	t_{AS}	1	30		ns
Address hold time	t_{AH}	1	30		ns
ALE guard time	t_{AD}	1	30		ns
$\overline{RD}$ pulse width	t_{RR}	5	150		ns
Data output delay from $\overline{RD}$	t_{RD}	5		150	ns
Data float from $\overline{RD}$	t_{DF}	1		30	ns
$\overline{RD}$ control interval	t_{RI}	5	150		ns
$\overline{W}$ pulse width	t_{WW}	3	90		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	2	60		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	1	30		ns
$\overline{W}$ control interval	t_{WI}	3	90		ns
Reset Output Delay	t_{ROD}	3		90	ns
Interrupt Output Delay	t_{IOD}	2		60	ns

5.3 General Purpose I/O Interface

Overview

Overview	Page
Information about the GP I/O Interface	5-66
Timing of the GP I/O Interface	5-68
Internal Registers of the GP I/O Interface	5-69
Input Mode	5-76
Output Mode	5-78
Interrupt Mode	5-80
Usage of the GP I/O Interface as ALIS V2.1 Control Interface	5-82

5.3.1 Information about the GP I/O Interface

Description

For additional access to external devices with a slow interface behavior a 4 bit General Purpose I/O interface is implemented in the PITA.

Pinning

Pin	Pin Name	General Purpose I/O Function	SPI EEPROM Function
2	GP0	I/O/Int.	SO
3	GP1	I/O/Int.	SI
4	GP2	I/O/Int.	SCK
5	GP3	I/O/Int.	–

Application Interrupt

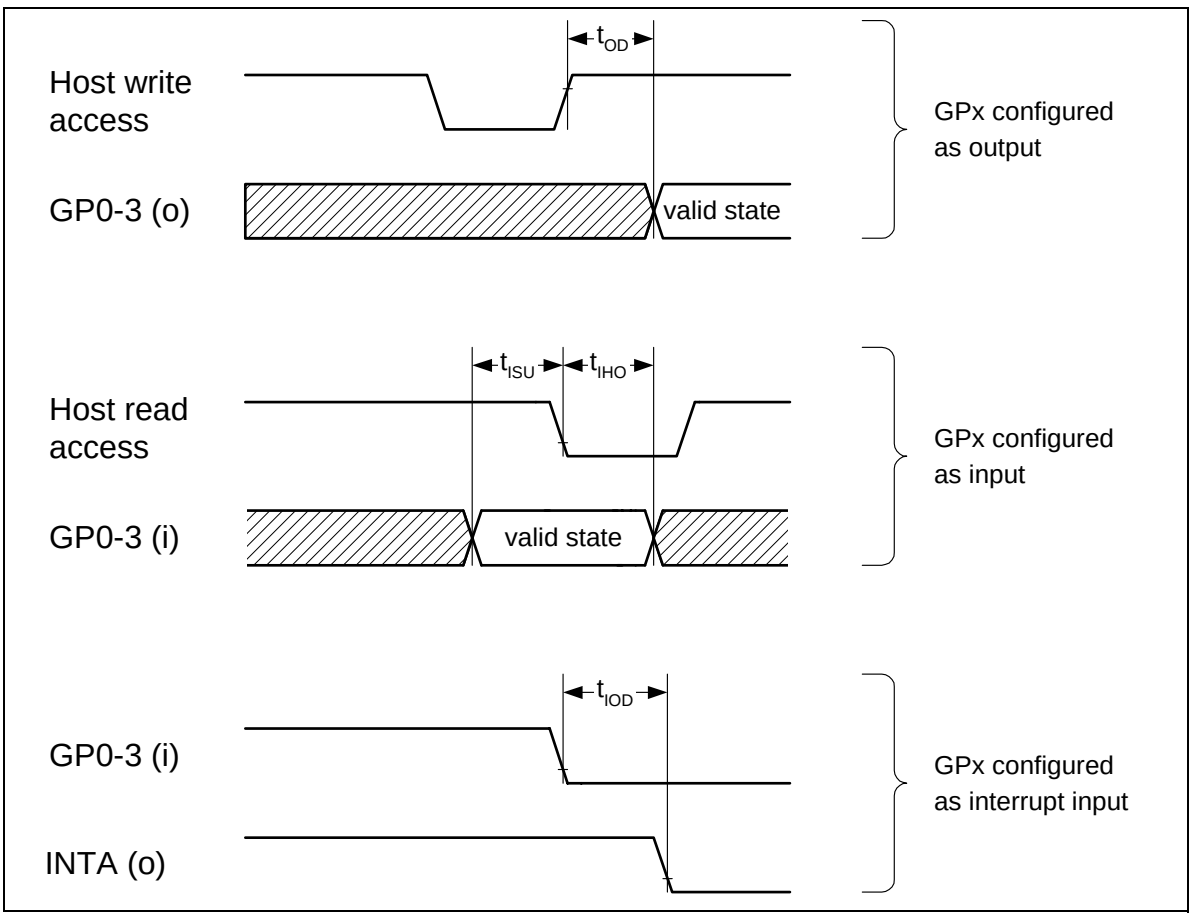
- The PCI interface supports 2 separate interrupt inputs.
- Four pins of the general purpose I/O interface can be used as additional interrupt inputs.
- Each of these 6 interrupts has an Interrupt_Enable bit and an Interrupt_Control_Status bit.
- For the two separate inputs ($\overline{INT0}$ and INT1) the enable bit is located in the Interrupt Control Register.
- For the General Purpose I/O the enable bit is located in the Interface Control Register.

Control Registers for GPx Pins

Register	Register Bit	Description
Interrupt Control Register - ICR	GPx_INT	GP Interrupt Status
GP I/O Interface Control Register	GPx_INT_En	GP Interrupt Enable
	GPx_OUT_En	GP Output Enable
	GPx_OUT	GP Output Value
	GPx_IN	GP Input Value

5.3.2 Timing of the GP I/O Interface

Timing Diagram



Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
GPx Output Data Delay	t_{OD}		90	ns
GPx Input Data Setup	t_{ISU}	30		ns
GPx Input Data Hold	t_{IHO}	30		ns
GPx Interrupt Output Delay	t_{IOD}		90	ns

5.3.3 Internal Registers of the GP I/O Interface

Internal Register: 00h

Bit 5	GP3_INT
Type	RC
Default Value	0b
Description	The GP3 pin can be used as ’active low’ interrupt input if GP3_Int_En=’1’ and GP3_Out_En=’0’. The bit is set to ’1’ if both are true and low is detected at this pin.

Bit 4	GP2_INT
Type	RC
Default Value	0b
Description	The GP2 pin can be used as ’active low’ interrupt input if GP2_Int_En=’1’ and GP2_Out_En=’0’. The bit is set to ’1’ if both are true and low is detected at this pin.

Bit 3	GP1_INT
Type	RC
Default Value	0b
Description	The GP1 pin can be used as ’active low’ interrupt input if GP1_Int_En=’1’ and GP1_Out_En=’0’.

Internal Register: 00h (cont'd)

Bit 2	GP0_INT
Type	RC
Default Value	0b
Description	The GP0 pin can be used as 'active low' interrupt input if GP0_Int_En='1' and GP0_Out_En='0'.

Internal Register: 18h

Bit 31:0	GP I/O Interface Control Register
Type	00000000h

Bit 31:28	Reserved
Type	H
Default Value	0h
Description	Reserved

Bit 27	GP3_Int_En
Type	RW
Default Value	0b
Description	Bit 27='1': GP3 is configured as input, the pin is used as an interrupt input with GP3_Int_en as corresponding bit in the Interrupt Control Register. Bit 27='1': GP3 is not used as an interrupt pin.

Internal Register: 18h (cont'd)

Bit 26	GP2_Int_En
Type	RW
Default Value	0b
Description	Bit 26='1': GP2 is configured as input, the pin is used as an interrupt input with GP2_Int_en as corresponding bit in the Interrupt Control Register. Bit 26='0': GP2 is not used as an interrupt pin.

Bit 25	GP1_Int_En
Type	RW
Default Value	0b
Description	Bit 25='1': GP1 is configured as input, the pin is used as an interrupt input with GP1_Int_en as corresponding bit in the Interrupt Control Register. Bit 25='0': GP1 is not used as an interrupt pin.

Bit 24	GP0_Int_En
Type	RW
Default Value	0b
Description	Bit 24='1': GP0 is configured as input, the pin is used as an interrupt input with GP0_Int_en as corresponding bit in the Interrupt Control Register. Bit 24='0': GP0 is not used as an interrupt pin.

Internal Register: 18h (cont'd)

Bit 23:20	Reserved
Type	H
Default Value	000b
Description	Reserved

Bit 19	GP3_Out_En
Type	RW
Default Value	0b
Description	Bit 19='1': GP_3 is configured as output pin. Bit 19='0': GP_3 is configured as input pin.

Bit 18	GP2_Out_En
Type	RW
Default Value	0b
Description	Bit 18='1': GP_2 is configured as output pin. Bit 18='0': GP_2 is configured as input pin.

Bit 17	GP1_Out_En
Type	RW
Default Value	0b
Description	Bit 17='1': GP_1 is configured as output pin. Bit 17='0': GP_1 is configured as input pin.

Internal Register: 18h (cont'd)

Bit 16	GP0_Out_En
Type	RW
Default Value	0b
Description	Bit 16='1': GP_0 is configured as output pin. Bit 16='0': GP_0 is configured as input pin.

Bit 15:12	Reserved
Type	H
Default Value	000b
Description	Reserved

Bit 11	GP3_IN
Type	R
Default Value	0b
Description	Actual Value on the GP3 pin (pin feedback)

Bit 10	GP2_IN
Type	R
Default Value	0b
Description	Actual Value on the GP2 pin (pin feedback)

Internal Register: 18h (cont'd)

Bit 9	GP1_IN
Type	R
Default Value	0b
Description	Actual Value on the GP1 pin (pin feedback)

Bit 8	GP0_IN
Type	R
Default Value	0b
Description	Actual Value on the GP0 pin (pin feedback)

Bit 7:4	Reserved
Type	H
Default Value	0000b
Description	Reserved

Bit 3	GP3_OUT
Type	RW
Default Value	0b
Description	The GP3 pin is driven with the value written to this output register if the GP3_OUT_En is set to '1'.

Internal Register: 18h (cont'd)

Bit 2	GP2_OUT
Type	RW
Default Value	0b
Description	The GP2 pin is driven with the value written to this output register if the GP2_OUT_En is set to '1'.

Bit 1	GP1_OUT
Type	RW
Default Value	0b
Description	The GP1 pin is driven with the value written to this output register if the GP1_OUT_En is set to '1'.

Bit 0	GP0_OUT
Type	RW
Default Value	0b
Description	The GP0 pin is driven with the value written to this output register if the GP0_OUT_En is set to '1'.

5.3.4 Input Mode

Description

For using a general purpose I/O pin as input pin, the control register must be configured as follows:

GPx_OUT_En = ‘0’ (Output disabled)

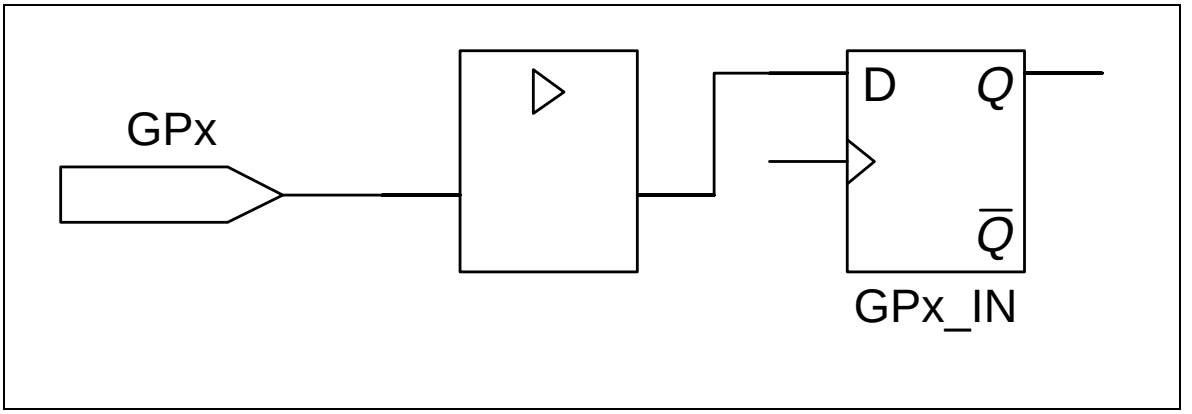
GPx_INT_En = ‘0’ (Interrupt disabled)

(x := [0, 3])

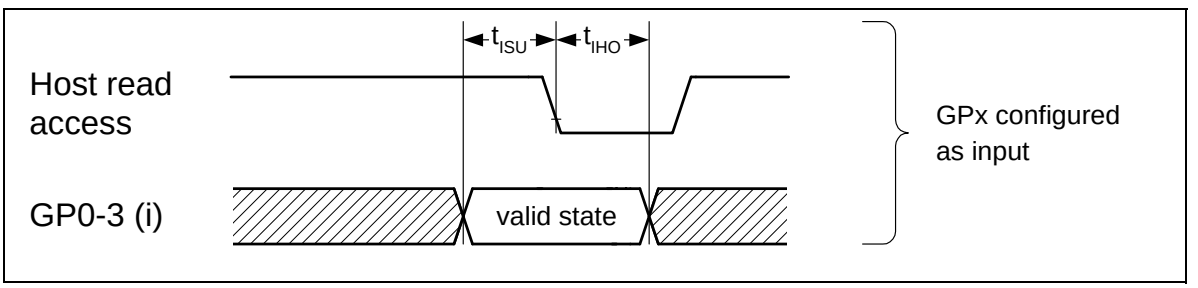
Description of the internal register 18h on page 5-70.

The GPx_OUT and GPx_INT bits can be treated as don’t care in this mode. The current signal value at the pin GPx can be read from register bit GPx_IN.

Internal Structure of a GPx Input Pin



Timing Diagram



Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
GPx Input Data Setup	t_{ISU}	30		ns
GPx Input Data Hold	t_{IHO}	30		ns

5.3.5 Output Mode

Description

For using a general purpose I/O pin as output pin, the control register must be configured as follows:

GPx_OUT_En = ‘1’ (Output enabled)

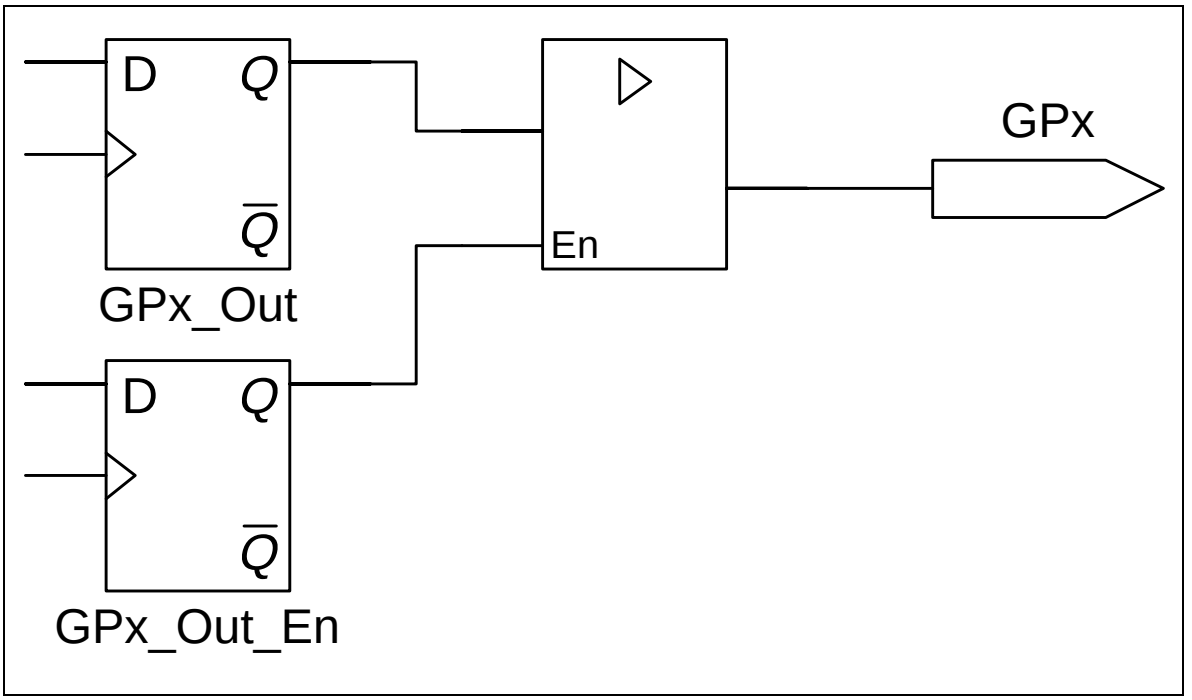
GPx_INT_En = ‘don’t care’

(x := [0, 3])

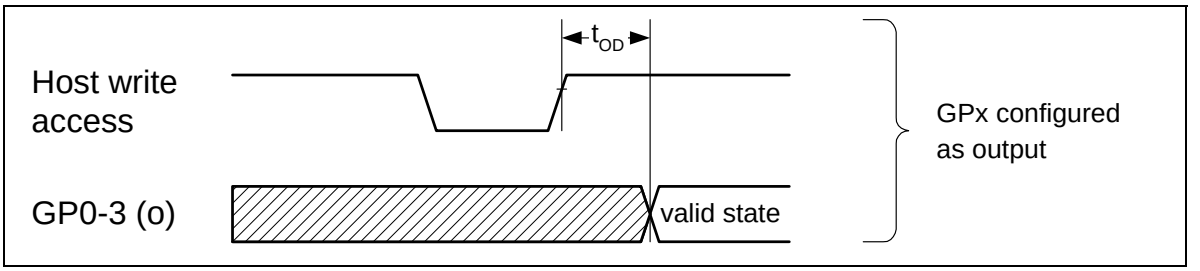
Description of the internal register 18h on page 5-70.

The GPx_IN and GPx_INT register bits can be treated as don’t care in this mode. The GPx pin will drive the connected signal line with the value defined in the GPx_OUT register bit, which is programmed by the host.

Internal Structure of a GPx Output Pin



Timing Diagram



Abbreviation of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
GPx Output Data Delay	t_{OD}		90	ns

5.3.6 Interrupt Mode

Description

For using a general purpose I/O pin as output pin, the control register must be configured as follows:

GPx_OUT_En = ‘1’ (Output disabled)

GPx_INT_En = ‘1’ (Interrupt enabled)

(x := [0, 3])

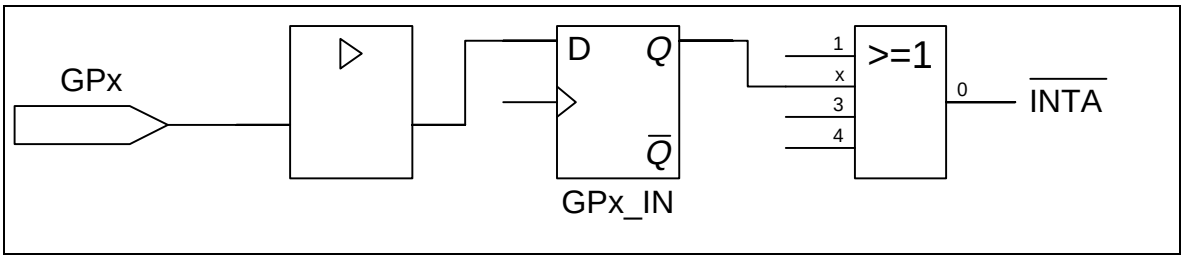
Description of the internal register 18h on page 5-70.

The GPx_OUT register bit can be treated as don’t care in this mode. The GPx pin acts as an active low interrupt input pin.

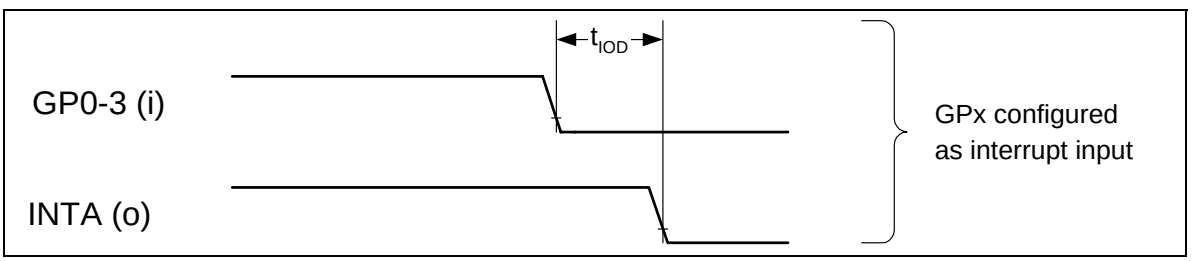
If the device detects ’0’ at the GPx pin

- the GPx_INT register is set to ’1’
- an interrupt on the PCI bus is generated
- the current state of the GPx pin can be read from GPx_IN bit or can be treated as don’t care.

Internal Structure of a GPx Interrupt Input pin



Timing Diagram



Abbreviation of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
GPx Interrupt Output Delay	t_{IOD}		90	ns

5.3.7 Usage of the GP I/O Interface as ALIS V2.1 Control Interface

The serial control interface of the ALIS V2.1 can be realized by software using the General Purpose I/O pins.

The GP3 pin is used as $\overline{CS}$ pin while the other three GPx pins are shared with the SPI EEPROM Interface.

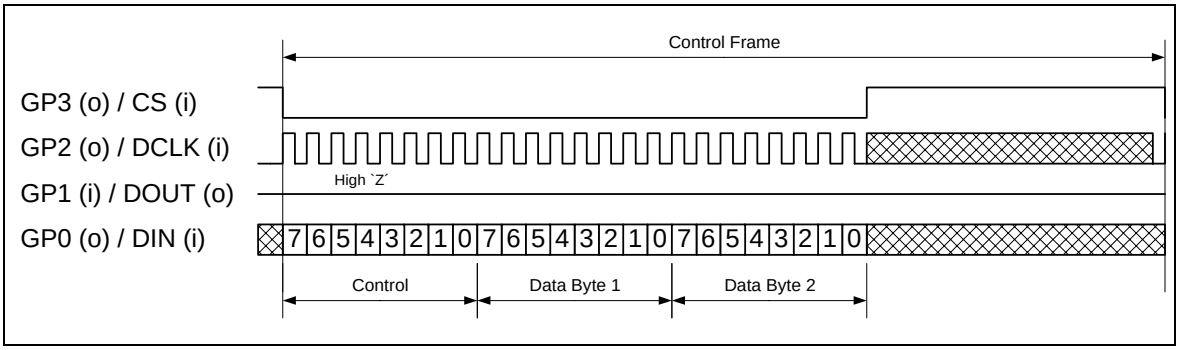
The GP3 pin is driven high during the automatic EEPROM configuration phase after a system reset to disable the ALIS V2.1 control interface.

Pin description on page 7-7.

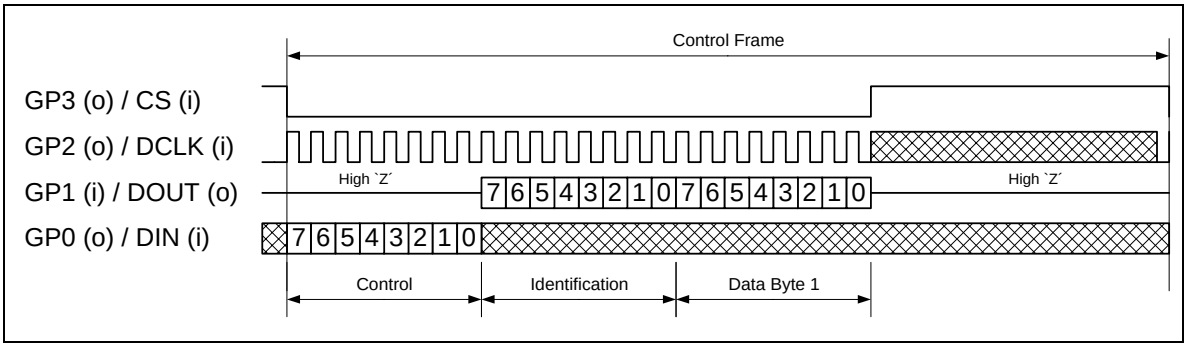
Description

PITA Signals		ALIS Signals	Description
GP3	Out	CS	Chip select (active low), for enabling the PSB4596 Control Interface.
GP2	Out	DCLK	Clock signal for the Control Interface. (PSB4596 accepts 1 kHz to 1024 kHz)
GP1	In	DOUT	Data input for PITA, data output from PSB4596. Data input is latched at the negative DCLK edge.
GP0	Out	DIN	Data output from PITA, data input for PSB4596. Data output changes with the rising DCLK edge.
INT1	In	INT	Interrupt signal (high active)
SRST	Out	RESET	Reset signal (low active)

Timing Diagram for a Write Transaction with two Data Bytes transmitted



Timing Diagram for a Read Access with one Data Byte received via DOUT



5.4 SPI EEPROM Interface

Overview

Overview	Page
Information about the SPI EEPROM Interface	5-85
Timing of the SPI EEPROM Interface	5-88
Internal Registers for the SPI EEPROM Interface	5-90

5.4.1 Information about the SPI EEPROM Interface

Description

Three pins are used to provide an SPI™-compatible serial interface to a 256 x 8 bit EEPROM. These pins also do double-duty as part of the General Purpose Interface. Two other pins are also used to select the EEPROM chip and to enable/ disable the automatic reconfiguration of the configuration space by the EEPROM. This would occur after a system reset.

The EEPROM can be used for:

- Automatic reconfiguration of the PITA.
- Customer specific purposes (e.g. storage of serial board numbers).

Automatic reconfiguration of the PITA

Parts of the PCI Configuration Space can be configured with data from this external EEPROM after system reset. The following sequence is processed by the PITA:

- The PITA checks:
  - Whether the ELD (EEPROM_Load) pin is clamped to ’1’.
  - Whether the first byte in the EEPROM (address location 00h) is AAh.
- If the first step was successful, the PITA starts:
  - Reading out four bytes starting with address 01h.
  - Writing the read values in the configuration space address 00h.
  - Reading out the next four bytes.
  - Writing the read values in the configuration space address 04h.
  - And so on.

Note

During the configuration phase, all access to the PCI interface are answered with ’Retry’ by the PITA.

Using the EEPROM for customer specific purposes

The contents of the EEPROM can be programmed by writing a command to the EEPROM Control Register and initiating a read/write transaction to the EEPROM.

Note

If the automatic reconfiguration of the PITA is used (ELD pin clamped to ’1’), only those addresses in the EEPROM not mapped to the PCI configuration space should be used.

Starting a read or write transaction

The contents of the EEPROM can be programmed by writing a command to the EEPROM Control Register and initiating a read/write transaction to the EEPROM.

- The host writes
  - The EEPROM Command value before the next EEPROM transfer is started.
  - The EEPROM Byte Address value for read or write access.
  - The EEPROM Data value for the ’Write Status Register’ and ’Write Data to Memory Array’.
- The host sets the EEPROM_Start bit.
- If the EEPROM interface detects the asserted EEPROM_Start bit; it
  - Interprets the EEPROM Command.
- Starts the read or write transaction to the connected EEPROM.
- If the transactions are started via the EEPROM Control register, then the EEPROM interface does not check for a connected EEPROM.

After finishing the transaction:

- The EEPROM control module:
  - Deasserts the EEPROM_Start bit.
  - Generates an interrupt in the EEPROM Control Int Register, if the EEPROM_Control_Int_en bit is set to ’1’.
- If The EEPROM Command Register is set to RDSR or READ, then the value of the EEPROM is available in the EEPROM Data Register.

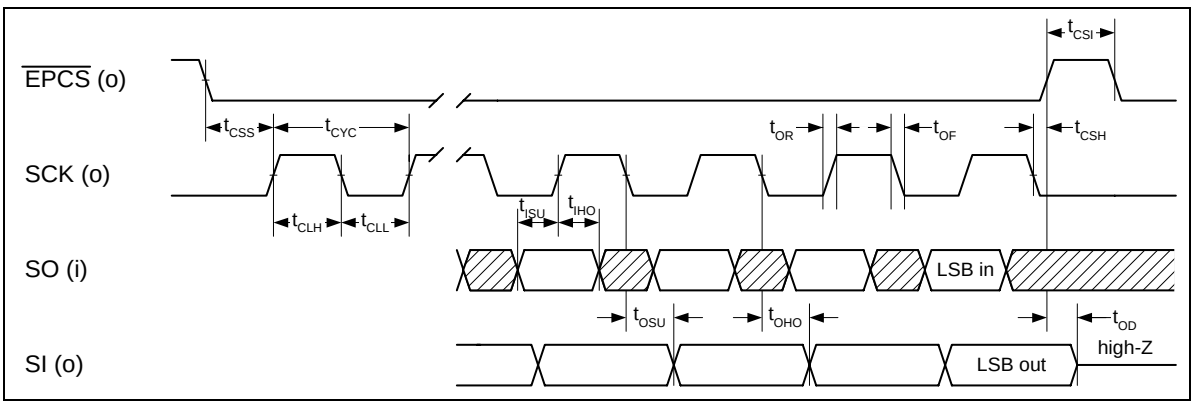
Connection of an ALIS V2.1 device to the Serial Control Interface

For the connection of an ALIS V2.1 device to the Serial Control Interface of the PITA the GP3 pin is additionally used as low active chip select signal CS to the ALIS V2.1.

The GP3 pin is always driven ’high’ and therefore the ALIS V2.1 interface is inactive during the phase of automatic initialization of the PCI Configuration Space.

5.4.2 Timing of the SPI EEPROM Interface

Timing Diagram



Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Chip Select Setup Time	t_{CSS}	500		ns
Chip Select Hold Time	t_{CSH}	500		ns
Chip Select Inactive	t_{CSI}	500		ns
Clock Cycle Time	t_{CYC}	1000		ns
Clock HIGH Time	t_{CLH}	410		ns
Clock LOW Time	t_{CLL}	410		ns
Clock Output Rise Time	t_{OR}		2	µs
Clock Output Fall Time	t_{OF}		2	µs
Input Data Setup Time	t_{ISU}	100		ns
Input Data Hold Time	t_{IHO}	100		ns
Output Data Setup Time	t_{OSU}		500	ns

Abbreviations of the Timing Diagram (cont'd)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Output Data Hold Time	t_{OHO}	0	500	ns
Output Disable Time	t_{OD}		500	ns
Write Cycle Time	t_{WC}		10	ms

Note

The SCK is a strobed clock signal (i.e. it is only active as long as valid data is transferred on SI/SO line) and output data is written on the falling edge and input data is latched on the rising edge. Although the first SCK edge is positive, the PITA drives the first valid bit on SI (output) with the falling edge of $\overline{\text{EPCS}}$, so the minimum setup time with respect to the first SCK rising edge is guaranteed.

5.4.3 Internal Registers for the SPI EEPROM Interface

Internal Register: 00h

Bit 28	EEPROM_Control_Int_En
Type	RW
Default Value	0b
Description	Enable for the EEPROM_Control_Int interrupt bit

Bit 12	EEPROM_Control_Int
Type	RC
Default Value	0b
Description	The EEPROM_Control_Int_En bit and the EEPROM are set to ’1’ if the transaction is finished.

Internal Register: 24h

Bit 31:0	EEPROM Control Register
Default Value	00000000h

Bit 31:25	Reserved
Type	H
Default Value	0000h
Description	Reserved

Internal Register: 24h (cont'd)

Bit 24	EEPROM_Start
Type	RW
Default Value	0b
Description	Bit 24='1': An EEPROM transaction is started with the EEPROM Command, EEPROM Data and EEPROM Byte Address. BIT 24='0': An EEPROM transaction can be started.

Bit 23:16	EEPROM Command
Type	RW
Default Value	00h
Description	The following SPI commands are supported: '00000110': WREN Set Write Enable Latch '00000100': WRDI Reset Write Enable Latch '00000101': RDSR Read Status Register '00000001': WRSR Write Status Register '00000011': READ Read Data from Memory Array '00000010': WRITE Write Data to Memory Array 'OTHERS': No action

Bit 15:8	EEPROM Byte Address
Type	RW
Default Value	00h
Description	Byte Address for the next EEPROM read or write transaction.

Internal Register: 24h (cont'd)

Bit 7:0	EEPROM Data
Type	RW
Default Value	00h
Description	• Transaction with a read command: After the transaction has been finished this register contains the byte that has been read from the EEPROM. • Transaction with a write command: The contents of this register will be written to the EEPROM Byte Address if the connected EEPROM after the EEPROM_Start bit is set.

6 Configuration of the PITA

Pinstrapping

Pinstrapping is used for:

- Loading the Subsystem Vendor ID.
- Loading the least significant 4 bits of the Subsystem ID to the PCI Configuration Space.

Several output pins from the parallel microcontroller interface and the general purpose I/O interface are implemented as tristate output pins.

During PCI reset they are driven in tristate mode and the external logic value is latched in the Subsystem ID (4 LSBs) and the Subsystem Vendor ID. This means that the signals on board, connected to these pins, must be forced with pullup/ pulldown resistors to the desired value if they are not driven by the PITA.

Pins Used for Pinstrapping During PCI Reset

Signal Name	Usage during PCI Reset (pinstrapping)	I/O
PAD(7:0)	Subsystem Vendor ID(15:8)	IO
PA(7:0)	Subsystem Vendor ID(7:0)	OTS
GP3	Subsystem ID(3)	IO
GP2	Subsystem ID(2)	IO
GP1	Subsystem ID(1)	IO
GP0	Subsystem ID(0)	IO

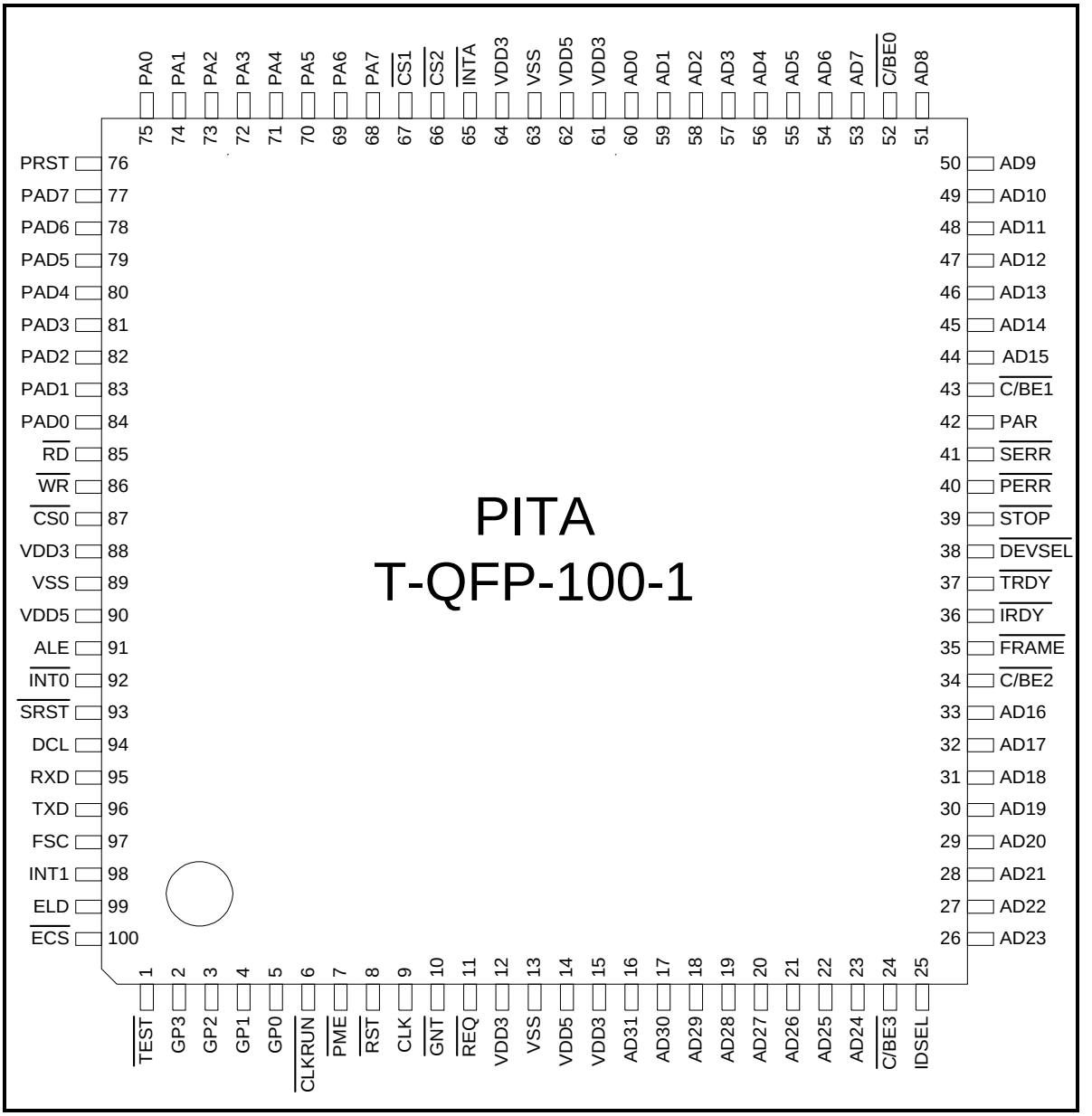
Automatic reconfiguration of the PITA with the serial EEPROM

The PITA can also be configured by the EEPROM after system reset. Pinstrap values are overwritten by this process if the procedure described in “Automatic reconfiguration of the PITA” on page 85 was successful.

7 Pinning

PITA Pinout

This illustration shows the numbered pins and their respective signals:



Overview

The following table lists the interfaces and their respective pins:

Interface	Total	In	Out	I/O	Page
PCI bus	52	4	5	43	7-3
Parallel Interface	23	3	14	8	7-4
Serial Interface	5	2	2	1	7-6
GP I/O Interface	4	0	0	4	7-7
Special EEPROM Signals	2	1	1	0	7-8
Test IF	1	1	0		7-8
Power Supply	11	11	0		7-8
Total	100	11	22 (+11 Power Supply)	56	-

Description of PIN Types

Type	Description
O	Output Pin
I	Input Pin
IO	Bidirectional Input/Output Pin
(OD)	Open Drain

This table lists the Pins Characteristics of the PCI Bus

Pin No.	Signal Name	Pin Count	Type	Function
9	CLK	1	I	PCI - Clock (max. 33 MHz)
8	$\overline{\text{RST}}$	1	I	PCI - Reset
16 - 23, 26 - 33, 44 - 51, 53 - 60	AD(31:0)	32	IO	PCI - Address-/Data bus
24, 34, 43, 52	$\overline{\text{C/BE}}$(3:0)	4	IO	PCI - Command/Byte Enable Bus (Byte Enables are low active)
42	PAR	1	IO	PCI - Parity
65	$\overline{\text{INTA}}$	1	OD	PCI - Interrupt Signal
25	IDSEL	1	I	PCI - Initialization Device Select Signal For CardBus boards this signal must set to ‘1’
35	$\overline{\text{FRAME}}$	1	IO	PCI - Frame
36	$\overline{\text{IRDY}}$	1	IO	PCI - Initiator Ready
37	$\overline{\text{TRDY}}$	1	IO	PCI -Target Ready
38	$\overline{\text{DEVSEL}}$	1	IO	PCI - Device Select
39	$\overline{\text{STOP}}$	1	IO	PCI - Stop
11	$\overline{\text{REQ}}$	1	OTS	PCI - Bus Request
10	$\overline{\text{GNT}}$	1	I	PCI - Bus Grant

This table lists the Pins Characteristics of the PCI Bus (cont'd)

Pin No.	Signal Name	Pin Count	Type	Function
40	$\overline{\text{PERR}}$	1	IO	PCI - Parity Error
41	$\overline{\text{SERR}}$	1	OD	PCI - System Error
7	$\overline{\text{PME}}$	1	OD	PCI - Power Management Event
6	$\overline{\text{CLKRUN}}$	1	I	Clock Run

This table lists the Pins Characteristics of the Parallel Interfaces

Pin No.	Signal Name	Pin Count	Type	Function
76	PRST	1	O	Active high reset
66, 67, 87	$\overline{\text{CS}}$(2:0)	3	O	Chip Select Signals for three devices connected to the parallel microcontroller interface.
84 - 77	PAD(7:0)	8	IO	- Multiplexed Bus Mode: Address/Data bus for the parallel interface. - Non-Multiplexed Bus Mode: Data bus for the parallel interface.

This table lists the Pins Characteristics of the Parallel Interfaces (cont'd)

Pin No.	Signal Name	Pin Count	Type	Function
75 - 68	PA(7:0)	8	OTS	- Multiplexed Bus Mode: Not used; pins can be left not connected. - Non-Multiplexed Bus Mode: Address bus for the parallel interface.
91	ALE	1	O	Address Latch Enable Signal, active high. In non-multiplexed mode the ALE input of peripheral devices must be connected to VSS.
86	$\overline{WR}$	1	O	Write Signal, active low
85	$\overline{RD}$	1	O	Read Signal, active low
92	$\overline{INT0}$	1	I	Standard active low interrupt input for connected devices, which is forwarded to the PCI interface ($\overline{INTA}$).
98	INT1	1	I	Standard Active High Interrupt Input for connected devices, which is forwarded to the PCI interface ($\overline{INTA}$).

This table list the Pins Characteristics of the Serial Interface

Pin No.	Signal Name	Pin Count	Type	Function
93	$\overline{\text{SRST}}$	1	O	Active low reset output.
97	FSC	1	I	Frame Synchronisation Clock signal, 8 kHz.
94	DCL	1	I O (OD)	Serial Data Clock Signal. The direction of this pin can be controlled by the DCL_Out_En bit in the internal registers. By default this pin is input. For PSB4596 V2.1 mode, this pin must configured as output (open drain), for all other modes this pin must be input.
95	RXD	1	I	Serial Data Input Signal
96	TXD	1	O (OD)	Serial Data Output Signal

This table lists the Pins Characteristics of the General Purpose I/O Interface

Pin No.	Signal Name	Pin Count	Type	Function
2	GP3	1	IO	General Purpose I/O Pin 3 This pin is driven high during the automatic EEPROM configuration if ELD = ‘1’.
3	GP2	1	IO	General Purpose I/O Pin 2 Serial EEPROM Interface : SCK - Serial Clock Signal.
4	GP1	1	IO	General Purpose I/O Pin 1 Serial EEPROM Interface : SO - Serial Data Output from EEPROM (input to the PITA).
5	GP0	1	IO	General Purpose I/O Pin 0 Serial EEPROM Interface : SI - Serial Data Input to the EEPROM (output from the PITA).

This table lists the Pins Characteristics of the Special EEPROM Signals

Pin No.	Signal Name	Pin Count	Type	Function
99	ELD	1	I	EEPROM Load '1' -> EEPROM Configuration is enabled. '0' -> EEPROM Configuration is disabled.
100	$\overline{\text{ECS}}$	1	O	EEPROM Chip Select (SPI Signal)

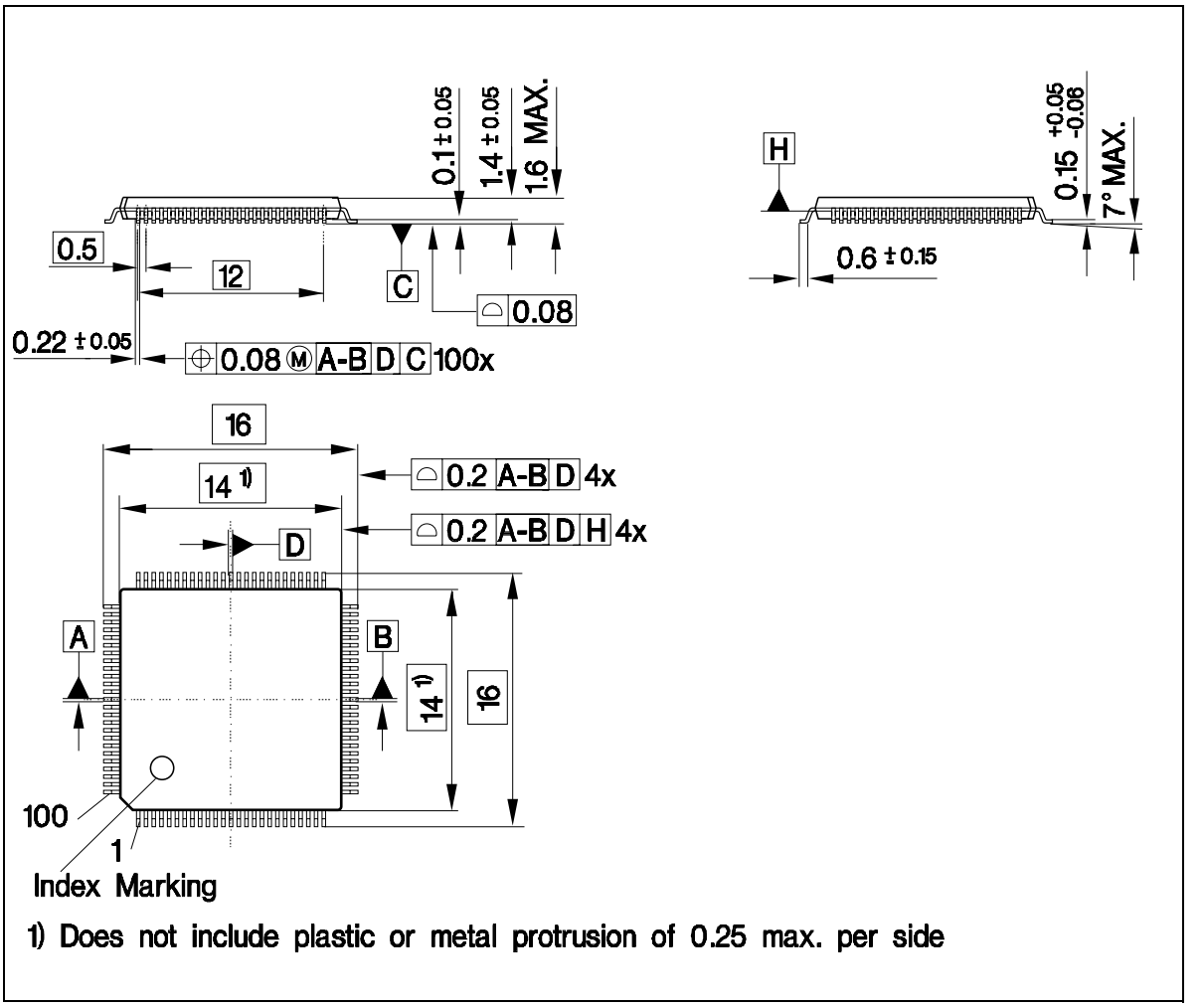
This table lists the Pins Characteristics of the Test IF

Pin No.	Signal Name	Pin Count	Type	Function
1	$\overline{\text{TEST}}$	1	I	Test Input

This table lists the Pins Characteristics of the Power Supply

Pin No.	Signal Name	Pin Count	Type	Function
12, 15, 61, 64, 88	VDD3	5	I	Positive Power Supply 3.3V ± 10%
14, 62, 90	VDD5	3	I	Positive Power Supply 5V ± 10%
13, 63, 89	VSS	3	I	Ground 0V

8 Package Outlines



9 Precaution

Overview:

Overview	Page
Absolute Maximum Ratings	9-2
DC Characteristics	9-3
AC Characteristics	9-5
Capacitances	9-6

9.1 Absolute Maximum Ratings

This Table shows the Parameters for the Absolute Maximum Ratings

Parameter		Limit Values	Unit
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD5} + 0.3	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Maximum voltage on V_{DD3}/V_{DD5}	V_{DD}	7	V

Note:

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device.

Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.

9.2 DC Characteristics

Description

The following DC characteristics are valid for all pins of the PITA except the PCI Interface.

Conditions

T_A = 0 to 70 °C; V_{DD5} = 5 V ± 10 %, V_{DD3} = 3.3 V ± 10 %, V_{SS} = 0 V;

DC Characteristics

Parameter	Sym	Limit Values			Unit	Test Condition	Rem.
		min	typ	max			
L-input voltage	V_{IL}	–0.3		0.8	V		
H-input voltage	V_{IH}	2.0		V_{DD5} + 0.3	V		
L-output voltage	V_{OL}			0.45	V	I_{OL} = 7 mA (TXD, RXD) I_{OL} = 2 mA (all others)	
H-output voltage	V_{OH}	2.4			V	I_{OH} = – 400 µA	
V_{DD3} Power supply current	I_{cc}		19		mA	All power states except $D3_{cold}$ (power off state)	
V_{DD5} Power supply current	I_{cc}		1		mA	All power states except $D3_{cold}$ (power off state)	

DC Characteristics (cont'd)

Parameter	Sym	Limit Values			Unit	Test Condition	Rem.
		min	typ	max			
Input leakage current	I_{LI}			1	uA	$0\ V < V_{IN} < V_{DD5}$	1)
Output leakage current	I_{LO}			1	uA	$0\ V < V_{OUT} < V_{DD5}$	

1) (except for $\overline{TEST}$, $\overline{INT0}$ which are internally pulled up (I_{LI} = 300 uA) and INT1, $\overline{CLKRUN}$ which are internally pulled down (I_{LIh} = 500 uA)

9.3 AC Characteristics

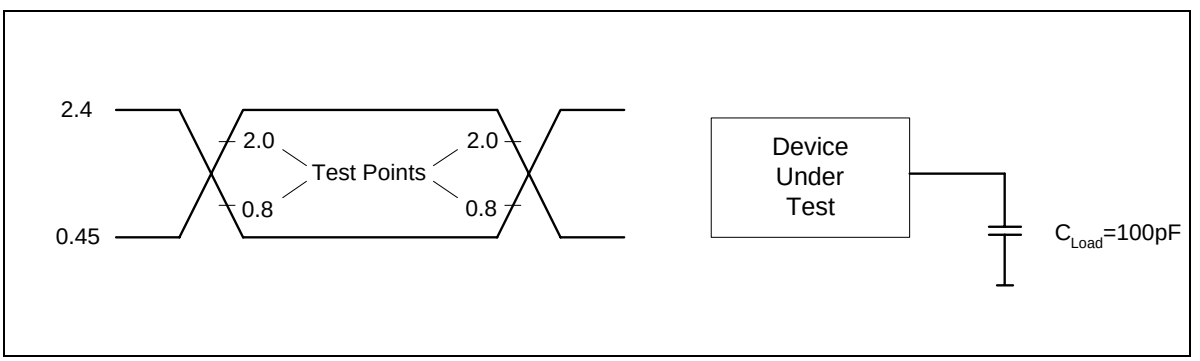
Description

Inputs are driven to 2,4 V for a logical ’1’ and to 0.45 V for a logical ’0’. Timing measurements are made at 2.0 V for a logical ’1’ and 0.8 V for a logical ’0’.

Conditions

T_A = 0 to 70 °C, V_{DD5} = 5 V ± 10%, V_{DD3} = 3.3 V ± 10%, V_{SS} = 0 V.

AC Testing Input/Output Waveform



9.4 Capacitances

Conditions

T_A = 25 °C, V_{DD5} = 5 V ± 10%, V_{DD3} = 3.3 V ± 10%, V_{SS} = 0 V, unmeasured pins grounded.

Capacitances

Parameter	Symbol	Limit Values		Unit	Rem.
		min.	max.		
Input Capacitance	C_{IN}		7	pF	
I/O Capacitance	$C_{I/O}$		7	pF	

10 Configuration Space Register of the PITA

Overview

	Page
Description of the Register Types	10-2
Configuration Space Register	10-3
Registers which do not occur elsewhere in the Data Sheet	10-13

10.1 Description of the Register Types

Type	Description
R	**read only** • these bits are initialized by pinstrapping during PCI reset
H	**read only** • hardwired
RC	**read clear** • these bits are set by the internal logic • these bits can be read out and reset by writing logical “1” to them • writing logical “0” doesn’t influence the states of these bits
RW	**read write** • these bits can be read out and written via the PCI bus
EW	**EEPROM write** • these bits can be set by an external EEPROM after a system reset

10.2 Configuration Space Register

00h

Ad.	Bit	Type	Default Value	Register Name	Page
00h	31:16	H/EW	2104h	Device ID	10-13
	15:0	H/EW	110Ah	Vendor ID of Siemens AG.	10-13

04h

Ad.	Bit	Type	Default Value	Register Name	Page
04h	31:0		0290 0000h	PCI Status Register	10-13
	31	RC	0b	Parity Error Detected	10-13
	30	RC	0b	System Error Signaled	5-58
	29	RC	0b	Master Abort Detected	5-58
	28	RC	0b	Target Abort Detected	5-58
	27	RC	0b	Target Abort Signaled	5-58
	26:25	H	01b	DEVSEL Timing	4-19 4-21
	24	RC	0b	Data Parity Error Reported	10-13
	23	H	1b	Fast Back-to-Back Capability	4-23
	22	H	0b	User Defined Functions	10-13
	21	H	0b	66 MHz Capability	10-13

04h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	20	H/EW	1b	Capabilities	10-13
	19:16	H	0000b	Reserved	10-13
	15:0			Command Register	10-13
	15:10	H	000000b	Reserved	10-13
	9	H	0b	Fast Back-to-Back Enable	4-23
	8	RW	0b	System Error Enable	5-58
	7	H	0b	Address/Data Stepping Enable (not used)	10-13
	6	RW	0b	Parity Error Response	10-13
	5:3	H	000b	The PITA does not support the Special Cycle Command.	10-13
	2	RW	0b	Master Enable	5-58
	1	RW	0b	Memory Access Enable	4-8
	0	H	0b	I/O Access Enable	10-13

08h

Ad.	Bit	Type	Default Value	Register Name	Page
08h	31:8	H/EW	028000h	Class Code/PCI network device	10-16
	7:0	H	01h	Revision ID	10-16

0Ch

Ad.	Bit	Type	Default Value	Register Name	Page
0Ch	31:24	H	00h	BIST	10-17
	23:16	H	00h	Header Type	10-17
	15:8	H	00h	Master Latency Timer	10-17
	7:0	H	00h	Cache Line Size	10-17

10h

Ad.	Bit	Type	Default Value	Register Name	Page
10h	31:0 31:12 11:0	 RW H	00000000h	Base Register 0	4-8

14h

Ad.	Bit	Type	Default Value	Register Name	Page
14h	31:0 31:12 11:0	 RW H	00000000h	Base Register 1	4-9

18h

Ad.	Bit	Type	Default Value	Register Name	Page
18h	31:0	H	00000000h	Base Address Register 2 (not used)	4-9

1Ch

Ad.	Bit	Type	Default Value	Register Name	Page
1Ch	31:0	H	00000000h	Base Address Register 3 (not used)	4-9

20h

Ad.	Bit	Type	Default Value	Register Name	Page
20h	31:0	H	00000000h	Base Address Register 4 (not used)	4-10

24h

Ad.	Bit	Type	Default Value	Register Name	Page
24h	31:0	H	00000000h	Base Address Register 5 (not used)	4-10

28h

Ad.	Bit	Type	Default Value	Register Name	Page
28h	31:0		0000 02C0	CardBus CIS Pointer	4-11
	31:28	H	0000b	ROM Image Number	4-11
	27:3	H	000058h	Address Space Offset	4-11
	2:0	H	000b	Address Space Indicator	4-12

2Ch

Ad.	Bit	Type	Default Value	Register Name	Page
2Ch	31:20 19:16	H/EW R or EW	000h pinstrap value or EEPROM-value	Subsystem Device ID	4-12
	15:0	R/EW	pinstrap value or EEPROM-value	Subsystem Vendor ID	4-12

30h

Ad.	Bit	Type	Default Value	Register Name	Page
30h	31:0	H	00000000h	Reserved	10-18

34h

Ad.	Bit	Type	Default Value	Register Name	Page
34h	31:8	H	00h	Reserved	4-28
	7:0	H	40h	Capabilities Pointer	4-28

38h

Ad.	Bit	Type	Default Value	Register Name	Page
38h	31:0	H	00000000h	Reserved	10-18

3Ch

Ad.	Bit	Type	Default Value	Register Name	Page
3Ch	31:24	H	00h	Max_Lat	10-19
	23:16	H	00h	Min_Gnt	10-19

3Ch (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	15:8	H	01h	Interrupt pin	10-19
	7:0	RW	FFh	Interrupt Line	10-19

40h

Ad.	Bit	Type	Default Value	Register Name	Page
40h	31:0		1229 0001	Power Management Capabilities (PMC)	4-28
	31:30 29:28 27	H H/EW H	00b 01b 0b	PME_Support	4-28
	26	H/EW	0b	D2_Support	4-28
	25	H/EW	1b	D1_Support	4-28
	24:22	H	000b	Reserved	4-28
	21	H	1b	DSI	4-28
	20	H	0b	Reserved	4-28
	19	H/EW	1b	PME Clock	4-28
	18:16	H	001b	Version The value 001b indicates that the device complies with the Revision 1.0 of the PCI Power Management Interface Specification.	4-28
	15:8	H	00h	Next Item Ptr	4-28

40h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	7:0	H	01h	Capability ID	4-28

44h

Ad.	Bit	Type	Default Value	Register Name	Page
44h	31:24	H	00h	DATA Register	4-32
	23:16	H	00h	PMCSR_BSE Bridge Support Extensions	4-32
	15:8	H	00h	Power Management Control/Status register	4-32
	15	RC	0b	PME Status	4-32
	14:13	H	00b	Data Scale	4-32
	12:9	RW	0h	Data Select	4-32
	8	RW	0b	PME_En	4-32
	7:2	H	00h	Reserved	4-32
	1:0	RW	00b	Power State	4-32

48h

Ad.	Bit	Type	Default Value	Register Name1	Page
48h	31:0			Power Data Register 1	10-20

48h (cont'd)

Ad.	Bit	Type	Default Value	Register Name1	Page
	31:30	H	00b	Reserved	10-20
	29:28	H/EW	00b	Data_Scale in Data_Select = 2	10-20
	27:20	H/EW	00h	DATA in Data_Select = 2	10-20
	19:18	H/EW	00b	Data_Scale in Data_Select = 1	10-20
	17:10	H/EW	00h	DATA in Data_Select = 1	10-20
	9:8	H/EW	00b	Data_Scale in Data_Select = 0	10-20
	7:0	H/EW	00h	DATA in Data_Select = 0	10-20

4Ch

Ad.	Bit	Type	Default Value	Register Name	Page
4Ch	31:0			Power Data Register 2	10-22
	31:30	H	00b	Reserved	10-22
	29:28	H/EW	00b	Data_Scale in Data_Select = 5	10-22
	27:20	H/EW	00h	DATA in Data_Select = 5	10-22
	19:18	H/EW	00b	Data_Scale in Data_Select = 4	10-22
	17:10	H/EW	00h	DATA in Data_Select = 4	10-22
	9:8	H/EW	00b	Data_Scale in Data_Select = 3	10-22

4Ch (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	7:0	H/EW	00h	DATA in Data_Select = 3	10-22

50h

Ad.	Bit	Type	Default Value	Register Name	Page
50h	31:0			Power Data Register 3	10-24
	31:20	H	000h	Reserved	10-24
	19:18	H/EW	00b	Data_Scale in Data_Select = 7	10-24
	17:10	H/EW	00h	Data_Value in Data_Select = 7	10-24
	9:8	H/EW	00b	Data_Scale in Data_Select = 6	10-24
	7:0	H/EW	00h	Data_Value in Data_Select = 6	10-24

54h

Ad.	Bit	Type	Default Value	Register Name	Page
54h	31:0	H	00h	CardBus CIS	10-25

10.3 Registers which do not occur elsewhere in the Data Sheet

00h

Bit 31:16	Device ID
Type	H or EW
Default Value	2104h
Description	Identifies the PITA within all PCI devices from Siemens Semiconductors.

Bit 15:0	Vendor ID
Type	H or EW
Default Value	110Ah
Description	110A is the Vendor ID of Siemens AG.

04h

Bit 31:0	PCI Status Register
Default Value	02900000h

Bit 31	Parity_Error_Detected
Type	RC
Default Value	0b
Description	This bit is set, if a parity error is detected during a transaction with the PITA. This is done independently from the status of the ‘Parity Error Response’ bit.

04h (cont'd)

Bit 24	Data_Parity_Error_Reported
Type	RC
Default Value	0b
Description	The PCI Master asserts this bit if it detects the $\overline{\text{PERR}}$ signal on the PCI bus asserted during a PCI transaction initiated by itself.

Bit 22	User_Defined_Functions
Type	H
Default Value	0b
Description	The PITA has no user defined functions.

Bit 21	66_MHz_Capability
Type	H
Default Value	0b
Description	The PITA is not a 66 MHz device (0 - 33 MHz supported.)

Bit 20	Capabilities
Type	H or EW
Default Value	1b
Description	If this bit is set, the PCI device has additional capabilities defined in the PCI Configuration Space Header. Additional capabilities can be found in the Cap_Ptr under address 34h.

04h (cont'd)

Bit 19:16	Reserved
Type	H
Default Value	0000b
Description	

Bit 15:0	Command Register

Bit 15:10	Reserved
Type	H
Default Value	000000b
Description	

Bit 7	Address/Data_Stepping_Enable
Type	H
Default Value	0b
Description	not used
Bit 6	Parity_Error_Response
Type	RW
Default Value	0b
Description	If this bit is set to '1', the PCI interface reports data parity errors by asserting the $\overline{\text{PERR}}$ signal.

04h (cont'd)

Bit 5:3	
Type	RW
Default Value	0b
Description	The PITA does not support the Special Cycle Command. The PITA does not generate Memory Write and invalidate transactions. The PITA does not support VGA Palette snooping.

Bit 0	I/O_Access_Enable
Type	H
Default Value	0b
Description	The PCI interface does not support I/O commands.

08h

Bit 31:8	Class_Code
Type	H or EW
Default Value	028 000h
Description	PCI network device

Bit 7:0	Revision ID
Type	H
Default Value	01h
Description	Revision of the PCI device

0Ch

Bit 31:24	BIST
Type	H
Default Value	00h
Description	The PITA has no built-in self test.

Bit 23:16	Header_Type
Type	H
Default Value	00h
Description	

Bit 15:8	Master_Latency_Timer
Type	H
Default Value	00h
Description	Unused

Bit 7:0	Cache_Line_Size
Type	H
Default Value	00h
Description	The PITA does not support the cache line size register because it supports only single data transactions.

30h

Bit 31:0	Reserved
Type	H
Default Value	0000 0000h
Description	Reserved

38h

Bit 31:0	Reserved
Type	H
Default Value	0000 0000h
Description	

3Ch

Bit 31:24	Max_Lat
Type	H
Default Value	00h
Description	Set to ’0’ because only single data transactions are supported.
Bit 23:16	Mint_Gnt
Type	H
Default Value	00h
Description	Set to ’0’ because only single data transactions are supported.

Bit 15:8	Interrupt_Pin
Type	H
Default Value	01h
Description	As a single function device, the PITA uses the INTA signal.

Bit 7:0	Interrupt_Line
Type	RW
Default Value	FFh
Description	These Bits show the interrupt line which is used by this system. For a x86 system the value FF means unknown. These registers are written during the initialization of the operating system.

48h

Bit 31:0	Power Data Register 1

Bit 31:30	Reserved
Type	H
Default Value	00b
Description	Reserved

Bit 29:28	Data_Scale in Data_Select=2
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select_field is set to 2.

Bit 27:20	DATA in Data_Select=2
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 2

48h (cont'd)

Bit 19:18	Data_Scale in Data_Select=1
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to1.

Bit 17:10	DATA in Data_Select=1
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 1.

Bit 9:8	Data_Scale in Data_Select=0
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to 0.

Bit 7:0	DATA in Data_Select=0
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 0.

4Ch

Bit 31:0	Power Data Register 2

Bit 31:30	Reserved
Type	H
Default Value	00b
Description	Reserved

Bit 29:28	Data_Scale in Data_Select=5
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select_field is set to 5.

Bit 27:20	DATA in Data_Select=5
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 5.

4Ch (cont'd)

Bit 19:18	Data_Scale in Data_Select=4
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to 4

Bit 17:10	DATA in Data_Select=4
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 4.

Bit 9:8	Data_Scale in Data_Select=3
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to 3-

Bit 7:0	DATA in Data_Select=3
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 3.

50h

Bit 31:0	Power Data Register 3

Bit 31:30	Reserved
Type	H
Default Value	00b
Description	Reserved

Bit 19:18	Data_Scale in Data_Select=7
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to 7.

Bit 17:10	DATA in Data_Select=7
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 7.

50h (cont'd)

Bit 9:8	Data_Scale in Data_Select=6
Type	H or EW
Default Value	00b
Description	This register is mapped to the Data_Scale field if Data_Select field is set to 6.

Bit 7:0	DATA in Data_Select=6
Type	H or EW
Default Value	00h
Description	This register is mapped to the DATA register if the Data_Select field is set to 6.

54h

Bit 31:0	Cardbus_CIS
Type	H
Default Value	00h
Description	Default Value: 00h Up from this register, the Cardbus CIS structure is implemented (not supported in this version of PITA)

11 Internal Register of the PITA

Overview

	Page
Description of the Register Types	11-2
Internal Register	11-3
Registers which do not occur elsewhere in the Data Sheet	11-10

11.1 Description of the Register Types

Type	Description
R	**read only** • these bits are initialized by pinstrapping during PCI reset
H	**read only** • hardwired
RC	**read clear** • these bits are set by the internal logic • these bits can be read out and reset by writing logical “1” to them • writing logical “0” doesn’t influence the states of these bits
RW	**read write** • these bits can be read out and written via the PCI bus
EW	**EEPROM write** • these bits can be set by an external EEPROM after a system reset

11.2 Internal Register

00h

Ad.	Bit	Type	Default Value	Register Name	Page
00h	31:0		00000000h	ICR - Interrupt Control Register	11-10
	31:29	H	000b	Reserved	11-10
	28	RW	0b	EEPROM_Control_Int_En	5-90
	27	RW	0b	Retry_Counter_Down_ Int_En	4-35
	26	RW	0b	FIFO_Overflow_Empty_ Int_En	5-10
	25	RW	0b	DMA_Write_Counter_ Overflow_Int_En	5-10
	24	RW	0b	DMA_Write_Counter_Int_ En	5-10
	23:18	H	000000b	Reserved	11-10
	17	RW	0b	INT0_En	11-10
	16	RW	0b	INT1_ En	11-10
	15:13	H	000b	Reserved	11-10
	12	RC	0b	EEPROM_Control_Int	5-90
	11	RC	0b	Retry_Counter_Int	4-35
	10	RC	0b	FIFO_Overflow_Empty_ Int	5-10
	9	RC	0b	DMA_Write_Counter_ Overflow_Int	5-10
	8	RC	0b	DMA_Write_Counter_Int	5-10

00h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	7:6	H	0b	Reserved	11-10
	5	RC	0b	GP3_INT	5-69
	4	RC	0b	GP2_INT	5-69
	3	RC	0b	GP1_INT	5-69
	2	RC	0b	GP0_INT	5-69
	1	RC	0b	INT0	11-10
	0	RC	0b	INT1	11-10

04h

Ad.	Bit	Type	Default Value	Register Name	Page
04h	31:0		00000000h	DMA Control Register	5-11
	31:09	H	0000000h	Reserved	5-11
	8	RW	0b	DMA Start	5-11
	7:6	H	00b	Reserved	5-11
	5:0	RW	000000b	DMA Select - all modes IOM-2 Mode 1 IOM-2 Mode 2 IOM-2 Mode 3 Single Modem Mode V2.1 Single Modem Mode V3.X Dual Modem+Voice Mode	5-11 5-16 5-20 5-23 5-31 5-36 5-44

08h

Ad.	Bit	Type	Default Value	Register Name	Page
08h	31:12 11:0	RW H	00000h 000h	Circular Buffer Start Address	5-13

0Ch

Ad.	Bit	Type	Default Value	Register Name	Page
0Ch	31:02 1:0	R H	00000000h 00b	Actual Circular Buffer Pointer	5-13

10h

Ad.	Bit	Type	Default Value	Register Name	Page
10h	31:0		00000000h	ALIS Command Register 1	5-36
	31:25	H	00h	Reserved	5-36
	24	RW	0b	New_ALIS_Command_1	5-36
	23:16	RW	00h	ALIS_Received_Data_1	5-36
	15:8	RW	00h	ALIS_Command_1	5-36
	7:0	RW	0b	ALIS_Transmit_Data_1	5-36

14h

Ad.	Bit	Type	Default Value	Register Name	Page
14h	31:0		00000000h	ALIS Command Register 2	5-39
	32:25	H	000h	Reserved	5-39
	24	RW	0b	New_ALIS_Command_2	5-39
	23:16	RW	00h	ALIS_Received_Data_2	5-39
	15:8	RW	00h	ALIS_Command_2	5-39
	7:0	RW	00h	ALIS_Transmit_Data_2	5-39

18h

Ad.	Bit	Type	Default Value	Register Name	Page
18h	31:0		00000000h	GP I/O Interface Control Register	5-70
	31:28	H	0h	Reserved	5-70
	27	RW	0b	GP3_Int_En	5-70
	26	RW	0b	GP2_Int_En	5-70
	25	RW	0b	GP1_Int_En	5-70
	24	RW	0b	GP0_Int_En	5-70
	23:20	H	0000b	Reserved	5-70
	19	RW	0b	GP3_Out_En	5-70
	18	RW	0b	GP2_Out_En	5-70

18h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	17	RW	0b	GP1_Out_En	5-70
	16	RW	0b	GP0_Out_En	5-70
	15:12	H	0000b	Reserved	5-70
	11	R	0b	GP3_IN	5-70
	10	R	0b	GP2_IN	5-70
	9	R	0b	GP1_IN	5-70
	8	R	0b	GP0_IN	5-70
	7:4	H	0000b	Reserved	5-70
	3	RW	0b	GP3_OUT	5-70
	2	RW	0b	GP2_OUT	5-70
	1	RW	0b	GP1_OUT	5-70
	0	RW	0b	GP0_OUT	5-70

1Ch

Ad.	Bit	Type	Default Value	Register Name	Page
1Ch	31:0		00000000h	MISC - Miscellaneous Register	5-27
	31	RW	0b	IOM B1 Masking	5-27
	30	RW	0b	IOM B2 Masking	5-27
	29	RW	0b	IOM MON0/IC1 Masking	5-27
	28	RW	0b	IOM D+C/I0+MR+MX / IC2 Masking	5-27

1Ch (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	27	RW	1b	Serial Interface Buffer Mode	11-12
	26	RW	0b	Parallel Interface Mode	5-47
	25	RW	0b	Soft reset Serial Interface	11-12
	24	RW	0b	Soft reset Parallel Interface	5-47
	23:16	RW	00h	Retry Count Register	4-36
	15:12	H	0000b	Reserved	11-12
	11:0	RW	0000h	DMA Write Count Register	5-14

20h

Ad.	Bit	Type	Default Value	Register Name	Page
20h	31:0		00000000h	Serial Clock Select Register	
	31:2	H	00000000h	Reserved	
	1	RW	0b	DCL_Out_En	5-17 5-20 5-23 5-32 5-41
	0	RW	0b	Serial_Clock_Sel	5-17 5-20 5-23 5-32 5-41

24h

Ad.	Bit	Type	Default Value	Register Name	Page
24h	31:0		00000000h	EEPROM Control Register	5-90
	31:25	H	0000h	Reserved	5-90
	24	RW	0b	EEPROM Start	5-90
	23:16	RW	00h	EEPROM Command	5-90
	15:8	RW	00h	EEPROM Byte Address	5-90
	7:0	RW	00h	EEPROM Data	5-90

28h

Ad.	Bit	Type	Default Value	Register Name	Page
28h	31:0		00000000h	DMA TEST Register	11-12
	31:01	H	00000000h	Reserved	11-12
	0	RW	0b	Loop_Back_Mode	5-46

11.3 Registers which do not occur elsewhere in the Data Sheet

00h

Bit 31:0	ICR - Interrupt Control Register
Default Value	00000000h
Description	The interrupt enable bits for GP3-0 are placed in the GP I/O Interface Control Register. All interrupt enables are high active: Int_En='0' -> corresponding interrupt (bit) is disabled Int_En='1' -> corresponding interrupt (bit) is enables

Bit 31:29	Reserved
Type	H
Default Value	000b
Description	Reserved

Bit 23:18	Reserved
Type	H
Default Value	000000b
Description	Reserved

Bit 17	INT0_En
Type	RW
Default Value	0b
Description	Enable for the INT0 interrupt bit.

00h (cont'd)

Bit 16	INT_En
Type	RW
Default Value	0b
Description	Enable for the INT1 interrupt bit.

Bit 23:18	Reserved
Type	H
Default Value	000000b
Description	Reserved

Bit 1	INT0
Type	RC
Default Value	0b
Description	An interrupt is detected on pin $\overline{\text{INT0}}$ (low active).

Bit 0	INT1
Type	RC
Default Value	0b
Description	An interrupt is detected on pin $\overline{\text{INT1}}$ (low active).

1Ch

Bit 27	Serial Interface Buffer Mode
Type	RW
Default Value	1b
Description	Bit 27=’0’: The TXD pin is configured as PUSH/PULL output pin. Bit 27=’1’: The TXD pin is configured as OPEN DRAIN output pin.

Bit 25	Soft Reset Serial Interface
Type	RW
Default Value	0b
Description	Bit 25=’0’: Activates the low active reset signal $\overline{\text{SRST}}$ to the application. Bit 25=’1’: Deactivates the reset signal $\overline{\text{SRST}}$ to the application. Before asserting this bit the DMA_Start bit has to be reset.

28h

Bit 31:0	DMA Test Register
Default Value	00000000h

Bit 31:1	Reserved
Type	H
Default Value	00000000h
Description	Reserved

12 Abbreviations

AC	Alternating Current.
A/D	Analog to digital.
ADC	Analog to digital converter.
ALE	Address latch enable.
ALIS	Analog Line Interface Solution. Chip set consisting of PSB4595 and PSB4596.
DC	Direct Current.
DCL	Double Bit Clock. (In this context, only in the IOM-2 modes of the serial interface of the PITA, single bit in all other modes).
DMA	Direct Memory Access.
DD	Data Downstream.
DU	Data Upstream.
EEPROM = E^2PROM	Electrically erasable programmable read only memory.
FIFO RX FIFO TX FIFO	First in first out.
FSC	Frame Sync.
I/O	In/out.
IOM	ISDN Oriented Modular.
ISDN	Integrated Services Digital Network.
MSB	Most Significant Bit.
PITA	PCI Interface for Telephony/Data Applications.
PCI	Peripheral Component Interconnect.
RXD	Receive Direction.
TXD	Transmit Direction.

13 Index

Numerics

3PAC 2-2

A

Absolute Maximum Ratings 9-2
AC Characteristics 9-5
ALE after internal Softreset 5-51
ALE after setting the Parallel Interface Mode Bit 5-52
ALE after System Reset 5-50
ALIS V2.1 1-2
  Connection to the Serial Control Interface 5-87
  PITA Configuration after a System Reset 5-31
ALIS V3.X 1-2
  PITA Configuration after a System Reset 5-35
ALIS-A 2-2
ALIS-D 2-2

B

Base Address Register 4-7
  Structure of the Address Space 4-7

C

Capacitances 9-6
Configuration Space Register 10-3
  00h 10-3
  04h 10-3
  08h 10-4
  0Ch 10-5
  10h 10-5
  14h 10-5
  18h 10-6
  1Ch 10-6
  20h 10-6
  24h 10-6
  28h 10-7
  2Ch 10-7
  30h 10-8
  34h 10-8
  38h 10-8
  3Ch 10-8
  40h 10-9
  44h 10-10
  48h 10-10
  50h 10-12
  54h 10-12
Base Address Register 0
  10h 4-8
Base Address Register 1
  14h 4-9
Base Address Register 2
  18h 4-9
Base Address Register 3
  1Ch 4-9
Base Address Register 4
  20h 4-10
Base Address Register 5
  28h 4-10
Base Address Registert
  04h 4-8
Burst Read
  04h 4-19
Burst Write
  04h 4-21
Disconnect with Target Abort
  04h 5-58
do not occur in the data sheet
  00h 10-13
  04h 10-13
  08h 10-16
  0Ch 10-17
  30h 10-18
  38h 10-8, 10-18
  3Ch 10-19
  48h 10-20
  4Ch 10-22
  50h 10-24

54h 10-25
Fast Back to Back
04h 4-23
PCI Configuration Space
Special Qualities
28h 4-11
2Ch 4-12
Power Management
34h 4-28
40h 4-28
44h 4-32

D

DC Characteristics 9-3
DMA Algorithm
Function 5-6
DMA Controller 5-4
Function 5-5
DMA Start bit 5-7
DMA Write Counter 5-6
Dual Modem/Modem+Voice Mode 5-42

E

Electrical Characteristics
Power Management States 4-27

G

General Purpose I/O Interface 5-65
Input Mode 5-76
Interrupt Mode 5-80
Output Mode 5-78
Pinning 7-7

I

IEC-Q TE 1-2, 2-2
Interfaces
General Purpose I/O Interface 5-65
Parallel Interface 5-47
Serial DMA Interface 5-2
SPI EEPROM Interface 5-84
Internal Register
00h 10-5, 11-3
04h 11-4
08h 11-5
0Ch 11-5
10h 11-5
14h 11-6
18h 11-6
1Ch 11-7
20h 11-8
24h 11-9
28h 11-9
4Ch 10-11
ALIS
10h 5-36
14h 5-39
DMA Controller
00h 5-10
04h 5-11, 5-13, 5-31, 5-36, 5-38, 5-44
08h 5-13
0Ch 5-13, 5-14, 5-46, 5-47, 5-70
1Ch 5-14
do not occur in the data sheet
00h 11-10
1Ch 11-12
28h 11-12
GP I/O Interface
00h 5-69
18h 5-70
IOM-2 Mode 1
04h 5-16, 5-20, 5-23
IOM-2 Modes
1Ch 5-27
Loopback Mode
28h 5-46
Parallel Interface
1Ch 5-47
Retry Counter
00h 4-35
1Ch 4-36
Single Modem Mode V2.1
20h 5-41
Single Modem Mode v2.1
20h 5-17, 5-20, 5-23, 5-32
SPI EEPROM Interface

00h 5-36, 5-39, 5-90
24h 5-90
Interrupt Control Register 4-35
Interrupts
FIFO Overflow/Empty 5-9
Write Counter 5-9
IOM-2 Mode 1 5-15
IOM-2 Mode 2 5-18
IOM-2 Mode 3 5-21
IOM-2 Modes
General Description 5-24
Masking of IOM-2 Timeslots 5-26
Selection of IOM-2 Timeslots 5-24
IPAC 1-2, 2-1
ISAC 1-2
ISAR 1-2, 2-3
ISDN
Modem using ISAR 2-3
-S with IPAC 2-1
-U with 3PAC and IEC-Q TE 2-2

L

Loopback Mode 5-45

M

Multiplexed Mode
Read Transaction 5-56
Multiplexed Mode Write Transaction 5-55

N

Non Multiplexed Mode
Read Transaction 5-54
Write Transaction 5-53

P

Parallel Interface 5-47
Pinning 7-4
PC98 1-1
PCI Bus
Pinning 7-3
PCI Commands 4-14
PCI Configuration Space 4-2
Access to the 4-6
Construction of 4-4
PCI Master Controller
Supported PCI Commands 4-14
PCI Master Target Controller 4-13
PCI Target Controller
Supported PCI Commands 4-14
Pinning
Description of PIN Types 7-2
GP I/O Interface 7-7
Parallel Interfaces 7-4
Power Supply 7-9
Serial Interface 7-6
Special EEPROM Signals 7-8
Test IF 7-8
Pinstrapping 6-1
Power Management 4-24
Power Management State
D0 4-25
D1 4-25
D2 4-25
D3 4-26
D3cold 4-26
D3hot 4-26
Power Management States
Electrical Characteristics 4-27
Power Supply
Pinning 7-9

S

Serial DMA Interface 5-2
Serial Interface
Pinning 7-6
Single Modem Mode V2.1 5-29
Configuration after a System/Soft Reset 5-30
Single Modem Mode V3.X 5-33
Configuration after a System/Soft Reset 5-35
Software Modem
using ALIS-A and ALIS-D 2-2
Special EEPROM Signals
Pinning 7-8
SPI EEPROM Interface 5-84

After finishing the transaction 5-87
Starting a read or write transaction 5-86

T

Test IF
Pinning 7-8
Timing 5-57
Timing Diagram
ALE after internal Softreset 5-51
ALE after setting the Parallel Interface Mode Bit 5-52
ALE after System Reset 5-50
Burst Read 4-18
Burst Write 4-20
Dual Modem/Modem+Voice Mode 5-43
Fast Back to Back 4-22
GP I/O Interface
ALIS V2.1 Read 5-83
ALIS V2.1 Write 5-83
Input Mode 5-76
Interrupt Mode 5-80
Output Mode 5-79
IOM-2 all Modes 5-24
IOM-2 Mode 1 5-16
IOM-2 Mode 2 5-19
IOM-2 Mode 3 5-22
Loopback Mode 5-45
Multiplexed Mode Read 5-56
Multiplexed Mode Write 5-55
Non Multiplexed Mode Read 5-54
Non Multiplexed Mode Write 5-53
Parallel Interface
Multiplexed Address 5-62
Non Mulitplexed Address 5-63
Read 5-62
Write 5-62
Single Data Read 4-16
Single Data Write 4-17
Single Modem Mode V2.1 5-29
Single Modem Mode V3.X 5-34
SPI EEPROM Interface 5-88
Transaction Disconnect 5-57
Transaction Termination 5-60
Transaction Disconnect 5-57
Transaction Termination with Retry 5-60