SIEMENS

ICs for Communications

Joint Audio Decoder-Encoder

PSB 7280 Version 3.1

Data Sheet 1998-07-01

DS 1

PSB 7280		
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1 Introduction

1.1 Overview

The PSB 7280 Joint Audio Decoder Encoder is a device which implements voice compression algorithms using the Low-Delay Code Excited Linear Prediction (LD-CELP) standard as defined in the ITU-T G.728 Recommendation, and for 7-kHz voice using the Sub-Band Coded Adaptive Differential PCM (SBC-ADPCM) coding according to the G.722 Recommendation. In addition G.711 PCM audio coding is also supported.

Thus in the G.728 mode it compresses a digitized PCM (64 kbit/s) or linear (128 kbit/s) voice signal into a 16 kbit/s bit stream, and vice versa. The algorithm is implemented in 16-bit fixed point arithmetic and complies with the newest fixed point specification set forth by the ITU.

In the G.722 mode it compresses the PCM compressed (128 kbit/s) or the linear uncompressed (256 kbit/s) 7 kHz audio samples into a rate of 48/56/64 kbit/s, and vice versa.

The JADE finds applications in

- ISDN Videophones (H.320)
- Video Conference Systems
- Corporate Network voice concentrators, multiplexers and gateways
- Data-over-voice and Voice-over-data terminals.

Other potential application areas are:

- Networks (e.g. LANs) for packetized voice
- Digital Added Main-Line (DAML) & Digital Circuit Multiplication Equipment (DCME)
- Voice storage e.g. in PC based applications
- Message recording and distribution.

The interfaces of the JADE allow a seamless integration into IOM-2 based systems. After the circuit is set up in the proper mode of operation and parameter settings are programmed by a controlling software, the circuit runs independently of the rest of the system. Status and control information to/from the JADE can be transferred either inband the compressed audio data via the corresponding selected interface or outband using an 8-bit parallel host interface.

In a Videophone system using the 8 × 8 (formerly IIT) VCP (Video Codec and Multimedia Communications Processor) the Siemens PSB 7280 can work standalone without the need of external initialization. The default configuration of the JADE is such, that no host is needed in this case and the full communication is done between the VCP and the Siemens PSB 7280.

The voice compression algorithms are implemented by an embedded 16-bit fixed point Digital Signal Processor with all memories internal and no external memory needed.

Integration of these and other features, as well as perfectly matched interfaces with other ICs allows for the implementation of highly optimized, low cost system solutions e.g. for Videophones, Data-over-voice and Channel Multiplexing equipment.

For system integration, two serial HDLC/transparent data channels are implemented which can be serviced by an attached host (or the on-chip DSP). System functions and communication between the chip and an external controller is supported by a full-duplex 256-byte on-chip mailbox communication memory.

The circuit is offered in a Quad Flat Pack package with 100 pins (P-TQFP-100: size 14×14 mm, pitch 0.5 mm, height 1.4 mm).

Note: This Data Sheet gives a thorough description of the functions and hardware that forms the base of PSB 7280. It includes information (e.g. External Memory Interface) that is not needed for the PSB 7280 as a "*ready to use plug and play*" *G.728/G.722/G.711 audio compression device.*

1.2 Feature List

P-TQFP-100

Functions

- G.728 compression/decompression (16 kbit/s)
- G.722 compression/decompression for 7-kHz audio (64, 56, 48 kbit/s)
- G.711 compression/decompression (64 kbit/s)
- Digital sampling rate conversion (16 kHz - 8 kHz) for G.722 audio with 8-kHz Codec (bandwidth reduced to 3.4 kHz)
- Accepts/outputs uncompressed audio in 8-bit PCM A/μ law or 16-bit linear format
- Uncompressed/compressed audio switchable between different interface combinations (IOM/Serial Audio Interface, IOM/Host, Host/Host)
- Inband controlled H.221/H.223 oriented audio protocol, e.g. for direct serial connection to videocodec (VCP of 8 × 8 Inc., formerly IIT Inc.) as well as host based solutions
- Outband controlled audio protocol with optimized data rate
- Stable reaction on interrupt handshake timing violations of e.g. a slow host (Windows® PC)

System On-chip Functions

- Two universal serial HDLC/transparent data controllers
- IOM-2 monitor and C/I channels
- Generation of programmable system clock output
- Three programmable timers
- Programmable on-chip PLL for internal clock generation from ISDN low frequency (7.68 MHz) clock

Type	Ordering Code	Package
PSB 7280	Q67101-H6773	P-TQFP-100

Interfaces

- 4-line IOM-2/PCM interface
- 5-line serial audio interface, e.g. for connection to videocodec/H.221/223 processor
- Parallel 8-bit Host interface
- 4-line general purpose interface
- External memory interface to external SRAM with programmable waitstates (0 to 15), for development purposes only.

Control

- Programmable via parallel host interface
- Operating parameters and mode settings via a register bank
- Access to audio channels and HDLC/serial transparent data controllers from DSP or an external host
- Interface to external software via a full-duplex 256-byte on-chip mailbox
- H.221/H.223 oriented inband configuration/mode switching

General

- Supply voltage: 3.0 - 3.6 V
- Additional 4.5 to 5.5 V supply for connection to 5-V systems without external components
- Ambient temperature range 0 °C to + 70 °C
- P-TQFP-100 package

1.3 Logic Symbol

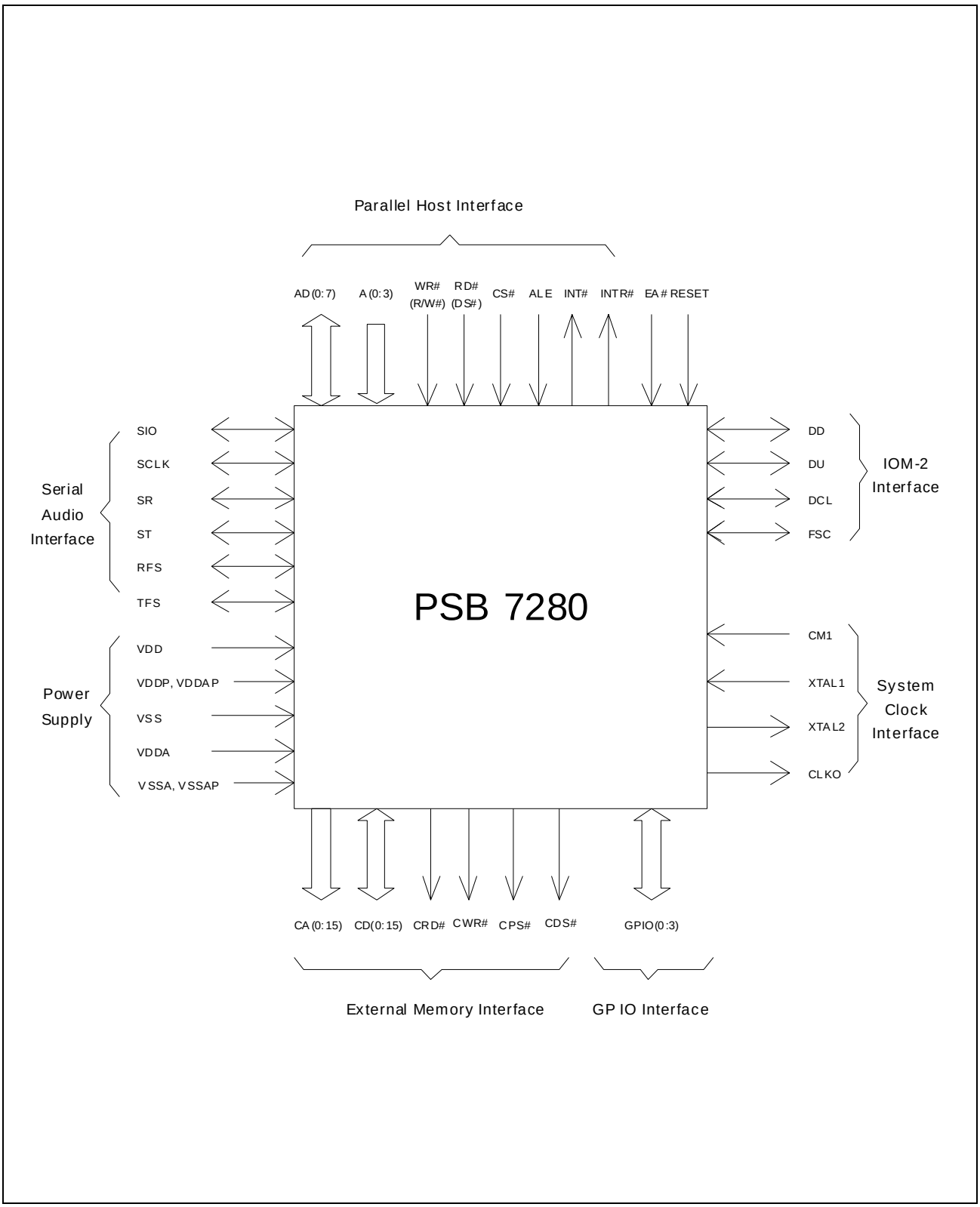


Figure 1

1.4 Pin Configuration

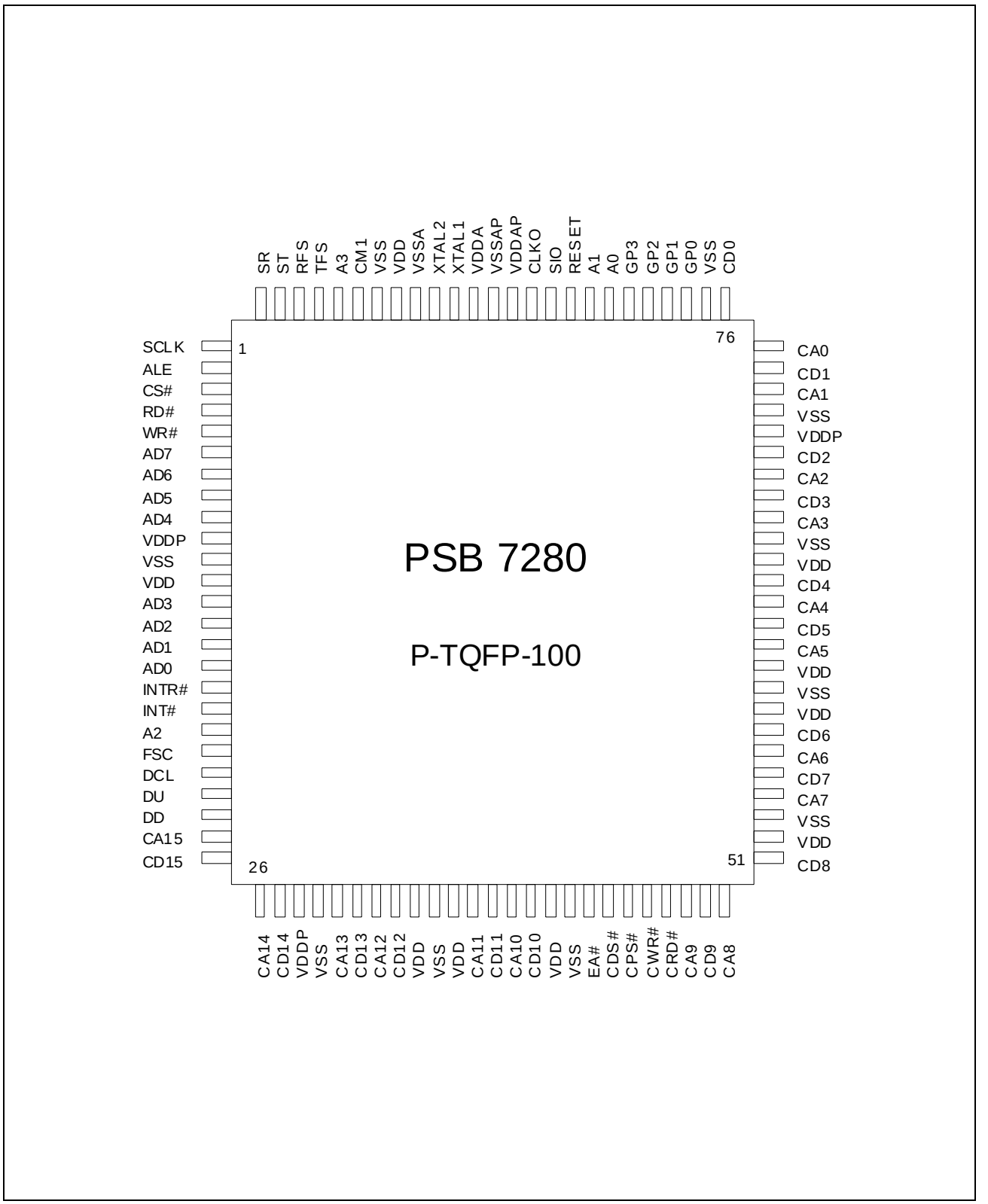


Figure 2

1.5 Pin Description

Table 1 Parallel Host Interface

Pin No.	Symbol	Function	Descriptions
16	AD0	I/O	**Multiplexed Bus Mode:** Address/Data Bus. Transfers addresses from the host to JADE and data between the host and the JADE Demultiplexed Bus Mode: Data bus. Transfers data between the host and the JADE
15	AD1	I/O	
14	AD2	I/O	
13	AD3	I/O	
9	AD4	I/O	
8	AD5	I/O	
7	AD6	I/O	
6	AD7	I/O	
4	$\overline{DS}$	I	Data Strobe. The rising edge marks the end of a valid read or write operation (Motorola bus mode).
	$\overline{RD}$	I	Read. This signal indicates a read operation (Siemens/Intel bus mode).
5	R/$\overline{W}$	I	Read/Write. A 1 (“high“) identifies a valid host access as a read operation. A 0 identifies a valid host access as a write operation (Motorola bus mode)
	$\overline{WR}$	I	Write. This signal indicates a write operation (Siemens/Intel bus mode).
3	$\overline{CS}$	I	Chip Select.
2	ALE	I	Address Latch Enable. A “high” on this line indicates an address on AD(0:7) (multipexed bus mode only). ALE also selects the interface mode
82	A0	I	Address Bits A(0:3) (demultiplexed bus type)
83	A1	I	
19	A2	I	
96	A3	I	

Table 1 Parallel Host Interface (cont'd)

Pin No.	Symbol	Function	Descriptions
17	$\overline{\text{INTR}}$	O (OD)	Interrupt Real-time. Interrupt output line for high priority interrupt status (serial audio receive/transmit, serial HDLC data receive/transmit data) to host.
18	$\overline{\text{INT}}$	O (OD)	Interrupt Request. Interrupt output line for all other interrupt states.

Table 2 IOM®-2 Interface

Pin No.	Symbol	Function	Descriptions
23	DD	I/O(OD)	Data Downstream on IOM-2/PCM interface.
22	DU	I/O(OD)	Data Upstream on IOM-2/PCM interface.
21	DCL	I/O(OD)	Data Clock. Clock frequency is twice the data rate, or equal to the data rate.
20	FSC	I/O(OD)	Frame Sync. Marks the beginning of a physical IOM-2 or PCM frame.

Table 3 Serial Audio Interface

Pin No.	Symbol	Function	Descriptions
1	SCLK	I/O	Serial Clock. Serial clock for SR and ST.
100	SR	I/O(OD)	Serial Data Receive. Should be connected to V_{SS} via a pulldown resistor if not used.
99	ST	I/O(OD)	Serial Data Transmit.
98	RFS	I/O	Audio Receive Frame Sync.
97	TFS	I/O	Audio Transmit Frame Sync.

Table 4 System Clocks

Pin No.	Symbol	Function	Descriptions
90	XTAL1	I	Crystal In or Clock In. If a crystal is used, it is connected between XTAL1 and XTAL2. If a clock signal is provided (via an external oscillator), this signal is input via XTAL1. In this case the XTAL2 output is to be left non-connected. The XTAL1 input has to be 50% duty cycle and must not exceed the voltage range between V_{SSA} and V_{DDA}.
91	XTAL2	O	Crystal Out. Left unconnected if a crystal is not used.
86	CLKO	O	Clock Out. Output clock of frequency equal to the internal frequency divided by a programmable factor.

Table 5 External Memory Interface (for Development Purposes only)

Pin No.	Symbol	Function	Descriptions
75	CA0	O	C-Bus Address.
73	CA1	O	Used for addressing ROM or RAM external to the chip.
69	CA2	O	Is to be left NC if not used.
67	CA3	O	
63	CA4	O	
61	CA5	O	
56	CA6	O	
54	CA7	O	
50	CA8	O	
48	CA9	O	
39	CA10	O	
37	CA11	O	
32	CA12	O	
30	CA13	O	
26	CA14	O	
24	CA15	O	

Table 5 External Memory Interface (for Development Purposes only) (cont'd)

Pin No.	Symbol	Function	Descriptions
76	CD0	I/O	C-Bus Data. Data bus for external ROM or RAM. Is to be left NC if not used.
74	CD1	I/O	
70	CD2	I/O	
68	CD3	I/O	
64	CD4	I/O	
62	CD5	I/O	
57	CD6	I/O	
55	CD7	I/O	
51	CD8	I/O	
49	CD9	I/O	
40	CD10	I/O	
38	CD11	I/O	
33	CD12	I/O	
31	CD13	I/O	
27	CD14	I/O	
25	CD15	I/O	
43	$\overline{EA}$	I	External program Access enable When "high", an access to program address range (0000_H-$7FFF_H$) fetches an instruction from on-chip ROM. Access to 8000_H-$FFFF_H$ addresses external memory via the External Memory Interface. When "low", an access to 0000_H-$FFFF_H$ (including 0000_H-$7FFF_H$, normally reserved for on-chip software) accesses external program memory via the External Memory Interface.
47	$\overline{CRD}$	O	C-Bus Read to external memories. Left NC if not used.
46	$\overline{CWR}$	O	C-Bus Write to external memories. Left NC if not used.
45	$\overline{CPS}$	O	C-Bus Select line for external program memory. Left NC if not used.
44	$\overline{CDS}$	O	C-Bus Select line for external data memory. Left NC if not used.

Table 6 General Control

Pin No.	Symbol	Function	Descriptions
95	CM1	I	Clock Mode Selects the option for the generation of the DSP internal working clock.
85	SIO	I/O	Serial I/O line. When programmed as input, a rising or falling (selectable) edge on this line may generate a maskable interrupt $\overline{\text{INT}}$ (host) or $\overline{\text{INT1}}$ (DSP). When programmed as output, its state is directly controlled by the DSP or the host.
84	RESET	I	Reset input. Reset time: > 1 ms.

Table 7 General Purpose I/O Interface

Pin No.	Symbol	Function	Descriptions
81	GP0	I/O (OD)	General purpose I/O pins
80	GP1	I/O (OD)	
79	GP2	I/O (OD)	
78	GP3	I/O (OD)	

Table 8 Power Supply

Pin No.	Symbol	Function	Descriptions
11	V_{SS}	I	Ground (common to V_{DD} and V_{DDP}) .
29	V_{SS}	I	
35	V_{SS}	I	
42	V_{SS}	I	
53	V_{SS}	I	
59	V_{SS}	I	
66	V_{SS}	I	
72	V_{SS}	I	
77	V_{SS}	I	
94	V_{SS}	I	
12	V_{DD}	I	Positive power supply voltage (3.0 - 3.6 V).
36	V_{DD}	I	
60	V_{DD}	I	
93	V_{DD}	I	
34	V_{DD}	I	*Note: In former versions, pins 34, 41, 52, 58 and 65 could be connected to V_{DDP} . This version requires them to be connected to V_{DD} .*
41	V_{DD}	I	
52	V_{DD}	I	
58	V_{DD}	I	
65	V_{DD}	I	
10	V_{DDP}	I	Positive power supply voltage (4.5 - 5.5 V) for external interfaces.
28	V_{DDP}	I	
71	V_{DDP}	I	
89	V_{DDA}	I	Separate positive power supply voltage (3.0 - 3.6 V) for Clock Generation Unit (Oscillator).
92	V_{SSA}	I	Separate Ground (0 V) for Clock Generation Unit (Oscillator).
87	V_{DDAP}	I	Separate positive power supply voltage (3.0 - 3.6 V) for Clock Generation Unit (PLL). *Note: The power supply for the PLL requires pin 87 connected to V_{DDAP}. In former versions pin 87 was connected to V_{DDP}*
88	V_{SSAP}	I	Separate Ground (0 V) for Clock Generation Unit (PLL)

1.6 Functional Block Diagram

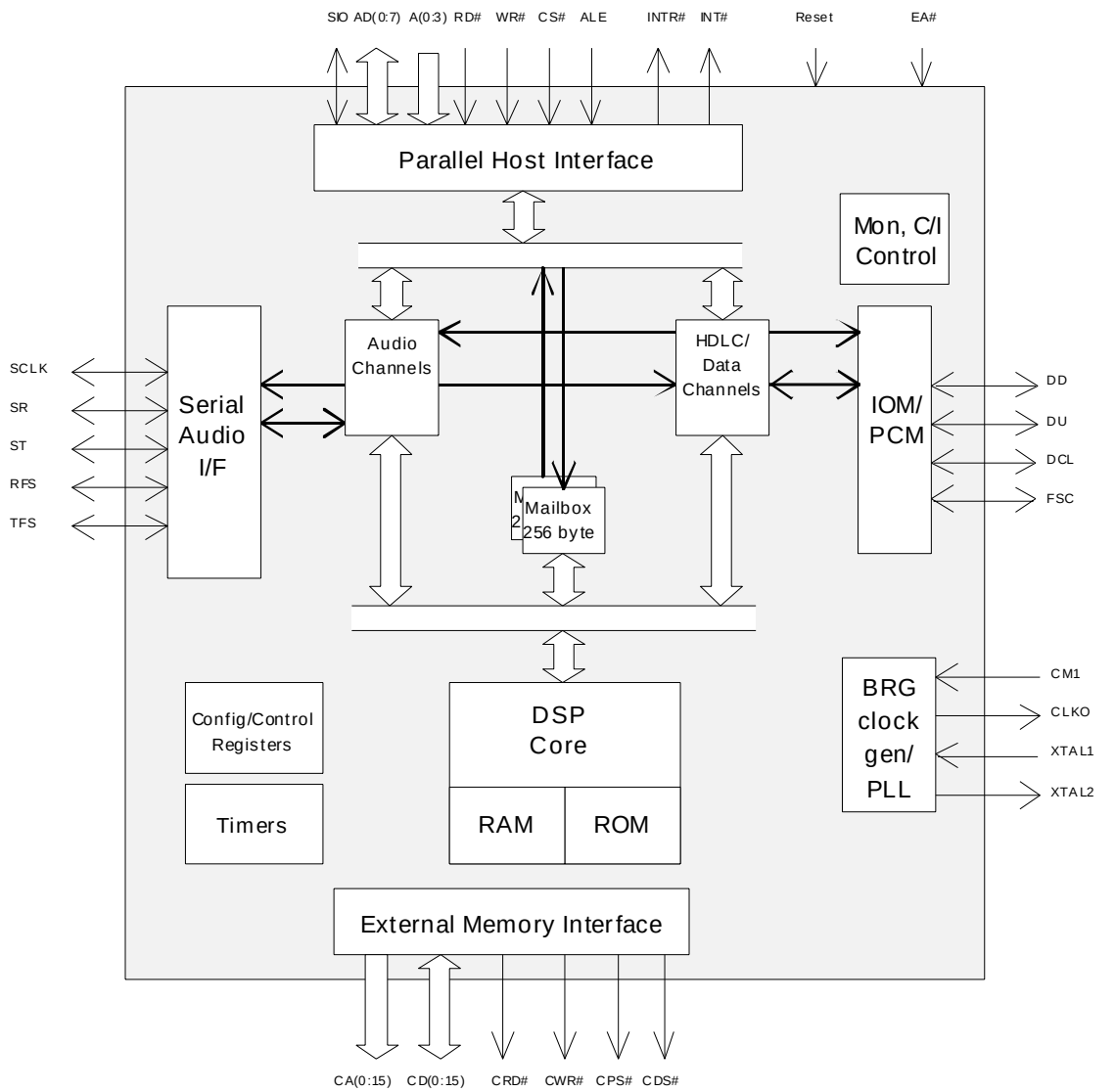


Figure 3

Detailed description see **Chapter 2**.

1.7 System Integration

Example of integration in ISDN/analog videophone:

The first example represents a low-cost solution for a desk-top standalone videophone that connects to an ISDN S0 bus (ISDN basic access) or an analog telephone line.

The ISDN basic access consists of two 64 kbit/s so-called B-channels to carry user information (voice, data,…), and a separate 16 kbit/s D-channel primarily used for signaling. The video and audio are both compressed so that they are carried, along with additional control information, in the two B-channels, or 128 kbit/s.

The general aspects of videotelephony are covered by ITU-T H.320 recommendation. The video is compressed according to the H.261 (sometimes called "p × 64") or the H.263 recommendation.

For the ISDN videophone (H.320) the compressed video and audio signals are multiplexed together with additional synchronization and control information into two B-channels, which are separately switched via the network and thus have to be resynchronized at the other end. The multiplexing and resynchronization of the B-channels is specified by the H.221 recommendation (see **Figure 4**).

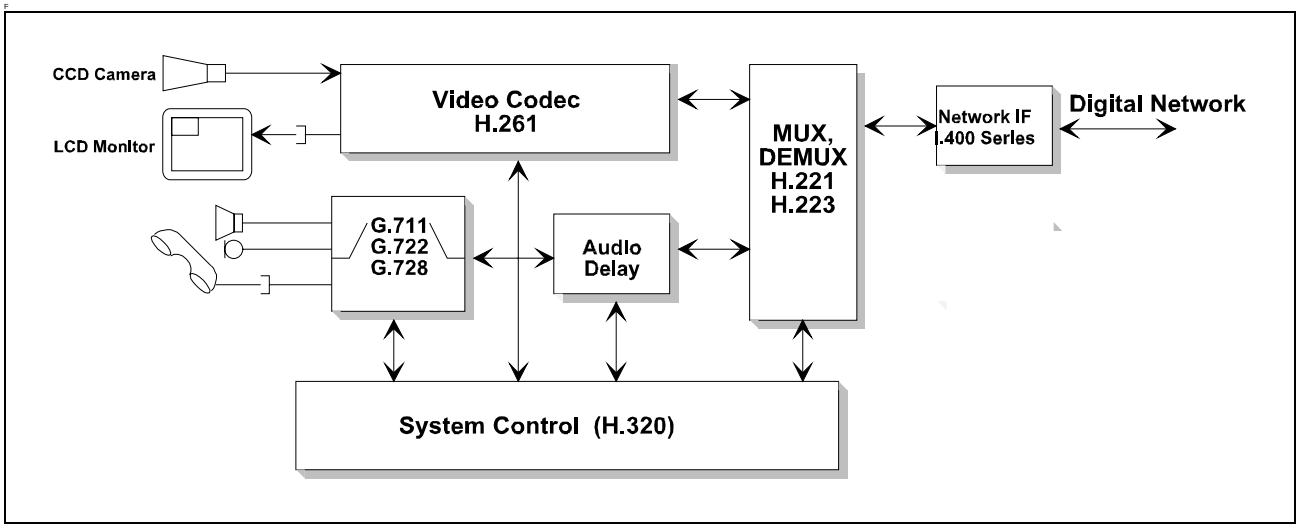


Figure 4

Using non-parametric compression techniques, audio can be compressed to 64 kbit/s PCM (logarithmical A- or μ-law approximation for 3.1-kHz voice acc. to G.711) or 48/56/64 kbit/s sub-band coded adaptive PCM (for 7-kHz audio acc. to G.722). This leaves, however, only approximately 64 kbit/s for video on the ISDN which, at this rate, yields only a marginally good picture quality. For the analog videophone it's not even possible to transfer only audio at this data rate.

In order to make the best possible use of the total bandwidth and obtain the best possible video quality, the audio should require only a small fraction of the total data rate. This is made possible by using parametric compression techniques such as LD-CELP (16 kbit/s). Above all, the corresponding norms (G.728) are internationally adopted

standards, so that compatibility between equipment from different manufacturers is ensured.

A low-cost H.320 videophone solution for ISDN line as a PCI card for commercial PC's is shown in **Figure 5**.

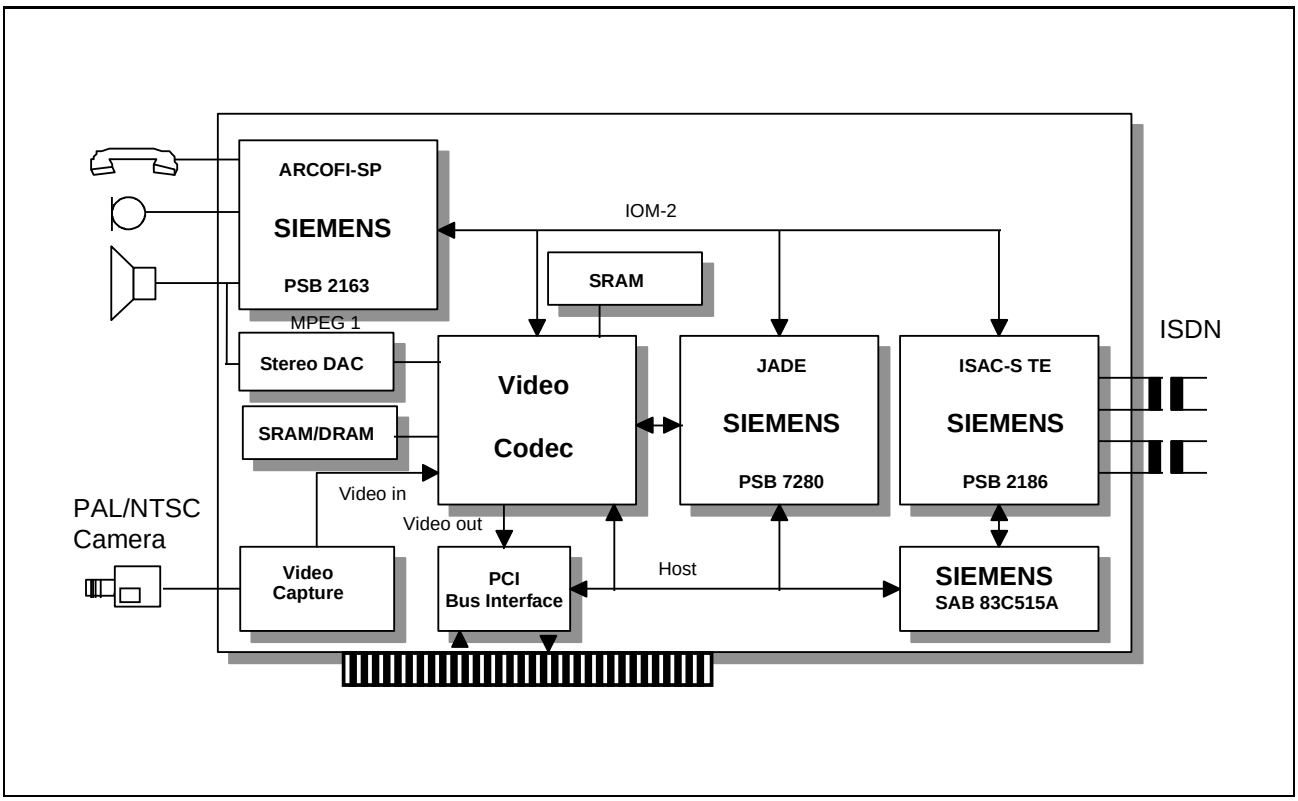


Figure 5

The JADE and the video codec chip (e.g. the Video Communication Processor "VCP" from 8 × 8 Inc.) constitute the heart of the videophone.

Both (together with the microcontroller 83C515) are connected to the PC via the PCI bus using PCI bus interface (e.g. the "VPIC" of 8 × 8 Inc.).

The JADE compresses/decompresses audio according to the ITU-T standards G.728, G.722 and G.711 and runs a fully inband controlled protocol on the interface to the video codec. It receives/transmits uncompressed audio via the IOM-2 interface from/to the ARCOFI-SP. The setup for this application is done automatically after a hardware reset, so no additional initialization by a host is required. Since the JADE has all its memories on chip, no external SRAM needs to be connected.

The ARCOFI-SP (Audio Ringing Codec Filter) is a hands-free codec for 3.1-kHz voice which performs detection and elaborate balancing of the received and transmitted audio to suppress undesirable effects due to acoustical feedback of the signal from the remote subscriber. The quality obtained is very close to that of echo-free full duplex conferencing.

The video is captured by a PAL/NTSC camera and digitized and demodulated e.g. by a standard SAA 7110 which is directly connected to the video processor. Alternatively, a digital camera may be used, which can be connected directly to the video processor.

The video processor compresses and decompresses video according to the ITU-T standards H.261 and multiplexes/demultiplexes video, audio and data according to H.221/223. The video processor uses DRAMs and SRAMs to store data and program code.

When operating in the ISDN mode, the H.221 multiplexed data stream is sent via the two B-channels of the IOM-2 interface to the ISAC-S-TE (ISDN Subscriber Access Controller for S-interface) which transmits them to the ISDN according to I.430 S0 interface recommendation. The ISAC-S-TE also handles, together with the attached microcontroller (e.g. SAB 83C515), D-channel layer-2 and layer-3 call control signaling.

The reverse functions are performed on the B-channels received from the network.

Instead of an S0, it is conceivable to implement any other layer-1 interface just by replacing the ISAC-S TE by an appropriate transceiver, e.g. by a transceiver for **2-wire** digital transmission ISAC-P PSB 2196 or ISDN echo canceller for 2B1Q.

To achieve “lip synchronization”, the audio may be delayed with respect to the video. This is necessary because of the higher transmission delay suffered by the video signal, due to the elaborate H.261/263 video compression. A delay of approximately 0.5 seconds is enough in most practical cases. To make maximum use of the existing memory in the system, the delay is performed by the video processor with its external RAMs.

In videophone applications calling for high quality, 7-kHz wide-band audio, the PSB 7280 can be switched to G.722 mode. In this case the rate of the compressed audio is 48, 56 or 64 kbit/s.

When decoding MPEG bitstreams, the audio D/A conversion is provided by a stereo audio DAC.

Demonstration board designs for H.320 PC based videophones containing the chip set from Siemens AG and 8 × 8 Inc. are available and can be ordered from Siemens/8 × 8.

2 General Architecture and Functions

2.1 Architecture

Figure 6 shows a sketch of the PSB 7280 architecture with its most important functional modules.

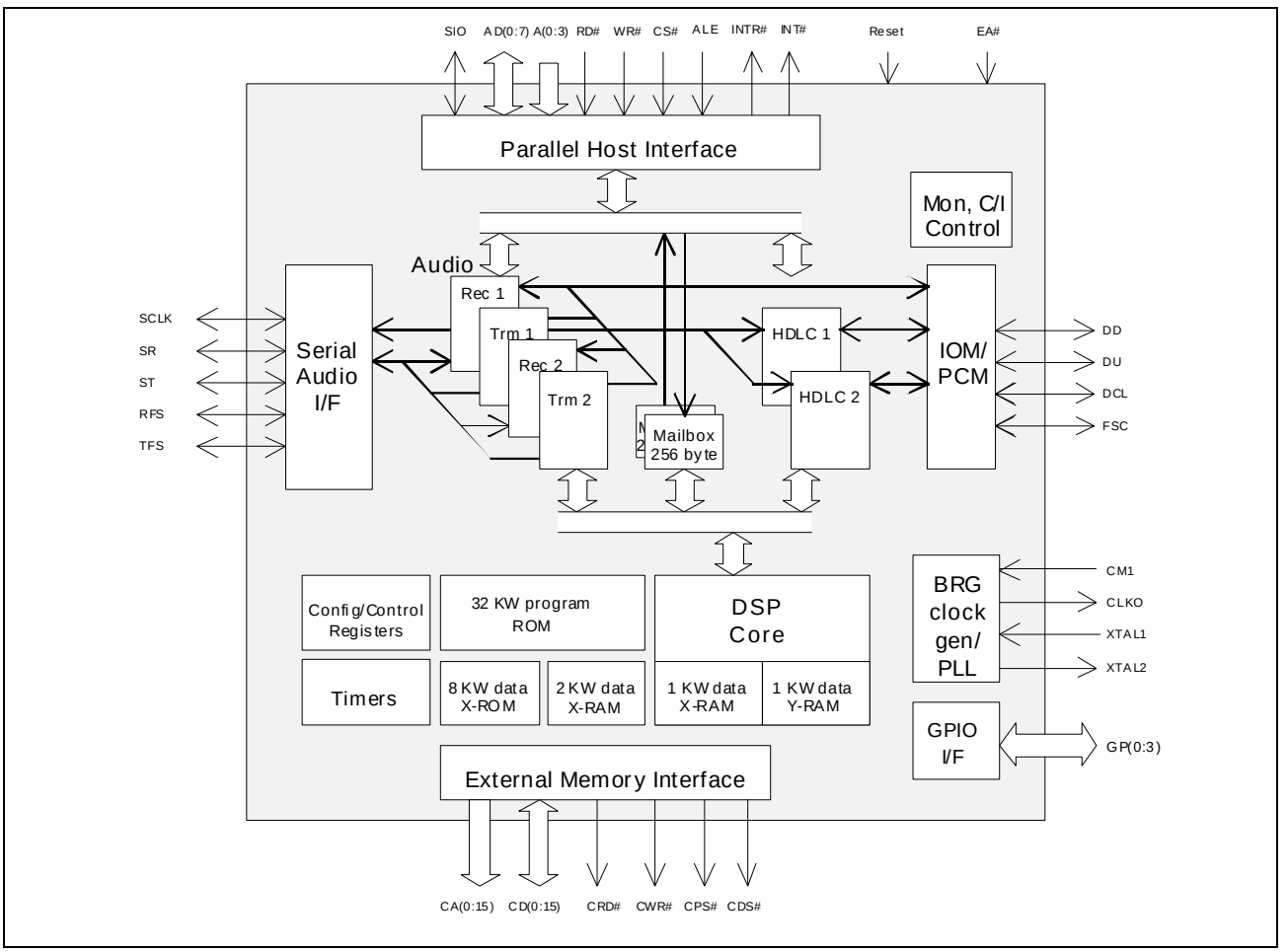


Figure 6

The audio processing of the PSB 7280 is based on a 16-bit fixed point DSP core, **SPCF** (Signal Processor Core Fast).

The **Clock Generator** is responsible for generating the internal clocks for the SPCF. A **Baud Rate Generator** provides an output clock of programmable rate.

The **Parallel Host Interface** is used to control the circuit through an associated host via interrupt handshake procedures. Alternatively, the circuit can be controlled via the serial audio interface, thus enabling standalone applications to be implemented. Communication between the host, if used, and the DSP is interrupt supported, via a full-duplex 256-byte on-chip **Communication Memory Mailbox**.

Two receive and two transmit audio channels are provided. They are input/output on the **ISDN Oriented Modular** (IOM-2) or the **Serial Audio Interface** (SAI) interfaces in individually programmable time-slots. These channels are accessed from the DSP and/or the parallel host interface.

The two **HDLC Controller** channels can be serviced by the DSP or the parallel host interface. The serial data for the HDLC controllers are located in programmable time-slots on IOM-2 and/or SAI.

For development purposes, the **External Memory Interface** allows programs to be executed from an external memory and external data memory to be used.

2.2 Functions

2.2.1 Summary of the Functions

The main functions implemented by the PSB 7238 are:

– G.728 compression/decompression (16 kbit/s)
– G.722 compression/decompression for 7-kHz audio (64, 56, 48 kbit/s)
– G.711 compression/decompression (64 kbit/s)
– Digital sampling rate conversion (16 kHz - 8 Hz) for G.722 audio with 8-kHz codec (bandwidth reduced to 3.4 kHz)
– Accepts/outputs uncompressed audio 8-bit PCM A/μ law or 16-bit linear format
– Uncompressed/compressed audio switchable between different interface combinations (IOM/Serial Audio Interface, IOM/Host, Host/Host)
– Inband controlled H.221/H.223 oriented audio protocol, e.g. for direct serial connection to videocodec (VCP of 8 × 8 Inc., formerly IIT Inc.)
– Outband controlled audio protocol with optimized data rate
– Stable reaction on interrupt handshake timing violations of e.g. a slow host (Windows® PC)

For more details on the hardware (necessary for a better understanding of some of the topics described in the present chapter), please refer to the other chapters of this data sheet.

2.2.2 Audio Functions and Supplementary Features

General

The uncompressed/compressed audio is applied to the interfaces as follows:

Uncompressed Audio	Compressed Audio
IOM-2 (transparent)	SAI (H.221/223 oriented audio protocol or transparent)
IOM-2 (transparent)	Host IF (interrupt handshake protocol with minimized interrupt load for the host)
Host IF (interrupt handshake protocol)	Host IF (interrupt handshake protocol)

“Transparent” means that data is received/transmitted in a time-slot without protocol.

1. Full Duplex G.728 Encoding/Decoding of One Audio Channel

Audio coding according to ITU-T G.728 fixed point recommendation using Low Delay Code Excited Prediction (LD-CELP, 16 kbit/s), offering toll quality audio. The postfilter of the G.728 may be switched on (offering a higher quality impression) or off (providing objective better S/N values).

2. Full Duplex G.722 Encoding/Decoding of One Audio Channel

Audio coding for 7-kHz voice using the Sub-Band Coded Adaptive Differential PCM (SB-ADPCM) algorithm according to the G.722 Recommendation.

3. Serial H.221/223 Oriented Audio Protocol

The PSB 7280 supports a serial H.221/223 oriented audio protocol for direct connection to a Videocodec (VCP of 8×8 Inc.). This protocol provides an outband synchronization of the audio bit streams by using block structures for the compressed audio data.

3 Interfaces and Memory Organization

3.1 Interfaces

3.1.1 IOM®-2 Interface

Electrical Interface

The IOM-2 interface is a 4-wire interface with two data lines (DD and DU, programmable open drain or push-pull), a data clock line (DCL input/output) and a frame sync signal (FSC input/output). The data clock is by default equal to twice the data rate (“Double Rate”). However, DCL may be set equal to the data rate (“Single Rate”) by programming. In standalone configuration the clock signal is always “Double Rate”.

In terminal applications, the bit rate on the interface is normally 768 kbit/s, in line card applications it is 2048 kbit/s (for details, see IOM-2 Interface Reference Guide). However, the data rate may be different (between 16 kbit/s and 4.096 Mbit/s and the DCL rate correspondingly between 16 kHz and 4.096 MHz), since the interface can be considered as a general purpose TDM (Time-Division Multiplex) highway.

The total number of time-slots on the interface is not explicitly programmed: instead, the FSC signal (at repetition rate 8 kHz) always marks the TDM physical frame beginning (see **Figure 7**).

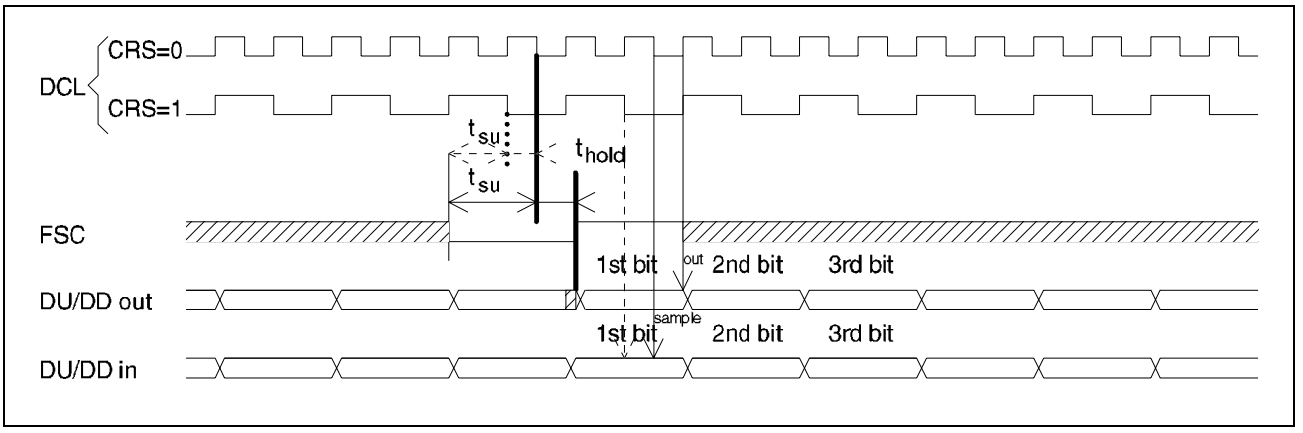


Figure 7

DCL — Bits on DU/DD are clocked out with the rising edge of DCL and latched in with the falling edge of DCL. Frequency 16 kHz to 4.096 MHz.

FSC (8 kHz) — Marks the beginning of the physical frame on DU and DD. The first bit in the frame is output after the rising edge of FSC. The first bit in the frame is latched in with the first falling edge after FSC has gone “high” if CRS = 1, or after the second edge (at 3/4) if CRS = 0.

Channels

The following channels may be programmed on the IOM-2 interface: two receive audio channels, two transmit audio channels, one monitor channel, two C/I channels, two receive and two transmit HDLC channels:

Audio receive 1 and receive 2 channels Audio transmit 1 and transmit 2 channels	Independently programmable on DD or DU, with programmable locations (start at bit 1…512) and lengths (1…32 bits) w.r.t. FSC
Monitor channel	Programmable on DD(in)/DU(out) or DD(out)/DU(in), with programmable time-slot (3rd byte in multiplex 0, …, 15) after FSC
Two C/I channels	Programmable on DD(in)/DU(out) or DD(out)/DU(in), with programmable length (4 or 6 bits) and position (4^{th} byte in multiplex 0, …, 15) after FSC
Two HDLC receive and transmit channels	Independently programmable on DD or DU, with programmable locations (start at bit 1…512) and lengths (1…256 bits) w.r.t. FSC

The transfer of voice samples is performed with the help of an interrupt with repetition rate 8 kHz derived from the FSC signal. A double-buffered register is provided for each channel, accessible from the DSP and from the parallel host interface. The double buffered register ensures that enough time is always provided for reading and writing data before an overflow/underflow occurs, independent of the location of the time-slots. Alternatively, the audio samples can be transferred between the DSP or Host and IOM-2 by using an interrupt generated when a programmable number (1…32) of bits are shifted out (number independent of the time-slot length on the line).

Outside the time-slots where transmission takes place the DU and DD lines are in high impedance.

3.1.2 Serial Audio Interface

The Serial Audio Interface is a generic 5-line serial interface with the following lines:

SCLK	Serial Bit Clock	Input or output.
SR	Serial Receive	Input/output.
ST	Serial Transmit	Input/output.
RFS	Receive Frame Sync	Input or output.
TFS	Transmit Frame Sync	Input or output.

Figure 8 shows an example where RFS is input and TFS is output.

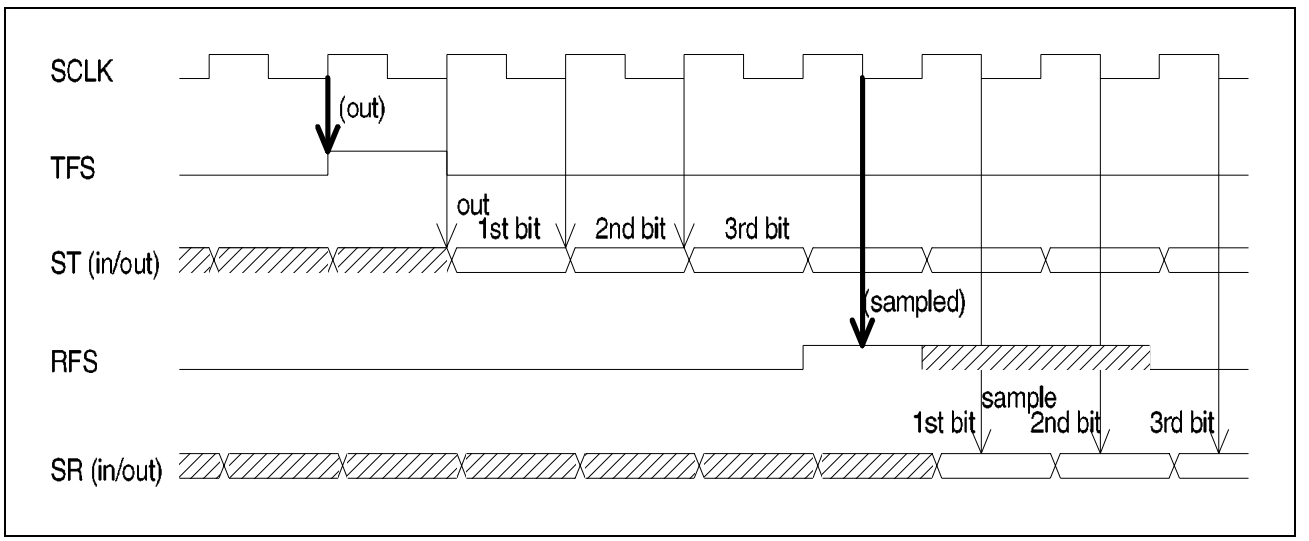


Figure 8

SCLK Input or output

Bits on SR/ST are clocked out with the rising edge of SCLK and latched in with the falling edge of SCLK. Alternatively, bits can be clocked out with the falling edge of SCLK and latched in with the rising edge. When SCLK is programmed as output, it is derived from a programmable baud rate generator. Additionaly, SLCK can be set to strobed operation.

RFS Input or output

Marks the beginning of the physical frame on SR.

When input	Sampled with a falling edge of SCLK.
When output	Clocked out with the rising or falling edge of SCLK (duration = 1 SCLK period). Repetition rate (continuous mode) or number of pulses (burst mode) is programmable

TFS Input or output

Marks the beginning of the physical frame on ST.

When input	Sampled with a falling edge of SCLK .
When output	Clocked out with the rising or falling edge of SCLK (duration = 1 SCLK period). Repetition rate (continuous mode) or number of pulses (burst mode) is programmable.

SCLK is derived from the chip-internal DSP clock via a programmable baud rate generator (division factor 1, 2, 3, …, 1024).

The Receive Frame Sync (RFS), when programmed as output, has two selectable modes of operation:

– In the **continuous mode** (CONT = 1), pulses are continuously generated, separated by a distance
  16 × (PRD + 1) bits from each other, where PRD = 0, …, 255.
– In the **burst mode** (CONT = 0), pulses are generated upon command a programmable number of times (REP + 1: 1, …, 1024), spaced 16 bits apart from each other.

The same applies to TFS when it is an output.

Channels

Two Audio receive and transmit channels	Independently programmable on SR, ST, DU or DD with programmable locations (start at bit 1…512) and lengths (1…32 bits) with respect to RFS/TFS.
Two HDLC receive and transmit channels	Independently programmable on SR, ST, DU or DD with programmable locations (start at bit 1…512) and lengths (1…256 bits) with respect to RFS/TFS.

3.1.3 Parallel Host Interface

The parallel host interface can be selected to be either of the

(1) Motorola type with control signals $\overline{CS}$,R/$\overline{W}$, $\overline{DS}$

(2) Siemens/Intel demultiplexed bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$

(3) or of the Siemens/Intel multiplexed address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE

The selection is performed via pin ALE as follows:

ALE tied to $V_{DD} \rightarrow$ (1)

ALE tied to $V_{SS} \rightarrow$ (2)

Edge on ALE $\rightarrow$ (3)

The occurence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the multiplexed bus type. A return to one of the other is possible only if a hardware reset is issued.

3.1.4 External Memory Interface

The external memory interface allows the connection of both program and data memories to the PSB 7280. The access to either type of memory is determined by the signals $\overline{CPS}$ and $\overline{CDS}$, respectively. In standard applications, the external memory interface used as a program memory interface is normally not needed, but is reserved for development purposes.

The upper 32k half (8000_H-$FFFF_H$) of the address space is reserved for execution of software from external memory.

For executing software in the lower address range 0000_H-$7FFF_H$, a control line EA (External Access) determines whether program is fetched from internal or external memory. Thus, in standard applications, the $\overline{EA}$ line should always be “high”.

The DSP program execution can be controlled from the outside by loading the PC-counter of the DSP via the parallel host interface.

The external memory interface implements:

– protection against reading the internal ROM.

3.1.5 Clock Interface

The chip internal clock is derived from a crystal connected across XTAL1,2 or from an external clock input via pin XTAL1. Two different clock options are provided, controlled by the clock mode pin CM1.

These clock modes are:

CM1 = 0 The internal clock circuitry generates a frequency 4.5 times the input on XTAL1(,2). The internal frequency required is 34.56 MHz and is obtained by providing a frequency of 7.68 MHz on XTAL1 input.

CM1 = 1 The internal frequency is directly input via XTAL1(,2). When using a crystal, a 34.56 MHz crystal swinging at its basic harmonic has to be connected to XTAL1,2.

After reset the pin CLKO outputs a frequency of 7.68 MHz, independent of the selection of CM1 bit. Alternatively, CLKO can be programmed to output the frequency of a programmable divider (CKOS bit in register 2002_H). Thus, a clock of frequency equal to the internal clock divided by a programmable baud rate factor (1, 2, 3,…, 2^{19}) can be generated.

When using the PLL (CM1 = 0), it is made sure that during reset phase CLKO delivers a continuous 7.68 MHz clock. When using the non-PLL mode (CM1 = 1) CLKO goes low while reset phase.

3.2 Shared Memories

*Note: The absolute addresses for the different internal register banks and memories are given here and in the rest of this Data Sheet both as seen from the host **and** from the embedded DSP, the latter information being included for the sake of completeness only.*

Directly Accessible Register Bank (DARB)

The host accesses directly via its 8-bit address bus the so-called **Directly Accessible Register Bank (DARB)** located between DSP addresses 3000_H and $30FF_H$.

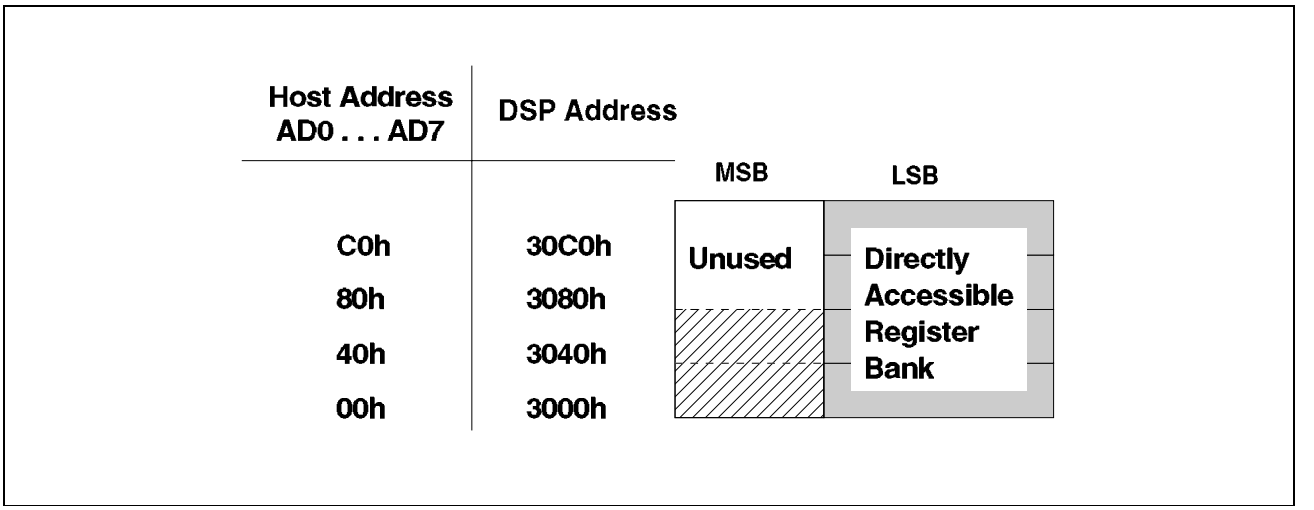


Figure 9

This area is in turn divided into four blocks of 64 bytes each according to their functions. Not all the addresses in each of these 64-byte areas are used. An overview of the functions of these 64-byte areas is given in **Figure 10**, please refer also to the appropriate chapters for a detailed description.

1. Locations for reading and writing samples “in real time” from/to the serial interfaces (IOM-2 and serial audio interface) - **Input/Output area** (see **Chapter 3.3.1**).
2. Area for communication between the host and the embedded DSP, for programming parameters and reporting status conditions - **DSP/Host Com area** (see **Chapter 3.3.2** and **Chapter 3.3.3**).
3. Register bank for HDLC Controller 1 - accessed by host if HHA1 (configuration bit) is ‘1’ - **HDLC1**.
4. Register bank for HDLC Controller 2 - accessed by host if HHA2 (configuration bit) is ‘1’ - **HDLC2**.

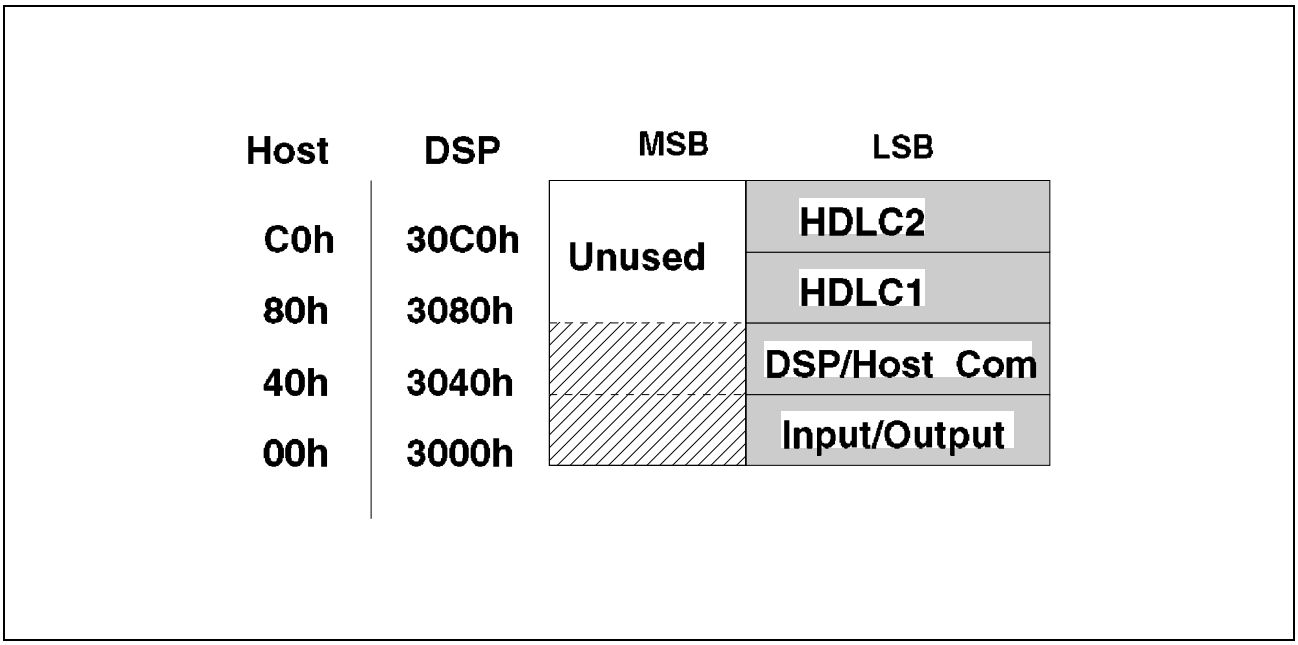


Figure 10

3.3 Directly Accessible Register Bank

3.3.1 Input/Output Registers

This area contains the locations for receiving/transmitting real-time audio and data between the serial interfaces (IOM-2 and serial audio interface) and the host (or embedded DSP).

The PSB 7280 implements two receive and two transmit audio channels, denoted RC1,2 and XC1,2, respectively. Further, two receive and two transmit channels are provided to access the HDLC1,2 receiver input data and the HDLC1,2 transmitter output, respectively, called HR1,2 and HX1,2.

Transfer of audio samples is interrupt supported, whereby two possibilities are provided:

– interrupt status generated after a programmable number of bits (1…32) have been shifted in/out;
– interrupt indicating the start of a physical frame (normally at 8 kHz, either from FSC, RFS or TFS frame sync pulses): in this case the number of significant bits depends on the time-slot length programmed for that channel on the line (DU/DD/SR/ST).

The interrupt statuses may generate a maskable interrupt on the high priority interrupt lines $\overline{\text{INTR}}$ (Host) and/or INT0 (embedded DSP), respectively.

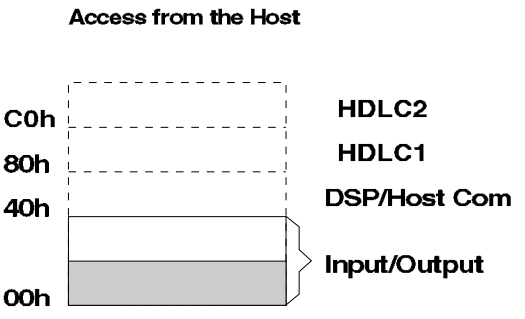
RC1, RC2, XC1, XC2, HR1, HR2, HX1, HX2 channel registers are located in the address range 00_H - $3F_H$ for the host, and in the memory mapped area 3000_H - $303F_H$ for the DSP. The register banks for the host and the DSP are physically separate from each other. The read registers and write registers are physically separate.

The addresses for these registers are such that a 32-bit sample can be accessed from the DSP via only two 16-bit read/write operations (16-bit data bus). From the host, the access is byte-by-byte (8-bit data bus).

List of Registers

RC1: 32-bit register for audio receive channel 1 (read)
RC2: 32-bit register for audio receive channel 2 (read)
XC1: 32-bit register for audio transmit channel 1 (write)
XC2: 32-bit register for audio transmit channel 2 (write)
HRR1: 32-bit register for reading data from HDLC receiver 1 input shift register
HRW1: 32-bit register for writing data to be loaded into HDLC receiver 1 input
HXR1: 32-bit register for reading data from HDLC transmitter 1 output
HXW1: 32-bit register for writing data to HDLC transmitter 1 output shift register
HRR2: 32-bit register for reading data from HDLC receiver 2 input shift register
HRW2: 32-bit register for writing data to be loaded into HDLC receiver 2 input
HXR2: 32-bit register for reading data from HDLC transmitter 2 output
HXW2: 32-bit register for writing data to HDLC transmitter 2 output shift register

Memory Map



Host Address A0 - A7	Host Write	Host Read
1Fh	HXW2 (31:24)	HXR2 (31:24)
1Eh	HXW2 (23:16)	HXR2 (23:16)
1Dh	HXW2 (15:8)	HXR2 (15:8)
1Ch	HXW2 (7:0)	HXR2 (7:0)
1Bh	HRW2 (31:24)	HRR2 (31:24)
1Ah	HRW2 (23:16)	HRR2 (23:16)
19h	HRW2 (15:8)	HRR2 (15:8)
18h	HRW2 (7:0)	HRR2 (7:0)
17h	HXW1 (31:24)	HXR1 (31:24)
16h	HXW1 (23:16)	HXR1 (23:16)
15h	HXW1 (15:8)	HXR1 (15:8)
14h	HXW1 (7:0)	HXR1 (7:0)
13h	HRW1 (31:24)	HRR1 (31:24)
12h	HRW1 (23:16)	HRR1 (23:16)
11h	HRW1 (15:8)	HRR1 (15:8)
10h	HRW1 (7:0)	HRR1 (7:0)
07h	XC2 (31:24)	RC2 (31:24)
06h	XC2 (23:16)	RC2 (23:16)
05h	XC2 (15:8)	RC2 (15:8)
04h	XC2 (7:0)	RC2 (7:0)
03h	XC1 (31:24)	RC1 (31:24)
02h	XC1 (23:16)	RC1 (23:16)
01h	XC1 (15:8)	RC1 (15:8)
00h	XC1 (7:0)	RC1 (7:0)

Figure 11

Alignment of Data for Audio Channels

The most significant bit is always the first bit received/transmitted. Therefore, if audio is processed in units of N bits (N programmable between 1 and 32), the alignment of the data for receive and transmit audio channels in the registers is as shown in the **Figure 12**.

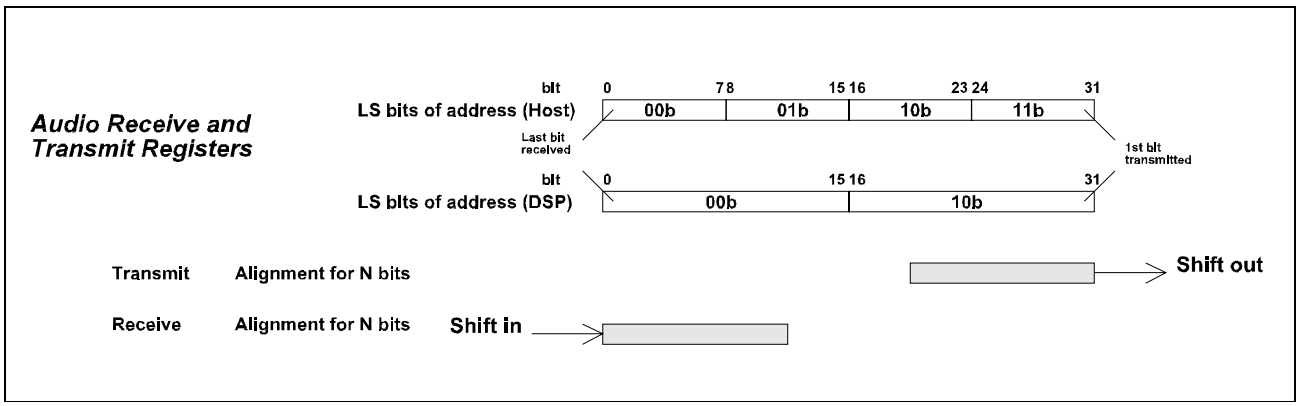


Figure 12

Alignment of Data for HDLC/Transparent Serial Data Receiver and Transmitter Registers

In the HDLC controllers the reception/transmission of most significant or least significant bit can be selected by control switches (RMSB, XMSB). Nevertheless, for serial data communication, the convention is that the least significant bit of user data is received/transmitted first. In order to have an identical format for the data in the serial controller input/output registers as in the FIFOs, the data is aligned in the registers as shown below (the available options for data unit sizes when pre/postprocessing HDLC/transparent data are: 1, 2 or 4 bytes).

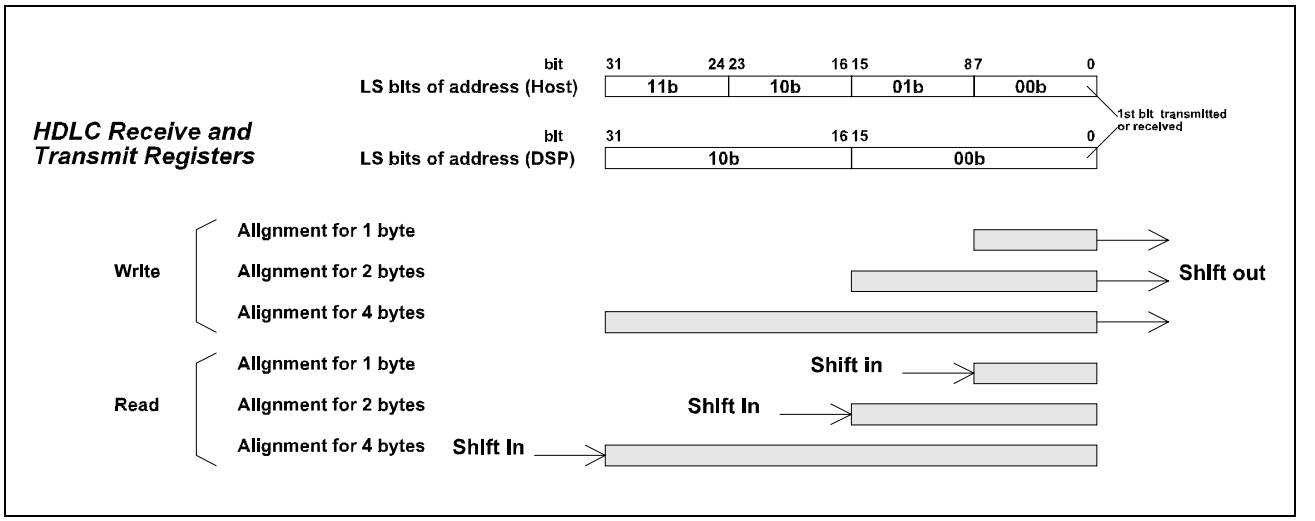


Figure 13

3.3.2 DSP/Host Com Area with a Multiplexed Host Interface

The DSP/host communication area contains the registers to support hardware and software interrupts and special purpose registers that support communication between the embedded DSP and the host. In multiplexed mode, address and data are multiplexed on pins AD(0-7). It is necessary e.g for indirect programming of the configuration and control registers from the host and for a complete access to all host addresses

3.3.2.1 Access to DSP/Host Com Area

The address mapping in multiplexed mode is given in **Table 9**.

Table 9 Address Mapping of DSP/Host Com Area (Multiplexed Mode)

DSP Address	DSP Write (always 16bit wide)	DSP Read (always 16 bit wide)	Host Address AD0-7	Host Write (always 8bit wide)	Host Read (always 8bit wide)
			FF_H-FE_H	reserved	reserved
			FD_H-FC_H	reserved	reserved
			77_H	Acknowledge $\overline{INT}$ MSB	
3076_H	Acknowledge $\overline{INT}$		76_H	Acknowledge $\overline{INT}$ LSB	
			75_H	Interrupt $\overline{INT}$ Mask MSB	Interrupt $\overline{INT}$ Status MSB
3074_H	Interrupt $\overline{INT}$ Mask	Interrupt $\overline{INT}$ Status	74_H	Interrupt $\overline{INT}$ Mask LSB	Interrupt $\overline{INT}$ Status LSB
			73_H	Acknowledge $\overline{INTR}$	
3072_H	Acknowledge $\overline{INTR}$				
			71_H	Interrupt $\overline{INTR}$ Mask MSB	Interrupt $\overline{INTR}$ Status MSB
3070_H	Interrupt $\overline{INTR}$ Mask	Interrupt $\overline{INTR}$ Status	70_H	Interrupt $\overline{INTR}$ Mask LSB	Interrupt $\overline{INTR}$ Status LSB
			$6C_H$	reserved	reserved

Table 9 Address Mapping of DSP/Host Com Area (Multiplexed Mode) (cont'd)

DSP Address	DSP Write (always 16bit wide)	DSP Read (always 16 bit wide)	Host Address AD0-7	Host Write (always 8bit wide)	Host Read (always 8bit wide)
			$6A_H$	reserved	reserved
3061_H	Cntrl DSP → Host MSB	Cntrl Host → DSP MSB	61_H	Cntrl Host → DSP MSB	Cntrl DSP → Host MSB
3060_H	Cntrl DSP → Host LSB	Cntrl Host → DSP LSB	60_H	Cntrl Host → DSP LSB	Cntrl DSP → Host LSB
	Note: Read and write accesses to 3060_H and 3061_H from the DSP are 8-bit wide only.				
3058_H	IND Interrupt Status	INDB (LSBit)	58_H	INDB (LSBit)	IND Interrupt Status
3050_H	INHB (LSBit)	INH Interrupt Status	50_H	INH Interrupt Status	INHB(LSBit)
			$4C_H$	Mailbox IO write	Mailbox IO read
			$4A_H$	Mailbox write address	
			48_H	Mailbix read address	
			47_H	Ext. Memory Data high	
			46_H	Ext. Memory Data low	
			45_H	Ext. Memory Addr high	
			44_H	Ext. Memory Addr low	

Table 9 Address Mapping of DSP/Host Com Area (Multiplexed Mode) (cont'd)

DSP Address	DSP Write (always 16bit wide)	DSP Read (always 16 bit wide)	Host Address AD0-7	Host Write (always 8bit wide)	Host Read (always 8bit wide)
3041_H	Reg Data DSP → Host	Reg Data Host → DSP	41_H	Reg Data Host → DSP	Reg Data DSP → Host
3040_H	RDY(LSBit)	Conf/Cont Reg Address	40_H	Conf/Cont Reg Address	RDY(LSBit)

The functions of these registers are described below.

Indirect Access to Configuration and Control Registers

Writing of hardwired registers (configuration and control registers) in the DSP memory (from 2000_H to $203F_H$) can be effected through the parallel host interface.

For the last case two directly accessible locations are provided in the DSP/host com area (host addresses 40_H and 41_H). A write operation in the first of these registers with a command (read/write) and a 6-bit address offset will cause the DSP to read or write a configuration/control register in address space 2000_H - $203F_H$. The second location (host address 41_H) contains the data read/written from/to the requested location.

DSP Address	DSP Write (always 16bit wide)	DSP Read (always 16 bit wide)	Host Address AD0-7	Host Write (always 8bit wide)	Host Read (always 8bit wide)
3041_H	Reg Data DSP → Host	Reg Data Host → DSP	41_H	Reg Data Host → DSP	Reg Data DSP → Host
3040_H	RDY(LSBit)	Conf/Cont Reg Address	40_H	Conf/Cont Reg Address	RDY(LSBit)

The procedure is described in **Table 10**.

Table 10

For reading a register from address (2000_H + a5:0)	Host writes byte: 1 0 a5 a4 a3 a2 a1 a0 to address 40_H. This causes RDY bit to be set to 0. Internally, an RACC interrupt status (INT1 line) is generated to the DSP. Firmware: DSP reads address 3040_H, recognizes a “read” access (most significant bit = 1), fetches data from (2000_H + a5:0), writes into 3041_H and sets RDY bit (address 3040_H/40_H) to ‘1’. After polling RDY bit to be ‘1’, the host can read the data from 41_H, and access 40_H for another operation.
For writing a register at address (2000_H + a5:0)	Host writes data into address 41_H. Host writes byte: 0 0 a5 a4 a3 a2 a1 a0 to address 40_H. This causes RDY bit to be set to 0. Internally, an RACC interrupt status (INT1 line) is generated to the DSP. Firmware: DSP reads address 3040_H, recognizes a “write” access (most significant bit = 0), fetches data from 3041_H, writes it into (2000_H + a5:0), and sets RDY bit (address 3040_H/40_H) to ‘1’. After polling RDY bit to be ‘1’, the host can access 40_H for another operation.

Software Interrupts

For communication between the host software and the DSP software, the soft interrupt registers IND (from DSP to host) and INH (from host to DSP) can be used.

Interrupt from Host to DSP

A write operation by the host to address 50_H (INH) causes a maskable INH interrupt status to be generated on INT1 to the DSP, and the Interrupt Host Busy bit INHB (address 50_H, readable by host) to be set to ‘1’. Having recognized an INH interrupt status, the DSP (firmware) reads address 3050_H (INH). This read operation automatically resets the HINT interrupt status bit in the DSP Interrupt Status Register for INT1 (address 3074_H). The INHB bit can be written by the DSP again to ‘0’ to indicate that it is ready to accept a new interrupt from the host, which it would usually (but not necessarily) do after it has read the INH register. The 16-bit control register located at $60/61_H$ ($3060/3061_H$) may contain additional information for the DSP to read after an INH interrupt. Please refer to the specific interface procedures for details.

Interrupt from DSP to Host

For a soft interrupt from the DSP to the host, the procedure is identical. In this case, the soft interrupt is a maskable interrupt on line $\overline{INT}$. The interrupt vector is written by the DSP in address 3058_H (IND). Simultaneously, the Interrupt DSP Busy bit INDB (address 58_H, writable by host) is set to '1'. Having recognized an IND interrupt status, the host reads address 58_H (IND), which automatically resets the DINT interrupt status bit in the Host Interrupt Status Register for $\overline{INT}$ (address 75_H). The INDB bit can be written by the host again to '0' to indicate that it is ready to accept a new interrupt from the DSP. The 16-bit control register located at $60/61_H$ ($3060/3061_H$) may contain additional information for the host to read after an IND interrupt. Please refer to the specific interface procedures for details.

Registers for Accessing the External Memory

In normal operation, the program bus of the DSP is connected via the external memory interface to the external memory bus so that instructions are fetched from an external memory when an address between 8000_H and $FFFF_H$ is hit, if $\overline{EA}$="High". If $\overline{EA}$="Low", the whole address range is for off-chip programs.

If the bit LDMEM (see description of Configuration and Control Registers, **Chapter 4**) is set to '1' and bit DACC is '0' (see description of Configuration and Control Registers, **Chapter 5.3**), the external memory interface address and data buses are connected to the outputs of registers address low/high (at host address $44/45_H$) and data low/high (at host address $46/47_H$), respectively. This feature can be used to down-load programs into a memory connected to the PSB 7280.

When a write access to the data high register (address 47_H) is detected, this activates the external memory interface write signal $\overline{CWR}$ for the duration of the host $\overline{WR}$ signal (independent of any possible wait states in NRW(3:0)). Thus the host writes one word of data into an external memory by effecting the following write operations:

Write Address Low + High
Write Data Low
Write Data High (operation is carried out during this write cycle).

When LDMEM is '1', the $\overline{CPS}$ signal is permanently active.

Note: When LDMEM is '0', the $\overline{CPS}$ signal is activated when a read access - program fetch - is performed on the external memory interface.

Registers Pertaining to the Mailbox

The function of these host registers is described in detail in the next section.

Hardware Interrupt Registers

In the following the interrupts for the host are listed, as well as, for completeness, those for the embedded DSP.

The interrupts are grouped so that the high priority interrupt statuses may cause a maskable interrupt on $\overline{\text{INTR}}$ (“Interrupts Real-time” for host) and/or INT0 (DSP), and the lower priority interrupt statuses on $\overline{\text{INT}}$ (host) and/or INT1 (DSP).

High priority interrupts ($\overline{\text{INTR}}$/INT0):

FSC, RFS, TFS
BFUL1, BFUL2, BEMP1, BEMP2, BFHR1, BFHX1, BFHR2, BFHX2

Lower priority interrupts ($\overline{\text{INT}}$/INT1):

T1, T2, T3
SAIN
HDLC1, HDLC2
HINT (to DSP) or DINT (to Host)
RACC (to DSP only)
GPI
MDR, MER, MDA, MAB, CIC1, CIC2

The active level of $\overline{\text{INTR}}$ and $\overline{\text{INT}}$ lines is “low”, of INT0 and INT1 “high”.

The interrupt line will remain active as long as an interrupt status (if unmasked) is not explicitly acknowledged, or the cause of the interrupt status has not been removed.

The registers for the interrupt status as well as the configuration and control registers (from address 2000_H upwards) are described in detail in **Chapter 5**.

3.3.2.2 Mailbox

The mailbox is implemented as physically two separate 256-byte memory blocks. Only least significant bytes are used. One is read-only by the DSP and write-only by the host, the other is write-only by the DSP and read-only by the host.

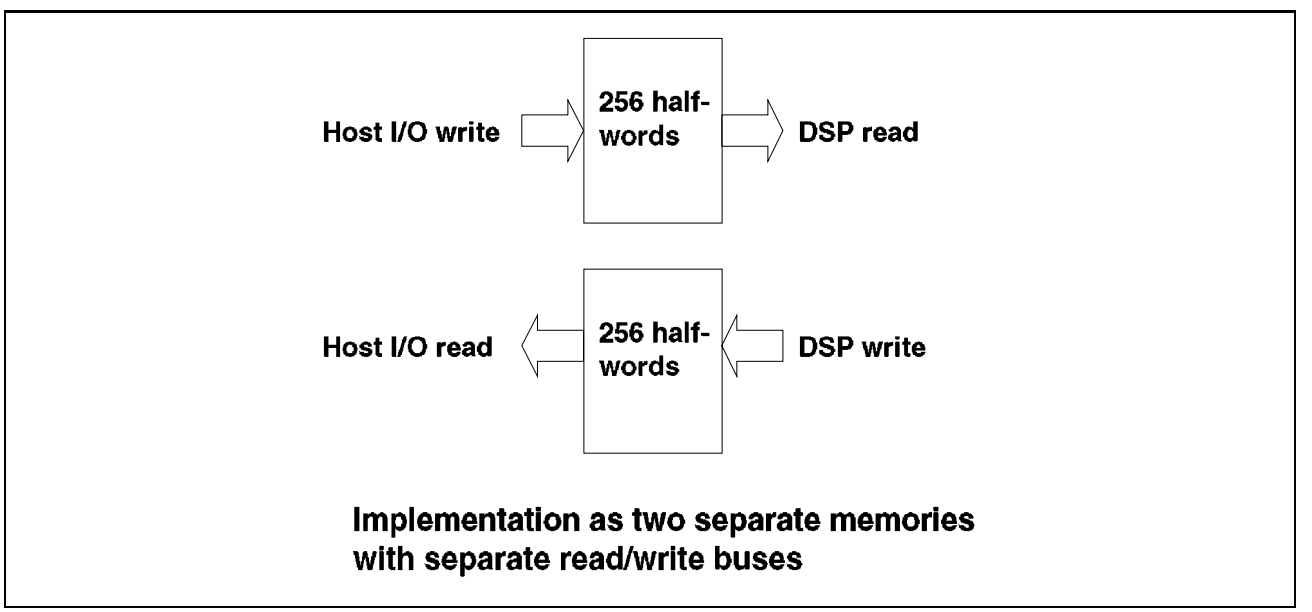


Figure 14

Since the two memories are totally independent, data transfer from host to DSP can take place simultaneously with data transfer from DSP to host (full duplex operation).

The mailbox is seen from the host as an I/O device. Thus, to read or write a byte in the mailbox, the host accesses a single location (separate for read and for write mailbox). The address is given by an address register directly programmable by the host. This address is autoincremented every time an access by the host to the mailbox I/O address is performed. Thus, for sequential, fast access, the mailbox is seen as a 256-byte, full duplex FIFO. For random accesses to the mailbox the host has to reprogram the address register(s). This is summarized in the **Figure 15**.

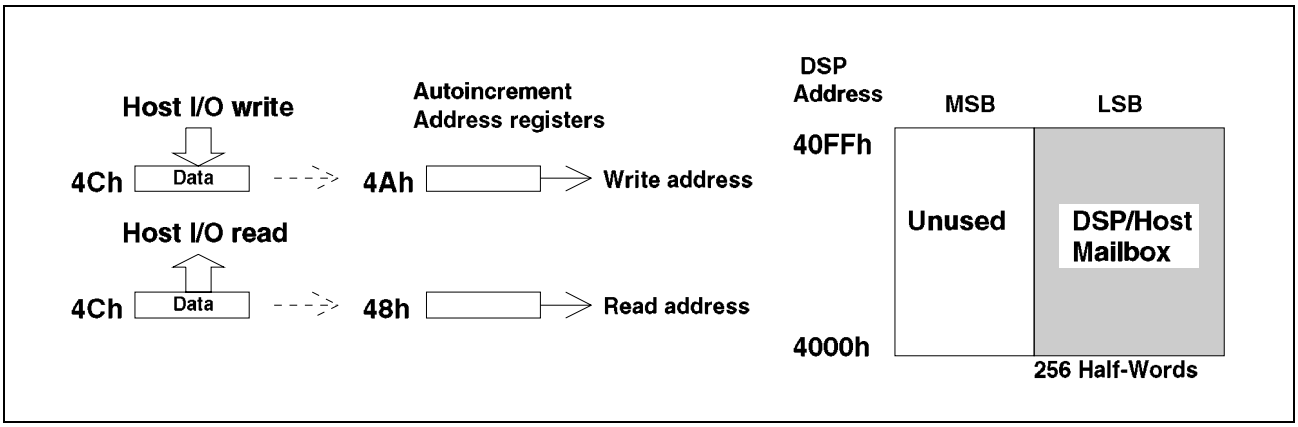


Figure 15

I/O Access from the Host to the Mailbox (Summary)

Read

Host programs the desired start address (00_H to FF_H) into address register 48_H.
Loop:
A read access from host to $4C_H$ gives the data from the current location in the read mailbox pointed to by the address register in 48_H.
The address register is autoincremented.
Go to Loop.

Write

Host programs the desired start address (00_H to FF_H) into address register $4A_H$.
Loop:
A write access from host to $4C_H$ writes the data into the current location in the write mailbox pointed to by the address register in $4A_H$.
The address register is autoincremented.
Go to Loop.
(In the case of overflow, the address register 48_H or $4A_H$ wraps around to 00_H.)

Software Handling of Communication via Mailbox

To indicate that data is ready to be read by the host/DSP, the DSP/host may use a general purpose 8-bit interrupt register located in the host/DSP comm section of the Directly Accessible Register Bank (DARB), associated with a 16-bit soft command and status word in the same area. This protocol is implemented in software. The same applies for indicating to the host/DSP that data has been read, in other words, the memory in one direction is free. See example below for using the mailbox involving a handshake protocol between the DSP and the host.

Simultaneous read/write is not prohibited by hardware, but a handshake mechanism (via IND/INH software interrupt registers with optional control data) is implemented in software.

Procedure from host to DSP (example):

Host
Write mailbox (1 to 256 bytes) if free (released by DSP)
Write word in control register ($60\text{-}61_H$) (e.g. number of bytes in mailbox)
Write 8-bit vector in INH
Internally, this causes an INT1 interrupt to DSP, which recognizes a “soft interrupt” (firmware)

DSP: services INT1 and acknowledges by writing an 8-bit vector in IND

Host
Read IND
Jump into routine pointed to by IND: “Mailbox release”
Write further data, etc.

3.3.3 DSP/Host Com Area with a Demultiplexed Host Interface

The DSP/host communication area contains the registers to support hardware and software interrupts and special purpose registers that support communication between the embedded DSP and the host. In demultiplexed mode, data are available on pins on pins AD(0-7), whereas the address is supplied on pins A(0-3). This mode gives an additional and more microprocessor-like way of accessing the DSP/Host Com Area. The most important registers are accessible via 3 address pins only and by the use of an additional pin (A3) it is possible to access the complete range of the DSP/Host Com Area. The address mapping versus the multiplexed host interface is given in .

Table 11 Address Mapping of Multiplexed/Demultiplexed Host Interface

Address A0-3	Demultiplexed Mode Data D0-7	
	Host Write	Host Read

Address AD0-7	Multiplexed Mode Data AD0-7	
	Host Write	Host Read
FF_H - FE_H	reserved	reserved
FD_H - FC_H	reserved	reserved
77_H	Acknowledge $\overline{INT}$ MSB	
76_H	Acknowledge $\overline{INT}$ LSB	
75_H	Interrupt $\overline{INT}$ Mask MSB	Interrupt $\overline{INT}$ Status MSB
74_H	Interrupt $\overline{INT}$ Mask LSB	Interrupt $\overline{INT}$ Status LSB
73_H	Acknowledge $\overline{INTR}$	
71_H	Interrupt $\overline{INTR}$ Mask MSB	Interrupt $\overline{INTR}$ Status MSB
70_H	Interrupt $\overline{INTR}$ Mask LSB	Interrupt $\overline{INTR}$ Status LSB
$6C_H$	reserved	reserved
$6A_H$	reserved	reserved
61_H	Cntrl Host → DSP MSB	Cntrl DSP → Host MSB
60_H	Cntrl Host → DSP LSB	Cntrl DSP → Host LSB

Table 11 Address Mapping of Multiplexed/Demultiplexed Host Interface (cont'd)

Address A0-3	Demultiplexed Mode Data D0-7	
	Host Write	**Host Read**
$0F_H$	reseved	
$0E_H$	reseved	
09_H	Data register	Data register
08_H	Address register	Address register
07_H	Interrupt $\overline{INT}$ Mask MSB	Interrupt $\overline{INT}$ Status MSB
06_H	Cntrl Host $\rightarrow$ DSP MSB	Cntrl DSP $\rightarrow$ Host MSB
05_H	Cntrl Host $\rightarrow$ DSP LSB	Cntrl DSP $\rightarrow$ Host LSB
04_H	INDB (LSBit)	IND Interrupt Status
03_H	INH Interrupt Status	INHB (LSBit)
02_H	Mailbox IO write	Mailbox IO read
01_H	Mailbox write address	
00_H	Mailbox read address	

Address AD0-7	Multiplexed Mode Data AD0-7	
	Host Write	**Host Read**
58_H	INDB (LSBit)	IND Interrupt Status
50_H	INH Interrupt Status	INHB(LSBit)
$4C_H$	Mailbox IO write	Mailbox IO read
$4A_H$	Mailbox write address	
48_H	Mailbix read address	
47_H	Ext. Memory Data high	
46_H	Ext. Memory Data low	
45_H	Ext. Memory Addr high	
44_H	Ext. Memory Addr low	
41_H	Reg Data Host $\rightarrow$ DSP	Reg Data DSP$\rightarrow$ Host
40_H	Conf/Cont Reg Address	RDY(LSBit)

The shaded registers are mapped to the demultiplexed mode and can be accessed in demultiplexed mode by using address pins A(0-2), i.e. addressing 00_H to 07_H. Using A3 gives an additional way of accessing the DSP/Host Communication area by 2 registers only. The address register 08_H is written with the target address (from the multiplexed mode) and the data register 09_H contains the corresponding value or can be written with a new value for the target address.

The function of the registers 00_H to 07_H is the same as described in **Chapter 3.3.2.1**.

4 Functional Blocks

4.1 PLL and Baud Rate Generator

Clocking Modes

The clock generator including PLL generates the internal master clock derived from an input clock (or crystal) on pins XTAL(1:2).

Because of integrated decoupling capacitors, DC components of the input frequency on XTAL(1:2) are filtered out. Consequently, for a crystal input (nearly a sinusoid), an internal clock of nearly 50% duty cycle results.

The different clock modes available in the PSB 7280 are as follows:

CM1 = 0 PLL is activated by firmware after reset. The internal clock circuitry generates a frequency 4.5 times the input on XTAL(1,2). The internal frequency required is 34.56 MHz and is obtained by providing a frequency of 7.68 MHz on XTAL1 input.

CM1 = 1 PLL inactive. The internal frequency is directly input via XTAL(1,2). When using a crystal, a 34.56 MHz crystal swinging at its basic harmonic has to be connected to XTAL(1,2).

For the clock generation unit (oscillator and PLL) a separate supply voltage pin (V_{DDA} and V_{DDAP}) and a separate ground pin (V_{SSA} and V_{SSAP}) are provided.

The block diagram of the clock circuitry is shown in **Figure 16**.

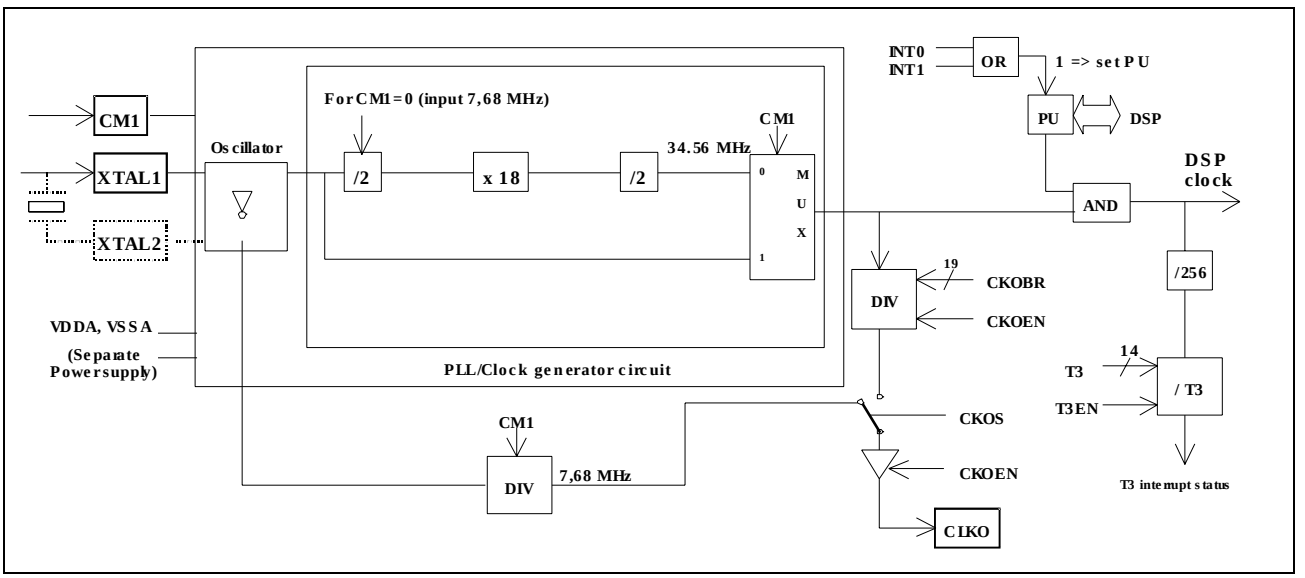


Figure 16

Note: When the PSB 7280 is reset via the RESET input, the following consecutive actions take place internally:

- *the PLL is initialized depending on the pin CM1*
- *if the PLL is chosen as a clock source, the PLL (frequency multiplier) goes through a transient state where the clock is not yet stable*
- *after the clock has become stable, the PSB 7280 (including the DSP) requires 42 clock cycles to be fully initialized.*
- *As a consequence, for a proper initialization the required total length of the RESET is 1 ms.*

Note: After a hardware reset, the JADE firmware needs to initialize its internal memories and interfaces. The time to do this is less than 10 ms. The user must take care to access the JADE only after this initialization phase is completed, i.e. 10 ms after the hardware reset.

Power-Down

The actual chip internal clock (“DSP clock”) is gated with the PU bit in the general configuration/control register. Thus, when PU is set to ‘0’ (either via the host or the DSP), clock distribution is stopped and the DSP is disabled. In this mode the power consumption is minimum (software power-down). Only an interrupt to the DSP (on INT0 or INT1) can restart the DSP clock.

The initial state of the PU bit is ‘1’.

The PU bit is used by the on-chip firmware for the firmware-controlled power-down (see **Chapter 6.1.3** for details).

IOM®-2 Clocks

The IOM-2 clocking is either provided by separate timing inputs DCL and FSC, independent of the other clocks, or may be generated by the JADE itself (CGEN bit in register $202B_H$). When generated by the JADE, only double rate clocking in TE mode (DCL = 1.536 MHz, FSC = 8 kHz) is supported.

When input, the DCL clock frequency is either equal to the data rate on DD/DU (if Clock Rate Select bit CRS = 1) or twice the bit rate (if CRS = 0, default value after reset). In the last case it is ensured that the internal IOM-2 bit clock has a phase such that output bits on DD/DU are correctly clocked out (see **Figure 17**).

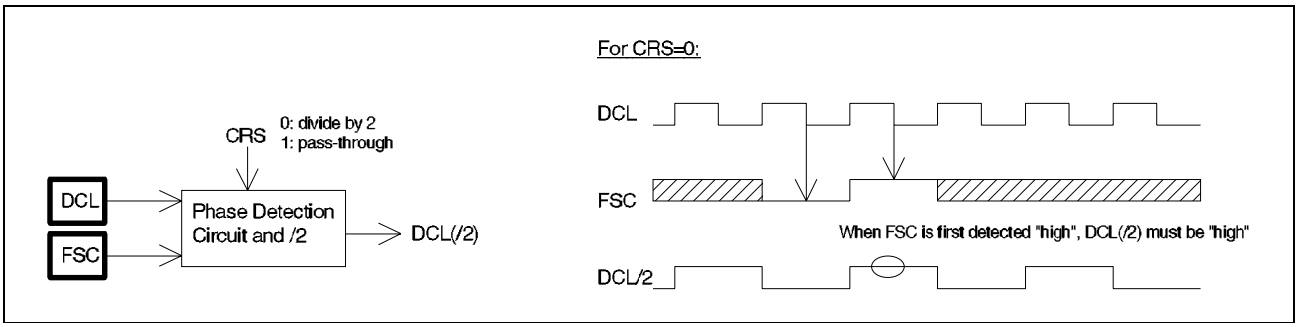


Figure 17

CLKO and Timers

After reset the auxiliary clock output CLKO outputs a frequency of 7.68 MHz, independent of the selection of CM1 bit. Alternatively, CLKO can be programmed (via CKOS bit in register 2002_H) to output a frequency obtained from the DSP clock via a programmable baud rate generator (baud rate factor 1, 2, 3, …, 2^{19}).

The wide range for the division factor for the CLKO output allows also for the possibility to use it as a time marker (period on the order of 10 ms to synchronize another device to the PSB 7280 time base).

When using the PLL (CM1 = 0), it is made sure that during reset phase CLKO delivers a continuous 7.68 MHz clock. When using the non-PLL mode (CM1 = 1) CLKO goes low while reset phase.

Timer T3 is derived from the **DSP clock** via a division by a programmable factor 1, …, 2^{14} with a prescaler of 256. This generates an interrupt status and a maskable interrupt on INT1, as an optional synchronous time base for the DSP software.

Two timers T1 and T2 are provided, **derived from the 8 kHz FSC** (usually a high-precision clock locked to the central clock of the synchronous network, e.g. ISDN) with division factors (1, 2, 3, …, 64) and (1, 2, 3, …, 128), cascaded - yielding a time base of hundreds of µs to around a second.

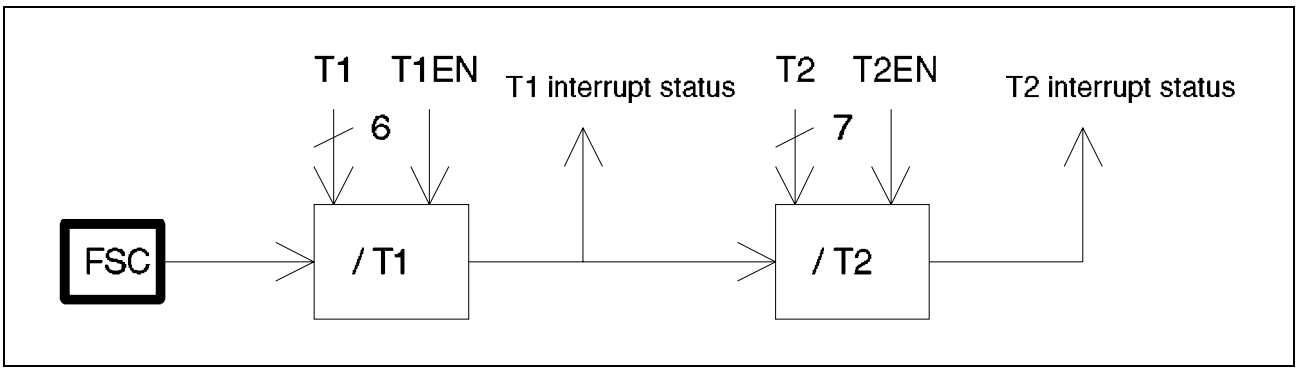


Figure 18

4.2 Audio and Data Reception/Transmission

The PSB 7280 supports a total of eight independent serial I/O-channels:

two receive and two transmit audio channels, and

two receive and two transmit data channels (pertaining to the two HDLC controllers).

The eight channels are transferred between the DSP and/or the parallel host interface and one of the serial interface lines: DD or DU (IOM-2), or SR or ST (Serial Audio Interface SAI). The capacity of each channel is individually determined by programming the time-slot length on the selected serial interface line.

Timing Generation

The selection of the line for each of the channels is performed via SLIN1,0 (00: DU; 01: DD; 10: SR; 11: ST). The timing logic is driven by the bit clock and frame synchronization signals corresponding to the selected line. These are:

DCL(/2) and FSC	for DD and DU.
SCLK and RFS	for SR.
SCLK and TFS	for ST.

The IOM-2 timing signals can be input or output of the PSB 7280, i.e. the circuit is a slave or master with respect to the IOM-2 interface. The selection is done by the CGEN bit in register $202B_H$.

The timing on the SAI lines SR and ST is either input or output. In the case where the timing is internally generated (i.e. the PSB 7280 functions as SAI master for SR and/or ST), a schematic diagram of the generation logic is shown in **Figure 19**.

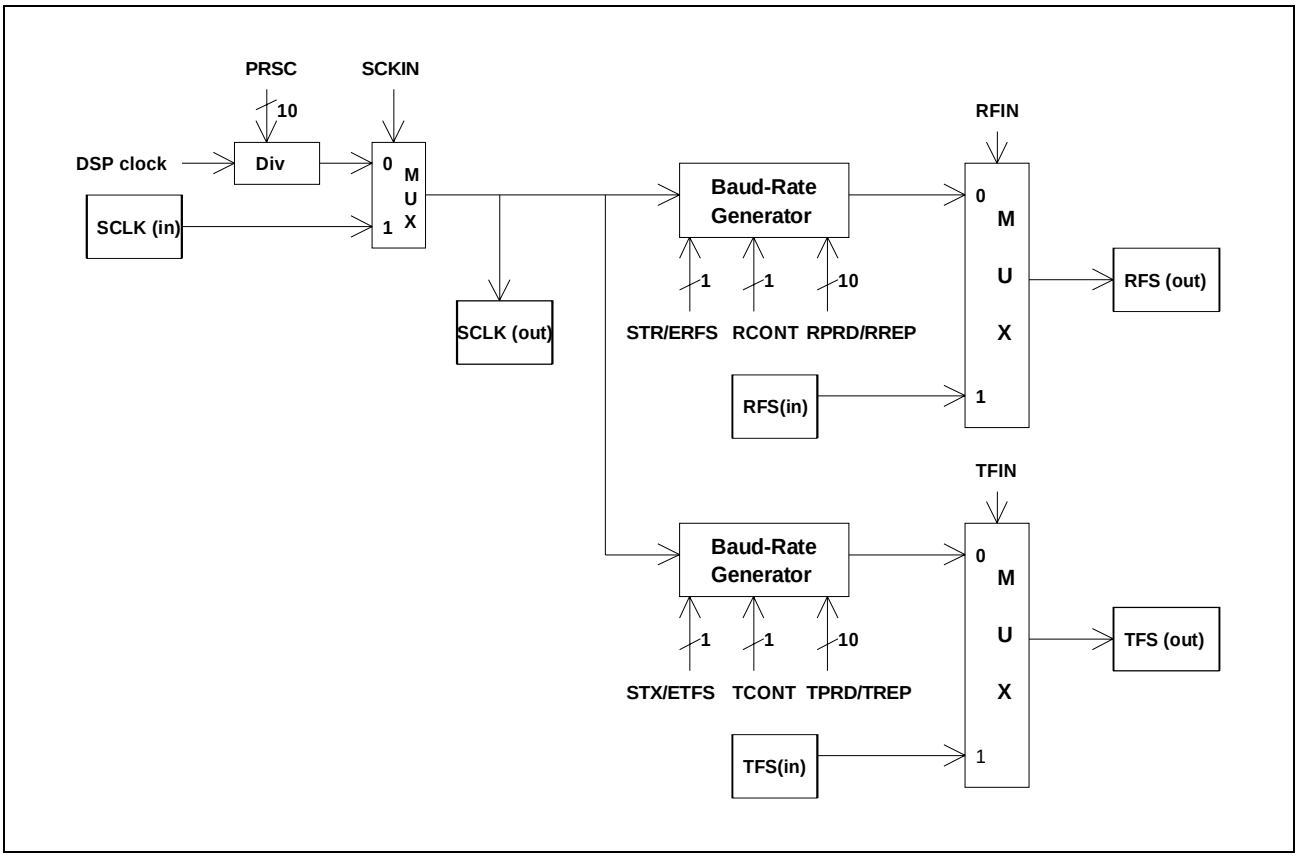


Figure 19 Timing Generation on SAI Lines - Frame Sync

For the frame sync signal RFS and/or TFS, two basic modes of operation are provided:

Case 1

If control bit RCONT = 1, pulses on RFS are continuously and periodically generated if ERFS (Enable RFS generation control bit in HDLC register bank) is set to ‘1’, of one bit period length and spaced (PRD + 1) $\times$ 16 bits apart, where PRD = 0, 1, …, 31.

Note: It suffices that the ERFS bits in one of the HDLC controller register banks is set to “1” in order for pulses to be generated.

Case 2

If RCONT = 0, a burst of REP + 1 pulses on RFS is generated, of one bit period duration and spaced 16 bit periods apart when a start command is issued by setting the STR bit to ‘1’. REP takes a value in the range 0 to 1.023.

Note: It suffices that the STR command in one of the HDLC controller register banks is issued in order for the generation of pulses start.

The same applies for TFS (control bits are ETFS and STX).

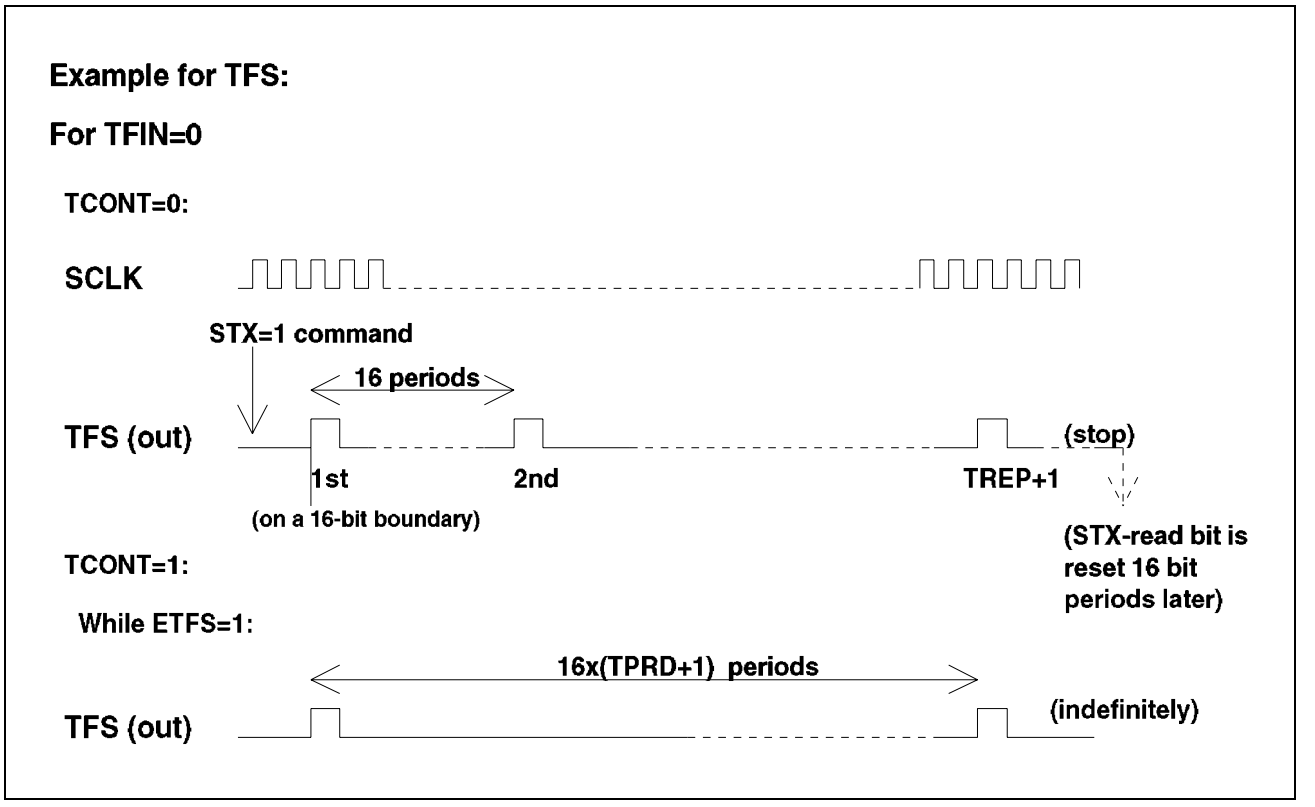


Figure 20 Timing Generation on SAI Lines - Continuous and Burst Mode

The uses of these modes are as follows:

Case 1

When the timing is input, or when it is internally generated with TCONT = 1, the interface can be used as a general time-division multiplex highway with time-slots of programmable lengths and locations for audio and data.

Case 2

When the timing is output with TCONT = 0, the interface is typically used to transfer messages or blocks of compressed or uncompressed audio or data, preceded by a header of control information pertaining to the transferred data block and synchronous to it. The blocks can be received and transmitted using one of the HDLC controllers in the transparent mode. An application of this mode of operation is the synchronous transfer of H.221/223 oriented data between the PSB 7280 and an attached VCP videocodec – see corresponding application note: “The PSB 7280 in Videophone Application with the VCP”).

Audio Channel Transfer

As mentioned in **Chapter 3**, all the serial channels (2 receive audio, 2 transmit audio, and two full-duplex HDLC/transparent data channels) can be transferred between one of the serial interfaces and the DSP or the host in a flexible manner.

The interface to each of the audio channels is a 32-bit wide shift register. In receive direction, when the shift register is filled to a programmable level (up to 32 bits), the whole 32-bit shift register is loaded into the receive channel read register set accessible from the DSP and from the host. Simultaneously, a maskable interrupt status is set. Similarly, in the transmit direction, transmit channel data is loaded from the write register pertaining to that channel (either from DSP or host register, as selected via a control bit) into the transmit shift register when a selectable number of bits have been shifted out.

The buffering of up to 32 bits reduces the reaction time of the DSP software.

As an alternative to this, the audio channel data can also be loaded from the shift register to the DSP/host registers (receive direction) and from the DSP/host registers into the shift register (transmit direction) at the occurrence of the frame sync pulse. In this case the number of significant bits in the registers is determined by the time-slot length programmed on the receive/transmit line. The DSP/host has 125 µs to read/write the register while new data is assembled or the contents of the shift register are transmitted, during the following frame. (This option could be used for DSP software synchronized on the 8-kHz time base).

The audio channel registers, each of length 2 words/4 bytes, are (see **Chapter 3**):

RC1	Receive channel 1.
RC2	Receive channel 2.
XC1	Transmit channel 1.
XC2	Transmit channel 2.

The relevant parameters for controlling the transfer of the audio channels are (independent for each channel):

EN	Enable channel.
LMOD	Load mode (either once per frame, or after LBIT bits have been received/transmitted).
LBIT	Load bits. Gives the number of bits (1 to 32) to be loaded, in multiples of the physical time-slot length.

The maskable interrupt status bits for controlling the transfer are:

BFUL Buffer full (RC1 or RC2).

BEMP Buffer empty (XC1 or XC2).

or optionally:

FSC Frame sync interrupt (FSC).

RFS Frame sync interrupt (RFS).

TFS Frame sync interrupt (TFS).

In addition, the control bits HXA1 and HXA2 control whether the corresponding transmit channel is loaded into the shift register from the XC1/2 register accessible from the DSP (HXA = 0) or from the host (HXA = 1).

The block diagrams for the receive and transmit audio channels are shown in **Figure 21** and **Figure 22**.

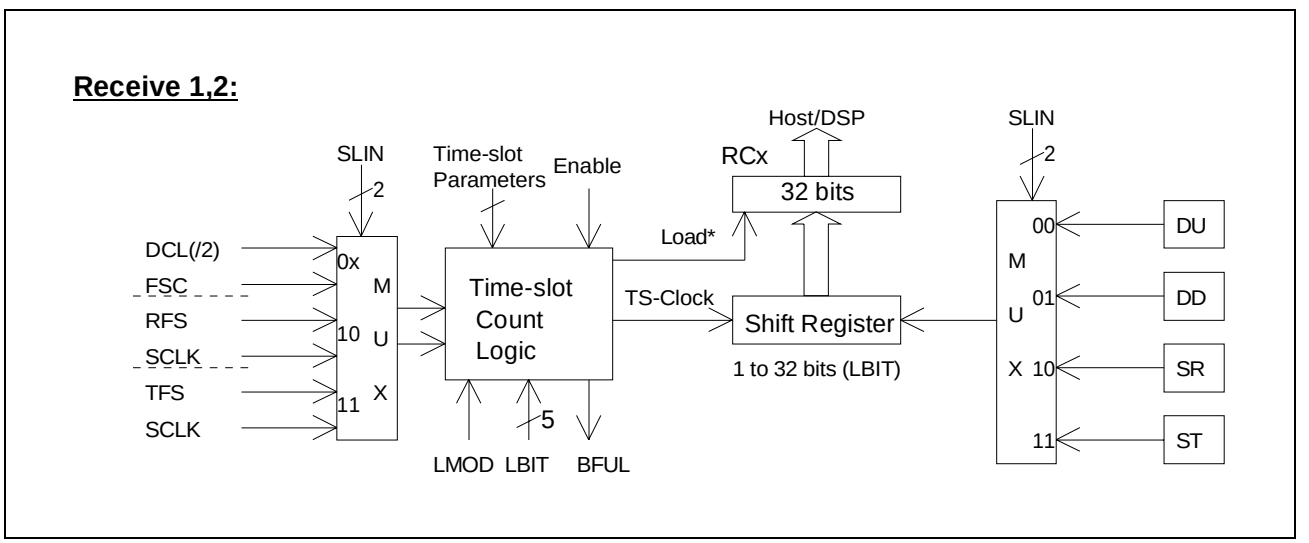


Figure 21

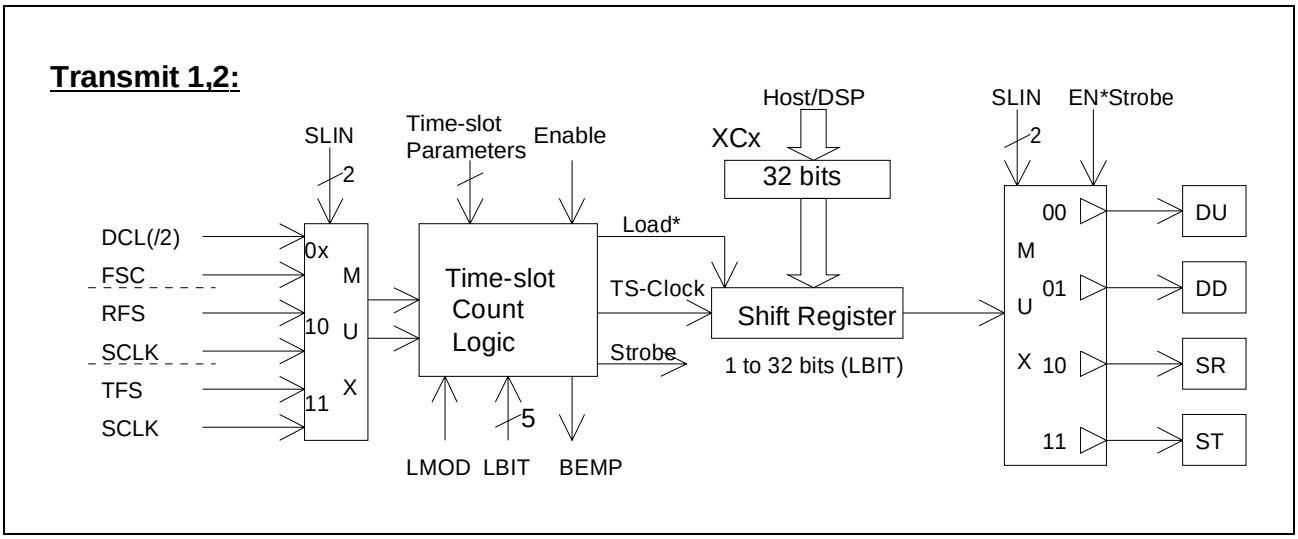


Figure 22

Caption to the Figures

In receive direction, the input data is loaded from the shift register into DSP accessible read registers and simultaneously into (physically separate) host accessible read registers.

In the transmit direction, data is loaded into the shift register from the transmit channel register accessible from the DSP (if HXA = 0) or the register accessible from the host (if HXA = 1). Two separate control bits HXA1 and HXA2 are provided for this purpose, for audio channel 1 and audio channel 2, respectively.

HDLC/Transparent Data Channel Transfer

The interface between the input of the HDLC/transparent data receiver and the DSP or host, and between the output of the transmitter and DSP or host is in each case a 32-bit long shift register.

Receiver in LMOD(1:0) = 01, 10, 11

In receive direction, when the shift register from the serial line is filled to a programmable level (1, 2 or 4), the whole 32-bit shift register is loaded into the HRR1/2 read registers, physically separate for DSP and host. In the same cycle the contents of the HRW1/2 write register accessible from the DSP (if HHR1/2 = 0) or host (HHR1/2 = 1) are loaded to the HDLC receiver input. In the next cycle the data from HRR1/2 is as a default loaded into HRW1/2 and a maskable interrupt status BFHR1/2 is generated to the DSP and host. The interrupt status is generated to both DSP and host, independent of the setting of HAH1/2. If the data in HRR1/2 is to be pre-processed, the HRW1/2 register can be overwritten by the DSP or host before the next 1, 2 or 4 bytes (programmable) have been shifted into the shift register.

After reset (RRES) when starting the receiver (RAC = 1), the reset status data of HRW and HRR is ignored by the receiver, i.e. the contents of HRW1/2 and HRR1/2 are not forwarded to the HDLC receiver, but only the data received from the line. The same applies to the interrupts: A BFHR1/2 interrupt is only generated after the first 1, 2 or 4 bytes of line data are available in the HRR1/2 register. Due to this pipeline, a latency occurs in the HDLC/transparent serial data reception, see section below.

The start of the reception can be in the same frame (w.r.t. the frame sync signal on the chosen line) as the setting of RAC = 1 since the time-slot count logic works independently of RAC.

In transparent mode (TMO = 1) the reception is only started at the beginning of the time-slot (time-slot aligned). If RAC is set to ‘1’ during the selected time-slot, the receiver waits for the beginning of the time-slot in the next frame.

Receiver in LMOD(1:0) = 00

The same applies for LMOD = 00, except the pre-processing is not available. The data from the bit-reversal unit is bypassed to the HDLC receiver. In addition, the loading of HRR1/2, HRW1/2 and the generation of the interrupt BFHR1/2 is done like in the other LMODs for observation of the data stream by the DSP or host only. Thus, the LMOD = 00 is identical with LMOD = 01, except pre-processing is not available and the receiver latency after reset is shortened, see section below.

Transmitter in LMOD(1:0) = 01, 10, 11

Similarly, in the transmit direction, after 1, 2 or 4 bytes (programmable) are shifted out of the shift register, the contents of the HXW1/2 write register accessible from DSP (if HHX1/2 = 0) or host (if HHX1/2 = 1) are loaded into the transmitter shift register. In the same cycle 1, 2 or 4 bytes are loaded from the HDLC transmitter output into the HXR1/2 read register, physically separate for DSP and host. In the next cycle the data from HXR1/2 is as a default loaded into HXW1/2 and a maskable interrupt status is generated to the DSP and host. The interrupt status is generated to both DSP and host, independent of the setting of HAH1/2. If the data in HXR1/2 is to be post-processed, the

HXW1/2 register can be overwritten by the DSP or host before the next 1, 2 or 4 bytes (programmable) have been shifted out of the shift register.

After reset (XRES), the reset status data of HXR1/2 and HXW1/2 is ignored by the transmitter, i.e. the contents of HXR1/2 and HXW1/2 are not transmitted to the line, but only the data from the HDLC transmitter. In the first cycle after the transmitter has been activated (XAC = 1), the data from the HDLC transmitter is immediately passed to the HXR1/2 register for post-processing. The line-transmission is not yet started! In the first cycle after the DSP or host (programmable via HHX1/2) has written the HXW1/2 register with the post-processed value, this value is passed through the bit-reversal unit into the shift register and the transmission is started as soon as the next beginning of the selected time-slot is detected.

The start of the transmission can be in the same frame (w.r.t. the frame sync signal on the chosen line) as the setting of XAC = 1 and/or the writing to the HXW1/2 register since the time-slot logic works independently of XAC.

In transparent mode (TMO = 1) the transmission is only started at the beginning of the time-slot (time-slot aligned). If the first write to HXW1/2 happens during the selected time-slot, the transmitter waits for the beginning of the time-slot in the next frame.

Transmitter in LMOD(1:0) = 00

The same applies for LMOD = 00, except the post-processing is not available. The data from the HDLC transmitter is after XAC = 1 directly passed through the bit-reversal unit into the shift register. In addition, the loading of HXR1/2, HXW1/2 and the generation of the interrupt is done like in the other LMODs for observation of the data stream by the DSP or host only. Thus, the LMOD=00 is identical with LMOD = 01, except post-processing is not available and the transmitter latency after reset is shortened, see section below. The transmission is in this case started by the setting of XAC = 1. No write to HXW1/2 is necessary.

The start of the transmission can be in the same frame (w.r.t. the frame sync signal on the chosen line) as the setting of XAC = 1 since the time-slot logic works independently of XAC.

In transparent mode (TMO = 1) the transmission is only started at the beginning of the time-slot (time-slot aligned). If XAC is set to ‘1’ during the selected time-slot, the transmitter waits for the beginning of the time-slot in the next frame.

The HDLC/transparent data channel registers, each of length 2 words/4bytes, are (see **Chapter 3**):

HRR1 HDLC Receive Read 1.

HRR2 HDLC Receive Read 2.

HRW1 HDLC Receive Write 1.

HRW2 HDLC Receive Write 2.

HXR1 HDLC Transmit Read 1.

HXR2 HDLC Transmit Read 2.

HXW1 HDLC Transmit Write 1.

HXW2 HDLC Transmit Write 2.

The relevant parameters for controlling the transfer of the HDLC/transparent data channels are:

LMOD(1:0) Load mode (access byte by byte without delay, or access in 1, 2 or 4 byte units with a corresponding serial data delay).

HHR Access to HDLC/transparent data receiver input from DSP (HHR = 0) or from host (HHR = 1).

HHX Access to HDLC/transparent data output shift register from DSP (HHX = 0) or from host (HHX = 1).

The access right to the receiver and transmitter input/output from the DSP or the host (determined by bits HHR1/2 and HHX1/2) is independent of who is allowed to service the HDLC controller (determined by bits HAH1/2).

The maskable interrupt status bits for controlling the transfer are:

BFHR Buffer full for HDLC receiver (new data can be read from HRR and written into HRW).

BFHX Buffer full for HDLC transmitter (new data can be read from HXR and written into HXW).

The block diagrams for the receive and transmit HDLC controller channels are shown in the **Figure 23** and **Figure 24**.

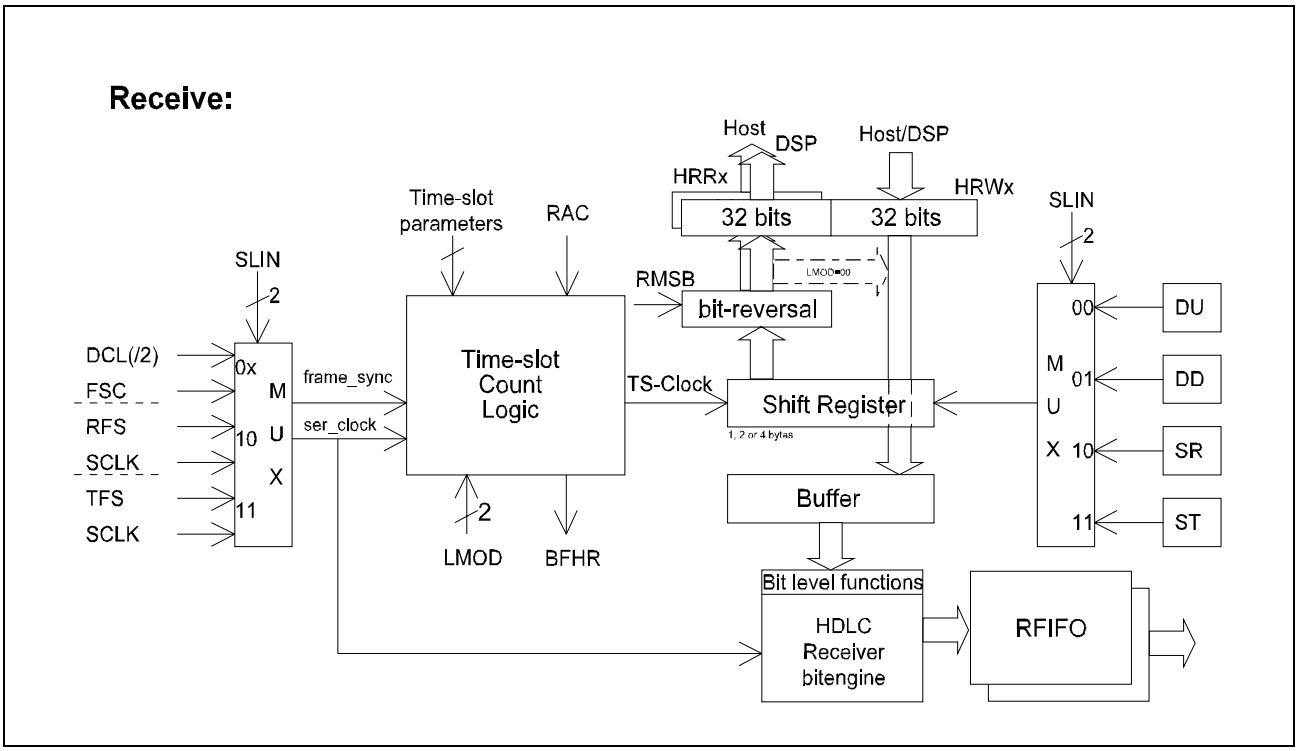


Figure 23

Caption to the Figure

The data from the shift register is loaded into DSP accessible receive read registers (HRR1/2) and simultaneously into (physically separate) host accessible receive read registers. Data to the HDLC receiver is loaded from the receive write register (HRW1/2) accessible from the DSP (if HHR = 0) or the register accessible from the host (if HHR = 1). Two separate control bits HHR1 and HHR2 are provided for this purpose, for HDLC channel 1 and channel 2, respectively.

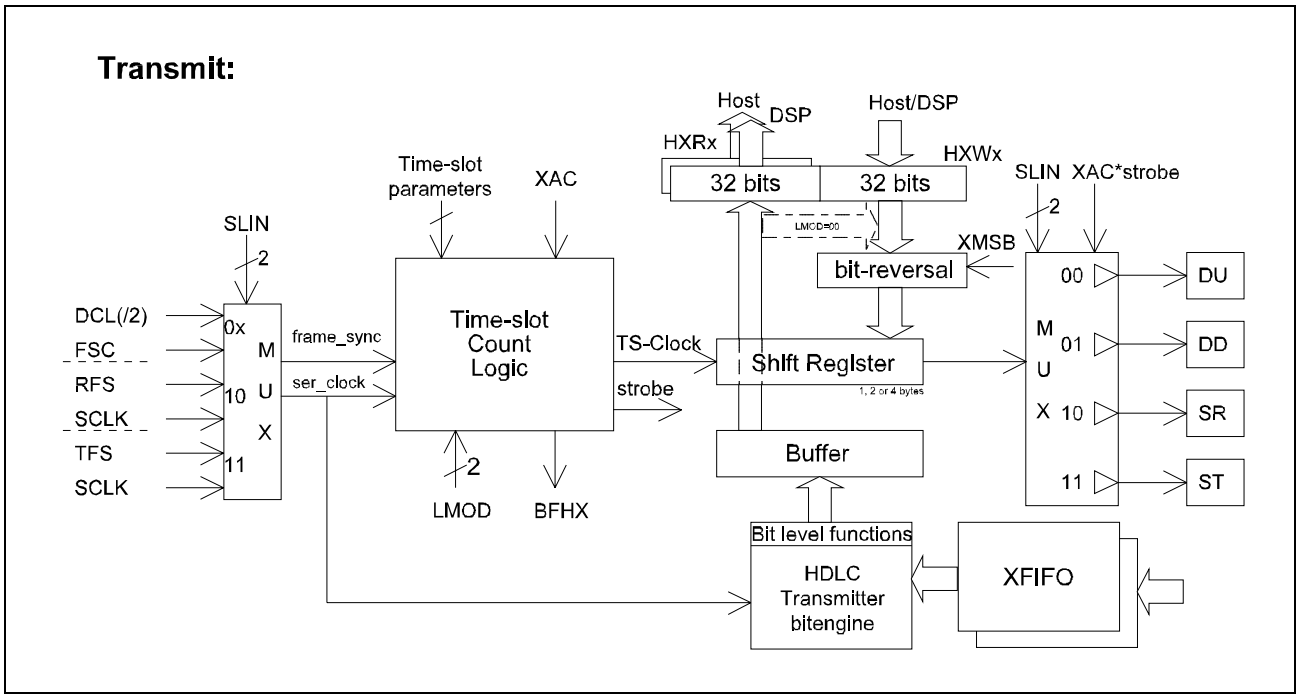


Figure 24

Caption to the Figure

The data from the HDLC transmitter is loaded into DSP accessible transmit read registers (HXR1/2) and simultaneously into (physically separate) host accessible read registers. Data is loaded into the shift register from the transmit write register (HXW1/2) accessible from the DSP (if HHX = 0) or the register accessible from the host (if HHX = 1). Two separate control bits HHX1 and HHX2 are provided for this purpose, for HDLC channel 1 and channel 2, respectively.

The access right to the receiver and transmitter write registers (HRW1/2, HXW1/2) from the DSP or the host (determined bits HHR1,2 and HHX1,2) is independent of who is allowed to service the HDLC controller (determined by bits HAH1,2).

Note on Time-Slots of HDLC/Transparent Data Communication Controllers

If a time-slot is still active (either in receive or transmit direction) when a new frame sync pulse is detected, the programmed length of the time-slot is not reduced but the time-slot remains active until its end. However, the time-slot count logic for the new frame starts immediately at the detection of the new frame sync pulse. A new time-slot can start immediately after the currently active time-slot has been closed, thus permitting a permanent reception or transmission (“time-slot length” = “distance between two consecutive frame sync's”).

The case where “time-slot length” > “distance between two consecutive frame sync's” should not occur.

Bit-Reversal Units

The bit-reversal units are working byte-based, i.e. when enabled via bits RMSB or XMSB for receiver and transmitter, respectively, each byte inside the 32 bit data path is reversed:

31	30	o	25	24	23	22	o	17	16	15	14	o	9	8	7	6	o	1	0
24	25	o	30	31	16	17	o	22	23	8	9	o	14	15	0	1	o	6	7

The bit-reversal unit is independent of the LMOD bits, but in case of LMOD = 00, 01, 10 not all bytes contain valid data.

When disabled (RMSB/XMSB=0), the bit-reversal units are transparent.

Note on Latency of HDLC/Transparent Serial Data

When an HDLC receiver is enabled (via bit RAC), the HDLC receiver is clocked with the serial interface clock even outside the selected time-slot. However, the logic at the input of the HDLC receiver is only clocked with the serial clock during the selected time-slot. Consequently, N bits are loaded into HRR register from the serial line after N clock edges inside the selected time-slot (N is equal to 8, 16 or 32 depending on LMOD). Similarly, data from HRW register is loaded into HDLC receiver only after a certain number of clock edges inside the selected time-slot have occurred. The HDLC bit-engine works on serial data, thus adding a delay of N clock cycles, but not necessarily inside the time-slot. The latency (delay) of received data from the input pin to the HDLC FIFO is given in the following as a function of LMOD (C_{TS} means the number of clock edges inside the active time-slot, C means the number of clock edges independent of the active time-slot):

Table 12 Receiver Delays

	Start & Stationary
LMOD = 00	8 C_{TS} + 9 C
LMOD = 01	16 C_{TS} + 9 C
LMOD = 10	32 C_{TS} + 17 C
LMOD = 11	64 C_{TS} + 33 C

Similarly, latencies apply in the case of the data from the output of the HDLC transmitter FIFOs to the serial output pin. Those are different for the first 1, 2 or 4 bytes (“start”) and the following bytes (“stationary”):

Table 13 Transmitter Delays

	Start	**Stationary**
LMOD = 00	10 C	10 C + 8 C_{TS}
LMOD = 01	11 C + Δt	10 C + 16 C_{TS}
LMOD = 10	19 C + Δt	18 C + 32 C_{TS}
LMOD = 11	35 C + Δt	34 C + 64 C_{TS}

Δt: Delay between BFHX1/2 interrupt status and write to HXW1/2 register by DSP or host (programmable via HHX1/2).

During reception/transmission the delay is dynamically increased by the number of zero insertions in the path between the line and the HDLC receiver/transmitter. Thus, the numbers in the table refer to the beginning and the end of the frame and any state inside a frame when no zero insertions are in the pipeline.

The receiver latencies have to be taken into account in systems where the serial clock is not continuous but is immediately disabled after the last serial data bit has been received.

The transmitter latencies have to be taken into account in systems where the transmitter shall start transmitting accurately in one special frame (w.r.t. the line frame sync signal), e.g. when the transmission has to be started in the first time-slot of a frame-sync burst.

4.3 HDLC Controller

The two internal HDLC controllers of the PSB 7280 can be independently serviced

– either via the Parallel Host Interface
– or by the DSP (SPCF).

Important Notes

1. From the point of view of the end user/system manufacturer, only the servicing of the HDLC controllers via the host is of relevance, since the servicing via the DSP is done by on-chip firmware invisible to the end user.
2. If the packet oriented protocol on the Serial Audio Interface used in videophone applications with the VCP (from 8×8, Inc.) videocodec is needed, the HDLC1 controller is serviced by the on-chip firmware, in other words, it cannot be accessed by the host: only HDLC2 controller will then be available to the user.

The servicing of the HDLC controller(s) via the host and via the embedded DSP are exclusive of each other. The access to the register banks of the two HDLC controllers is determined by the “HDLC Controller Access from Host” bits HAH1 (for HDLC1) and HAH2 (for HDLC2):

– When HAHx is ‘0’, the SPCF is allowed to access the HDLC register bank, and the host interface bus is disconnected from the HDLC controller;
– When HAHx is ‘1’, the host is allowed to access the HDLC register bank, and the SPCF data bus is disconnected from the HDLC controller.

The address spaces of the two HDLC controllers for the host interface bus and for the SPCF data bus is shown in **Figure 25** (see also **Chapter 5**):

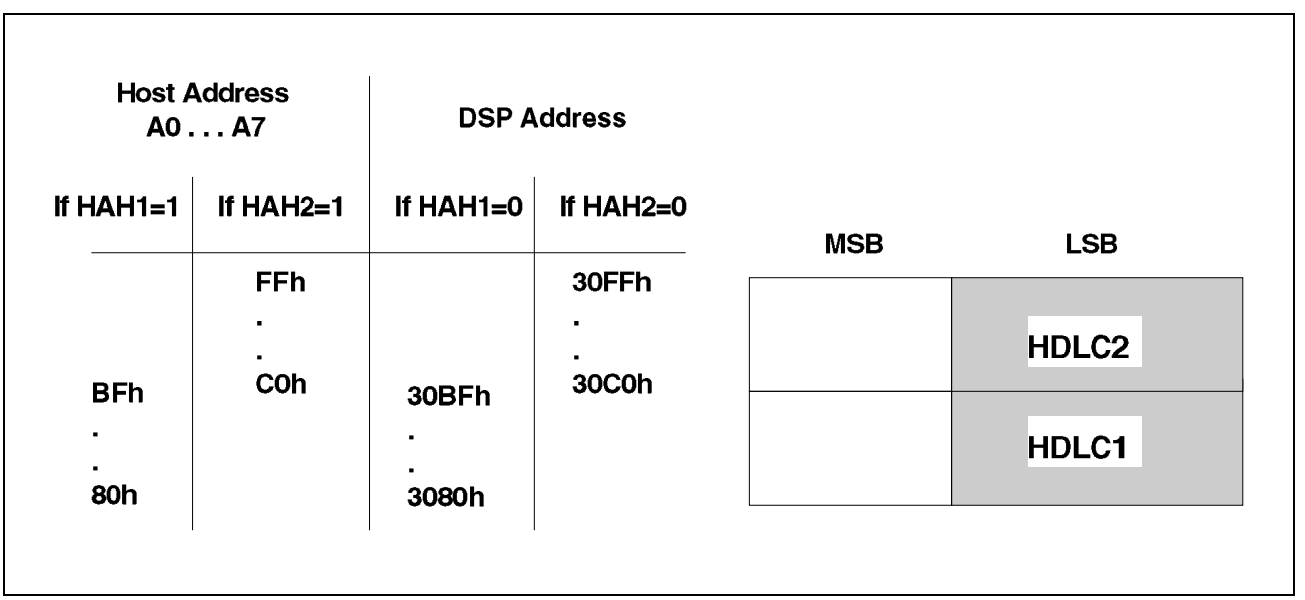


Figure 25

In the rest of this paragraph, for the sake of simplicity, a reference to “Host” (or “Host software”) implies HDLC driver software running on a host (e.g. provided by the user) or on the DSP (e.g. firmware).

HDLC Applications

The integrated HDLC controller opens the way for numerous applications that may be realized with the PSB 7280 in a very cost-effective manner. Some of the more obvious are:

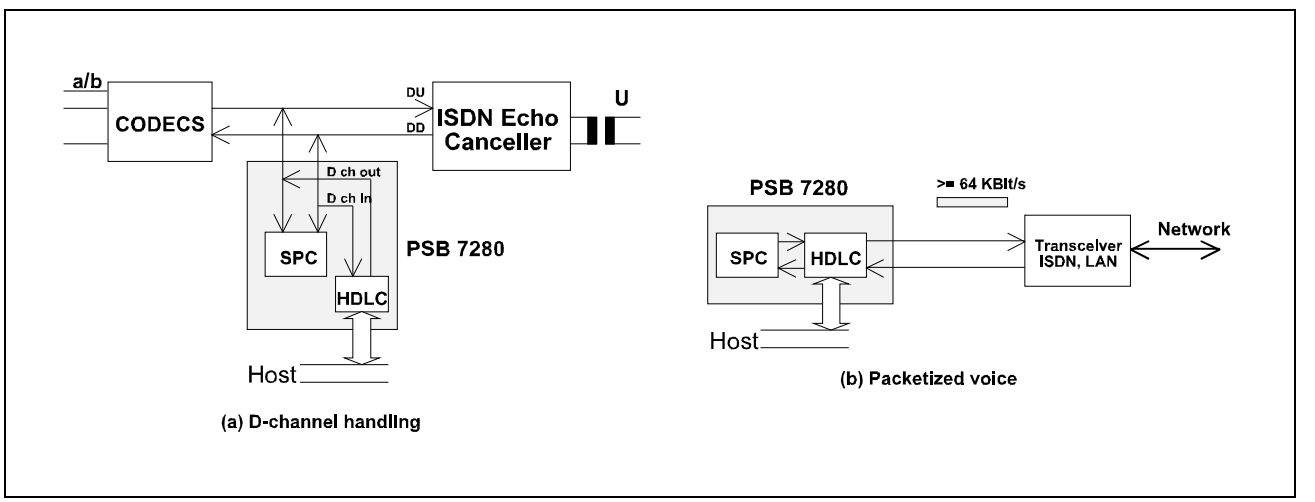


Figure 26

For non-HDLC serial protocols, the transparent mode of the HDLC controllers can be used.

a) D-channel handling in point-to-point configurations, e.g. on Digital Circuit Multiplication Equipment.
b) Packetized voice e.g. with G.728.

Functions of the HDLC Controllers

The HDLC controllers perform the following functions:

In HDLC Mode

Bit level functions:

– flag generation/detection
– zero bit insertion/deletion after 5 ones
– CRC generation/check
– abort generation
– inter-frame time fill generation.

Programmable features for HDLC transmission:

– Idle (‘1’) or flag (‘0111111’) as inter-frame time fill
– CRC generated yes/no (if no, the frame is closed with a closing flag only).
– CRC according to CCITT polynomial of order 16 or 32:
  CRC-16: $x^{16} + x^{12} + x^5 + 1$
  (checksum: $1D0F_H$)
  CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
  (checksum: $C704DD7B_H$)

Programmable features for HDLC reception:

– CRC written in receive FIFO yes/no
– CRC according to CCITT polynomial of order 16 or 32 (common with transmitter).

Reception of back-to-back frames and consecutive frames with a shared flag, as well as flags with shared ‘0’s is possible.

HDLC Frame Format

The HDLC transmitter starts an HDLC frame with a flag. It continues with the data from the XFIFO (including the address). The end of a frame is indicated by a closing flag preceded by the 16/32-bit CRC checksum or by an abort sequence. When no frame is being transmitted inter-frame time-fill ‘1’ or “flags” is transmitted during the programmed time-slot. Outside the selected time-slot, the output line is in “high impedance” state.

The HDLC receiver hunts for flags which are not followed by another flag or an abort sequence. It stores the information - including the address field - in the RFIFO until the end of the frame is detected. The status of the received frame (CRC status, end of frame condition etc.) is reported via a status byte which is stored in the RFIFO immediately following the last byte of the frame, and, simultaneously, in a register.

In Transparent Mode

In this mode, data is received and transmitted fully transparently without HDLC framing. The received data is stored in the receive FIFO so that byte alignment in the FIFO corresponds to byte alignment in the serial time-slot (if the length of the time-slot is a multiple of 8 bits). Similarly, in transmit direction the byte alignment in the FIFO corresponds to the time-slot boundaries in the transmit time-slot, if its length is a multiple of 8 bits. When the transmit FIFO is empty, idle (‘1’) is transmitted during the active time-slot. Outside the selected time-slot, the output line is in “high impedance” state.

Details on the Operation of the HDLC Receiver

The HDLC receive FIFO size is 2×32 bytes. One half of the FIFO is connected to the receiver shift register while the second half is accessible from the controlling software.

The status bits pertaining to the HDLC receiver are:

Table 14

RPF	Receive Pool Full 32 bytes of a frame have arrived in the receive FIFO. The frame has not yet been completely received.	
RME	Receive Message End One complete frame of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte. No RPF is generated in this case. The number of bytes stored is given by RBC bits 0 - 4.	
RFO	Receive Frame Overflow Indicates that a frame has been lost because the FIFO was full at the reception of the beginning of a frame.	
RBC	Receive Byte Count register (RBCH, RBCL) 16 bits wide. Total number of bytes in received frame, including the status byte.	
RSTA	Receive Status Register Contains the following information:	
	VFR	Valid Frame Indicates whether the frame length is a multiple of 8 bit.
	RDO	Receive Data Overflow At least one byte of the frame has been lost because it could not be stored in the FIFO.
	CRC	CRC check Correct (1) or incorrect (0).
	RAB	Receive Message Aborted By the remote station (7 consecutive ‘1’s received), yes (1) or no (0).

The HDLC receiver is controlled by the following bits:

RAC Receiver Active
Sets the receiver in an active state, where the receiver hunts for an opening flag.
In transparent mode, when RAC is set to ‘1’, storage of bytes in the receive FIFO starts time-slot aligned (if the receive time-slot length is a multiple of 8 bits).

RMC Receive Message Complete
Acknowledges a previous RPF or RME status. Frees the FIFO pool for the next received frame or part of a frame.

RMD Receive Message Delete
Reaction to an RPF interrupt. The remaining part of the current frame is to be ignored by the receiver (which goes into the “hunt” mode, starting in the DSP/host-inaccessible part of the RFIFO); the receive FIFO is cleared of that frame.

RRES Receiver Reset
Resets the HDLC receiver, which goes into an idle state (RAC cleared), clears the receive FIFO and aborts any HDLC frame being received.

In the case of a frame of length less than 64 bytes, the whole frame may be stored in the receive FIFO. After the first 32 bytes have been received, the HDLC controller prompts via RPF the controlling software to read data from the FIFO. When the data has been read, the FIFO is released by issuing the RMC command, after which the rest of the frame, when ready, is made available (see **Figure 27**).

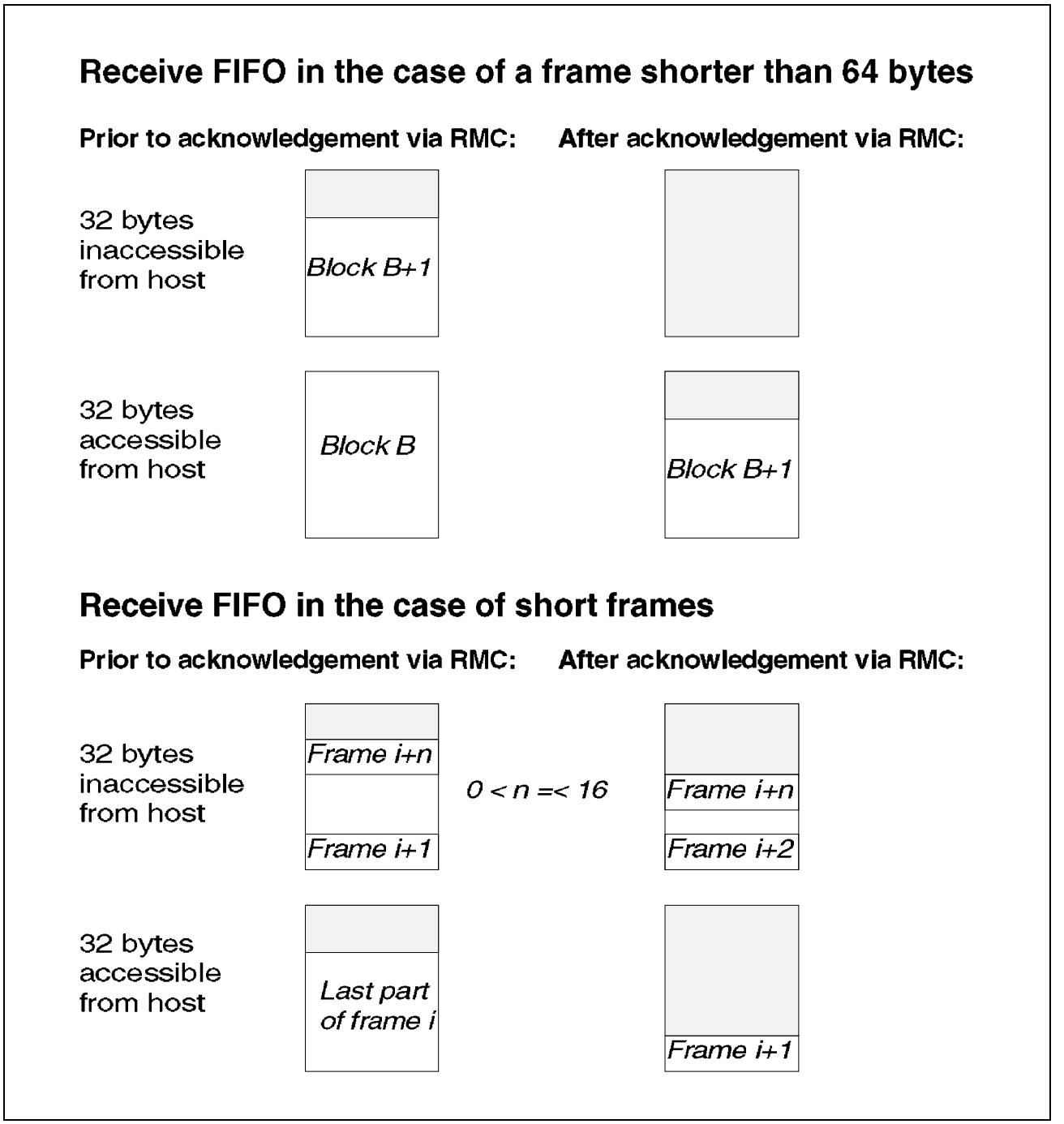


Figure 27

When a frame is not longer than 32 bytes, the whole frame is received in one block. The reception of the frame is reported via the RME interrupt status. This interrupt status is also generated when the final part of a frame longer than 32 bytes has been written in the FIFO.

The Receive Status Register (RSTA) contains the status pertaining to the current frame (Data Overflow yes/no, CRC Check, Abort yes/no). This status byte is also appended in the receive FIFO after the last data byte of the corresponding frame. The number of valid

bytes (including the status byte) stored in the receive FIFO can be read out from the receive byte count register. The receive frame status and receive byte count information is valid after the occurrence of the RME interrupt status, and remains valid until the software issues an acknowledgement via RMC.

In the case of frames at least 64 bytes long, the controlling software will repeatedly be prompted by RPF to read out the FIFO in blocks of 32 bytes (except the final block). After reading each data block, it is acknowledged RMC, which releases the FIFO. The availability of the remainder block of length 0 to 31 bytes (excluding the status byte) is reported via RME instead of RPF.

In the case of several consecutive short frames, the number of frames that can be stored is only limited by the FIFO size. After an RME interrupt status, one frame is available in the FIFO for reading. Through the RMC command the next frame is copied in the accessible half and the corresponding space is freed in the upper (inaccessible) half.

Bits 0 - 4 of the RBC register represent the number of bytes stored in the RFIFO. Bits 5 - 15 indicate the total number of 32-byte blocks which were stored before the reception of the remainder block.

If a frame cannot be stored due to a full FIFO, the RFO interrupt status is generated.

The RMD command is used to disable the reception of the rest of a frame after the controlling software has checked that the frame is to be discarded (e.g. because of a wrong address, or because of inability to process it).

Note: Only minimum length check (16 bits between flags) is performed on the receive frame.

Details on the Operation of the HDLC Transmitter

The transmit FIFO size is 2×32-bytes. One half is connected with the transmit shift register while the other half is accessible via the controlling software.

The interrupt status bits pertaining to the HDLC transmitter are:

XPR Transmit Pool Ready
One data block may be entered into the transmit FIFO.

XDU Transmit Data Underrun
Transmitted frame was terminated with an abort sequence because no data was available in the transmit FIFO and yet no XME command has been issued.

ALLS All Sent
When ‘1’, indicates that the last bit of a frame has been transmitted on the line and that both parts of XFIFO are empty (in either HDLC or transparent mode).

The following status bits are provided:

XDOV Transmit Data Overflow
Indicates that more than 32 bytes have been written into the transmit FIFO.

The HDLC transmitter is controlled by the following bits:

XF Transmit Frame
Initiates transmission of an entire frame, or part of one (up to 32 bytes).

XME Transmit Message End
Indicates that after the transmission of data from the FIFO pool, the frame is to be closed with a closing flag (and possibly a CRC checksum).

XRES Transmitter Reset
Resets the HDLC transmitter, clears the transmit FIFO, aborts any HDLC frame being transmitted and generates an XPR status after the command has been completed.

XNEW Transmitter Restart
Resets the transmitter state machine without any loss of data (i.e. FIFO data). The transmission of the current frame can be restarted with the first bit of the start flag.

After up to 32 bytes have been written to the FIFO, transmission is started by issuing the XF command. The opening flag (in the case of HDLC) is generated automatically. The HDLC controller requests another data block by an XPR interrupt status if there are no more than 32 bytes in the FIFO and the frame close command bit XME has not been set. To this the software responds by writing another pool of data and issuing a transmit command XF for that data. If transmission of earlier data (or of a previous frame) is still underway when a new transmission command XF is issued, software access to the FIFO is blocked until the first transmission is completed (see **Figure 28**).

For closing a frame in HDLC mode the DSP/host has two possibilities:

1. When XME and XF bits are set in the same command, all remaining bytes in the FIFO are transmitted, the CRC field (programmable) and the closing flag of the HDLC frame are appended and after all data has been transmitted to the line the HDLC controller generates a new XPR interrupt. Thus, a delay is caused between the transmission of two frames which is filled with interframe timefill values (programmable flags or ‘1’s).
2. To avoid the gap between two frames and time-optimize the transmission, the XF command can be set first for the last FIFO of the frame. After the corresponding XPR interrupt has been detected, the DSP/host may set XME = 1 and then start writing the next frame for the XFIFO (max. 32 bytes) which is again transmitted by an XF command. The HDLC transmitter will automatically insert the CRC field (programmable), the closing flag for the first frame and the start flag for the second frame.

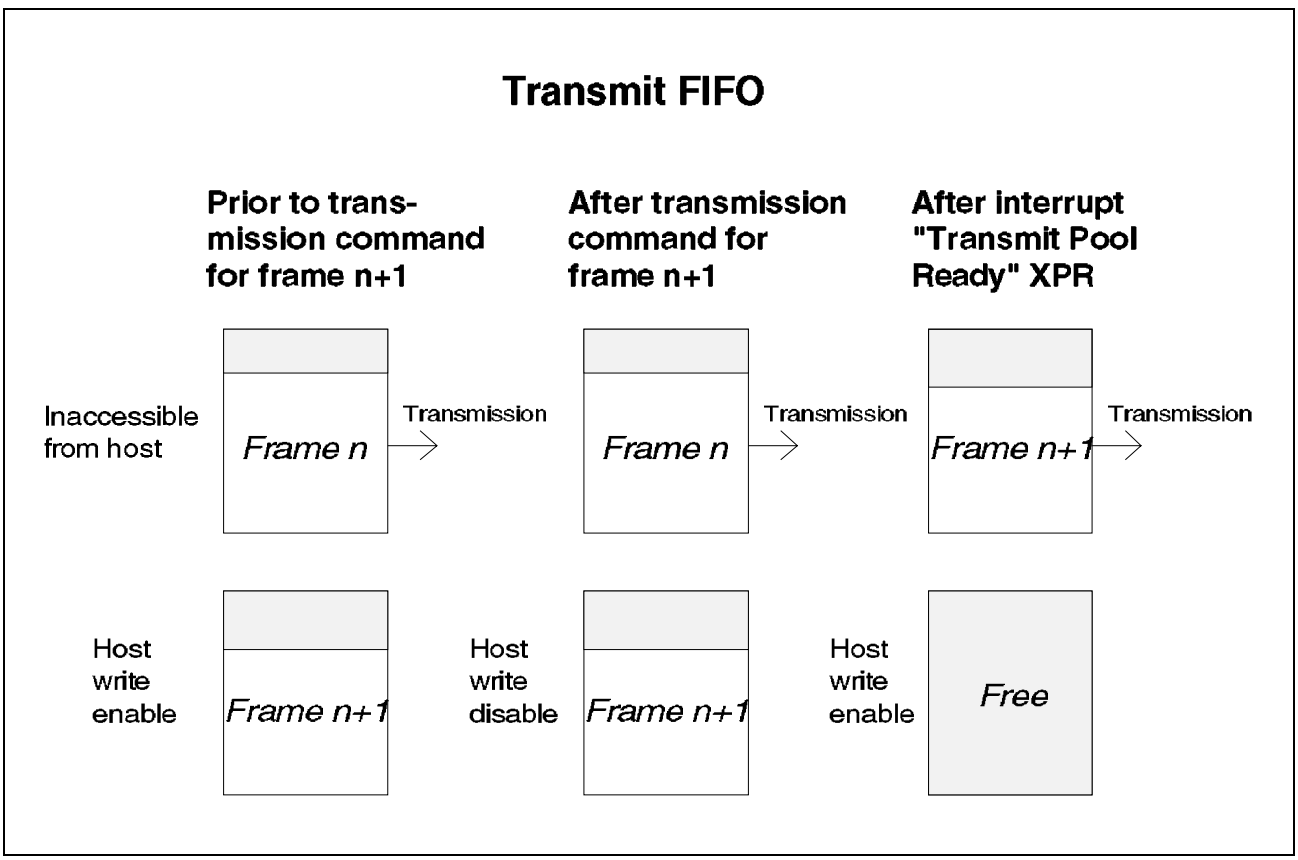


Figure 28

The host does not necessarily have to transfer a frame in blocks of 32 bytes. As a matter of fact, the sub-blocks issued by the host and separated by an XF command, can be between 0 and 32 bytes long.

If the transmit FIFO runs out of data and the XME command bit has not been set, the frame is terminated with an abort sequence (seven ‘1’s) followed by inter-frame time fill, and the host will be advised by a Transmit Data Unterrun (XDU) interrupt status.

4.4 IOM®-2 Functions

The IOM-2 functions supported by the PSB 7280 are:

– layer-1 functions in terms of the frame structure supporting any number n of 4-byte multiplexes (n = 1, …, 16), the number is implicitly determined by the DCL clock (see **Chapter 2**)
– one monitor channel of programmable location
– two C/I channels.

See **Figure 29**.

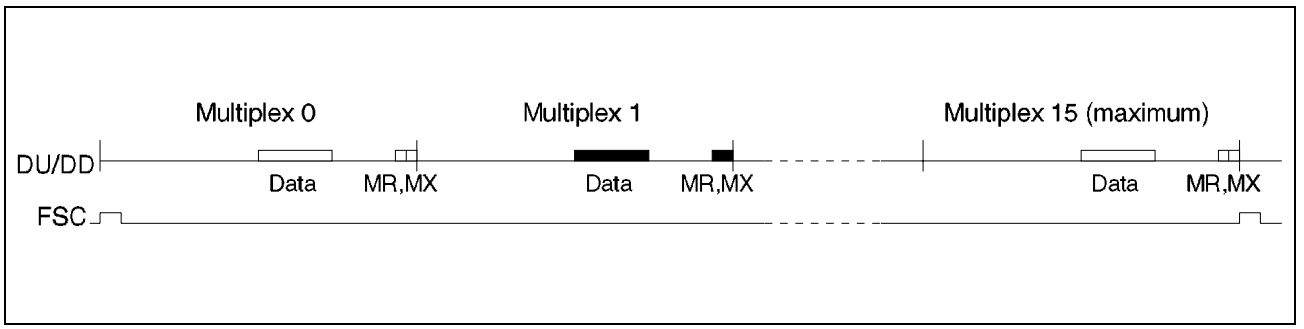


Figure 29 Monitor Channel

Parameters

SLIN = 0: Monitor transmit data on DU, receive data on DD

SLIN = 1: Monitor transmit data on DD, receive data on DU

CH(0:3): Monitor channel in 3rd byte of multiplex 0, …, 15 (common to receive and transmit channel) (CH(0:3) = 0001 in the example)

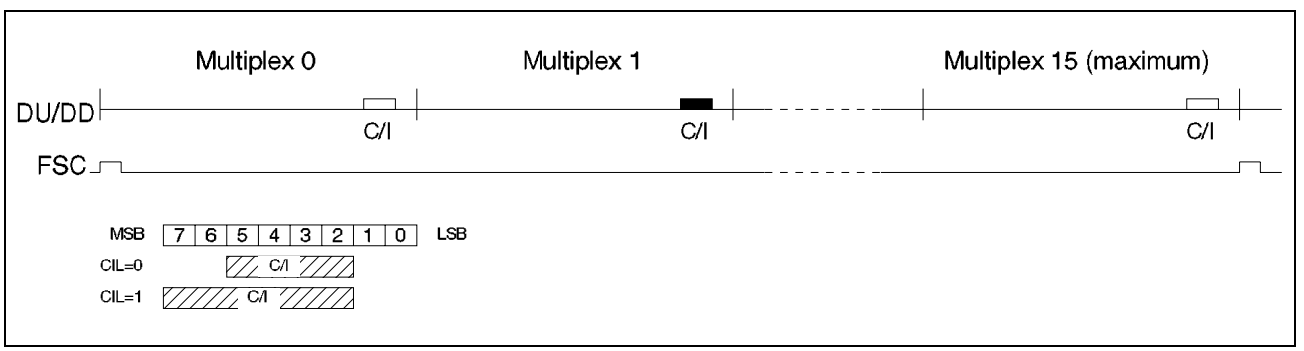


Figure 30 C/I Channels (2 Independent Channels)

Parameters

SLIN = 0:	C/I channel transmit data on DU, receive data on DD
SLIN = 1:	C/I channel transmit data on DD, receive data on DU
CH(0:3)	C/I channel in 4th byte of multiplex 0, …, 15, common for receive and transmit channel (CH(0:3) = 0001 in the example)
CIL:	C/I channel length is 4 bits (0) or 6 bits (1)
DLL:	Double last look yes (1) or no (0)

4.4.1 Monitor Channel Protocol

Use of Monitor Channel

In the case where a *local host* is present, the Monitor channel may be used e.g. for data exchange between the local host and another controller attached to the IOM-2 bus. For this the basic monitor channel protocol as explained in this section is sufficient.

*Note: The monitor channel protocol is not implemented **on-chip** on the PSB 7280. The monitor channel protocol has to be implemented via the host: this allows the implementation of data exchange with a remotely located controller.*

General Description of Monitor Channel Protocol

The monitor channel consists of 8 bits for the monitor data channel (MON) and 2 bits for the flow control (MX and MR). The transmitter controls the monitor data channel and the MX bit on one line while evaluating the condition of the MR bit on the other line. The receiver evaluates the MX bit of one line and latches its monitor data value. It controls the MR bit of the other line. The monitor channel protocol is shown in **Figure 31**.

The hardware performs reception and transmission of monitor channel messages (packets) byte-by-byte under software control.

The received and transmitted monitor channel bytes are stored in the Monitor data transmit (MONX) register and Monitor data Receive (MONR) register, respectively.

The software controls the monitor channel via two control bits in the monitor channel control register:

MRE	Monitor channel Receiver Enable.
MRC	MR bit Control.
MXC	Monitor channel Transmitter Control.

The monitor channel status is reported to the software via four bits in the monitor channel status register:

MDR	Monitor channel Data Received.
MER	Monitor channel End of Reception.
MDA	Monitor channel Data Acknowledged.
MEA	Monitor End of Acknowledgement.
MAB	Monitor channel Abort.

Inactivity

The transmitter indicates its inactivity with the idle state of the MX bit (1) and by transmitting the value FF_H (or high impedance) in the monitor data channel. The receiver responds to this inactivity via the idle (1) condition of the MR output bit.

Monitor Packet Transfer

The message transfer starts when the transmitter transmits the value of the first byte of the monitor data channel and sets the MX bit to its active state (0). The MX bit remains active until the receiver acknowledges the data or the transmitter software aborts the transmission. The receiver recognizes the change of the MX bit to the active state and latches the contents of the monitor data channel. Since the monitor channel address is always transmitted as the first byte of a message, all receiving devices compare (per hardware or software) the first value with their own address. If a device recognizes its address it acknowledges the data by changing its MR bit to the active state (0).

The transmitter recognizes this change and can now transmit the next byte of the message. This is done by transmitting the value in the monitor data channel and setting the MX bit to the inactive, idle (1) state for one frame and then changing it back to the active (0) state. The receiver recognizes the transition of MX from the inactive to the active state and latches the contents of the monitor data channel.

The receiver acknowledges the data transfer by setting the MR bit to the inactive (1) state for one frame and then back to the active (0) state. This procedure is repeated until all the data is transferred. Once the receiver has acknowledged the last value the transmitter switches its MX bit and the monitor channel into the idle (1) state. The receiver recognizes this idle state after it has received two consecutive frames with an idle MX bit and will then set its own MR bit in the idle (1) state.

The transmitter recognizes the change of the MR bit and indicates the idle condition after the second frame. If the receiver wants to abort a transmission, then it will set its MR bit into an idle (1) condition. The transmitter recognizes the abort condition after the second frame with an idle MR bit and switches its MX bit and the monitor data channel to idle.

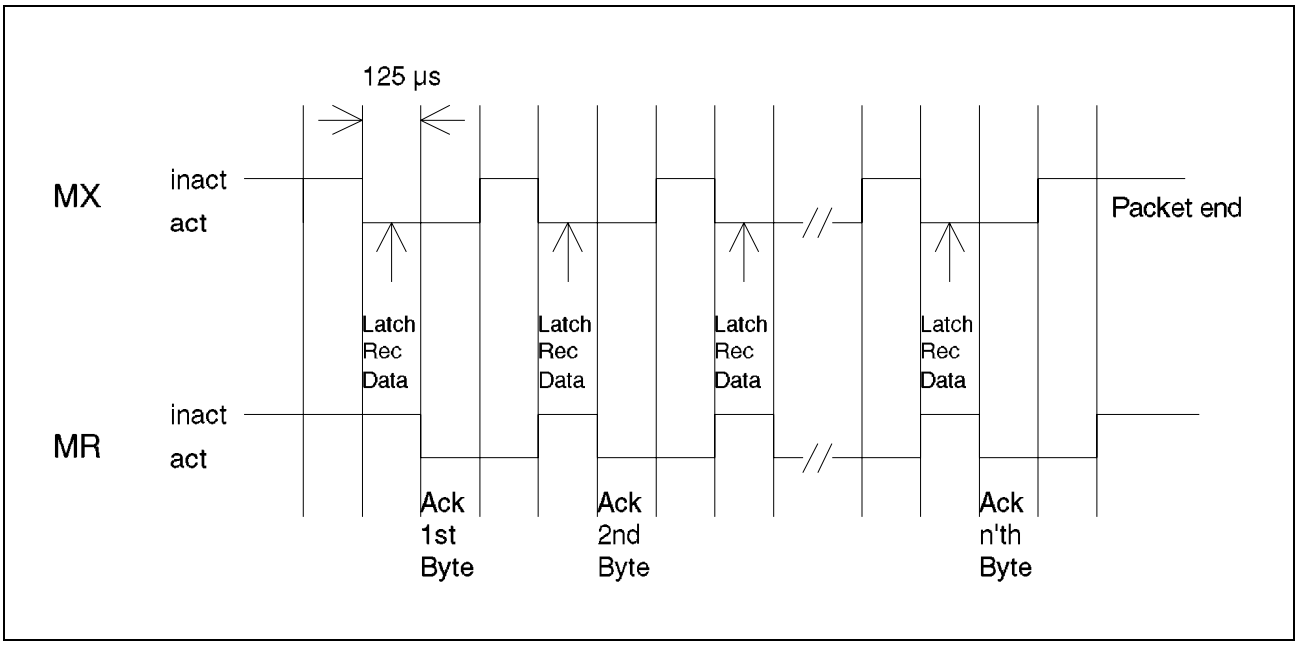


Figure 31

Note: For simplification of the diagram the states of MX and MR are shown as '0' or '1' during the entire 125-µs frame without regard to the bit positions they actually occupy.

Software Handling of Monitor Channel Transmission

The idle state of the transmitter is maintained when the MXC (Monitor channel Transmit Control) bit is 0. In order to transmit the first byte, its value is written into the MONX (Monitor channel Transmit) register. After the MXC bit is set to 1, the monitor channel hardware sends the byte from MONX and controls the MX bit accordingly (MX:1→0). When the hardware detects the acknowledgment from the other end (received MR bit = 0), it will set the MDA (Monitor Data Acknowledged) bit. When this is detected by the software, it writes the next byte in MONX register. This byte is sent and the MX bit controlled accordingly. The acknowledgment by the other end is again indicated by the MDA status bit. This procedure is repeated until all the data is transmitted. After the last MDA status the software sets the MXC bit back to 0 and the transmit channel including the MX bit returns to the idle state.

If an abort request from the receiving end is detected by the hardware, the MAB (Monitor channel Abort) status bit is set.

In the PSB 7280 the Monitor channel transmitter implements the so-called **maximum speed** option of this protocol, whereby the acknowledgment of every byte (except the first) by the receiving end is anticipated. This means that an MDA interrupt status is generated as soon as the received MR bit is detected to go from 0 to 1. Transmission of the next byte is started as soon as the software has reacted to this interrupt. Thus a maximum transfer speed of 32 kbit/s can be obtained.

Each data byte is transmitted at least twice (only twice if the receiver is fast enough so that the transmitter works at maximum speed), namely once when MX is 1, and once when MX is 0 in the next frame. The only exception is the first byte, which is transmitted in three consecutive frames (where MX = 1, 0, 0, respectively).

In order for the transmitter to recognize that the receiver has correctly acknowledged the last byte, the interrupt status MEA is set after the received MR bit is received at 1 in two consecutive frames (interrupt status different from MAB). The condition for generating an MEA interrupt status is the **recognition of a MR = 0, 1, 1 sequence when MXC = 0**.

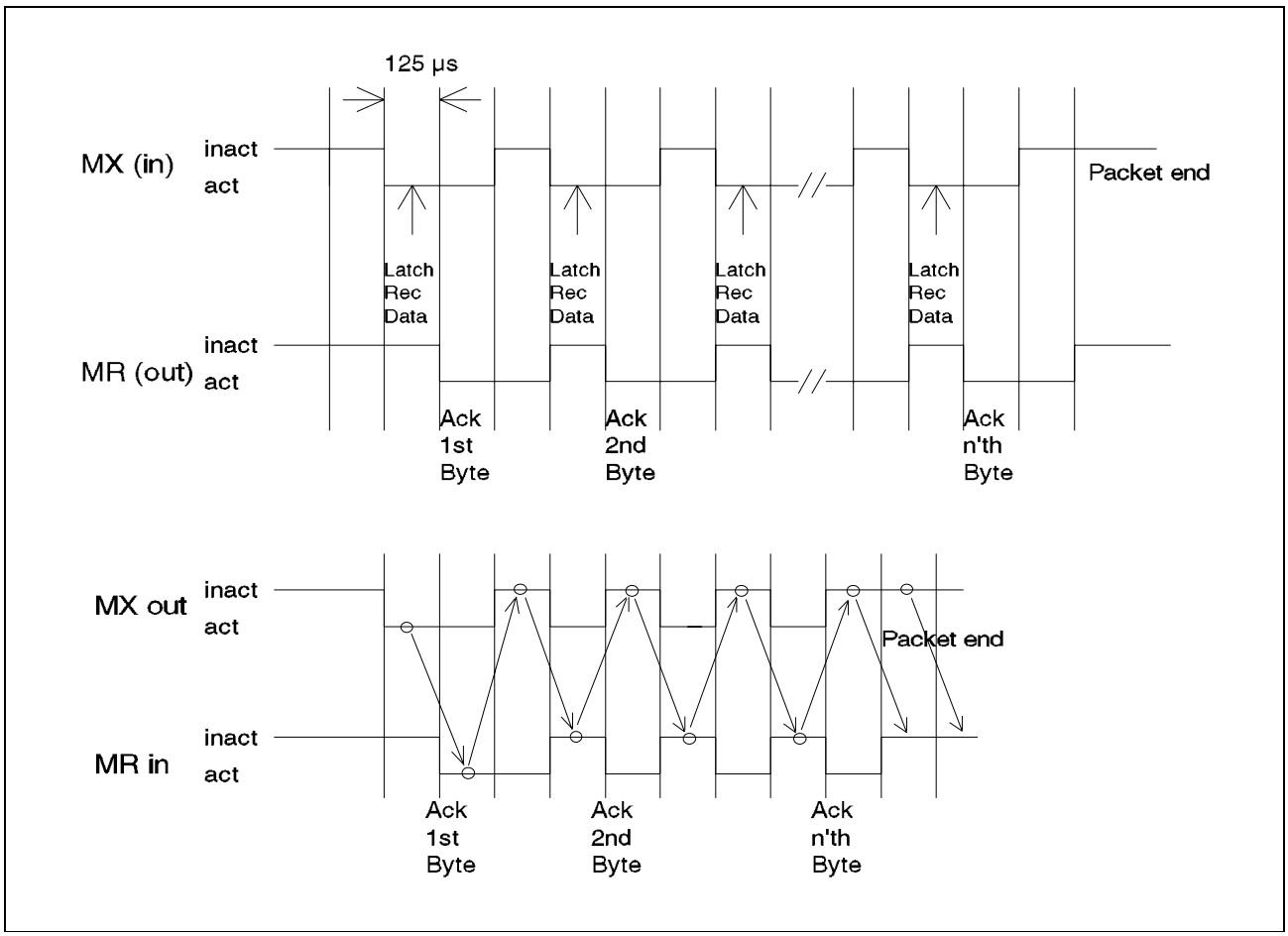


Figure 32

Figure 32 shows the general case, **Figure 33** the maximum speed case.

Software Handling of Monitor Channel Reception

The receiver of the monitor channel is controlled via the MRE bit. As long as the MRE bit is zero, no evaluation of the received MX bit is done. If the MRE bit is set to 1, then the monitor channel hardware waits for a start of a monitor packet. When the start of a packet is recognized with a monitor byte matching monitor receive address, acknowledgement can be enabled by the software by setting the MR control bit MRC to 1. The hardware performs acknowledgement by setting the transmitted MR bit to 0.

Upon the reception of the next byte the hardware sets the MDR status bit. When the monitor byte is read from the MONR register, this byte is acknowledged via transmit MR = 0. Every new byte is similarly indicated by the MDR status, and acknowledged after a read of the MONR register. If the hardware recognizes the end of a packet, it indicates this via the MER status (MRE = 1).

The receiver of the PSB 7280 does not perform a double-last-look check on the received data (i.e. compare the data received while MX = 0 with the data in the previous frame with MX = 1).

When MRC = 0, it is made sure that the receiver only receives the first byte of a packet and does not latch any further bytes in MONR until the beginning of the next packet.

Thus the conditions for latching the first byte of a packet is:

(MRE = 1) & (MX = 0 after having been 1 in at least two consecutive frames).

Any further bytes are latched into MONR only if:
(MRE $\times$ MRC = 1) & (previously received byte has been read from MONR register) & (MX = 0).

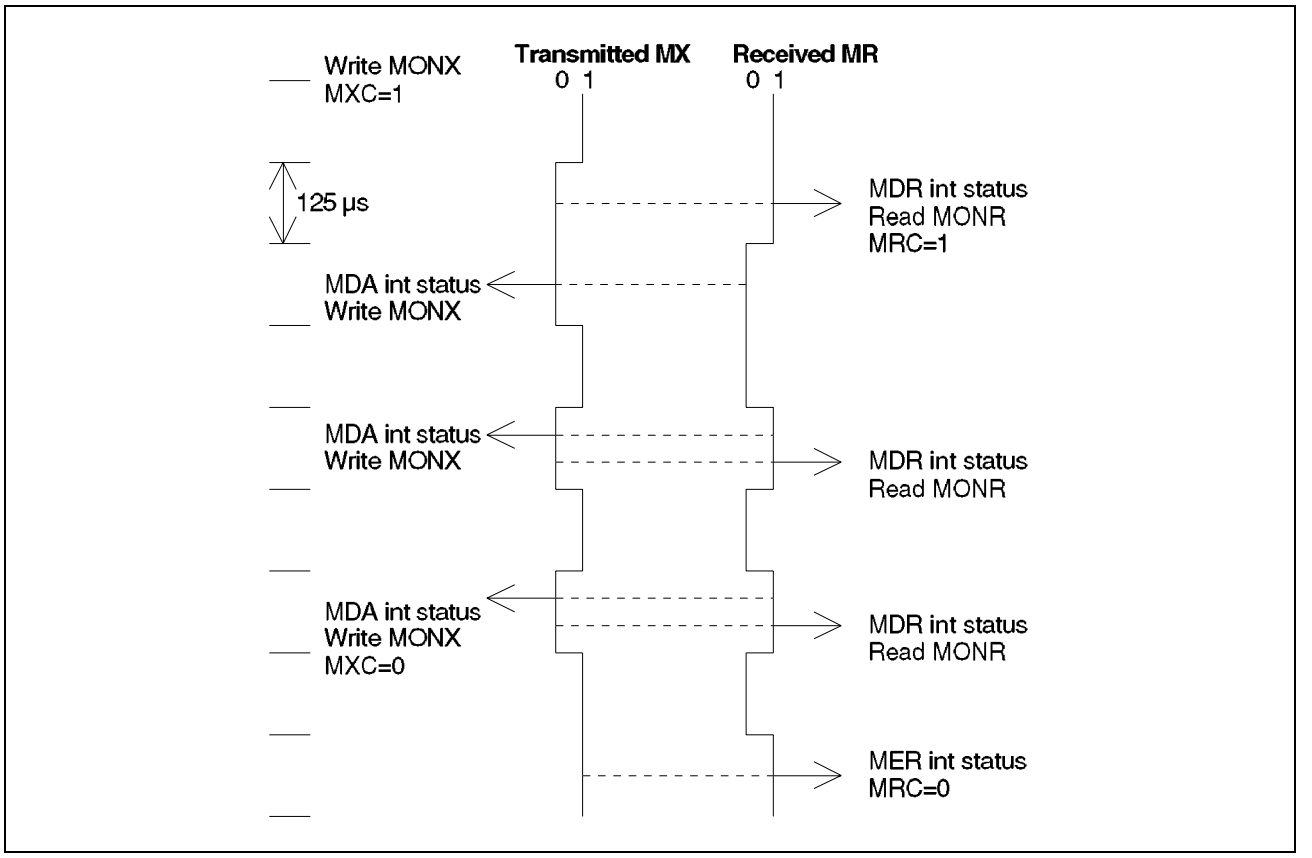


Figure 33

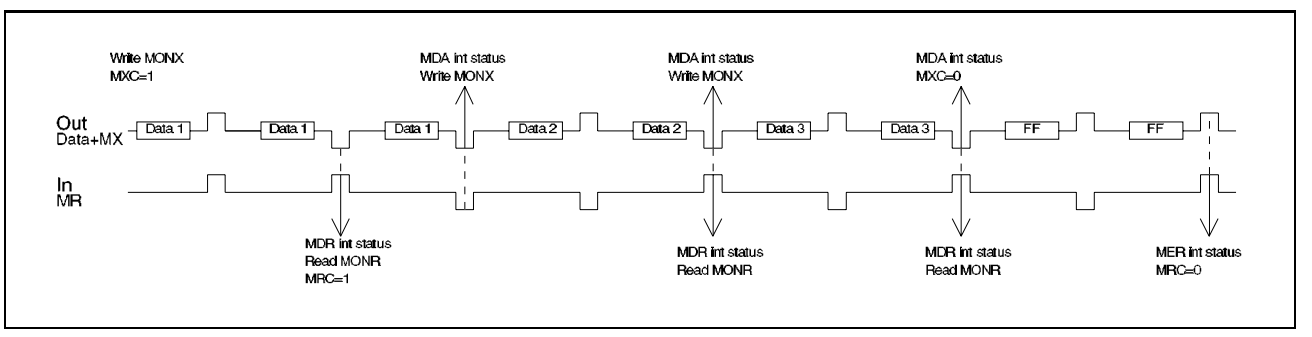


Figure 34

Monitor Channel Data Transfer

A hardware model of the monitor channel is shown in **Figure 35**.

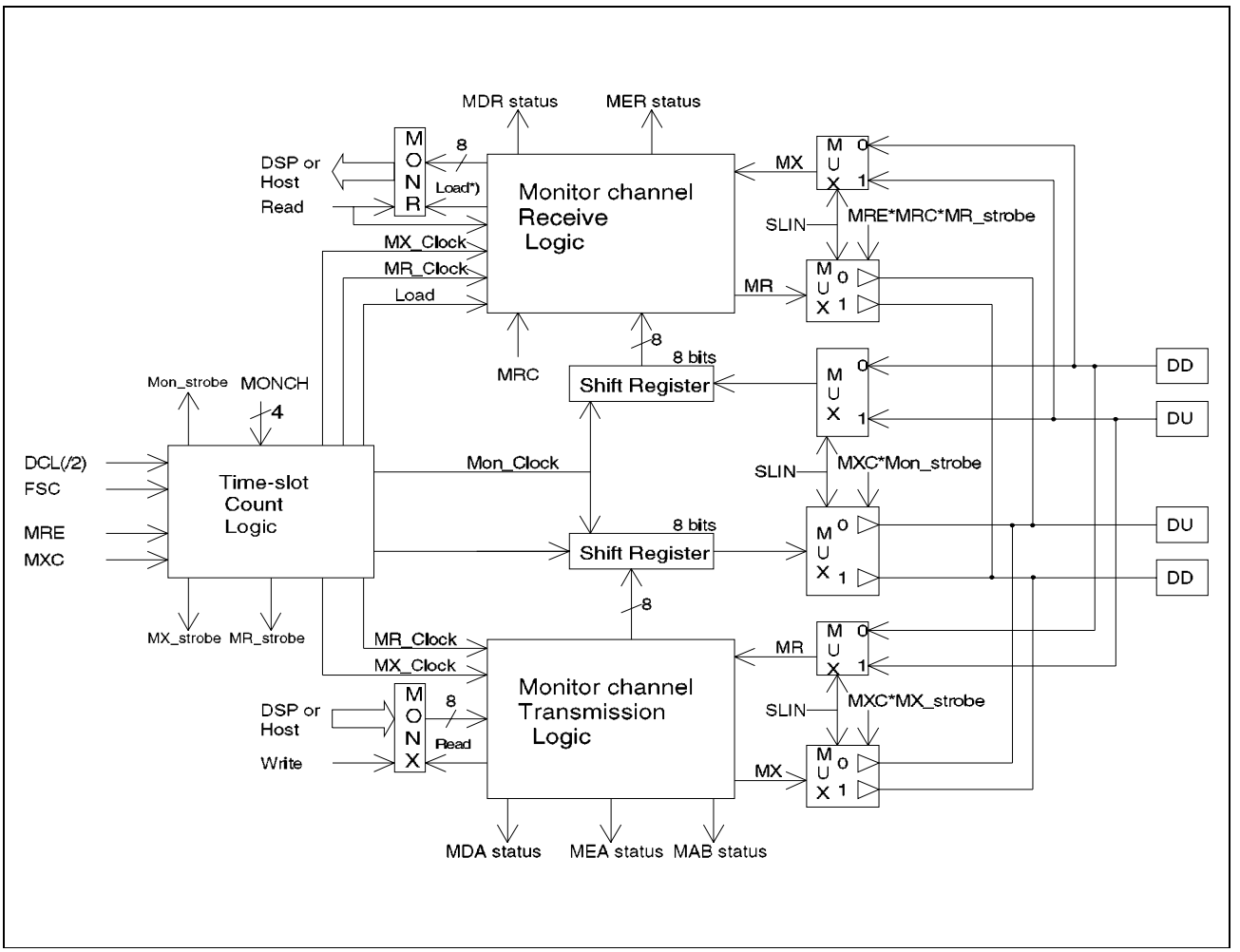


Figure 35

*) MRC has to be ‘1’ and MONR has to be read before any new value from the same packet is loaded into MONR. Thus, while MRC = 0, only the first byte of a packet is loaded into MONR.

4.4.2 C/I Channel

The two C/I channels are controlled via the C/I Transmit (CIX) and C/I Receive (CIR) registers, the C/I channel Enable (CIEN) and the C/I Change (CIC) interrupt status bit.

In addition, an Awake (AWK) control bit is provided. When this bit is set to ‘1’, the output line is unconditionally “low” until AWK is set to ‘0’ again. This bit is used in ISDN terminal applications to “wake up” the IOM-2 interface, i.e. to require clocking to be generated on DCL and FSC by an upstream circuit – typically an ISDN S-Bus Access Controller ISAC-S.

When the AWK bit is set to ‘0’, the output line is released only after the next FSC pulse has been detected, to avoid sending an invalid code in the outgoing C/I channel. C/I data reception and processing begins after setting of CIEN to 1. It is made sure that no invalid code is sent or received. AWK overrides any data normally transmitted during the C/I time-slot even if CIEN = 1. When CIEN is ‘0’ and AWK is ‘0’, the outgoing C/I channel is permanently in high-impedance state.

The block diagram of the C/I channel handler is shown in **Figure 37**.

In the receive direction, a change is recognized either using Double Last Look (DLL = 1) or not (DLL = 0).

Without Double Last Look

A change in received C/I channel is recognized after a new value is recognized once.

The new value is loaded into CIR for the DSP to read, and a CIC interrupt status is generated.

If further changes in receive C/I code take place before a previous changed value in CIR has been read, the changed values are not loaded in CIR.

When the first changed value is read by the DSP, the latest changed value is loaded in CIR and a CIC interrupt status is generated anew. Any possible changes that occurred between the first and the latest are thus lost.

With Double Last Look

A change in received C/I is recognized after a new value is detected in two consecutive frames.

This is shown in **Figure 36**.

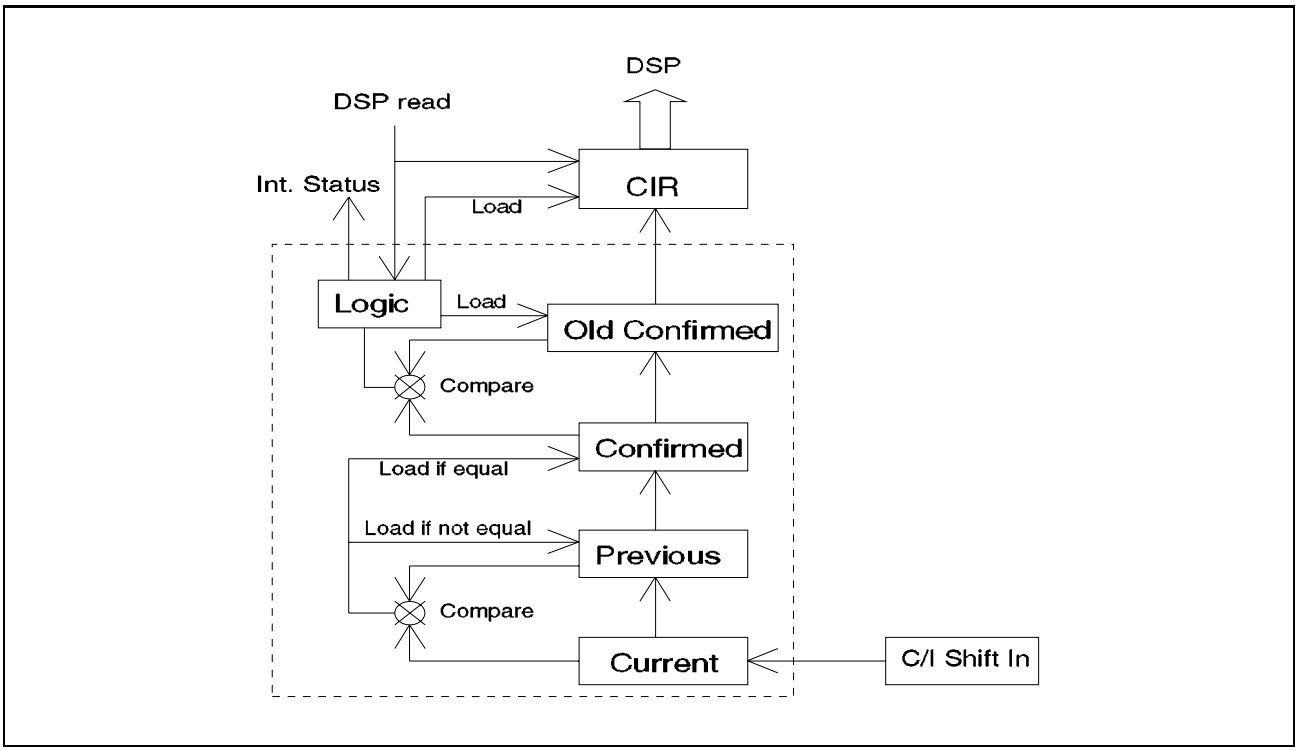


Figure 36

Algorithm

“Current” is compared to “Previous”:

– If they are not equal, “Current” is loaded into “Previous”, and a new comparison is performed in the next frame. No further actions are taken.
– If they are equal, the new value takes the place of “Confirmed”. “Confirmed” is compared to “Old Confirmed”:
  If they are equal, no actions are taken.
  If they are not equal, “Confirmed” is copied to “Old Confirmed”.

If CIR register has been read, “Old Confirmed” is compared to CIR:

– If they are equal, no actions are taken.
– If they are not equal, “Old Confirmed” is copied to CIR and a CIC interrupt status is generated.

C/I Channel Data Transfer

The block diagram of the C/I channel handler is shown in **Figure 37**.

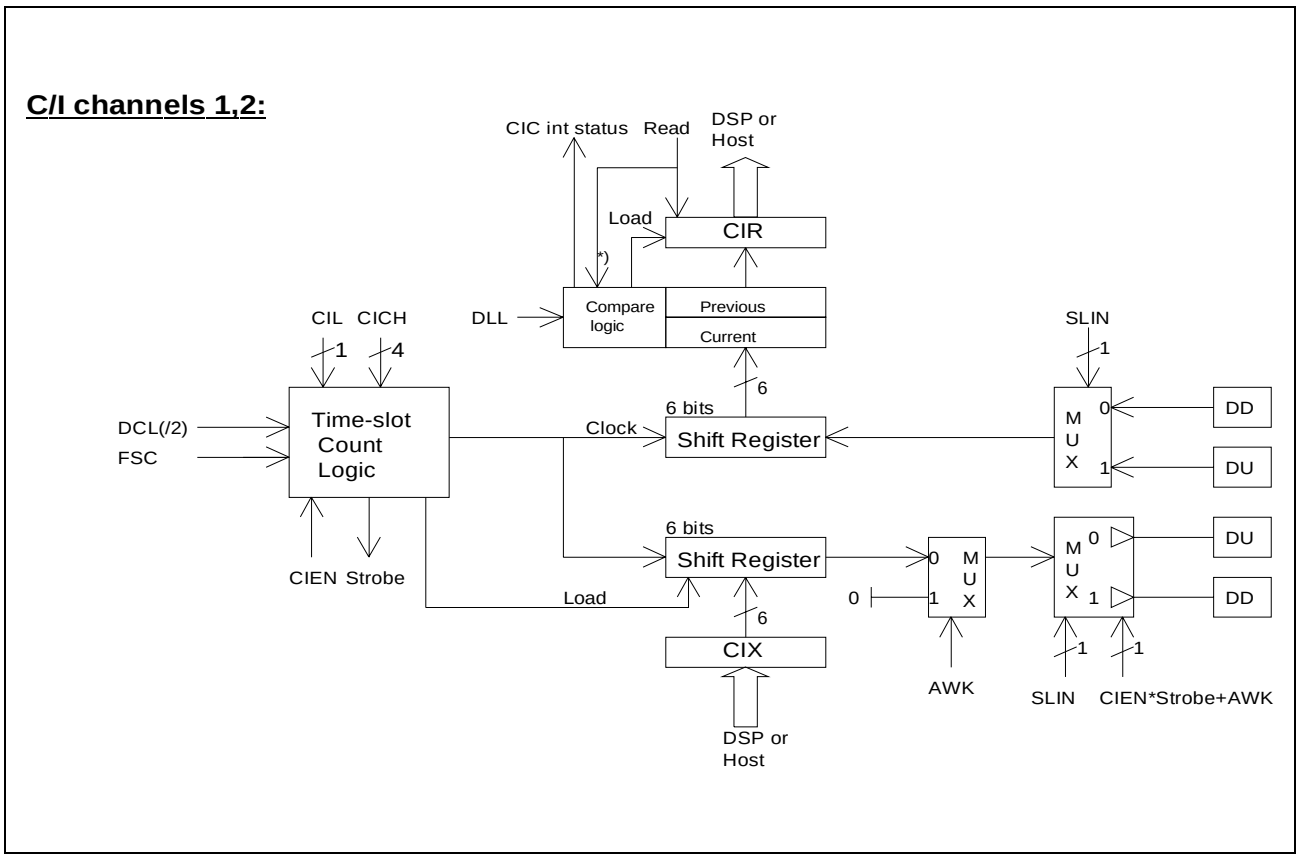


Figure 37

*) Read of the old changed value is the condition of loading of a new changed value. Thus, when several changes occur before the first changed value has been read, only the first and the last change are available.

4.5 Programming Indirectly Accessible Registers

Registers in the memory mapped (DSP X-data RAM) area from 2000_H upwards are read and written:

– via the Parallel Host Interface by using two registers (Conf/Cont Reg Address Register at address $40_H/3040_H$ and Conf/Control Reg Data Register at address $41_H/3041_H$)

4.5.1 Programming via Parallel Host Interface (see also **Chapter 3.3.2**)

For writing a configuration/control register (addresses 2000_H-$203F_H$), the host writes in the data register the data byte to be written and in the address register the write command:

Bit 7							Bit 0
0	0	A5	A4	A3	A2	A1	A0

where A(5:0) gives the offset of the register to be written. This causes an RACC (Register Access) interrupt status to the DSP. The DSP software transfers the data byte to the requested address 2000_H + A(5:0) and writes the RDY bit (least significant bit of address $40_H/3040_H$) to ‘1’ again (which was set to ‘0’ by hardware at the time of writing of the address register). By sensing the state of bit RDY the host is able to start a new access to address and data registers when the DSP is ready.

For reading a configuration/control register (addresses 2000_H - $203F_H$), the host writes in the address register the read command:

Bit 7							Bit 0
1	0	A5	A4	A3	A2	A1	A0

where A(5:0) gives the offset of the register to be read. This causes a RACC (Register Access) interrupt status to the DSP. The DSP software transfers the contents of the requested address 2000_H + A(5:0) into the data register and writes the RDY bit to ‘1’.

5 Register Description

5.1 Interrupt Structure

As explained in **Chapter 3**, the interrupt statuses are grouped on two interrupt lines, “high priority” and “low priority” interrupts, respectively.

High Priority Interrupts ($\overline{\text{INTR}}$)

FSC, RFS, TFS
BFUL1, BFUL2, BEMP1, BEMP2, BFHR1, BFHX1, BFHR2, BFHX2

Lower Priority Interrupts ($\overline{\text{INT}}$)

T1, T2, T3
SAIN
HDLC1, HDLC2
DINT
GPI
MDR, MER, MDA, MEA, MAB, CIC1, CIC2

Corresponding interrupt status register exist for the internal DSP.

The interrupt status registers are physically separate for the host and for the DSP. Thus, when an interrupt status is generated, the interrupt status bit is set in both registers.

The interrupt status disappears from the interrupt status register when the cause of the interrupt status is removed by the software, or the interrupt is explicitly acknowledged.

Whenever possible, an interrupt status is made to disappear when the cause of that interrupt status is removed (example: in/out audio data channel interrupts), in order to spare the explicit writing of an acknowledge register address. In other cases the interrupt statuses are explicitely acknowledged by writing a ‘1’ in a virtual acknowledge register.

The interrupt status bits have individual mask bits which have no influence on the setting of the interrupt status bits, but only on the generation of the interrupt on the interrupt line. When the mask bit is 0, the generation of the interrupt for the corresponding interrupt status on line $\overline{\text{INTR}}$ or $\overline{\text{INT}}$ is prevented.

5.2 Interrupt Status Registers

Register Map for Host Interrupts

Host Interrupt Status for $\overline{\text{INTR}}$:

	Bit 15							Bit 8
71_H	FSC	RFS	TFS					

	Bit 7							Bit 0
70_H	BFUL1	BFUL2	BEMP1	BEMP2	BFHR1	BFHX1	BFHR2	BFHX2

FSC FSC detected

RFS RFS detected

TFS TFS detected

BFUL1 Receive channel 1 sample of programmable length (1...32 bits) available in RC1

BFUL2 Receive channel 2 sample of programmable length (1...32 bits) available in RC2

BEMP1 Transmit channel 1 sample of programmable length (1...32 bits) can be written in XC1

BEMP2 Transmit channel 2 sample of programmable length (1...32 bits) can be written in XC2

BFHR1 HDLC 1 receiver shift register can be read and/or written (1, 2 or 4 bytes) in HR1

BFHX1 HDLC 1 transmitter shift register can be read and/or written (1, 2 or 4 bytes) in HX1

BFHR2 HDLC 2 receiver shift register can be read and/or written (1, 2 or 4 bytes) in HR2

BFHX2 HDLC 2 transmitter shift register can be read and/or written (1, 2 or 4 bytes) in HX2.

Interrupt Mask Registers

	Bit 15							Bit 8
71_H	FSC	RFS	TFS					

	Bit 7							Bit 0
70_H	BFUL1	BFUL2	BEMP1	BEMP2	BFHR1	BFHX1	BFHR2	BFHX2

A ‘0’ in a bit position masks the corresponding interrupt (default value, i.e. after Reset). The mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set.

Acknowledge Register

	Bit 15							Bit 8
73_H	FSC	RFS	TFS					

The interrupt status bit is reset when the host writes a ‘1’ in the corresponding bit position.

The other interrupt status bits are reset when the input/output registers are read or written:

BFUL1 Reset when RC1 (address 00_H) is read

BFUL2 Reset when RC2 (address 04_H) is read

BEMP1 Reset when XC1 (any of $00\text{-}03_H$) is written

BEMP2 Reset when XC2 (any of $04\text{-}07_H$) is written

BFHR1 Reset when HRR1 (any of $10\text{-}13_H$) is read

BFHX1 Reset when HXR1 (any of $14\text{-}17_H$) is read

BFHR2 Reset when HRR2 (any of $18\text{-}1B_H$) is read

BFHX2 Reset when HXR2 (any of $1C\text{-}1F_H$) is read.

Host Interrupt for $\overline{\text{INT}}$

	Bit 15							Bit 8
75_H	T1	T2	T3	SAIN		DINT	HDLC1	HDCL2

	Bit 7							Bit 0
74_H	MDR	MER	MDA	MEA	MAB	GPI	CIC1	CIC2

T1	Timer T1 expired
T2	Timer T2 expired
T3	Timer T3 expired
SAIN	Serial Audio Input Interrupt (from SIO line)
DINT	Software interrupt from DSP
HDLC1	Interrupt from HDLC Controller 1
HDLC2	Interrupt from HDLC Controller 2
MDR	Monitor Channel Data Received
MER	Monitor Channel End of Reception
MDA	Monitor Channel Data Acknowledged
MEA	Monitor End of Acknowledgment
MAB	Monitor Channel Abort Request
GPI	General Purpose Interrupt occured
CIC1	C/I Channel 1 Change
CIC2	C/I Channel 2 Change.

Interrupt Status Mask Register

	Bit 15							Bit 8
75_H	T1	T2	T3	SAIN		DINT	HDLC1	HDCL2

	Bit 7							Bit 0
74_H	MDR	MER	MDA	MEA	MAB	GPI	CIC1	CIC2

A ‘0’ in a bit position masks the corresponding interrupt (default value, i.e. after reset). The mask bit affects only the generation of the interrupt, but not the interrupt status bit from being set. Undocumented mask bits must be always set to ‘0’.

Acknowledge Register

	Bit 15							Bit 8
77_H	T1	T2	T3	SAIN				

	Bit 7							Bit 0
76_H		MER	MDA	MEA	MAB			

The interrupt status bit is reset when the host writes a ‘1’ in the corresponding bit position. The other interrupts are acknowledged as follows:

DINT Reset when IND Int. Status register is read

HDLC1 Reset when HDLC Controller 1 interrupt register is read

HDLC2 Reset when HDLC Controller 2 interrupt register is read

MDR Reset when MONR register is read

GPI Reset when GP Int Status register is read

CIC1 Reset when CIR1 register is read

CIC2 Reset when CIR2 register is read.

*Note: Since no direct access to the MONR, CIR1, CIR2 and GP Int Status registers for the host is allowed (these registers are in the configuration and control register area 2000_H upwards), they are read using the procedure via address and data registers as decribed in **Chapter 2** – in principle giving the host the possibility to handle the Monitor and C/I channels via the DSP.*

5.3 Indirectly Accessible Configuration and Control Registers

Table 15 Summary

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2000_H	Chip Version Nr			VN5	VN4	VN3	VN2	VN1	VN0
2001_H	External Memory	LDMEM	CAEN		DACC	NRW3	NRW2	NRW1	NRW0
2002_H	General Config	PU	CRS	CKOEN	CKOS	ODS	CKOBR18	CKOBR17	CKOBR16
2003_H	CLKO Baud Rate2	CKOBR15	CKOBR14	CKOBR13	CKOBR12	CKOBR11	CKOBR10	CKOBR9	CKOBR8
2004_H	CLKO Baud Rate1	CKOBR7	CKOBR6	CKOBR5	CKOBR4	CKOBR3	CKOBR2	CKOBR1	CKOBR0
2005_H	SAI Mode	SODS	SPS	DSE			SCKIN	PRSC9	PRSC8
2006_H	SCLK Baud Rate	PRSC7	PRSC6	PRSC5	PRSC4	PRSC3	PRSC2	PRSC1	PRSC0
2007_H	RFS Mode	RFIN	RCONT	RFE	RFSEL	RFPS		RREP9	RREP8
2008_H	RFS Per/Rep Rate	RREP7	RREP6	RREP5	RPRD4/ RREP4	RPRD3/ RREP3	RPRD2/ RREP2	RPRD1/ RREP1	RPRD0/ RREP0
2009_H	TFS Mode	TFIN	TCONT	TFE	TFSEL	TFPS		TREP9	TREP8
$200A_H$	TFS Per/Rep Rate	TREP7	TREP6	TREP5	TPRD4/ TREP4	TPRD3/ TREP3	TPRD2/ TREP2	TPRD1/ TREP1	TPRD0/ TREP0
$200B_H$	SIO Config						SAIO	SOUT	SINTC
$200C_H$	Timer 1	T1EN		T15	T14	T13	T12	T11	T10
$200D_H$	Timer 2	T2EN	T26	T25	T24	T23	T22	T21	T20
$200E_H$	Timer 3 Mode	T3EN		T313	T312	T311	T310	T39	T38
$200F_H$	Timer 3	T37	T36	T35	T34	T33	T32	T31	T30
2010_H	HDLC Cntr Access							HAH1	HAH2
2011_H	Rec Audio Ch1 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
2012_H	Rec Audio Ch1 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1
2013_H	Rec Audio Ch1 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	
2014_H	Rec Audio Ch2 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
2015_H	Rec Audio Ch2 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1
2016_H	Rec Audio Ch2 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	
2017_H	Tx Audio Ch1 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
2018_H	Tx Audio Ch1 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1

Table 15 Summary (cont'd)

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2019_H	Tx Audio Ch1 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	HXA
$201A_H$	Tx Audio Ch2 Cfg	EN	SLIN1	SLIN0	LEN4	LEN3	LEN2	LEN1	LEN0
$201B_H$	Tx Audio Ch2 TS	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1
$201C_H$	Tx Audio Ch2 Mode	TS0	LMOD	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	HXA
$201D_H$	HDLC1 Ser Rec Path				SLIN1	SLIN0	LMOD1	LMOD0	HHR
$201E_H$	HDLC1 Ser Tx Path				SLIN1	SLIN0	LMOD1	LMOD0	HHX
$201F_H$	HDLC2 Ser Rec Path				SLIN1	SLIN0	LMOD1	LMOD0	HHR
2020_H	HDLC2 Ser Tx Path				SLIN1	SLIN0	LMOD1	LMOD0	HHX
2021_H	Mon Ch Config				SLIN	MONCH3	MONCH2	MONCH1	MONCH0
2022_H	Mon Ch Cntr						MRE	MRC	MXC
2023_H	IC Mon Channel Id	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
2024_H	Monitor Tx/Rec	MONR7/ MONX7	MONR6/ MONX6	MONR5/ MONX5	MONR4/ MONX4	MONR3/ MONX3	MONR2/ MONX2	MONR1/ MONX1	MONR0/ MONX0
2025_H	C/I Ch Mode					CIEN1	AWK1	CIEN2	AWK2
2026_H	C/I Ch 1 Config		SLIN	CICH3	CICH2	CICH1	CICH0	CIL	DLL
2027_H	C/I Ch 2 Config		SLIN	CICH3	CICH2	CICH1	CICH0	CIL	DLL
2029_H	C/I Channel 1			CIR5/ CIX5	CIR4/ CIX4	CIR3/ CIX3	CIR2/ CIX2	CIR1/ CIX1	CIR0/ CIX0
$202A_H$	C/I Channel 2			CIR5/ CIX5	CIR4/ CIX4	CIR3/ CIX3	CIR2/ CIX2	CIR1/ CIX1	CIR0/ CIX0
$202B_H$	IOM Config							FODS	CGEN
$202C_H$	PLL Config 1	M0	CM1		MAX	BYPA	LOCK	SWCK	PU
$202D_H$	PLL Config 1	N4	N3	N2	N1	N0	M3	M2	M1
2030_H	GP Output Config					IOC3	IOC2	IOC1	IOC0
2031_H	GP Direction					IOD3	IOD2	IOD1	IOD0
2032_H	GP Data					IOR3	IOR2	IOR1	IOR0
2033_H	GP Strobe					IOS3	IOS2	IOS1	IOS0
2034_H	GP Int Status					IOINT3	IOINT2	IOINT1	IOINT0
2035_H	GP Int Mask					IOIM3	IOIM2	IOIM1	IOIM0

Note:

VN(5:0)	Read only (hardwired).
MAD(7:0)	Loaded from AD(7:0) at reset, may be written thereafter.
MONR	A read of MONR acknowledges MDR interrupt status (for Host and for DSP).
CIR	A read of CIR acknowledges the C/I Change CIC int status (for Host and for DSP).
GP Int Status	A read of GP Int Status acknowledges the GP IO interrupt status (for Host and DSP).

Description of Configuration and Control Registers

Unless otherwise indicated, all register bits are initialized to ‘0’ after a hardware reset.

When read, register bits that are not in use (or reserved for future use) are not defined, i.e. their value may be either ‘0’ or ‘1’.

During the initialization phase the firmware does a re-programming on the following registers of the configuration/control block to setup the default configuration for the communication with a video-processor (see **Chapter 6.2.3.3**), i.e. the hardware reset values given in the register description below are overwritten by the following values:

Table 16

Address	Data	Description
2005_H	04_H	SCLK is an output
2006_H	$1B_H$	SCLK Baud Rate = 34.56 MHz / 28 = 1.23 MHz
2011_H	$8F_H$	Receive Uncompressed Audio: DU line, 16 bit linear
2012_H	10_H	Position of first bit in time-slot: 32
2013_H	42_H	Interrupt generated after 2 samples of 16 bits stored
2017_H	AF_H	Transmit Uncompressed Audio: DD line, 16 bit linear
2018_H	10_H	Position of first bit in time-slot: 32
2019_H	42_H	Interrupt generated after 2 samples of 16 bits stored
$201D_H$	10_H	HDLC1 receiver connected to SR line
$201E_H$	18_H	HDLC1 transmitter connected to ST line

Moreover, the firmware uses registers 2007_H and 2009_H for setting up the appropriate number of frame syncs.

The firmware also initialises the PLL Config registers $202C_H$ and $202D_H$ to its appropriate values in case the PLL mode is selected via the CM1 pin. In case the non-PLL mode is chosen, the firmware does not use these registers.

Chip Version Number Register **Read** **Address 2000_H**

Value after reset: 20_H

VN(5-0)	Version Number of Chip

External Memory Interface Register **Read/Write** **Address 2001_H**

Value after reset: 00_H

LDMEM	Load Memory. If LDMEM = 0, the external memory interface is connected with the program bus. It is used for connecting an external software RAM or EPROM. If LDMEM = 1, the external memory interface address and data buses are connected to the outputs of registers address low/high (at host address $44/45_H$) and data low/high (at host address $46/47_H$), respectively. This mode is used to download a program into an external RAM.
CAEN	If $\overline{EA}$=1 and LDMEM = 0: Enable address lines (CA bus) to external SRAM for program/data fetch; no meaning in other cases. 0: CA bus switched off, no program/data fetch possible (reset value). 1: CA bus active, external program/data fetch possible.
DACC	Data Access, selects program or data memory connected to SRAM-interface. 0: program memory connected (reset value). 1: data memory connected, can be written by using “MOV” instruction, must be read by using “MOVP”.
NRW(3-0)	Number of wait states for external interface. The number of wait states is NRW (1111_B = 0 wait states, 0000_B = 15 wait states), takes the value 0000_B after reset. SRAM connected for development purpose should be capable of zero wait states.

General Configuration Register **Read/Write** **Address 2002_H**

Value after reset: $B0_H$

PU	Power Up	
	0	The DSP clock is turned off. It can be started again with a DSP interrupt.
	1	Normal operation This is the value of PU after a hardware reset.
CRS	Clock Rate Select	
	0	Input DCL is twice the bit rate on IOM-2.
	1	Input DCL is equal to the bit rate on IOM-2.
CKOEN	CLKO Enable	
	0	CLKO disabled (output high-impedance), CLKO generator initialized and idle.
	1	Enables generation of CLKO (value during and after reset).
	When PU is ’0’ and CKOEN is ’0’, all outputs and input/outputs of the PSB 7280 are in the high-impedance state.	
CKOS	Source clock for CLKO output pin	
	0	Internal DSP system clock is input for divider connected to CLKO.
	1	CLKO outputs 7.68 MHz, may be used to clock e.g. an ISAC-S (value during and after reset).
ODS	Open drain select for IOM DU and DD lines:	
	0	DD and DU are open drain (reset value).
	1	DD and DU are push-pull.
CKOBR (18-16)	Most significant bits of baud rate division factor for CLKO output from DSP clock.	

CLKO Baud Rate Registers **Read/Write Address 2003_H/2004_H**

Value after reset: 00_H

CKOBR(15-0) Less significant bits of baud rate division factor for CLKO output from DSP clock.

Serial Audio Interface Signal Register **Read/Write Address 2005_H-$200A_H$**

Value after reset: 00_H

SODS Serial Audio Interface Open Drain Select for SR and ST line

0 SR and ST are push-pull (Reset value)

1 SR and ST are open drain

SPS SCLK Polarity select

0 Data/Frame Sync out on rising edge, Data/Frame Sync in on falling edge (if DSE = 1, idle position outside strobe = 0)

1 Data/Frame Sync out on falling edge, Data/Frame Sync in on rising edge (if DSE = 1, idle position outside strobe = 1)

DSE Data Strobe Enable (only valid if SCLK is output)

0 SCLK is permanently active

1 SCLK is active only during the programmed timeslots for SR and ST. Outside the active timeslots, SR and ST remain as High-Z. The strobe signals of all audio receivers and transmitters to either SR or ST line are combined by logical OR and ANDed with internal SCLK.

SCKIN Serial Clock In

0 SCLK is an input

1 SCLK is an output

PRSC(9-0) Prescaler

SCLK is derived from the DSP clock by division through PRSC + 1 (1 to 1024)

RFIN RFS In

0 RFS is an input

1 RFS is an output

RCONT Continuous generation of RFS pulses

- 0 A number of pulses (spaced 16-bit periods from each other) equal to RREP + 1 (1, ..., 1024) is generated upon an STR command (see HDLC/transparent data controller register description).
- 1 When ERFS bit is ‘1’ (see HDLC/transparent data controller register description), continuous pulses on RFS are generated, spaced RPRD + 1 (1, ..., 32) 16-bit words from each other.

RFE RFS Clock Edge

- 0 When RFS is generated by the PSB 7280 (=output), it changes its state at the rising edge of the SCLK clock.
- 1 When RFS is generated by the PSB 7280 (=output), it changes its state at the falling edge of the SCLK clock.

RFSEL Receive Frame Sync Select (only valid if RFS is output)
(in both cases the polarity is selected by RFPS)

- 0 Single cycle RFS is generated
- 1 The data strobe is output on RFS pin. This only affects the RFS pin, the internal frame sync is generated and is input to the timeslot count logic of the audio receivers and transmitters connected to SR and ST line as in case RFSEL = 0. The strobe signals of all audio receivers and transmitters connected to SR and ST line will be combined by logical OR.

RFPS RFS polarity select

- 0 Rising edge marks the beginning of a new frame on the RFS line.
- 1 Falling edge marks the beginning of a new frame on the RFS line. If RFS is an output it is inverted vs. RFPS = 0

RPRD(4-0)/ Period of RFS pulse generation

RREP(9-0) Number of repetition of pulses
When RCONT = 0, RREP(9-0) gives the number of pulses (RREP + 1) to be generated, spaced 16 bits apart (up to 1024 pulses).
When RCONT = 1, RPRD(4-0) gives the spacing of continuously generated pulses in 16-bit word increments (up to 32).

TFIN TFS In

- 0 TFS is an input
- 1 TFS is an output

TCONT Continuous generation of TFS pulses

- 0 A number of pulses (spaced 16-bit periods from each other) equal to TREP + 1 (1, ..., 1024) is generated upon an STX command (see HDLC/transparent data controller register description).
- 1 When ETFS bit is ‘1’ (see HDLC/transparent data controller register description), continuous pulses on TFS are generated, spaced TPRD + 1 (1, ..., 32) 16-bit words from each other.

TFE TFS Clock Edge

- 0 When TFS is generated by the PSB 7280 (=output), it changes its state at the rising edge of the SCLK clock.
- 1 When TFS is generated by the PSB 7280 (=output), it changes its state at the falling edge of the SCLK clock.

TFSEL Transmit Frame Sync Select (only valid if TFS is output)
(in both cases the polarity is selected by TFPS)

- 0 Single cycle TFS is generated
- 1 The data strobe is output on TFS pin. This only affects the TFS pin, the internal frame sync is generated and is input to the timeslot count logic of the audio receivers and transmitters connected to SR and ST line as in case TFSEL = 0. The strobe signals of all audio receivers and transmitters connected to SR and ST line will be combined by logical OR.

TFPS TFS polarity select

- 0 Rising edge marks the beginning of a new frame on the TFS line.
- 1 Falling edge marks the beginning of a new frame on the TFS line. If TFS is an output it is inverted vs. TFPS = 0

TPRD(4-0)/ Period of TFS pulse generation

TREP(9-0) Number of repetition of pulses
When TCONT=0, TREP(9-0) gives the number of pulses (TREP+1) to be generated, spaced 16 bits apart (up to 1024 pulses).
When TCONT=1, TPRD(4-0) gives the spacing of continuously generated pulses in 16-bit word increments (up to 32).

SIO Configuration Register **Read/Write** **Address $200B_H$**

Value after reset: 00_H

SAIO	Serial Audio Interrupt line In/Out	
	0	SIO line is an input
	1	SIO line is an output
SOUT	Serial Audio Out value. If SAIO = 1 (SIO is output), value of SIO line (clocked out with the rising edge of SCLK).	
SINTC	Serial Audio Interrupt Configuration	
	0	If SIO is programmed as input (SIO = 0), a falling edge on SIO causes an interrupt, if unmasked.
	1	If SIO is programmed as input (SIO = 0), a rising edge on SIO causes an interrupt, if unmasked.

Timers **Read/Write Address $200C_H$-$200F_H$**

Value after reset: 00_H

T1EN Timer 1 Enable

0 Stops the timer and initializes it.

1 Enables the timer.

When T1EN = 1, the timer generates continuously a pulse of one FSC period width with a repetition rate determined by T1.

T1(5-0) Timer 1

Gives the division factor for timer 1 generation, starting from FSC (divided by 1 to 64).

T2EN Timer 2 Enable

0 Stops the timer and initializes it.

1 Enables the timer.

When T1EN = 1 and T2EN = 1, the timer expires periodically with a period determined by T1 and T2.

T2(6-0) Timer 2

Gives the division factor for timer 2 generation, starting from Timer 1 output (divided by 1 to 128).

T3EN Timer 3 Enable

0 Stops the timer and initializes it.

1 Enables the timer.

When T3EN = 1, the timer generates continuously a pulse of one clock width with a repetition rate determined by T1.

T3(13-0) Timer 3
Gives the division factor for timer 3 generation, starting from DSP clock (1 to 16384 prescaler 256).

HDLC Controller Access Register **Read/Write** **Address 2010_H**

Value after reset: 00_H

HAH1 Host Access to HDLC Controller 1

0 The DSP services the HDLC controller (register set including FIFOs is inaccessible from host).

1 The Host services the HDLC controller (register set including FIFOs is inaccessible from DSP).

This bit determines the access to the register area of the HDLC controller 1; it is independent of the HHR and HHX bits which determine the access from DSP or host to the HDLC serial input and output, respectively.

HAH2 Host Access to HDLC Controller 2

0 The DSP services the HDLC controller (register set including FIFOs is inaccessible from host).

1 The host services the HDLC controller (register set including FIFOs is inaccessible from DSP).

This bit determines the access to the register area of the HDLC controller 2; it is independent of the HHR and HHX bits which determine the access from DSP or host to the HDLC serial input and output, respectively.

Receive Audio Channel 1 **Read/Write Address 2011_H-2013_H**

Value after reset: 00_H

EN Enable

If inactive (0), no clock is generated for this channel, must be set to 0 during configuration of receive audio channel 1.

SLIN(1-0) Select Line

00 Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)

01 Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)

10 Channel time-slot on SR (frame sync RFS, clock SCLK)

11 Channel time-slot on ST (frame sync TFS, clock SCLK)

LEN(4-0) Length of channel time-slot
Channel time-slot length in bits = LEN + 1 (1, ..., 32 bits).

TS(8-0) Time-slot position

Position of first bit of time-slot from frame sync (0, ..., 511).

LMOD Load Mode

0 Sample of length LEN+1 loaded into read register (**from frame**-**1**) at the occurrence of frame sync.

1 (LBIT + 1) $\times$ (LEN + 1) bits are loaded into read register when ready (for software to be accessed via a “Buffer Full” interrupt status).

LBIT(4-0) Load Bits

Number of bits in aggregates of (LEN + 1) loaded into read register when ready, if LMOD = 1. The number of bits loaded is equal to (LBIT + 1) $\times$ (LEN + 1), the corresponding interrupt status is BFUL1.

Note: Since the number of bits is 32 maximum, the value of the product (LBIT + 1)$\times$ (LEN + 1) shall not exceed 32.

Receive Audio Channel 2 **Read/Write Address 2014_H-2016_H**

Value after reset: 00_H

EN — Enable

If inactive (0), no clock is generated for this channel, must be set to 0 during configuration of receive audio channel 2.

SLIN(1-0) — Select Line

- 00 Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)
- 01 Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)
- 10 Channel time-slot on SR (frame sync RFS, clock SCLK)
- 11 Channel time-slot on ST (frame sync TFS, clock SCLK)

LEN(4-0) — Length of channel time-slot channel time-slot length in bits = LEN + 1 (1, ..., 32 bits).

TS(8-0) — Time-slot position
Position of first bit of time-slot from frame sync (0, ..., 511).

LMOD — Load Mode

- 0 Sample of length LEN + 1 loaded into read register (**from frame - 1**) at the occurrence of frame sync.
- 1 (LBIT + 1) $\times$ (LEN + 1) bits are loaded into read register when ready (for software to be accessed via a ”Buffer Full” interrupt status).

LBIT(4-0) — Load Bits

Number of bits in aggregates of (LEN + 1) loaded into read register when ready, if LMOD = 1. The number of bits loaded is equal to (LBIT + 1) $\times$ (LEN + 1), the corresponding interrupt status is BFUL2.

Note: Since the number of bits is 32 maximum, the value of the product (LBIT + 1) $\times$ (LEN + 1) shall not exceed 32.

Transmit Audio Channel 1 **Read/Write Address 2017_H-2019_H**

Value after reset: 00_H

EN — Enable

If inactive (0), no clock is generated for this channel, and the channel is in high impedance, must be set to 0 during configuration of transmit audio channel 1.

SLIN(1-0) — Select Line

- 00 Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)
- 01 Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)
- 10 Channel time-slot on SR (frame sync RFS, clock SCLK)
- 11 Channel time-slot on ST (frame sync TFS, clock SCLK)

LEN(4-0) — Length of channel time-slot

Channel time-slot length in bits = LEN + 1 (1, ..., 32 bits).

TS(8-0) — Time-slot position

Position of first bit of time-slot from frame sync (0, ..., 511).

LMOD — Load Mode

- 0 Sample of length LEN + 1 loaded from write register into shift register (**for frame + 1**) at the occurrence of frame sync.
- 1 When shift register is about to become empty ((LBIT + 1) × (LEN + 1) bits shifted out), it is loaded from write register (for software to be accessed via a “Buffer Empty” interrupt status).

LBIT(4-0) — Load Bits

Number of bits in aggregates of (LEN + 1) loaded into output shift register when ready, if LMOD = 1. The number of bits loaded is equal to (LBIT + 1) × (LEN + 1), the corresponding interrupt status is BEMP1. Since the number of bits is 32 maximum, the value of the product (LBIT + 1) × (LEN + 1) shall not exceed 32.

HXA — Host Transmit Access

- 0 Channel originates from DSP
- 1 Channel originates from Host

Transmit Audio Channel 2 **Read/Write Address $201A_H$-$201C_H$**

Value after reset: 00_H

EN Enable

If inactive (0), no clock is generated for this channel, and the channel is in high impedance, must be set to 0 during configuration of transmit audio channel 2.

SLIN(1-0) Select Line

- 00 Channel time-slot on DU (frame sync FSC, clock DCL or DCL/2)
- 01 Channel time-slot on DD (frame sync FSC, clock DCL or DCL/2)
- 10 Channel time-slot on SR (frame sync RFS, clock SCLK)
- 11 Channel time-slot on ST (frame sync TFS, clock SCLK)

LEN(4-0) Length of channel time-slot

Channel time-slot length in bits = LEN + 1 (1, ..., 32 bits).

TS(8-0) Time-slot position

Position of first bit of time-slot from frame sync (0, ..., 511).

LMOD Load Mode

- 0 Sample of length LEN + 1 loaded from write register into shift register (**for frame + 1**) at the occurrence of frame sync.
- 1 When shift register is about to become empty ((LBIT + 1) $\times$ (LEN + 1) bits shifted out), it is loaded from write register (for software to be accessed via a ”Buffer Empty” interrupt status).

LBIT(4-0) Load Bits

Number of bits in aggregates of (LEN + 1) loaded into output shift register when ready, if LMOD = 1. The number of bits loaded is equal to (LBIT + 1) $\times$ (LEN + 1), the corresponding interrupt status is BEMP2. Since the number of bits is 32 maximum, the value of the product (LBIT + 1) $\times$ (LEN + 1) shall not exceed 32.

HXA Host Transmit Access

- 0 Channel originates from DSP
- 1 Channel originates from Host

HDLC Channel 1 Receive Path Register **Read/Write** **Address $201D_H$**

Value after reset: 00_H

SLIN(1-0)	Select Line	
	00	Channel on DU (frame sync FSC, clock DCL or DCL/2)
	01	Channel on DD (frame sync FSC, clock DCL or DCL/2)
	10	Channel on SR (frame sync RFS, clock SCLK)
	11	Channel on ST (frame sync TFS, clock SCLK)
LMOD(1-0)	Load Mode	
	00	When shift register contains one byte, it is loaded into HDLC receiver as soon as possible (and, in addition, to DSP/host read register for monitoring).
	XX	When shift register contains n bytes (XX = 01:n = 1; XX = 10:n = 2; XX = 11: n = 4), the contents is loaded into DSP and host read register, DSP or host (cf. HHR1 bit) write register is loaded into HDLC receive buffer, and read DSP or host read register is loaded into DSP or host write register (for software to be accessed via a “Buffer Full” interrupt status).
HHR	Host HDLC Receiver Access	
	0	DSP has access to modify HDLC receiver input (monitoring from host still possible).
	1	Host has access to modify HDLC receiver input (monitoring from DSP still possible).

HDLC Channel 1 Transmit Path Register **Read/Write** **Address $201E_H$**

Value after reset: 00_H

SLIN(1-0) Select Line

- 00 Channel on DU (frame sync FSC, clock DCL or DCL/2)
- 01 Channel on DD (frame sync FSC, clock DCL or DCL/2)
- 10 Channel on SR (frame sync RFS, clock SCLK)
- 11 Channel on ST (frame sync TFS, clock SCLK)

LMOD(1-0) Load Mode

- 00 When shift register is about to become empty, it (as well as DSP and Host read registers) is loaded from HDLC transmitter.
- XX When shift register contains n bytes (XX = 01:n = 1; XX = 10:n = 2; XX = 11: n = 4), the contents is loaded into DSP and host read register, DSP or host (cf. HHR bit) write register is loaded into HDLC receive buffer, and read DSP or host read register is loaded into DSP or host write register (for software to be accessed via a “Buffer Empty” interrupt status).

HHX Host HDLC Transmitter Access

- 0 DSP has access to modify HDLC transmitter output (monitoring of HDLC output from host still possible).
- 1 Host has access to modify HDLC receiver input (monitoring of HDLC output from DSP still possible).

HDLC Channel 2 Receive Path Register **Read/Write** **Address $201F_H$**

Value after reset: 00_H

SLIN(1-0)	Select Line	
	00	Channel on DU (frame sync FSC, clock DCL or DCL/2)
	01	Channel on DD (frame sync FSC, clock DCL or DCL/2)
	10	Channel on SR (frame sync RFS, clock SCLK)
	11	Channel on ST (frame sync TFS, clock SCLK)
LMOD(1-0)	Load Mode	
	00	When shift register contains one byte, it is loaded into HDLC receiver as soon as possible (and, in addition, to DSP/host read register for monitoring).
	XX	When shift register contains n bytes (XX = 01:n = 1; XX = 10:n = 2; XX = 11: n = 4), the contents is loaded into DSP and host read register, DSP or host (cf. HHR1 bit) write register is loaded into HDLC receive buffer, and read DSP or host read register is loaded into DSP or host write register (for software to be accessed via a “Buffer Full” interrupt status).
HHR	Host HDLC Receiver Access	
	0	DSP has access to modify HDLC receiver input (monitoring from host still possible).
	1	Host has access to modify HDLC receiver input (monitoring from DSP still possible).

HDLC Channel 2 Transmit Path Register **Read/Write** **Address 2020_H**

Value after reset: 00_H

SLIN(1-0)	Select Line	
	00	Channel on DU (frame sync FSC, clock DCL or DCL/2)
	01	Channel on DD (frame sync FSC, clock DCL or DCL/2)
	10	Channel on SR (frame sync RFS, clock SCLK)
	11	Channel on ST (frame sync TFS, clock SCLK)
LMOD(1-0)	Load Mode	
	00	When shift register is about to become empty, it (as well as DSP and Host read registers) is loaded from HDLC transmitter.
	XX	When shift register contains n bytes (XX = 01:n =1 ; XX = 10:n = 2; XX = 11: n = 4), the contents is loaded into DSP and .ost read register, DSP or .ost (cf. HHR bit) write register is loaded into HDLC receive buffer, and read DSP or .ost read register is loaded into DSP or .ost write register (for software to be accessed via a “Buffer Empty” interrupt status).
HHX	Host HDLC Transmitter Access	
	0	DSP has access to modify HDLC transmitter output (monitoring of HDLC output from host still possible).
	1	Host has access to modify HDLC receiver input (monitoring of HDLC output from DSP still possible).

Monitor Channel Configuration Register **Read/Write** **Address 2021_H**

Value after reset: 00_H

SLIN Select Line

0 Receive channel on DD, transmit channel on DU.

1 Receive channel on DU, transmit channel on DD.

MONCH(3-0) Monitor Channel position

Monitor channel (same time-slot for receive and transmit direction) located in the 3rd byte of multiplex MONCH (0 to 15).

Monitor Channel Control Register **Read/Write** **Address 2022_H**

Value after reset: 00_H

MRE Monitor channel Receive Enable

0: Receive monitor channnel inactive

1: Receive monitor channel active

MRC MR bit Control

0: No acknowledgement is sent in response to a received byte. When MRE = 1 and MRC = 0, only the first byte of a packet can received, further bytes (in the case that the first byte is acknowledged by another IC) are not loaded into MONR.

1: Acknowledgement via MR bit is enabled, acknowledgement takes place after MONR is read.

MXC Monitor Transmit Control

0: Transmit monitor channel inactive (high impedance)

1: Monitor channel transmission enabled

Monitor Channel Address (IC Identification) **Read/Write** **Address 2023_H**

Value after reset: 00_H

MAD Monitor Address
Latched at reset from lines AD(7-0) and programmable from host (if present) thereafter.

Monitor Channel Transmit/Receive Register Read/Write Address 2024_H

Value after reset: 00_H

MONX Monitor Transmit Register (write)
Value of monitor byte to be transmitted.

MONR Monitor Receive Register (read)
Value of received monitor channel byte. A read of this register enables the automatic acknowledgement of the received byte.

C/I Channel Mode Register Read/Write Address 2025_H

Value after reset: 00_H

CIEN1, 2 C/I Channel 1,2 Enable

0: Transmission of C/I channel disabled. (channel in high impedance).

1: Transmission of C/I channel enabled

AWK1, 2 Awake for C/I channel 1,2

0: C/I channel normal operation

1: A “low” is unconditionally sent on the line programmed for C/I transmit channel.

Note: When AWK is set to ‘1’ *the line (DD or DU) is immediately pulled low (non-synchronously with clock). When AWK is set to* ‘0’*, the line is “set free” only after the next rising edge of FSC is detected. One should avoid setting AWK to* ‘0’ *just when a rising edge on FSC is expected.*

C/I Channel 1, 2 Configuration Registers **Read/Write** **Address $2026_H/2027_H$**

Value after reset: 00_H

SLIN	Select Line	
	0	Receive channel on DD, transmit channel on DU.
	1	Receive channel on DU, transmit channel on DD.
CICH(3-0)	C/I Channel position	
	C/I channel (same time-slot for receive and transmit direction) located in the 4^{th} byte of multiplex CICH (0 to 15).	
CIL	C/I Channel Length	
	0:	4 bits
	1:	6 bits
DLL	Double Last Look	
	0:	No double last look
	1:	C/I channel change confirmed only after two consecutive identical values are received.

C/I Channel 1 Transmit/Receive Register **Read/Write** **Address 2029_H**

Value after reset: 00_H

CIX	C/I Channel Transmit Value of transmitted C/I channel
CIR	C/I Channel Receive (read) Value of received C/I channel

C/I Channel 2 Transmit/Receive Register **Read/Write** **Address $202A_H$**

Value after reset: 00_H

CIX	C/I Channel Transmit Value of transmitted C/I channel
CIR	C/I Channel Receive (read) Value of received C/I channel

IOM Configuration Register **Read/Write** **Address $202B_H$**

Value after reset: 00_H

CGEN	Clock Generation for IOM-2 interface (TE mode)	
	0	FSC and DCL are inputs (Reset value)
	1	FSC and DCL are outputs (DCL=1.536 MHz, FSC=8 kHz)
FODS	FSC/DCL Open Drain Select	
	0	FSC and DCL are push/pull (Reset value)
	1	FSC and DCL are open drain

PLL Configuration Register **Read/Write Address $202C_H$-$202D_H$**

Value after reset: 00_H

PU	Power Up for PLL	
	0	PLL is in power-down mode
	1	PLL is in power-up mode

General Purpose I/O Configuration Register **Read/Write** **Address 2030_H**

Value after reset: 00_H

IIOC(3-0)	I/O Line Configuration	
	0	pin GPx is open drain (with internal pull up registers)
	1	Pin GPx is push/pull

General Purpose I/O Data Direction Register **Read/Write** **Address 2031_H**

Value after reset: 00_H

IIOD(3-0) I/O Line Direction

0 pin GPx is input

1 Pin GPx is output

General Purpose I/O Data Register **Read/Write** **Address 2032_H**

Value after reset: 00_H

IIOR(3-0) I/O Line Data

In a **write access** to GPR the value will stored in the GPR. For those ports which are configured as output the value is driven on the corresponding pin GPx. As a consequence, GPR can be initialized even before the coressponding pin is configured as output.
A **read access** to GPR will return the current status on the pin GPx, independent of whether the pin GPx is configured as input or output.

General Purpose I/O Strobe Register **Read/Write** **Address 2033_H**

Value after reset: 00_H

IIOS(3-1) I/O Strobe Select

0 input pin GPx is not strobed

1 input pin GPx performes strobed operation

IIOS0 I/O Strobe Mode

0 strobe mode is disabled. GP0 is used as general I/O pin

1 strobe mode is selected (only valid if GP0 is configured as input).

If strobed operation is disabled, the input pins are sampled continuously.
If strobed is selected, input pins are latched during GP0 = 0. The latch is closed when GP0 = 1

General Purpose Interrupt Status Register **Read** **Address 2034_H**

Value after reset: 00_H

IOINTS(3-0) Input Interrupt Status Register

0 no state change is detected on pin GPx

1 a state change (0-1 or 1-0) is detected on pin GPx.

A maskable interrupt from any of the GPx pins is generated to the host if the GPI-mask bit in register 74_H is enabled.

General Purpose Interrupt Mask Register **Read/Write** **Address 2035_H**

Value after reset: 00_H

IIOINTM(3-0) Input Interrupt Mask Register

0 a “1” in IOINTSx does not generate an INT1 to the DSP

1 a “1” in IOINTSx generates an INT1 to the DSP

5.4 HDLC Controller Registers

As mentioned previously, the addresses for the HDLC registers are given here for the DSP for completeness only, since they are only relevant for the on-chip firmware.

The access to the register banks of the two HDLC controllers is determined by the “HDLC Controller Access from Host” bits HAH1 (for HDLC1) and HAH2 (for HDLC2):

– When HAHx is 0, the DSP is allowed to access the HDLC register bank, and thus to service the HDLC controller.
– When HAHx is ‘1’, the host is allowed to service the HDLC controller.

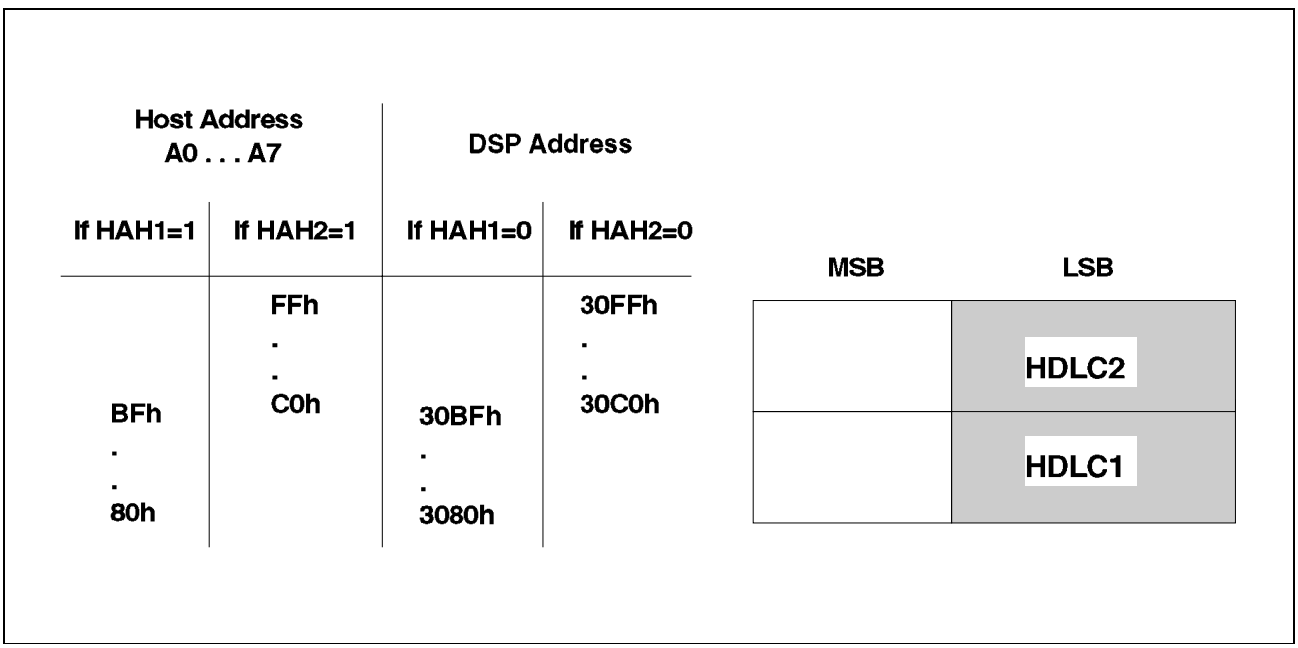


Figure 38

In the following tables the addresses are relative to the base address 80_H (HDLC1) or $C0_H$ (HDLC2). In each row, the upper line lists the read values, the lower the write values of the corresponding register.

Table 17

Byte Address Offset	Read Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00_H . . $1F_H$	RFIFO XFIFO								
20_H	STAR XCMD	XDOV XF	XFW XME	XCEC XRES	RCEC XNEW	BSY -	RNA -	STR -	STX STX
21_H	RSTA -	VFR -	RDO -	CRC -	RAB -	- -	- -	- -	- -
22_H	MODE MODE	TMO TMO	RAC RAC	XAC XAC	TLP TLP		- -	ERFS ERFS	ETFS ETFS
23_H	- -	- -	- -	- -	- -	- -	- -	- -	- -
24_H	RBCH -	OV -	RBC14 -	RBC13 -	RBC12 -	RBC11 -	RBC10 -	RBC9 -	RBC8 -
25_H	RBCL RCMD	RBC7 RMC	RBC6 RRES	RBC5 RMD	RBC4 -	RBC3 -	RBC2 -	RBC1 STR	RBC0 -
26_H	CCR0 CCR0	PU PU	ITF ITF	C32 C32	CRL CRL	RCRC RCRC	XCRC XCRC	RMSB RMSB	XMSB XMSB
27_H	CCR1 CCR1	RCS0 RCS0	RSCO RSCO	RFDIS RFDIS	XCS0 XCS0	TSCO TSCO	XFDIS XFDIS	- -	- -
28_H	TSAR TSAR	TSR5 TSR5	TSR4 TSR4	TSR3 TSR3	TSR2 TSR2	TSR1 TSR1	TSR0 TSR0	RCS2 RCS2	RCS1 RCS1
29_H	TSAX TSAX	TSX5 TSX5	TSX4 TSX4	TSX3 TSX3	TSX2 TSX2	TSX1 TSX1	TSX0 TSX0	XCS2 XCS2	XCS1 XCS1
$2A_H$	RCCR RCCR	RCC7 RCC7	RCC6 RCC6	RCC5 RCC5	RCC4 RCC4	RCC3 RCC3	RCC2 RCC2	RCC1 RCC1	RCC0 RCC0
$2B_H$	XCCR XCCR	XCC7 XCC7	XCC6 XCC6	XCC5 XCC5	XCC4 XCC4	XCC3 XCC3	XCC2 XCC2	XCC1 XCC1	XCC0 XCC0
$2C_H$	ISR IMR	RME RME	RPF RPF	RFO RFO	XPR XPR	XDU XDU	ALLS ALLS	- -	- -

Unless otherwise indicated, all register bits are initialized to ‘0’ after a hardware reset.

During the initialization phase the firmware does a re-programming on the following registers of the HDLC1 controller to setup the default configuration for the communication with a video-processor (see **Chapter 6.2.3.3**):

Table 18

Address	Data	Description
$30A2_H$	80_H	Transparent Mode
$30A5_H$	40_H	Receiver Reset
$30A6_H$	83_H	Power Up, MSB first for Receiver and Transmitter
$30AA_H$	$0F_H$	Receiver: 16 bit time-slot
$30AB_H$	$0F_H$	Transmitter: 16 bit time-slot
$30AC_H$	50_H	Interrupt Enable for RPF and XPR

When read, register bits that are not in use (or reserved for future use) are not defined, i.e. their value may be either ‘0’ or ‘1’.

Receive FIFO RFIFO Read Address 00-1F$_H$

The HDLC receive FIFO size is 2×32 bytes. One half of the FIFO is connected to the receiver shift register while the second half is accessible to the controlling processor. The least significant 5 bits of the address are not decoded for the FIFO access, thus always the same address may be used to read out the FIFO contents. With the first read access the first byte from the FIFO will be read, with the second read access the second byte and so on. A random access to the FIFO contents is not possible.

Transmit FIFO XFIFO Write Address 00-1F$_H$

The transmit FIFO size is 2×32 bytes. One half is connected with the transmit shift register while the other half is accessible to the controlling processor. The least significant 5 bits of the address are not decoded for the FIFO access, thus always the same address may be used to write to the FIFO. With the first write access the first byte is written to the FIFO, with the second write access the second byte and so on. A random access to the FIFO is not possible.

Status Register STAR Read Address 20_H

	Bit 7							Bit 0
STAR	XDOV	XFW	XCEC	RCEC	BSY	RNA	STR	STX

XDOV Transmit Data Overflow
Indicates that more than 32 bytes have been written into the transmit FIFO.
Set: In the write cycle of the 33 byte.
Reset: After reading STAR register, XRES or hardware reset.

XFW Transmit FIFO Write Enable
Data can be entered into the transmit FIFO.
Set: After the XF command execution has been finished, after XRES, after hardware reset.
Reset: After XF command has been given.

XCEC Transmitter Command Executing
If '1', a command is currently executed by the transmitter and no further command may be written into the XCMD register. When '0', a new command may be entered into XCMD.
Set: After a new command has been written to the XCMD register (with the rising edge of $\overline{WR}$).
Reset: After the new command has been executed, after hardware reset.

RCEC Reveiver Command Executing
If '1', a command is currently executed by the receiver and no further command may be written into the RCMD register. When '0', a new command may be entered into RCMD.
Set: After a new command has been written to the RCMD register (with the rising edge of $\overline{WR}$).
Reset: After the new command has been executed, after hardware reset.

BSY Busy state in the receive channel
A '0' indicates an "idle" state.
Set: After a '0' has been received, after RRES, after hardware reset.
Reset: After 15 consecutive ones have been received.

RNA Receive channel Not Active
Indicates whether flags/frames are being received on the line (0) or not (1).
Set: After 7 consecutive ones are received on the line.
Reset: After each received 0, after RRES, after hardware reset.

STR Status of generation of RFS pulses
Only valid when RFIN = 0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register is ‘0’.
A ‘1’ indicates that generation of pulses as a result of a previous STR command is still on-going.
This function may be used in connection with the HDLC controller when a predefined number of data units (e.g. words) are received, clocked by RFS pulses.
Set: With the rising edge of the first RFS pulse being generated.
Reset: 16 bit periods after the last RFS pulse, after hardware reset.

STX Status of generation of TFS pulses
Only valid when TFIN = 0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register = 0.
A ‘1’ indicates that generation of pulses as a result of a previous STX command is still on-going; STX is reset to ‘0’ 16 bit periods after the last TFS pulse has been generated.
This function may be used in connection with the HDLC controller when a predefined number of data units (e.g. words) are to be transmitted, clocked by TFS pulses.
Set: With the rising edge of the first TFS pulse being generated.
Reset: 16 bit periods after the last TFS pulse, after hardware reset.

Transmit Command Register XCMD (Write) Address 20_H

	Bit 7							Bit 0
XCMD	XF	XME	XRES	XNEW				STX

XF Transmit Frame
Initiates transmission of a pool of data (up to 32 bytes). The XFIFO is write protected. When the non-accessible part is empty, the contents of the accessible part is copied to the non-accessible part, an XPR interrupt status is generated and the accessible part is again writable from the DSP or host (determined by HAHx bit).

XME Transmit Message End
Indicates that after the transmission of data from the FIFO pool, the frame is to be closed with a CRC checksum (programmable) and a closing flag. Can be set together with XF or as a reaction to the XPR interrupt generated after the XF for the last FIFO. See **Chapter 4.3** for details.
Has no meaning in transparent mode.

XRES Transmitter Reset
When XAC = 1, this command resets the HDLC transmitter, clears the transmit FIFO, aborts any HDLC frame being transmitted and generates an XPR status after the command has been completed.
When XRES is issued while XAC = 0, this command initializes in addition the time-slot count logic for this channel.

XNEW Transmitter Restart
When set to ‘1’ during the transmission of the first FIFO (including the start flag) the transmitter state machine is reset to the starting state without any loss of data (i.e. FIFO data). XAC is reset to ‘0’ automatically. When XAC is reprogrammed to ‘1’, the transmission of the current frame is restarted with the first bit of the start flag.

STX Start command for TFS generation
Only valid when TFIN = 0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register is ‘0’.
When TCONT = 0, when STX is set, exactly TREP(9-0) pulses of one bit duration and spaced 16 bit periods from each other are generated. When STX command is given, generation of pulses starts at the next possible 16-bit boundary.
This function may be used in connection with the HDLC controller when a predefined number of data units (e.g. words) are transmitted, clocked by TFS pulses.

Receive Status Register RSTA Read Address 21_H

	Bit 7							Bit 0
RSTA	VFR	RDO	CRC	RAB				

This byte is the same as the byte appended in the RFIFO to the last byte (or CRC) of the frame. The value is updated after the end flag has been received and before RSTA is written to the RFIFO and RME interrupt status is generated.

The status register is completely reset with every start flag. Thus, the DSP/host should always use the RSTA value from the RFIFO to evaluate the status at the end of the corresponding frame, since the register contents does not necessarily refer to the current frame being read from the RFIFO.

Has no meaning in transparent mode.

VFR Valid Frame
Indicates whether the frame length is valid (1) or not (0).
Set: If the frame length (transparent data without zero insertion) is a multiple of 8 bits and the frame contains at least 16 bits.
Reset: All other frame lengths, with every new start flag

RDO Receive Data Overflow
At least one byte of the frame has been lost because it could not be stored in the FIFO.
Set: When one byte of frame data is available from the HDLC bitengine but cannot be stored in the RFIFO because it's full.
Reset: With every new start flag

CRC CRC check
Correct (1) or incorrect (0). The value is updated after the end flag has been received and before RSTA is written to the RFIFO and RME interrupt status is generated.
Set: CRC correct
Reset: CRC incorrect, with every new start flag

RAB Receive Message Aborted
Frame aborted by the remote station (7 consecutive '1's received), yes (1) or no (0).
Set: After 7 consecutiv '1's have been received
Reset: With every new start flag

Mode Register **MODE** **Read/Write** **Address 22_H**

	Bit 7							Bit 0
MODE	TMO	RAC	XAC	TLP			ERFS	ETFS

TMO Transparent Mode
A ‘1’ selects the transparent non-HDLC mode, where no HDLC framing functions are implemented. In transparent mode, data reception and transmission is started time-slot aligned.

RAC Receiver Active
Sets the receiver in an active state, where the receiver goes into the hunt mode [1)] (see **page 131**).
In transparent mode, when RAC is set to ‘1’, storage of bytes in the receive FIFO starts time-slot aligned.

XAC Transmitter Active
When ‘1’, the HDLC transmitter transmits on the line and in the time-slot assigned to it (interframe time-fill if no data is available). When XAC = 0, the time-slot assigned to the transmitter is in high impedance.
In transparent mode, when XAC is set to ‘1’, transmission of bytes from the transmit FIFO starts time-slot aligned.

TLP Test Loop
When ‘1’, output of the HDLC controller is connected to input (i.e. what is transmitted is simultaneously received). The loop is transparent.

ERFS Enable RFS generation
Only valid when RFIN = 0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register is ‘1’.
When RCONT = 1, an ERFS value of ‘1’ enables the generation of RFS pulses of one bit duration and spaced RPRD + 1 (1, ..., 32) 16-bit words from each other. Pulses are generated indefinitely until ERFS is set to ‘0’ again.

ETFS Enable TFS generation
Only valid when TFIN=0 (TFS pulses internally generated) and used if TCONT bit in TFS mode register is ‘1’.
When TCONT = 1, an ETFS value of ‘1’ enables the generation of TFS pulses of one bit duration and spaced TPRD + 1 (1, … , 32) 16-bit words from each other. Pulses are generated indefinitely until ETFS is set to ‘0’ again.

Receive Byte Count High RBCH Read Address 24_H

	Bit 7							Bit 0
RBCH	OV	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8

Receive Byte Count Low RBCL Read Address 25_H

	Bit 7							Bit 0
RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

OV Overflow
A ‘1’ indicates a frame at least 32.768 bytes long. Despite the overflow, the RBC(14-0) counter continues counting.
Set: When RBC(14-0) counter reaches 32.768.
Reset: After RRES, after hardware reset, with the last RMC (after RME)

RBC Receive Byte Count
Length of received frame (including status and CRC bytes). The register contents are valid after an RME interrupt status. RBC4-0 indicate the number of valid bytes currently in the DSP/host accessible part of RFIFO. Reset with the last RMC (after RME).

Receive Command Register RCMD Write Address 25_H

	Bit 7							Bit 0
RCMD	RMC	RRES	RMD				STR	

RMC Receive Message Complete
Acknowledges a previous RPF or RME status. Frees the FIFO pool for the next received frame or part of a frame.
Although the interrupt status register (ISR) is automatically reset after read, the RMC must be given in response to an RPF or RME interrupt to free the FIFO.
The FIFO is not considered to be free, even if completely read. The read on the FIFO can be done cyclically several times.

RRES Receiver Reset
When RAC = 1, this command resets the HDLC receiver, clears the receive FIFO and aborts any HDLC frame being received.
When RRES is issued while RAC = 0, this command initializes in addition the time-slot count logic for this channel.

RMD Receive Message Delete
Reaction to an RPF interrupt. The remaining part of the frame is to be ignored by the receiver (which goes into the hunt mode[1)] (see **page 131**) starting in the DSP/host inaccessible part of RFIFO); the receive FIFO is cleared of that frame.

STR Start command for RFS generation
Only valid when RFIN = 0 (RFS pulses internally generated) and used if RCONT bit in RFS mode register = 0.
When RCONT = 0, when STR is set, exactly RREP(9-0) pulses of one bit duration and spaced 16 bit periods from each other are generated. When STR command is given, generation of pulses starts at the next possible 16-bit boundary.
This function may be used in connection with the HDLC controller when a predefined number of data units (e.g. words) are received, clocked by RFS pulses.

Channel Configuration Register 0 CCR0 Read/Write Address 26_H

	Bit 7							Bit 0
CCR0	PU	ITF	C32	CRL	RCRC	XCRC	RMSB	XMSB

PU Power Up
Power down (0) or power up (1).

ITF Interframe Time-Fill
If ‘0’, idle (continuous logical 1) is transmitted when no frame is sent; continuous flag sequences, otherwise.
Has no meaning in transparent mode (where “idle” is always sent in the absence of data).

C32 Enable CRC-32
A ‘1’ selects the 32-bit CCITT-32 frame check sequence, as opposed to the 16-bit frame check sequence.
Has no meaning in transparent mode.

CRL CRC Reset Level
Defines the initialization for the internal receive and transmit CRC generators: A ‘0’ initializes the generators to (FFFF)FFFF$_H$, a ‘1’ to (0000)0000$_H$. Has no meaning in transparent mode.

RCRC Receive CRC On/Off
When ‘1’, the received CRC checksum is written to RFIFO. The checksum, consisting of last 2 (or 4) bytes in the received frame, is followed in the RFIFO by the status information byte (copied into RSTA register). Independently of RCRC the received checksum will be checked for correctness. RBCL/H include the CRC byte(s).
Has no meaning in transparent mode.

XCRC Transmit CRC On/Off
When ‘1’, the CRC checksum in transmit direction is not generated automatically. It has to be written as the last 2 or 4 bytes in XFIFO.
Has no meaning in transparent mode.

RMSB Receive MSB first
When RMSB = 0, the least significant bit of a byte in the receive FIFO is the bit first received (normal mode in HDLC/serial data communication protocols).
When RMSB = 1, the most significant bit of a byte in the receive FIFO is the first bit received.

XMSB Transmit MSB first
When XMSB = 0, the least significant bit of a byte in the transmit FIFO is the bit first transmitted (normal mode in HDLC/serial data communication protocols).
When XMSB = 1, the most significant bit of a byte in the transmit FIFO is the first bit transmitted.

Channel Configuration Register 1 CCR1 Read/Write Address 27_H

	Bit 7							Bit 0
CCR1	RCS0	RSCO	RFDIS	XCS0	TSCO	XFDIS		

RCS0 Receive Clock Shift 0
Together with RCS2 and RCS1 in TSAR, determines the clock shift relative to the frame synchronization signal. A clock shift of 0...7 is programmable.

RSCO Receive Time-Slot Continuous
When RSCO is equal to one, the time-slot capacity (normally given by register RCCR, between 1 and 256 bits) is “infinity”. This means that the time-slot will be always “active” so that data can be permanently received if RAC = 1.
If RFDIS = 0, and if the time-slot count logic has been reset (by issuing RRES while RAC = 0), time-slot logic can start operation and thus “activate” a time-slot only after the first frame sync pulse is detected (i.e. on FSC, RFS, or TFS, whichever has been selected). The time-slot offset register TSAR + bit RCS0 mark the instant when the “infinite” time-slot will be activated after the first frame sync pulse has occurred. If RFDIS = 1, reception can start immediately, without the necessity to wait for the first frame sync pulse.

RFDIS Receive Frame Sync Disregard
When RFDIS is ‘1’, the time-slot generation logic disregards frame syncs. In particular, if RFDIS = 1, receive time-slot is immediately considered as permanently “active”, and remains activated as long as this condition prevails, independent of RSCO.

XCS0 Transmit Clock Shift 0
Together with XCS2 and XCS1 in TSAX, determines the clock shift relative to the frame synchronization signal. A clock shift of 0...7 is programmable.

TSCO Transmit Time-Slot Continuous
When TSCO is equal to one, the time-slot capacity (normally given by register XCCR, between 1 and 256 bits) is “infinity”. This means that the time-slot will be always “active” so that data can be permanently transmitted if XAC = 1.
If TFDIS = 0, and if the time-slot count logic has been reset (by issuing XRES while XAC = 0), time-slot logic can start operation and thus “activate” a time-slot only after the first frame sync pulse is detected (i.e. on FSC, RFS, or TFS, whichever has been selected). The time-slot offset register TSAX + bit XCS0 mark the instant when the “infinite” time-slot will be activated after the first frame sync pulse has occurred. If TFDIS = 1, transmission can start immediately, without the necessity to wait for the first frame sync pulse.

TFDIS Transmit Frame Sync Disregard
When TFDIS is ‘1’, the time-slot generation logic disregards frame syncs. In particular, if TFDIS = 1, transmit time-slot is immediately considered as permanently “active”, and remains activated as long as this condition prevails, independent of TSCO.

Time-Slot Assignment Receive TSAR Read/Write Address 28_H

	Bit 7							Bit 0
TSAR	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0	RCS2	RCS1

TSR Time-Slot Receive
Selects one of up to 64 possible time-slots (00_H-$3F_H$) in which data is received. TSR gives the location of the time-slot in octets (granularity = octet). The bits RCS(2-0) give the exact starting point of the time-slot with one-bit precision. In other words, the time-slot position with respect to the frame sync is given by (TSR $\times$ 8 + RCS). The length of the time-slot is given by RCC(7-0).

RCS Receive Clock Shift
Together with RCS0, RCS1 and RCS2 mark the start of the time-slot with one-bit granularity.

Time-Slot Assignment Transmit TSAX Read/Write Address 29_H

	Bit 7							Bit 0
TSAX	TSX5	TSX4	TSX3	TSX2	TSX1	TSX0	XCS2	XCS1

TSX Time-Slot Transmit
Selects one of up to 64 possible time-slots (00_H-$3F_H$) in which data is transmitted. TSX gives the location of the time-slot in octets (granularity = octet). The bits XCS(2-0) give the exact starting point of the time-slot with one-bit precision. In other words, the time-slot position with respect to the frame sync is given by (TSX $\times$ 8 + XCS). The length of the time-slot is given by XCC(7-0).

XCS Transmit Clock Shift
Together with XCS0, XCS1 and XCS2 mark the start of the time-slot with one-bit granularity.

Receive Channel Capacity Register RCCR Read/Write Address $2A_H$

	Bit 7							Bit 0
RCCR	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0

RCC Receive Channel Capacity
Defines the number of bits in the receive time-slot.
Number of bits = RCC + 1 (1...256 bits/time-slot).

Transmit Channel Capacity Register XCCR Read/Write Address $2B_H$

	Bit 7							Bit 0
XCCR	XCC7	XCC6	XCC5	XCC4	XCC3	XCC2	XCC1	XCC0

XCC Transmit Channel Capacity
Defines the number of bits in the transmit time-slot.
Number of bits = XCC + 1 (1...256 bits/time-slot).

Interrupt Status Register ISR Read **Address $2C_H$**

	Bit 7							Bit 0
ISR	RME	RPF	RFO	XPR	XDU	ALLS		

RME Receive Message End
One complete frame of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte. No RPF is generated in this case. The number of bytes stored is given by RBC bits 0-4. Has no meaning in transparent mode.
Set: When the last part of a frame has been transferred to the DSP/host accessible part of RFIFO.
Reset: After ISR is read, after RRES, after hardware reset.

RPF Receive Pool Full
32 bytes of a frame have arrived in the receive FIFO. The frame has not yet been completely received. In transparent mode, signifies that 32 bytes can be read from the FIFO.
Set: When a part of a frame (but not the last part) has been transferred to the DSP/host accessible part of RFIFO.
Reset: After ISR is read, after RRES, after hardware reset.

RFO Receive Frame Overflow
Indicates that a frame has been lost because the FIFO was full at the reception of the beginning of a frame. In transparent mode, signifies that data has been lost because no room was available in RFIFO.
Set: The DSP/host inaccessible part of RFIFO is full and the beginning of a new frame is detected.
Reset: After ISR is read, after RRES, after hardware reset.

XPR Transmit Pool Ready
One data block may be entered into the transmit FIFO.
Set: After XF command has been executed and after XRES.
Reset: After ISR is read, after hardware reset.

XDU Transmit Data Underrun
Transmitted frame was terminated with an abort sequence because no data was available in the transmit FIFO and yet no XME command has been issued.
In transparent mode indicates the transmission has been stopped because no data was available in the transmit FIFO.
Set: When the HDLC bitengine requests new data from an empty XFIFO.
Reset: After ISR is read, after XRES, after hardware reset.

ALLS All Sent
When ‘1’, indicates that the last bit of a frame has been transmitted on the line and that both XFIFO parts are empty (in either HDLC or transparent mode).
Set: When the last bit of a frame has been transmitted to the line.
Reset: After ISR is read, after XRES, after hardware reset.

All ISR bits are acknowledged when ISR is read.

Interrupt Mask Register **IMR** **Write** **Address $2C_H$**

A ‘0’ in a bit position (status after reset) masks the corresponding bit in ISR.

	Bit 7							Bit 0
IMR	RME	RPF	RFO	XPR	XDU	ALLS		

1) “Hunt Mode”: The HDLC-receiver hunts for flags which are not followed by another flag or an abort sequence. Thus, the HDLC-receiver of the JADE will receive two frames correctly if they are separated by only one common flag (shared flag). It will also receive two frames correctly if they are separated by two flags (back-to-back frames). In case of a back-to-back frame the flags may share the ‘0’ or not.

6 Firmware Features

The JADE internal firmware starts automatically after a hardware reset.

Note: After a hardware reset, the JADE firmware needs to initialize its internal memories and interfaces. The time to do this is less than 10 ms. The user must take care to access the JADE only after this initialization phase is completed, i.e. 10 ms after the hardware reset.

In the initialization phase, the JADE will re-program some of the internal registers (see **Chapter 5.3** and **Chapter 5.4**). The default interface configuration is described in **Chapter 6.2.3.3**.

After the initialization phase is completed, the JADE can be started in the default mode or be reprogrammed and then started.

Note: The firmware features are using interrupt handshakes via the registers INH (Host write to 50_H) and IND (Host read from 58_H). A polling host should not directly poll the IND interrupt status register 58_H, but the DINT bit in INT# interrupt status register 75_H. This bit always shows whether an interrupt from the DSP has been generated or not, independently of the corresponding mask register. The mask register only decides whether an interrupt at INT# line is generated. After having recognized an IND interrupt status, the polling host may read out the register 58_H to get the interrupt number.

6.1 Basic Functions

6.1.1 Firmware Version Number

To obtain the version number of the on-chip firmware, the following interrupt handshake procedure has to be implemented by a host:

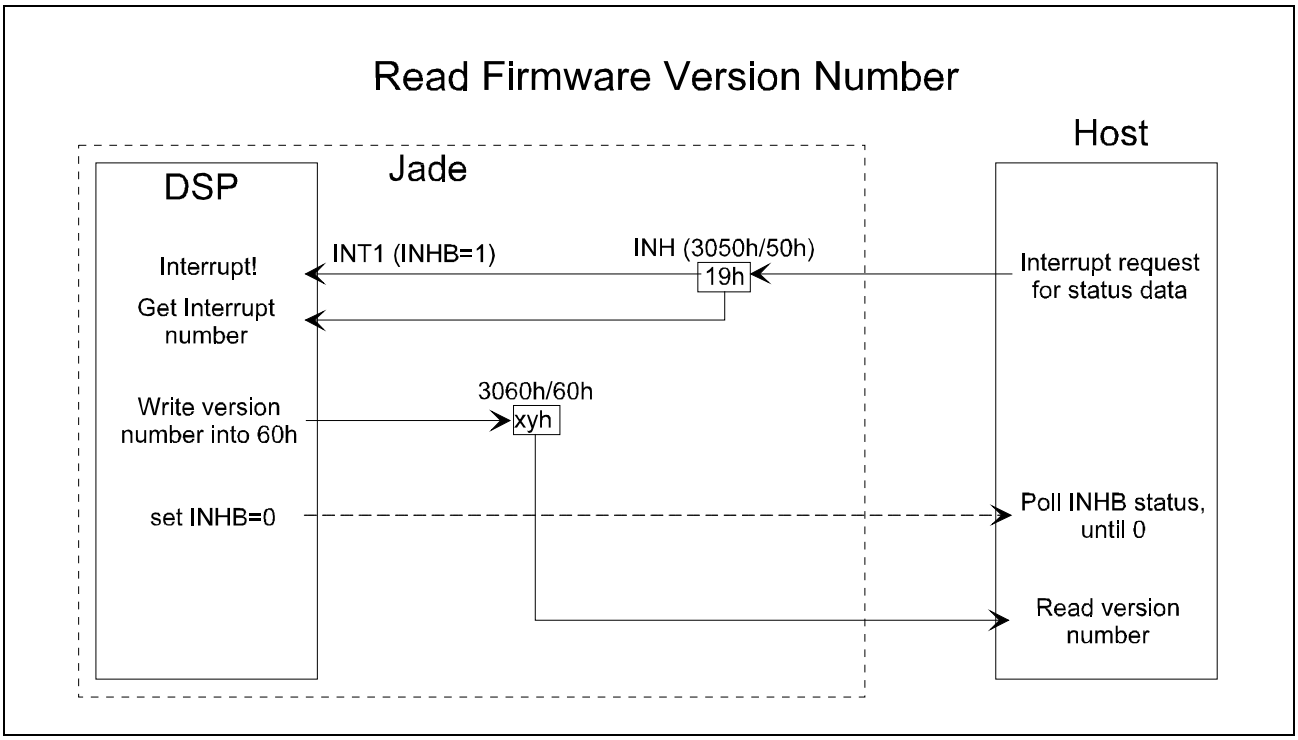


Figure 39

The following steps are executed:

1. The host generates an interrupt to the JADE by writing value 19_H into INH interrupt status register at address 50_H.
2. The JADE writes the firmware version number into communication register accessible from the host at address 60_H and resets the INHB bit to 0.
3. The host checks the INHB bit and as soon as it reads a '0' it may get the version number from register 60_H.

The version number of JADE 3.1 is (for historical reasons) 23_H, so the "xy_H" in the picture above has to be substituted by this number.

Note: The INHB=0 polling is not supported in some previous JADE versions (older than JADE 2.2 and JADE MM 1.2). Thus, if also these versions need to be identified by reading the version number, this can be obtained by waiting for 1 msec instead of polling the INHB=0 condition. For the JADE versions supporting the INHB=0 it is ensured that the INHB=0 condition becomes true in less than 1 msec.

6.1.2 Software Reset

A software reset (see **Figure 40**) is used to re-initialize the JADE without resetting the hardware. This means that e.g. not the whole configuration/control register area is reset, but only the firmware initialization (see **Chapter 5.3** and **Chapter 5.4**) is executed.

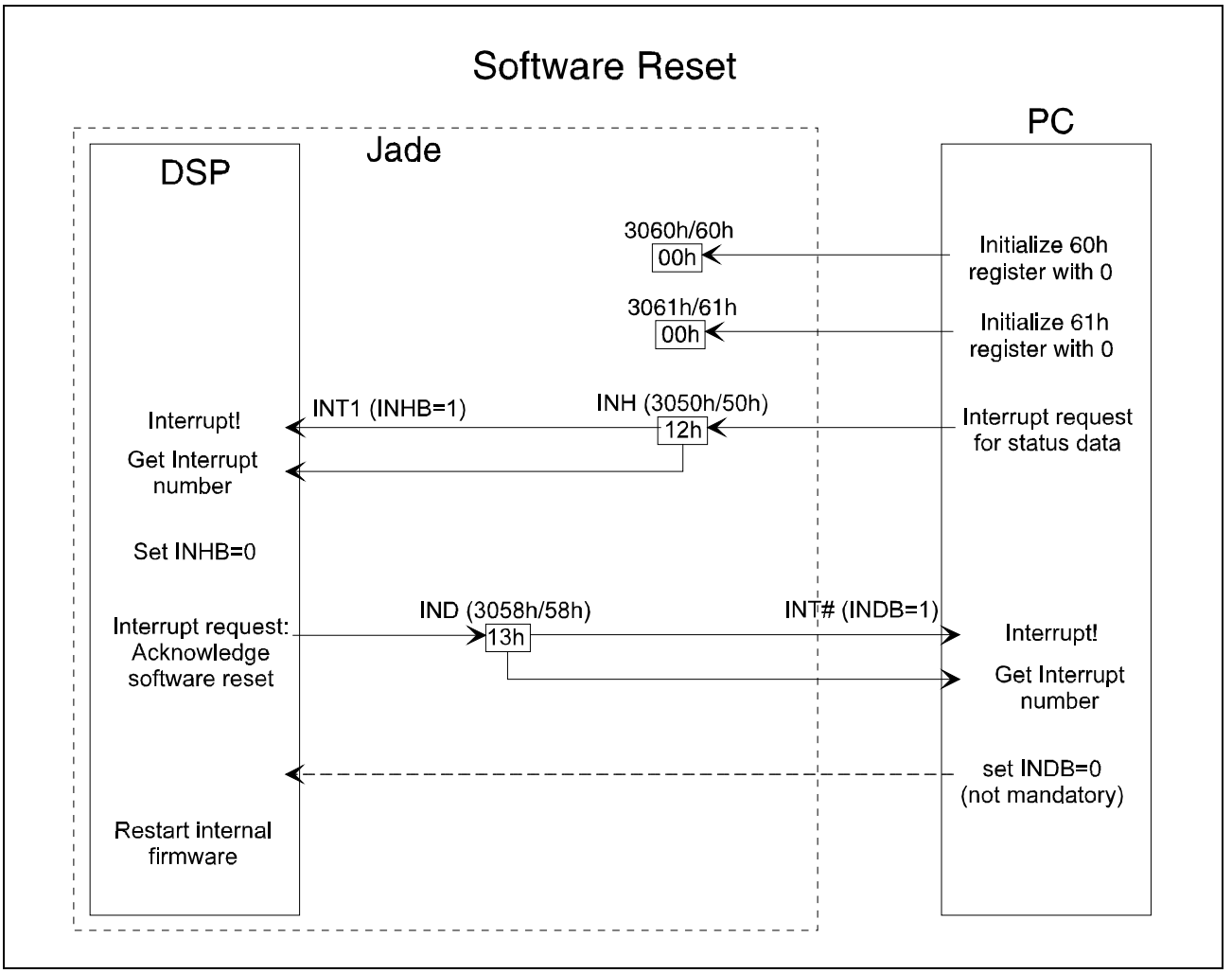


Figure 40

The following steps are executed:

1. The host initializes the control registers 60_H and 61_H by writing a '0' into it.
2. The host generates an interrupt to the JADE by writing value 12_H into INH interrupt status register at address 50_H.
3. The JADE resets the INHB bit and acknowledges the reception by generating an interrupt at $\overline{INT}$ line to the host by writing a value 13_H into IND interrupt status register at address 58_H.
4. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.
5. The JADE restarts its internal firmware beginning with the initialization phase.

For the restart of the internal firmware the JADE needs the same initialization time like after a hardware reset. So, the user should wait for 10 ms before it accesses the JADE again.

6.1.3 Power Down Command

In case the JADE is not currently needed in the system, the device can be powered down. Two options exists, one power-down including the PLL and one excluding it. These options are selected via the contents of the control register 60_H. A non-zero value leaves the PLL powered-up while the rest of the JADE goes power-down and a zero value in register 60_H includes the PLL in the power-down sequence and therefore is a complete power-down of the chip.

The power-up is triggered by one of the following interrupts: GPIO, Host interrupt and C/I channel interrupt.

The sequence to power-down the device is as follows:

1. The host initializes the control registers 60_H by writing a ‘0’ or a non-zero value into it (PLL included or excluded, see above).
2. The host generates an interrupt to the JADE by writing value 37_H into INH interrupt status register at address 50_H.
3. The JADE resets the INHB bit. There is no further acknowledge to this interrupt since the JADE will go to power-down almost immediately.
4. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.
5. The JADE firmware disables the CLKO pin, the PLL as selected and the DSP and can be woken up by any of the above mentioned interrupts. If the PLL was powered down, it takes longer to resume normal operation. If the PLL remained powered up, the firmware is immediately ready for resuming operation.

6.2 Audio Interfaces

In order to cover a wide range of applications, the JADE offers a variety of different interface combinations and protocols for the uncompressed/compressed data exchange.

The basic interfacing is like in **Figure 41**.

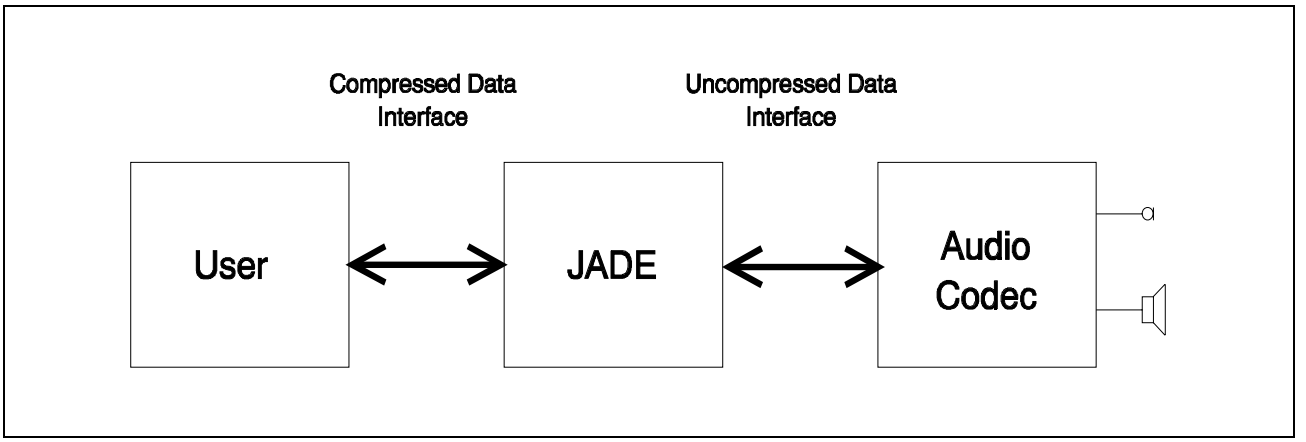


Figure 41

Two interfaces are necessary, one for compressed audio connected to a User and one for uncompressed audio connected to a Codec.

By switching the compressed/uncompressed data stream to different hardware interfaces (Host, IOM, Serial Audio Interface), the JADE is able to support standalone solutions using a video processor (compressed data provided on Serial Audio Interface) as well as host systems (e.g. software video coders using the host interface for the compressed data) or offline audio compression (compressed and uncompressed audio exchanged through host interface).

See **Figure 42** for the firmware layer structure and the corresponding structure of the description:

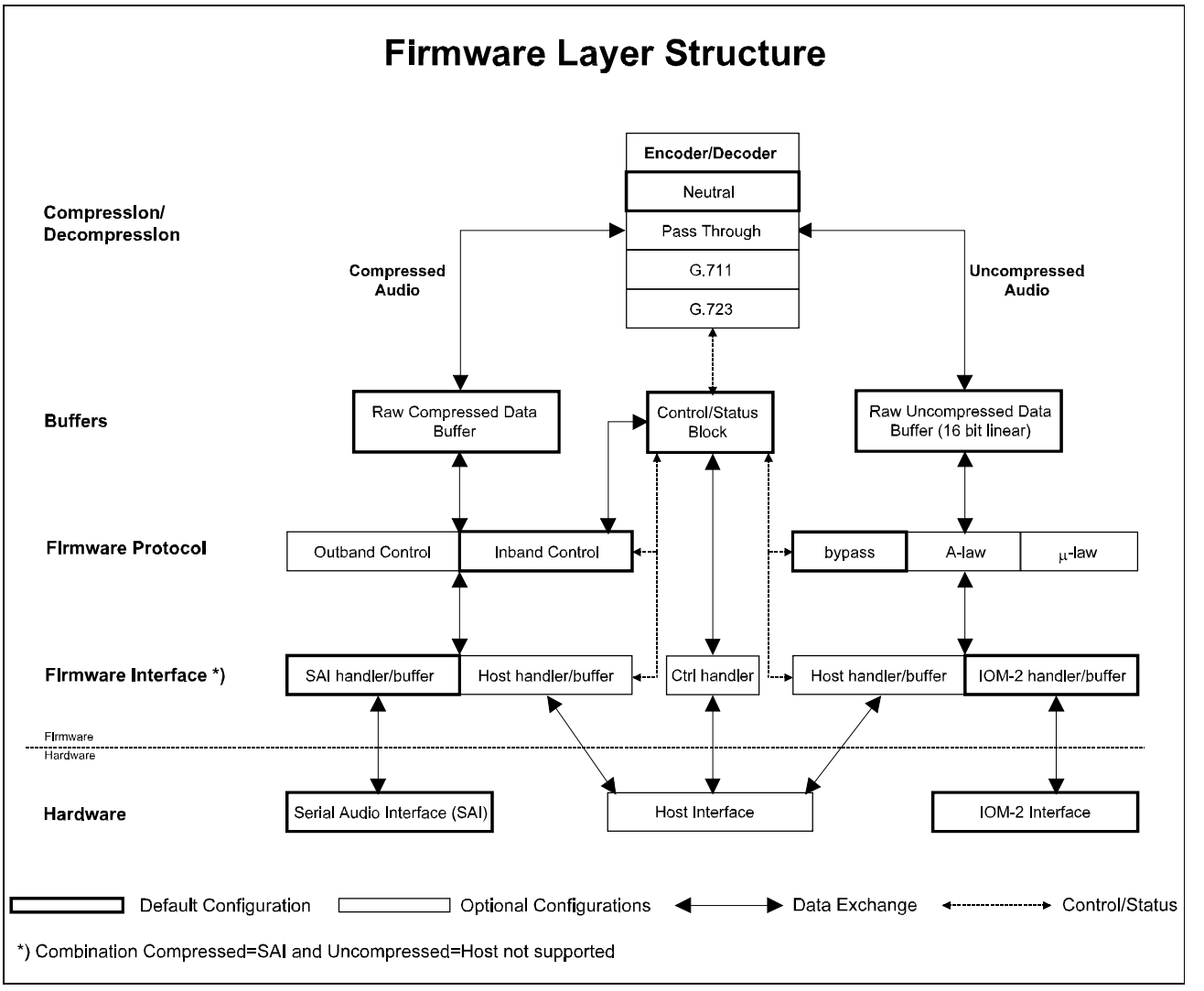


Figure 42

The audio interface description is split up into two basic parts: In the first part the protocol (data format, data packet size) and mode control (inband or outband) are described (**Chapter 6.1.2** and **Chapter 6.1.3**) which are independent of the selected hardware-interface combination, in the second part the individual timings and handshake procedures for the selected hardware-interface combination are described (**Chapter 6.2.3**).

6.2.1 Compressed Audio Protocols and Control of JADE

In the following sections the protocols for the exchange of compressed audio data between the JADE and a user are described.

6.2.1.1 Outband Control of JADE

All times that are given in this chapter refer to realtime processing of a 10 ms frame length of the audio data, which is the default setting of the JADE. When doing offline processing (compressed and uncompressed data exchanged through the host), the delay times in this chapter have to be substituted by the corresponding number of frames. For example, a delay time of 30 ms corresponds to three frames of audio data exchange when doing offline processing.

The host may change the JADE operating mode by sending a command block, and the JADE will send back a status block, if requested by the host. Command and status blocks consist of 8-bit words.

To exchange command and status blocks, the host initiates an interrupt handshake procedure.

See **Figure 43** for the host writing a new control block to the JADE:

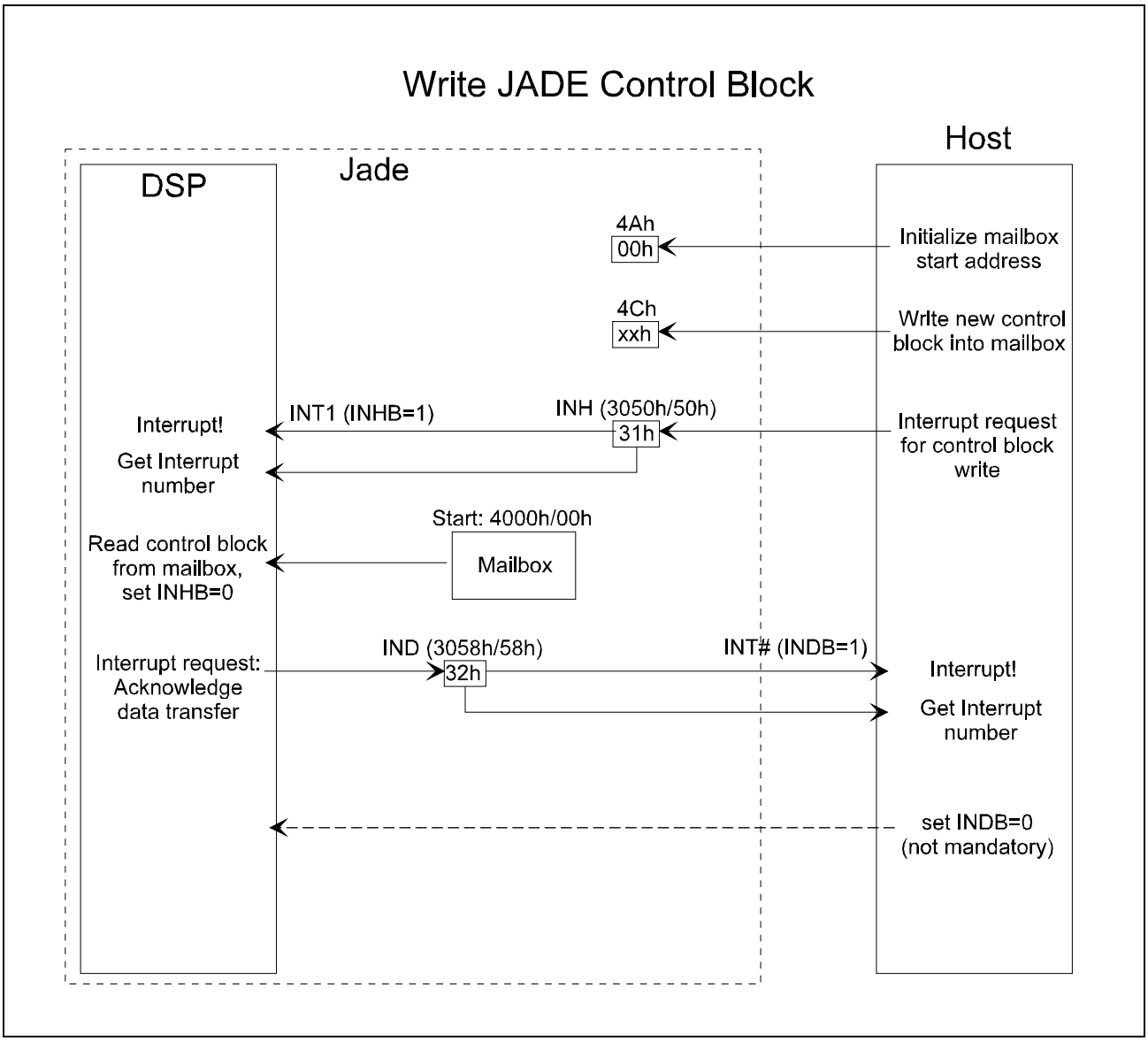

Write JADE Control Block
Host
Jade
DSP
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write new control block into mailbox
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
31h
Interrupt request for control block write
Get Interrupt number
Start: 4000h/00h
Read control block from mailbox, set INHB=0
Mailbox
IND (3058h/58h)
32h
INT# (INDB=1)
Interrupt request: Acknowledge data transfer
Interrupt!
Get Interrupt number
set INDB=0 (not mandatory)

Figure 43

The following steps are executed:

1. The host writes new control block into JADE mailbox using the procedure described in **Chapter 3.3.2.2**.
2. The host generates an interrupt to the JADE by writing value 31_H into INH interrupt status register at address 50_H.
3. The JADE reads the new control block from the mailbox, resets the INHB bit and acknowledges the reception by generating an interrupt at $\overline{INT}$ line to the host by writing a value 32_H into IND interrupt status register at address 58_H.
4. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.

Any changes to the current operating mode of the JADE take effect on the next input data packets, i.e. when a 10 ms frame length is selected, the next 10 ms packet of uncompressed data will be compressed using the new settings and the next 10 ms packet of compressed data will be decompressed using the new settings, too.

Due to internal buffering, a three stages pipeline appears in the JADE (input, compression/decompression, output). Each stage takes as long as determined by the frame length (default: 10 ms). For that reason, a mode switch affecting the input data of the JADE has to go through the whole pipeline before the output data reports the new settings. This results in a delay of three times the frame length (default: 30 ms) between the host requesting a new mode setting and the JADE delivering the first packet of data compressed/decompressed with these new settings and reporting the new settings in the status data block.

To change the control block data, the host must first set the mode to neutral (see MODE register description below) for at least three frames (default: 30 ms). Although the MODE word is part of the control block, it can be changed to neutral at any time. The switch to neutral mode before doing other changes to the control block is required to clear up the JADE's pipeline and make sure it does not have to process two different modes at once in the same pipeline. Following the neutral mode command, the host may transfer the control block with the new settings.

Some bits in the control block don't require this procedure (volume change, …). These are especially indicated in the description of the control block (see below).

See **Figure 44** for the host reading the current status data block from the JADE:

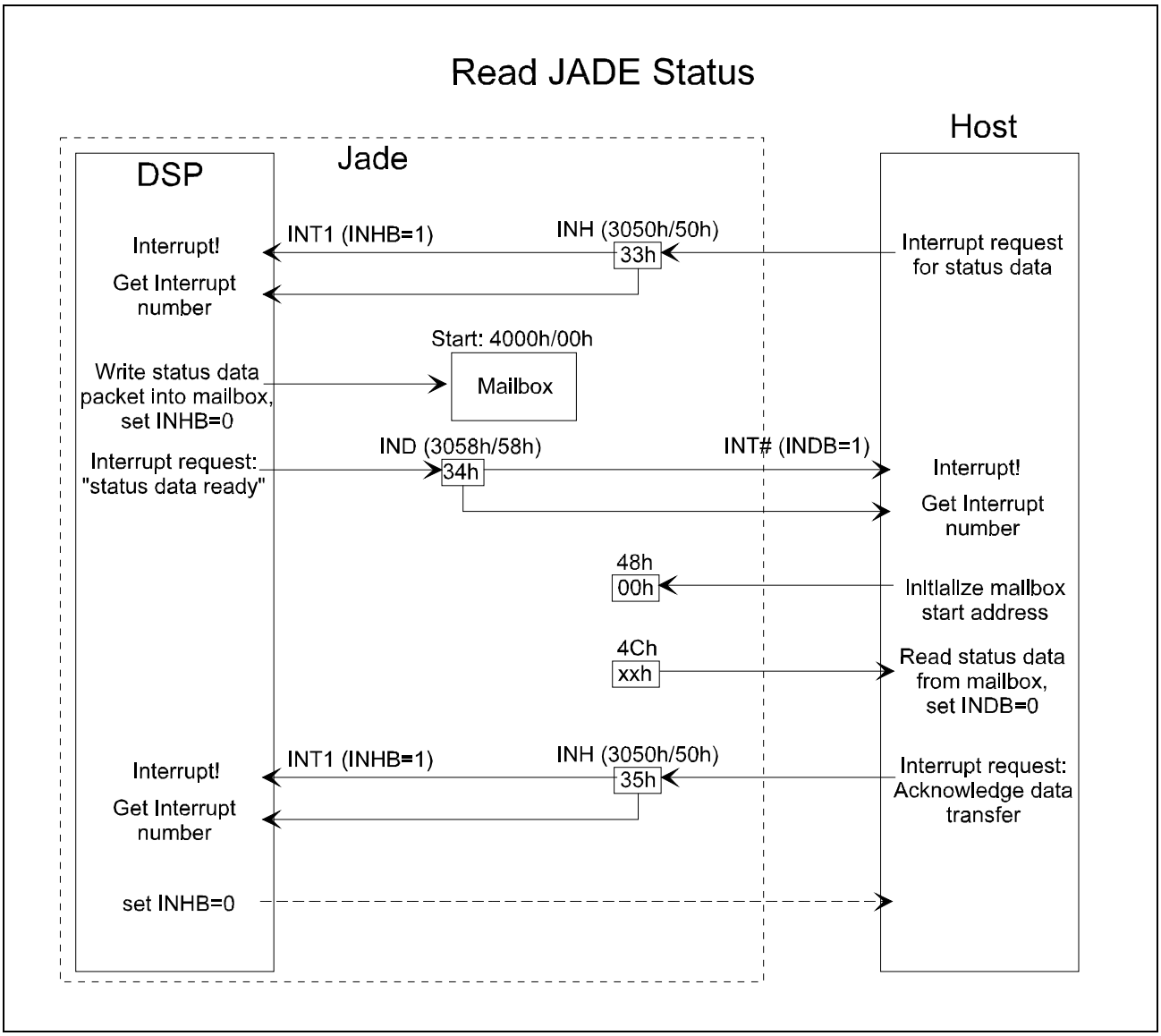

Read JADE Status
Host
Jade
DSP
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
33h
Interrupt request for status data
Get Interrupt number
Start: 4000h/00h
Write status data packet into mailbox, set INHB=0
Mailbox
Interrupt request: "status data ready"
IND (3058h/58h)
34h
INT# (INDB=1)
Interrupt!
Get Interrupt number
48h
00h
Initialize mailbox start address
4Ch
xxh
Read status data from mailbox, set INDB=0
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
35h
Interrupt request: Acknowledge data transfer
Get Interrupt number
set INHB=0

Figure 44

The following steps are executed:

1. The host generates an interrupt to the JADE by writing value 33_H into INH interrupt status register at address 50_H.
2. JADE writes the current status data into the mailbox, resets the INHB bit and generates an interrupt at $\overline{INT}$ line to the host by writing a value 34_H into IND interrupt status register at address 58_H.
3. The host reads the status data from the mailbox using the procedure described in **Chapter 3.3.2.2** and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped. The host acknowledges the transfer by writing a value 35_H into INH interrupt status register at address 50_H and by that generating an interrupt to the JADE.
4. The JADE resets the INHB bit.

Like stated before, there is a delay of three times the frame length (default: 30 ms) between the transfer of a new control block from the host to the JADE and the new settings being reported in the status data (transferred from the JADE to the host) due to the internal buffering pipeline of the JADE.

The structure of the control and status data blocks is identical. The host writes the control block to change the settings of the JADE and reads the status block to evaluate the current settings of the JADE.

The control/status block is organized in 8-bit words and has the following structure:

	(MSB)							(LSB)
CTRL	**PSEL**	**ISEL1**	**ISEL0**	**FLEN**	**0**	**0**	**0**	**1**
G728C	**0**	**0**	**0**	**UDF1**	**UDF0**	**ET0**	**1**	**PF728**
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
G722C	**TM722**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
MODE	**EM3**	**EM2**	**EM1**	**EM0**	**DM3**	**DM2**	**DM1**	**DM0**
OPT1	**I**	**0**	**0**	**0**	**0**	**L2**	**L1**	**L0**
OPT2	**0**	**S**	**Re1**	**Re0**	**Rd1**	**Rd0**	**e**	**d**
EVOL	**EV7**	**EV6**	**EV5**	**EV4**	**EV3**	**EV2**	**EV1**	**EV0**
DVOL	**DV7**	**DV6**	**DV5**	**DV4**	**DV3**	**DV2**	**DV1**	**DV0**

*Note: Unless otherwise indicated, the host has to switch the MODE to neutral for at least 3 frames (default: 30 ms) before it can change the control block. Only the underlined bits may also be changed on the fly disregarding that rule. After Reset, the JADE is automatically in the neutral mode, so changes to the control block can be done immediately after the JADE has finished its initialization phase (see **Chapter 6.2.3**).*

Mailbox Address 00_H

Value after reset: $C1_H$

	(MSB)							(LSB)
CTRL	**PSEL**	**ISEL1**	**ISEL0**	**FLEN**	**0**	**0**	**0**	**1**

PSEL Protocol Select

0 Outband controlled protocol selected, see current section.

1 Inband controlled protocol selected, see **Chapter 6.2.1.3**.

ISEL(1-0) Interface Select

00	Uncompressed audio:	Host IF
	Compressed data:	Host IF
01	Uncompressed audio:	IOM IF
	Compressed data:	Host IF
10	Uncompressed audio:	IOM IF
	Compressed data:	Serial Audio IF
11	Reserved	

FLEN Frame Length

0 10 ms frame length selected. The data packet size of compressed and uncompressed audio is determined by the frame length.

1 Reserved

Mailbox Address 01_H

Value after reset: $1B_H$

	(MSB)							(LSB)
G728C	**0**	**0**	**0**	**UDF1**	**UDF0**	**ET0**	**1**	**PF728**

UDF(1-0) Uncompressed Data Format (independent of the selected audio compression).

- 00 Reserved
- 01 G.711 A-Law
- 10 G.711 μ-Law
- 11 16-bit uncompressed audio

ET0 Decoder Excitation Signal set to 0.

- 0 Excitation Signal in the decoder is derived from the compressed G.728 data stream. This is the standard G.728 decompression mode.
- 1 Excitation Signal in the decoder is set to zero. By that the output signal of the decoder is muted with a more smooth transition than setting the decoder output directly to zero. This maybe switched on by the host when the compressed data is corrupted or not available.

PF728 G.728 Postfilter On/Off.

- 0 Postfilter Off
- 1 Postfilter On

Mailbox Address 03_H

Value after reset: 00_H

	(MSB)							(LSB)
G722C	**TM722**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

TM722 ITU-T Test Mode G.722.

0 Test Mode Off

1 Test Mode On, RS signal in compressed and uncompressed data, see ITU-T recommendation G.722 for details

Mailbox Address 04_H

Value after reset: 00_H

	(MSB)							(LSB)
MODE	**EM3**	**EM2**	**EM1**	**EM0**	**DM3**	**DM2**	**DM1**	**DM0**

EM(3-0), DM(3-0) Audio modes for encoder (EM(3-0)) and decoder (DM(3-0)).

0_H Neutral mode, no compressed audio data is exchanged

1_H Pass-through 16-bit linear 8 kHz or 16-kHz sampled data

2_H G.711 8-kHz sample rate A-law encoding/decoding

3_H G.711 8-kHz sample rate μ-law encoding/decoding

4_H G.722 16-kHz sample rate (wideband) sub-band ADPCM encoding/decoding

5_H G.728 8-kHz sample rate low delay code excited linear predictive coding (LD-CELP)

Mailbox Address 05_H

Value after reset: 00_H

	(MSB)							(LSB)
OPT1	**I**	**0**	**0**	**0**	**0**	**L2**	**L1**	**L0**

I Data is invalid. If I is set then the compressed data in this packet was missing or had errors. The data words in this packet are still sent to avoid buffer problems.

- 0 Data is valid
- 1 Data is invalid

L(2-0) Loopback modes, used for testing the audio subsystem.

- 000 No loopback (default)
- 001 Send received compressed data back to the user as encode data
- 010 Encode the decoded user data
- 011 Reserved
- 100 Reserved
- 101 Decode the encoded audio input data
- 110 Send the digital ADC output to the DAC input
- 111 Reserved

Mailbox Address 06_H

Value after reset: 00_H

	(MSB)							(LSB)
OPT2	**0**	**S**	**Re1**	**Re0**	**Rd1**	**Rd0**	**e**	**d**

S — Sampling Rate of the codec connected to the JADE, either 8 kHz or 16 kHz. If the sampling rate of the codec is different from the sampling rate expected by the selected speech coder, the JADE automatically uses over-/undersampling filters to convert the audio data.
When using G.728 mode and S = 1 indicating a 16-kHz codec is connected, the postfilter of G.728 is switched off to ensure the computational power for the over-/undersampling filters is available. The effect on the audio quality is negligible.
When using G.722 mode and S = 0 indicating an 8-kHz codec is connected, the bandwidth of the G.722 input/output data is reduced to 3.4 kHz. Nevertheless, the compressed data stream is fully compatible and interoperable with the G.722 standard.

0 Codec has 8 kHz sampling rate

1 Codec has 16 kHz sampling rate

Re(1-0), Rd(1-0) — Restricted number of bits for encode and decode. Only used for G.722, that offers modes where less than 8 bits per byte are used: 7 bits per byte (56 kbit/s) and 6 bits per byte (48 kbit/s).

00 8 valid bits per byte

01 7 valid bits per byte

10 6 valid bits per byte

11 Reserved

Rd is the same as the above, but indicates the mode of the data in this packet.

e — Encoding mute enable. After switching, a ramping function is implemented to avoid audible clicks.

0 Encoding Mute disabled

1 Encoding Mute enabled

Mailbox Address 07_H

Value after reset: 00_H

	(MSB)							(LSB)
EVOL	**EV7**	**EV6**	**EV5**	**EV4**	**EV3**	**EV2**	**EV1**	**EV0**

EV(7-0) Encoder Volume

00_H-FF_H Adjusts the gain on the analog input. Realized by multiplying the encoder input samples with (EV(7-0) + 1)/256, i.e. 00_H is the minimum and FF_H the maximum volume.

Mailbox Address 08_H

Value after reset: 00_H

	(MSB)							(LSB)
DVOL	**DV7**	**DV6**	**DV5**	**DV4**	**DV3**	**DV2**	**DV1**	**DV0**

DV(7-0) Decoder Volume

00_H-FF_H Adjusts the gain on the analog output. Realized by multiplying the decoder output samples with (DV(7-0) + 1)/256, i.e. 00_H is the minimum and FF_H the maximum volume.

The whole control/status block is usually only written once in the beginning of communication.

6.2.1.2 Compressed Audio Protocol with Outband Control

To minimize the bandwidth on the compressed audio interface, an outband controlled protocol is implemented in the JADE. This means that the mode settings for the JADE are usually done before audio data exchange is started using the procedure described in **Chapter 6.2.1.1**. During audio data transfer the JADE keeps its current mode settings and only compressed audio is exchanged.

The size and format of the compressed data is summarized in the table below for the various operating modes:

Table 19

Compression Mode	Compressed Data Packet Size in Bytes	Valid Bits per Byte[1)]
Neutral	0	0
8-kHz pass-through	160	8
16-kHz pass-through	320	8
G.711	80	8
G.722, 64 kbit/s	80	8
G.722, 56 kbit/s	80	7
G.722, 48 kbit/s	80	6
G.728	20	8

1) Always the most significant bits of a byte are valid and the least significant bits are ignored.

Note: Independently of the interface selection for the compressed audio, always the most significant bit of the most significant byte is transferred first, e.g. when using pass-through modes, the 16-bit samples are split up into two bytes and the most significant bit of the most significant byte is transferred first (big endian).

6.2.1.3 Compressed Audio Protocol with Inband Control

The following paragraph describes an H.221/H.223 oriented protocol which transfers the control information inband with the compressed audio data.

The user sends commands and data, and the provider sends status and data. Commands and data or status and data are grouped into blocks of 16-bit words.

Between the user and the JADE one data packet is transferred each way every 10 ms. The packet, that is transferred from the video processor to the JADE - called “command data” - consists of eight command words followed by the appropriate number of data words for the current speech algorithm:

Command Data Structure

0	Command header word
1	Checksum of words 2-7
2	Set mode
3	Set options
4	Set volume
5-7	Reserved for future expansion
8+	Compressed data: 0, 40, 80 or 160 words

The header of the command data packet describes the JADE operation modes in effect for data in the next packet. **See “Commands” on page 152** below for a detailed description of the above command words.

The packet that is transferred from the JADE to the video processor - called “status data” - consists of eight status words followed by the appropriate number of data words for the current speech algorithm:

Status Data Structure

0	Status header word
1	Capabilities
2	Mode status
3	Options status
4	Volume satus
5	Error conditions
6-7	Reserved for future expansion
8+	Compressed data; 0, 40, 80 or 160 words

The compressed data is between 0 and 160 words long depending on which of the decoding/encoding modes is active (neutral, G.728, G.711, G.722, 8-kHz samples pass-through or 16-kHz samples pass-through). Due to the different bit-rates of the decoding/encoding modes for 16 kbit/s, 48 kbit/s and 56 kbit/s only two, six or seven bits of a byte are used. The most significant bits of the byte are valid and the least significant bits are ignored. The first byte is the most significant byte of a word.

A header bit can indicate that the current compressed data is invalid. This means that it is not decoded and instead the sound from a previous packet is repeated. By that a simple interpolation of the speech signal is achieved to avoid an audible click.

The size of the command and data packets is the following (header excluded):

Mode	Compressed Words
Neutral	0
G.728	40
G.711	40
G.722	40
8-kHz pass-through	80
16-kHz pass-through	160

The communication between user and JADE starts in the neutral mode. To initiate transfer of speech data, the user sends a command data structure set to the desired compression mode(s) in a neutral size packet. The mode change affects the JADE's input pipeline stage in the next 10 ms period. This means that if the decode mode changes, the next packet from the user will change in size (corresponding to the new decode mode), while if the encode mode changes, the third packet from the JADE will be affected (packets from the JADE represent the output stage of the pipeline). As a general rule, any changes to the current operating mode or opetions (volume, mute, etc.) transferred to the JADE from the user take effect on the input captured on the next 10 ms boundary.

To change compression modes, the user must first send two neutral mode command packets. The first neutral mode command will be in a full-size packet per the current operating mode, while the following neutral mode command packet does only contain the 8 words header. Two neutral packets are required to clear the JADE's pipeline. During that time the JADE will reorganize its memory (if required) and re-initialize internal variables.

Note: When a mode change is requested by the user without sending two neutral packets before, the JADE may not work stable.

Commands

The following section defines the commands which are sent from the user to the JADE. Any changes in mode affects the input pipeline stage in the next 10 ms time-slot.

1. Command header word

0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1

2. Checksum

The sum of the six following words (regarded as signed 16-bit values) in the command header. If the checksum is wrong, no modes or options are changed, and an error status is sent back in the next status header.

3. Set Mode

x	x	x	x	x	x	x	x	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0

Audio modes for encoder (EM0:3) and decoder (DM0:3). The following modes are defined:

RESET	Special full word definition of the command mode. Reset is defined as 0xFFFF and returns the JADE to its power on default state.
0	Neutral mode, only command and status header information is exchanged.
1	Pass-through 16-bit linear 8 kHz or 16-kHz sampled data
2	G.711 8-kHz sample rate A-law encoding/decoding
3	G.711 8-kHz sample rate μ-law encoding/decoding
4	G.722 16-kHz sample rate (wideband) sub-band ADPCM encoding/decoding
5	G.728 8-kHz sample rate low delay code excited linear predictive coding (LD-CELP)

4. Set Options

I	x	x	P1	P0	L2	L1	L0	x	S	Re1	Re0	Rd1	Rd0	e	d

d — decoding mute enable (1) and disable (0). After switching, a ramping function is implemented to avoid audible clicks

e — encoding mute enable (1) and disable (0). After switching, a ramping function is implemented to avoid audible clicks

Re(1-0), Rd(1-0) — Restricted number of bits for encode and decode. Only used for G.722, that offers modes where less than 8 bits per byte are used: 7 bits per byte (56 kbit/s) and 6 bits per byte (48 kbit/s).

- 00 8 valid bits per byte
- 01 7 valid bits per byte
- 10 6 valid bits per byte
- 11 Reserved

S — Sampling Rate of the codec connected to the JADE, either 8 kHz (0) or 16 kHz (1). If the sampling rate of the codec is different from the sampling rate expected by the selected speech coder, the JADE automatically uses over-/undersampling filters to convert the audio data.
When using G.728 mode and S=1 indicating a 16-kHz codec is connected, the postfilter of G.728 is switched off to ensure the computational power for the over-/undersampling filters is available. The effect on the audio quality is negligible.
When using G.722 mode and S=0 indicating an 8-kHz codec is connected, the bandwidth of the G.722 input/output data is reduced to 3.4 kHz. Nevertheless, the compressed data stream is fully compatible and interoperable with the G.722 standard.

L(2-0) Loopback modes, used for testing the audio subsystem. The following loops are implemented:

- 000 No loopback (default)
- 001 Send received compressed data back to the user as encode data
- 010 Encode the decoded user data
- 011 Reserved
- 100 Reserved
- 101 Decode the encoded audio input data
- 110 Send the digital ADC output to the DAC input
- 111 Reserved

I Data is invalid. If I is set then the compressed data in this packet was missing or had errors. The data words in this packet are still sent to avoid buffer problems.

5. Set Volume

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0

Adjusts the gain on the analog input and output. Realized by multiplying the encoder samples with (EV(7-0) + 1)/256 and the decoder samples with (DV(7-0) + 1)/256, i.e. for maximum volume, the samples are not affected and for minimum volume they are divided by 256.

Status

The following section defines the status information that is sent from the JADE to the user. The status packet contains information about the current output pipeline stage, i.e. the modes used to generate the data in the status packet itself.

1. Status header word

0	1	0	0	1	0	0	0	0	0	0	0	1	1	1	1

2. Capabilities

C	S	0	0	0	0	0	0	0	0	0	L	W	µ	A	P

P Pass-through mode available (1) or not (0)

A G.711 - 8-kHz sample rate A-law coding available

µ G.711 - 8-kHz sample rate µ-law coding available

W G.722 - 16-kHz sample rate (wideband) sub-band ADPCM coding available

L G.728 - 8-kHz sample rate low delay code excited linear predictive coding (LD-CELP) available

S Symmetry required.
The JADE reports a 1 indicating the standards used for encoding must be the same as for decoding. Nevertheless, mixed G.711/G.728 encoding/decoding is possible with the JADE.

C Codec connected to the JADE (1) or not (0). Default is 1.

3. Mode Status

x	x	x	x	x	x	x	x	EM3	EM2	EM1	EM0	DM3	DM2	DM1	DM0

Report the audio mode or operation as defined in the command mode word above for the data that is in this packet.

4. Options Status

I	x	x	P1	P0	L2	L1	L0	x	S	Re1	Re0	Rd1	Rd0	e	d

Report the audio mode or operation per the bits as defined in the command options word above for the data in this packet.

5. Volume Status

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0

Report the gain on the analog input and output. Defined as in the command volume word above, i.e. 0 is the minimum volume, and 255 is the maximum.

6. Error Conditions

E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Set in response to an error, either in the command sequence or an internal error. All zero indicates no error.

Bit	**Error Condition**
0	Invalid checksum
1	Invalid audio mode
2	Invalid loopback mode
3	Hardware error
4	Packet timing error

6.2.2 Uncompressed Data Protocol

The uncompressed data protocol is quite simple. The default configuration is 8-kHz sampling rate and 16-bit linear data. The sampling rate can be switched between 8-kHz and 16 kHz (see S-bit in the control block) and the data format can be selected to be either 16-bit linear or 8-bit PCM (G.711 A-/µ-law). For a 10 ms framing the size of the uncompressed data (in bytes) is listed in the table below:

	16-bit linear	G.711 A-/µ-law
8-kHz sampling rate	160	80
16-kHz sampling rate	320	160

Note: Independently of the interface selection for the uncompressed audio, always the most significant bit of the most significant byte is transferred first, e.g. 16-bit linear samples are split up into two bytes and the most significant bit of the most significant byte is transferred first (big endian).

6.2.3 Audio Interface Timings

In this chapter the timings and/or interrupt handshake procedures are described for the different hardware interface selections (Host/Host, IOM/Host, IOM/Serial Audio Interface).

After a hardware reset the firmware automatically does all necessary initializations for the IOM/Serial Audio Interface combination described in **Chapter 6.2.3.3**. The other interface combinations can be configured by configuring the control block (see **Chapter 6.2.1.1**).

Note: After a hardware reset, the JADE firmware needs to initialize its internal memories and interfaces. The time to do this is less than 10 ms. The user must take care to access the JADE only after this initialization phase is completed, i.e. 10 ms after the hardware reset.

6.2.3.1 Uncompressed Data: Host IF
Compressed Data: Host IF

This interface combination is used for offline processing of audio (ISEL(1-0) = 00). I.e. the compression can be done faster than realtime, because the JADE is in each mode able to process audio at least in realtime. This definitely also depends on the capabilities of the host processor to provide a fast interrupt service to the handshake procedure described below. The most complex algorithm is G.728, in this mode the maximum possible speed is only slightly faster than realtime, because almost all of the computational power of the JADE is needed to compress the audio.

The basic structure of data exchange between the host and the JADE is for all compression modes the same, except for the 16-kHz pass-through mode. Thus, two different cases have to be considered:

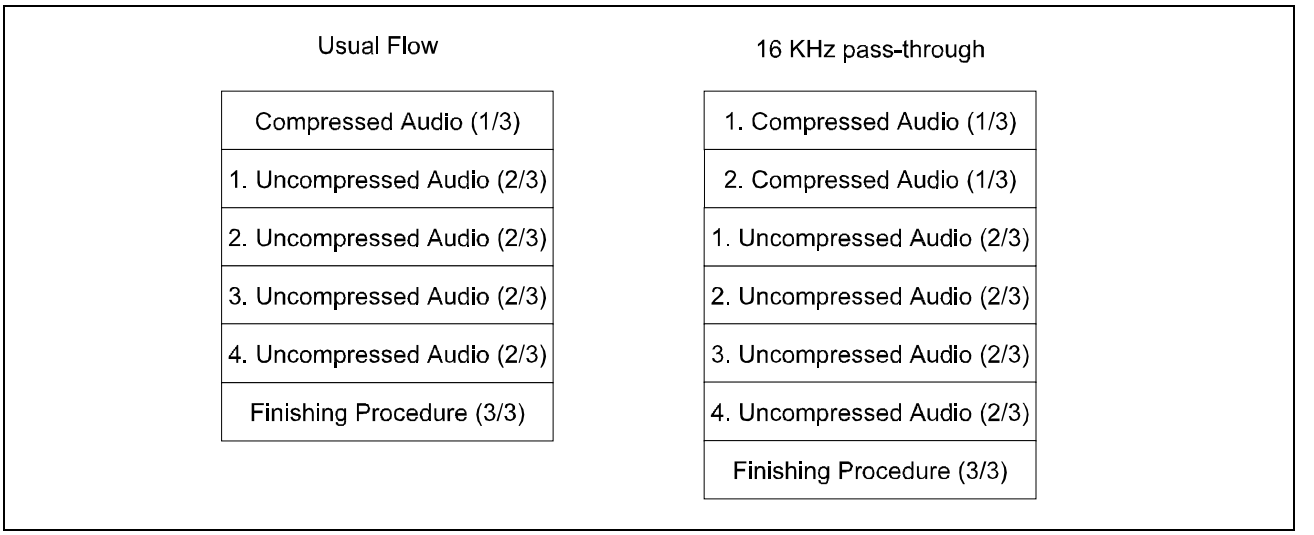


Figure 45

The picture shows the sequence of basic handshake procedures for one 10 ms frame. Basically, in both cases there are three blocks: The compressed audio exchange (basic procedure 1/3), the uncompressed audio exchange (basic procedure 2/3) and the finishing procedure (basic procedure 3/3).

The compressed audio exchange (1/3) is executed only once in a 10 ms frame, except of the 16-kHz pass-through mode. In the 16-kHz pass-through mode the mailbox cannot transfer the full data packet (320 or 336 bytes, depends on whether outband or inband control is selected) at once. Only for this mode the interrupt handshake procedure (1/3) is executed twice in one time frame. With the first run 256 bytes are transmitted in each direction, with the second run 64 bytes (outband control) or 80 bytes (inband control) are transmitted.

With the uncompressed audio handshake (2/3), 2.5 ms of uncompressed data are exchanged (20 samples for 8 kHz and 40 samples for 16-kHz sampling rate). This results in a four times repetition of this block to collect 10 ms of uncompressed data for the next frame.

Finally, a finishing handshake (3/3) is executed, which acknowledges the audio data exchange, offers the possibility to the host to request for other interrupt services and starts the next frame.

*Note: The first time frame after the Host/Host interface has been setup starts with the last part of the finishing handshake procedure (3/3), see **Figure 46** and table below.*

For the handshake procedure of the compressed audio see **Figure 46**:

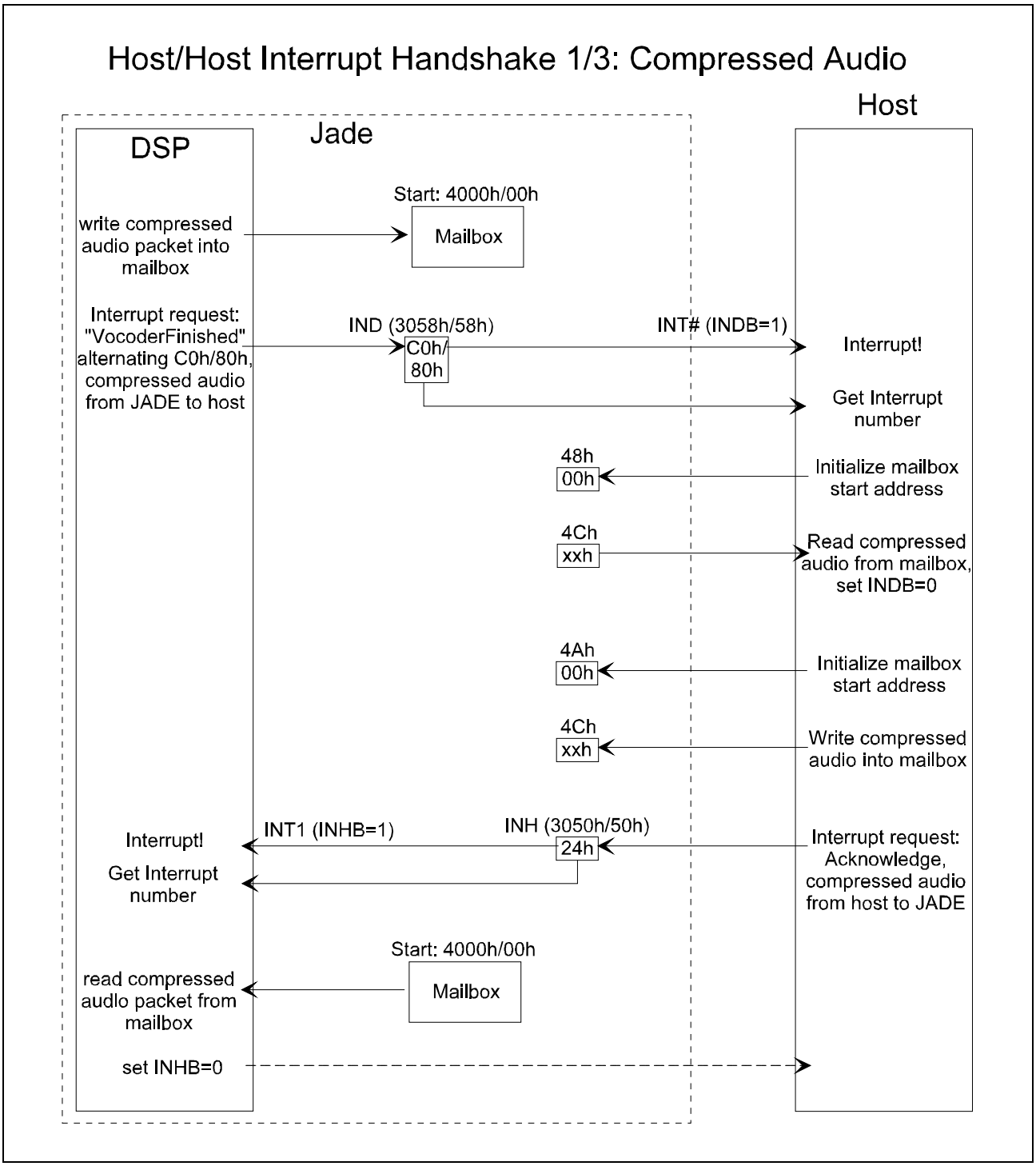


Figure 46

This procedure is (nearly) identical with the interrupt handshake when in IOM/Host mode (see **Chapter 6.2.3.2**) and the following steps are perfomed:

1. The JADE writes one frame of encoded audio data into the mailbox (most significant byte first).
2. The JADE generates a “VocoderFinished” interrupt at $\overline{INT}$ line to the host by writing a value $C0_H$ or 80_H (toggling) into IND interrupt status register at address 58_H. The value of this interrupt is each time toggling between $C0_H$ and 80_H to ensure that a polling host can consider a new “VocoderFinished”. For an interrupt driven host one should just connect both numbers to the same interrupt service routine.
3. The host reads the compressed audio frame from the mailbox using the procedure described in **Chapter 3.3.2.2** and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
4. The host writes the compressed audio frame for the decoder into the mailbox using the procedure described in **Chapter 3.3.2.2**.
5. The host generates an interrupt to the JADE by writing value 24_H into INH interrupt status register at address 50_H.
6. The JADE reads the compressed audio data from the mailbox and acknowledges the reception by resetting the INHB bit.

In the following, four 2.5 ms packets of uncompressed audio data are exchanged. See **Figure 47** for the handshake procedure:

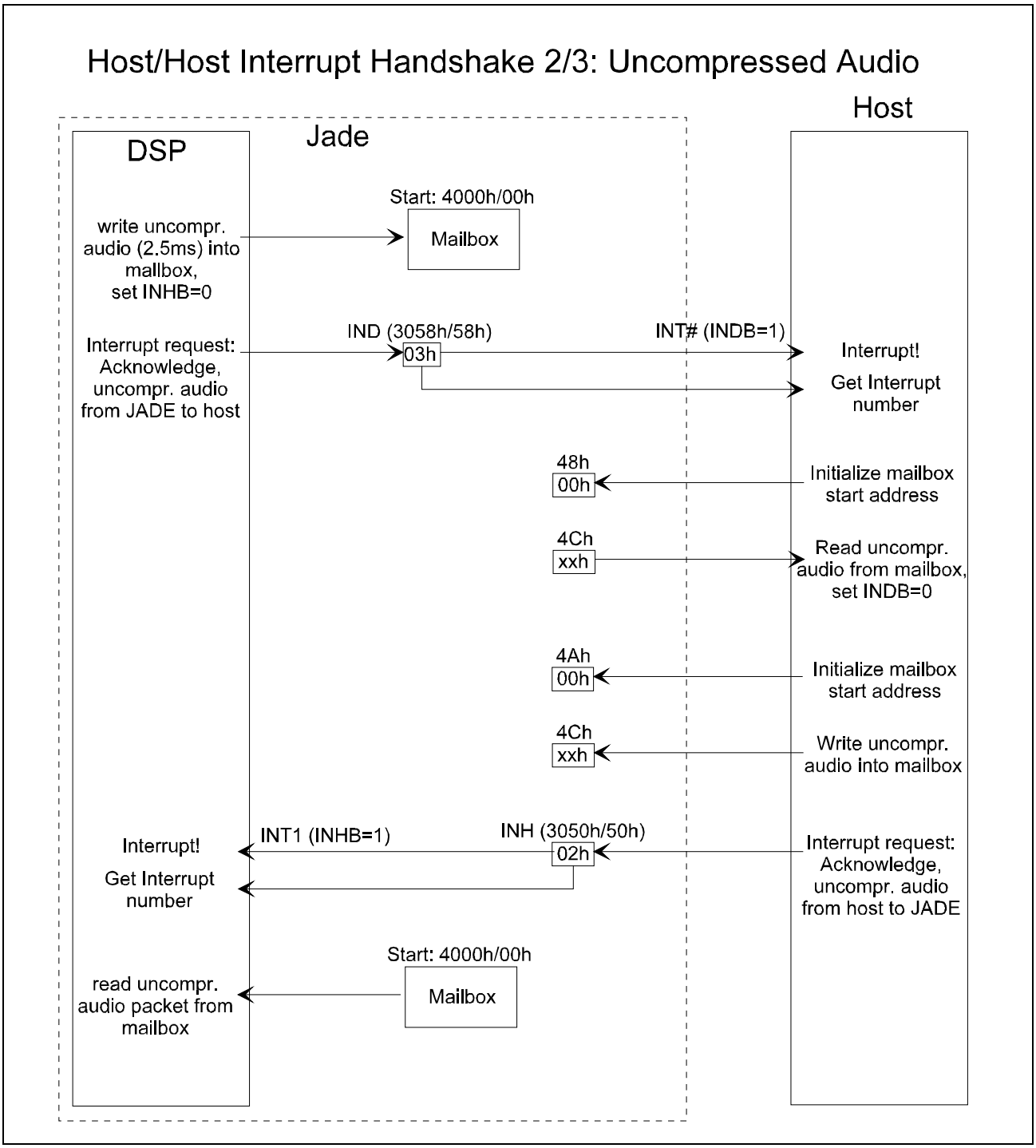

Host/Host Interrupt Handshake 2/3: Uncompressed Audio
Host
Jade
DSP
Start: 4000h/00h
write uncompr. audio (2.5ms) into mailbox, set INHB=0
Mailbox
IND (3058h/58h)
03h
INT# (INDB=1)
Interrupt request: Acknowledge, uncompr. audio from JADE to host
Interrupt!
Get Interrupt number
48h
00h
Initialize mailbox start address
4Ch
xxh
Read uncompr. audio from mailbox, set INDB=0
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write uncompr. audio into mailbox
INT1 (INHB=1)
INH (3050h/50h)
02h
Interrupt!
Get Interrupt number
Interrupt request: Acknowledge, uncompr. audio from host to JADE
Start: 4000h/00h
read uncompr. audio packet from mailbox
Mailbox

Figure 47

The following steps are executed:

1. The JADE writes a packet of uncompressed audio (2.5 ms) into the mailbox (most significant byte first).
2. The JADE generates an interrupt at $\overline{INT}$ line to the host by writing a value 03_H into IND interrupt status register at address 58_H.
3. This interrupt acknowledges the previous INH interrupt (either from the compressed data transfer or from the last uncompressed data transfer) and requests the current uncompressed data exchange.
4. The host reads the uncompressed audio from the mailbox using the procedure described in **Chapter 3.3.2.2** and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
5. The host writes a packet of uncompressed audio (2.5 ms) into the mailbox using the procedure described in **Chapter 3.3.2.2**.
6. The host generates an interrupt ot the JADE by writing value 02_H into INH interrupt status register at address 50_H.
7. The JADE reads the uncompressed audio data from the mailbox.

After the above procedure has been repeated four times, the finishing procedure is executed (see **Figure 48**):

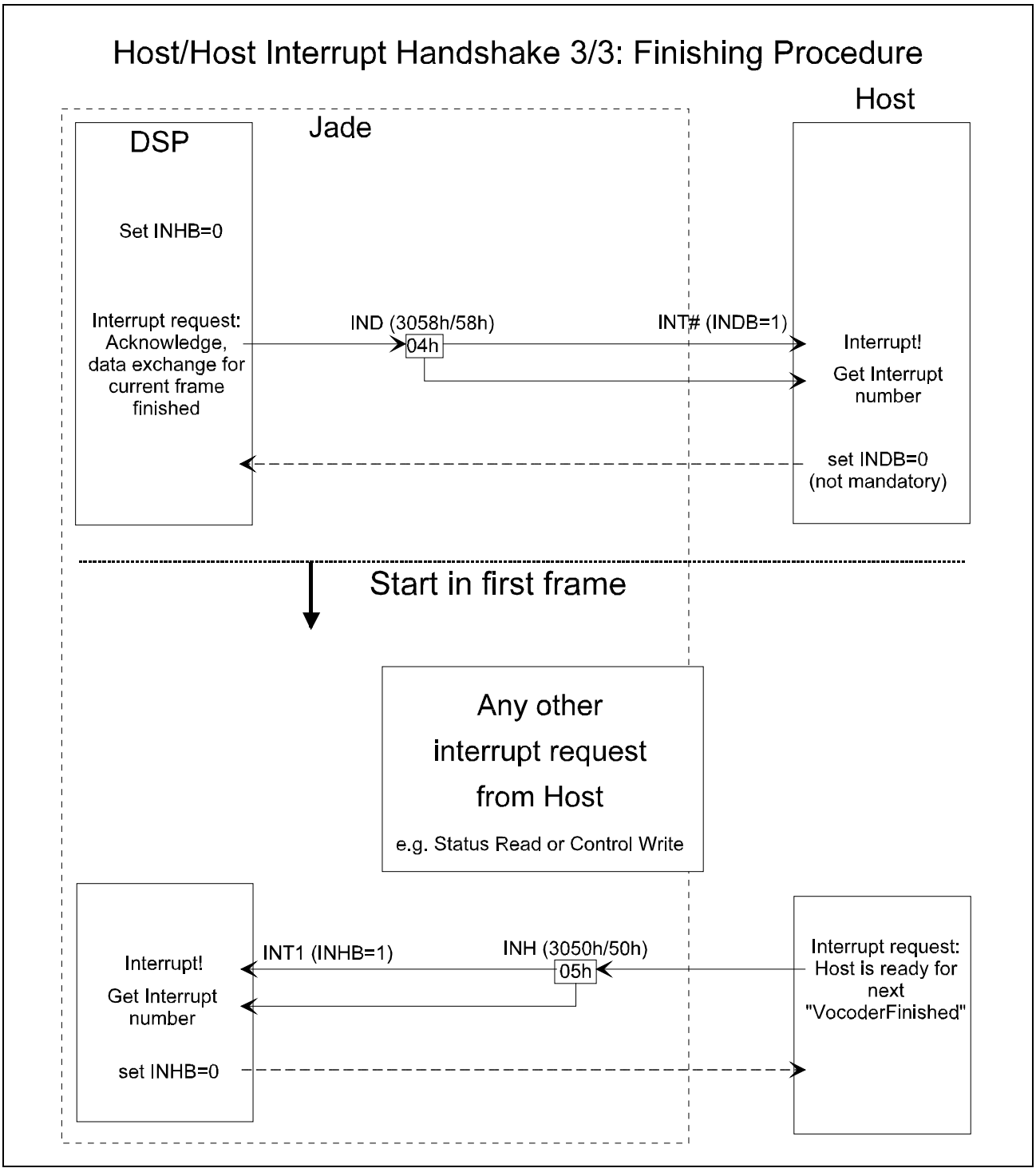

Host/Host Interrupt Handshake 3/3: Finishing Procedure
Host
Jade
DSP
Set INHB=0
Interrupt request: Acknowledge, data exchange for current frame finished
IND (3058h/58h)
04h
INT# (INDB=1)
Interrupt!
Get Interrupt number
set INDB=0 (not mandatory)
Start in first frame
Any other interrupt request from Host
e.g. Status Read or Control Write
Interrupt!
Get Interrupt number
set INHB=0
INT1 (INHB=1)
INH (3050h/50h)
05h
Interrupt request: Host is ready for next "VocoderFinished"

Figure 48

The following steps are executed:

1. The JADE generates an interrupt at $\overline{INT}$ line to the host by writing a value 04_H into INH interrupt status register at address 50_H.
2. The host may reset the INDB as a reaction to the JADE interrupt. This step is not mandatory and may be skipped.
3. Start point in first frame
   At this point, the host can request other interrupts, like Read Status or Write Control Block (see **Chapter 6.2.1.1**).
   The number of interrupts and the time to execute them is not limited by the JADE, but dedicated by the host itself. The host may request interrupts as long as it has not executed the next step of this table.
4. The host generates an interrupt to the JADE by writing value 05_H into INH interrupt status register at address 50_H.
   By that, the host indicates that it is ready to exchange the next frame of data.
5. The JADE resets the INHB bit.

With this procedure the handling of one frame of data is finished and the next frame is started beginning with the exchange of the compressed audio (procedure 1/3).

When starting the above protocol, it begins at the point marked with “Start in first frame”. This is to enable the host to have control of the real start time, so the host first has to generate a “Host Ready” interrupt (INH = 05_H) before the host will start with the exchange of the compressed audio (procedure 1/3). After that, the Host/Host handshake procedure is executed cyclically.

Note: A polling host should not directly poll the IND interrupt status register 58_H, but the DINT bit in $\overline{INT}$ interrupt status register 75_H. This bit always shows whether an interrupt from the DSP has been generated or not, independently of the corresponding mask register. The mask register only decides whether an interrupt at $\overline{INT}$ line is generated. After having recognized an IND interrupt status, the polling host may read out the register 58_H to get the interrupt number.

6.2.3.2 Uncompressed Data: IOM IF
Compressed Data: Host IF

The JADE can provide the uncompressed audio via the IOM interface while exchanging the compressed audio through the host interface (ISEL(1-0)=01).

After switching to IOM/host interface combination by programming the ISEL(1-0) bits in the control block, an initialization phase is executed by the JADE in which the internal firmware re-programs the configuration/control registers like in the default configuration (see **Chapter 5.3**) to setup the IOM interface for the communication with the analog front end (AFE). This initialization phase is < 10 ms.

The IOM interface is in TE mode (double DCL clock) and IC1/2 channels are selected for the 16 bit linear data transfer between the JADE and the analog front end (AFE). The DD line is output of the JADE, DU is input to the JADE.

This configuration may be changed by the host by just overwriting the corresponding registers after the default initialization has been completed.

An interrupt handshake protocol is implemented for the data exchange on the host interface. The basic timing for this protocol is determined by the uncompressed data rate at the IOM interface. See **Figure 49** for the interrupt handshake procedure:

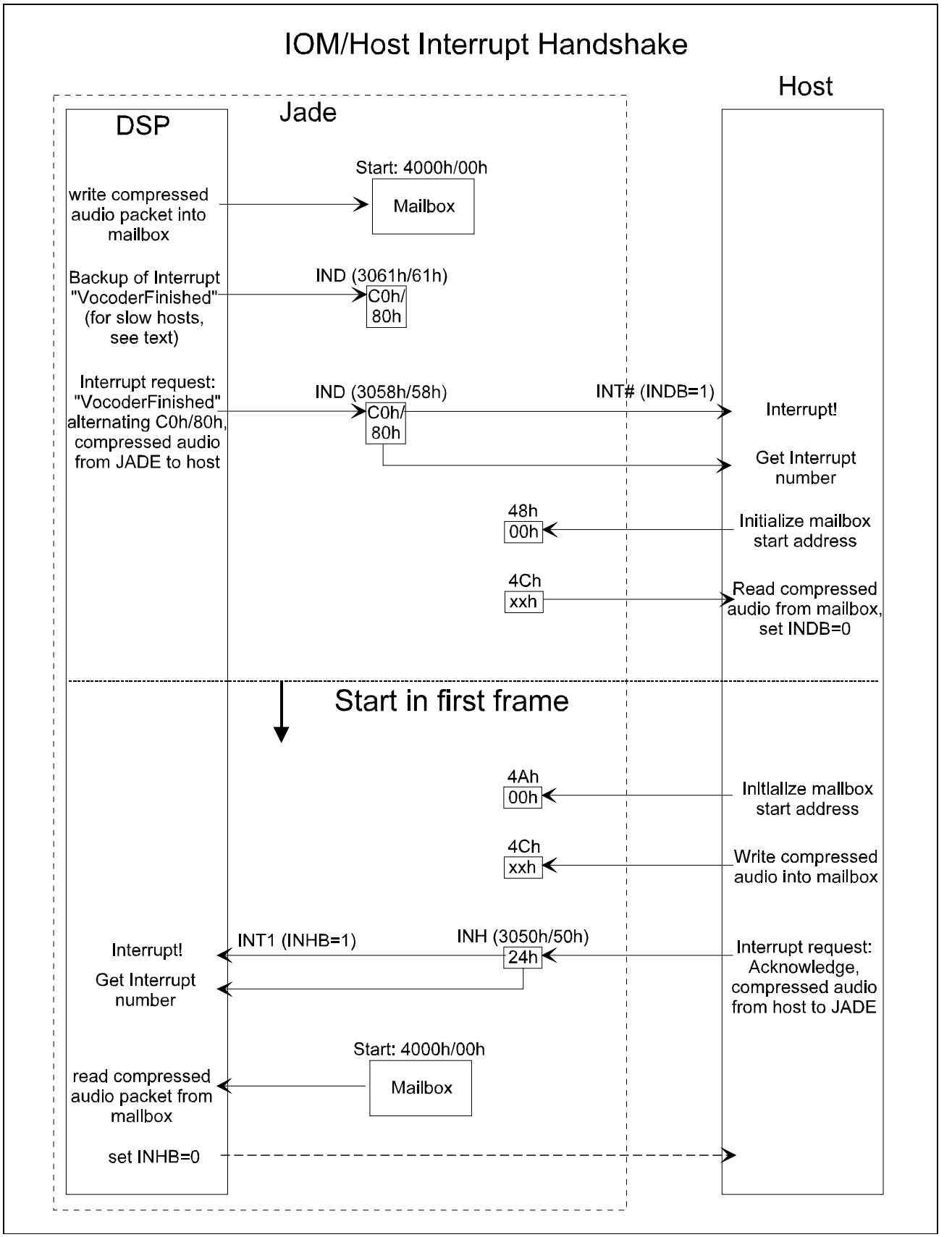

IOM/Host Interrupt Handshake
Host
Jade
DSP
Start: 4000h/00h
write compressed audio packet into mailbox
Mailbox
Backup of Interrupt "VocoderFinished" (for slow hosts, see text)
IND (3061h/61h)
C0h/ 80h
Interrupt request: "VocoderFinished" alternating C0h/80h, compressed audio from JADE to host
IND (3058h/58h)
C0h/ 80h
INT# (INDB=1)
Interrupt!
Get Interrupt number
48h
00h
Initialize mailbox start address
4Ch
xxh
Read compressed audio from mailbox, set INDB=0
Start in first frame
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write compressed audio into mailbox
Interrupt!
Get Interrupt number
INT1 (INHB=1)
INH (3050h/50h)
24h
Interrupt request: Acknowledge, compressed audio from host to JADE
Start: 4000h/00h
read compressed audio packet from mailbox
Mailbox
set INHB=0

Figure 49

The JADE starts the above interrupt procedure once every frame (default: 10 ms), except of the 16-kHz pass-through mode. In the 16-kHz pass-through mode the mailbox cannot transfer the full data packet (320 or 336 bytes, depends on whether outband or inband control is selected) at once. Only for this mode the above interrupt handshake procedure is executed twice in one time frame. With the first “VocoderFinished” 256 bytes are transmitted in each direction, with the second run 64 bytes (outband control) or 80 bytes (inband control) are transmitted.

The following steps are performed:

1. The JADE writes one frame of encoded audio data into the mailbox (most significant byte first).
2. The JADE writes a backup of the “VocoderFinished” interrupt number performed in the next step into the host accessible register 61_H. This is only used for detection of a missed interrupt when a slow host is connected, see text below.
3. The JADE generates a "VocoderFinished" interrupt at $\overline{INT}$ line to the host by writing a value $C0_H$ or 80_H (toggling) into IND interrupt status register at address 58_H. The value of this interrupt is each time toggling between $C0_H$ and 80_H to ensure that a polling host can consider a new “VocoderFinished”. For an interrupt driven host one should just connect both numbers to the same interrupt service routine.
4. The host reads the compressed audio frame from the mailbox using the procedure described in **Chapter 3.3.2.2** and may reset the INDB bit. The reset of the INDB bit is not mandatory and may be skipped.
5. Start point in first frame
   The host writes the compressed audio frame for the decoder into the mailbox using the procedure described in **Chapter 3.3.2.2**.
6. The host generates an interrupt to the JADE by writing value 24_H into INH interrupt status register at address 50_H.
7. The JADE reads the compressed audio data from the mailbox and acknowledges the reception by resetting the INHB bit. [1) 2)]

[1)] To keep the interrupt load for the host as small as possible, the JADE does not generate an acknowledge interrupt. It is guaranteed, that the INH interrupt 24_H is serviced within a time of 125 µs, so if the host sends the interrupt 24_H soon enough, it is guaranteed, that the interrupt handshake procedure is completed before the next “VocoderFinished” from the JADE appears. So, in this case the host does not need to check the status of INHB.

[2)] If the host wants to apply other actions, e.g. reading or writing of the control/status block, it has to wait for the INHB bit to be reset to 0. All these additional actions should be completed within the current time frame (default: within 10 ms after the “VocoderFinished” interrupt). Otherwise special situations in the interrupt sequence have to be considered by the host, see text below.

When starting the above procedure, it begins at the point marked with “Start in first frame”. This is to enable the host to have control of the real start time, so the host first has to deliver compressed data to the JADE and generate the corresponding interrupt. After that, the IOM/Host handshake procedure is executed cyclically.

Note: A polling host should not directly poll the IND interrupt status register 58_H, but the DINT bit in $\overline{INT}$ interrupt status register 75_H. This bit always shows whether an interrupt from the DSP has been generated or not, independently of the corresponding mask register. The mask register only decides whether an interrupt at $\overline{INT}$ line is generated. After having recognized an IND interrupt status, the polling host may read out the register 58_H to get the interrupt number.

Note: Some special situations have to be considered if one uses a slow host that cannot always ensure to finish the whole interrupt handshake in one frame period (default 10 ms), i.e. before the next VocoderFinished interrupt is generated by the JADE. Collisions between not finished interrupts and the new VocoderFinished Interrupt may occur.

Interrupt Conflicts with a Slow Host

In the following some special situations and the recommended handling are described to keep the host protocol stable also in situations where the host has not finished it’s interrupt requests before the begin of the next time frame, as long as the interrupt service delay is less than 160 ms.

The following descriptions apply for all encoder/decoder modes, except the 16-kHz pass-through. In the 16-kHz pass-through mode, the host must ensure that all interrupts are finished before the next “VocoderFinished” is generated by the JADE. This is because of the special double-”VocoderFinished” protocol, see text above.

If the interrupt service from the host is delayed by up to 160 msec, none of the Interrupts during this time (usually only one "VocoderFinished" every 10 msec) is lost, but they are delayed, too, until the host is able to service them. Thus, after a gap in interrupt service a burst of interrupts has to be serviced by the host.

The interrupts “Write JADE Control Block” and “Read JADE Status” are representative for all kinds of interrupts initiated by the host, so they are used in the following as an example for the corresponding type of interrupt.

1. “Write JADE Control Block” conflict with “VocoderFinished”, Case 1

A critical situation for the host may occur when a “Write JADE Control Block” (WCB) interrupt handshake is done immediately before the next time frame starting with the new "VocoderFinished" (VocFin) interrupt begins. See **Figure 50**.

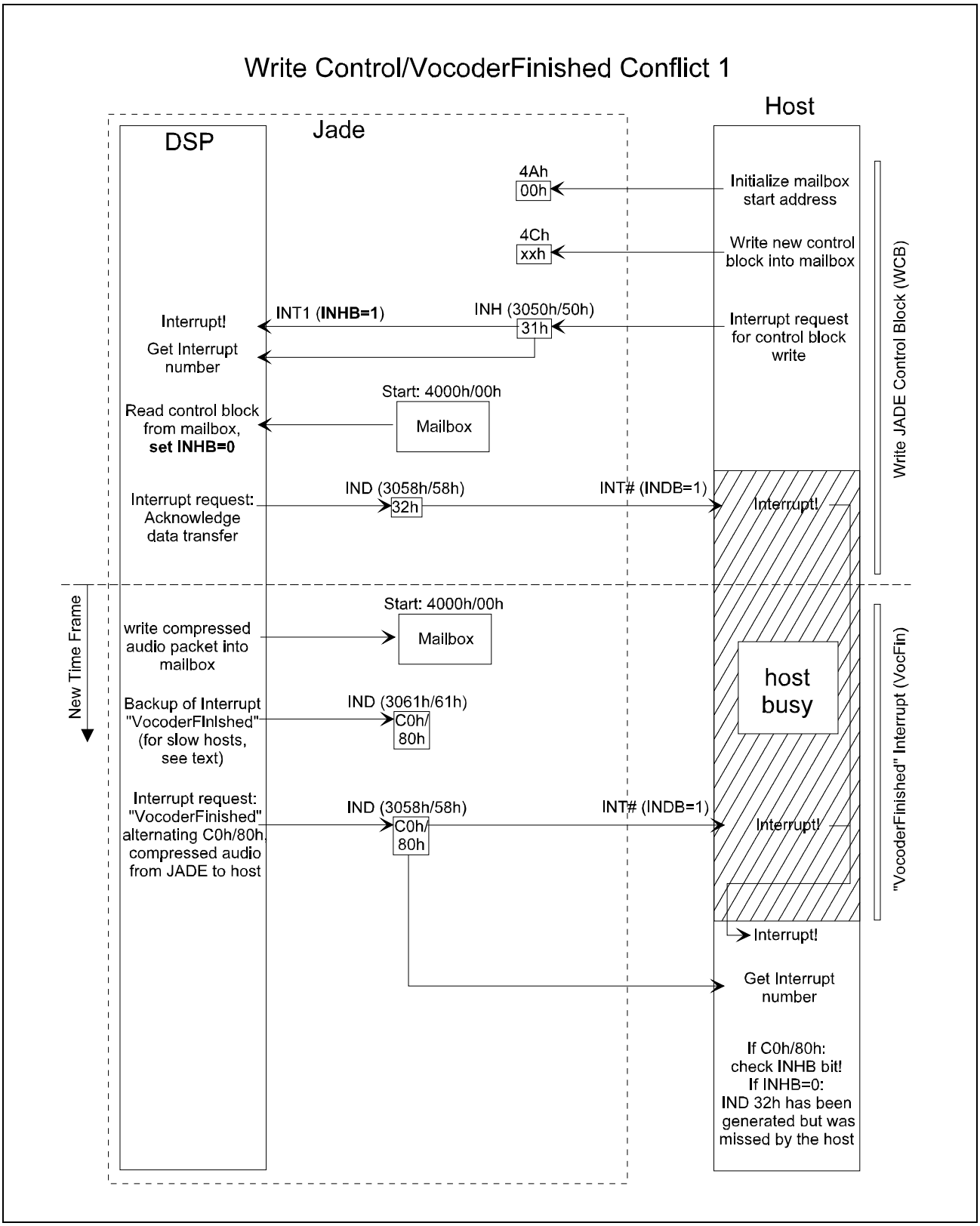

Write Control/VocoderFinished Conflict 1
Host
DSP
Jade
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write new control block into mailbox
Write JADE Control Block (WCB)
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
31h
Interrupt request for control block write
Get Interrupt number
Start: 4000h/00h
Read control block from mailbox, set INHB=0
Mailbox
IND (3058h/58h)
32h
INT# (INDB=1)
Interrupt request: Acknowledge data transfer
Interrupt!
New Time Frame
Start: 4000h/00h
write compressed audio packet into mailbox
Mailbox
host busy
Backup of Interrupt "VocoderFInished" (for slow hosts, see text)
IND (3061h/61h)
C0h/ 80h
Interrupt request: "VocoderFinished" alternating C0h/80h, compressed audio from JADE to host
IND (3058h/58h)
C0h/ 80h
INT# (INDB=1)
Interrupt!
"VocoderFinished" Interrupt (VocFin)
Interrupt!
Get Interrupt number
If C0h/80h: check INHB bit! If INHB=0: IND 32h has been generated but was missed by the host

Figure 50

In this case, the WCB interrupt handshake is finished correctly, but the acknowledge interrupt IND 32_H may be missed by the host if it is busy at that time, because the next VocFin may be generated by the JADE before the host is able to recognize the IND 32_H interrupt. The IND interrupt status register then is overwritten by the VocFin interrupt. If the host was busy during the time these two interrupts occured, it will afterwards only detect the VocFin interrupt and miss the acknowledge of the WCB.

To handle this situation, the host should have an internal status register indicating an outstanding acknowledge interrupt. In case a VocFin is detected and an acknowledge interrupt is outstanding, the host has to check the INHB bit. As shown in **Figure 50**, the INHB bit is reset in the WCB acknowledge procedure (see bold text). If the host detects INHB=0, the WCB interrupt has been acknowledged, but the host has missed the IND 32_H interrupt. If the host detects INHB=1, the WCB interrupt has not yet been serviced and will be serviced later. For this case see also the conflict situation below.

2. “Write JADE Control Block” conflict with “VocoderFinished”, Case 2

Another critical situation for the host may occur when a “Write JADE Control Block” (WCB) interrupt handshake is started in parallel with the new VocoderFinished interrupt of the new time frame.

See **Figure 51**.

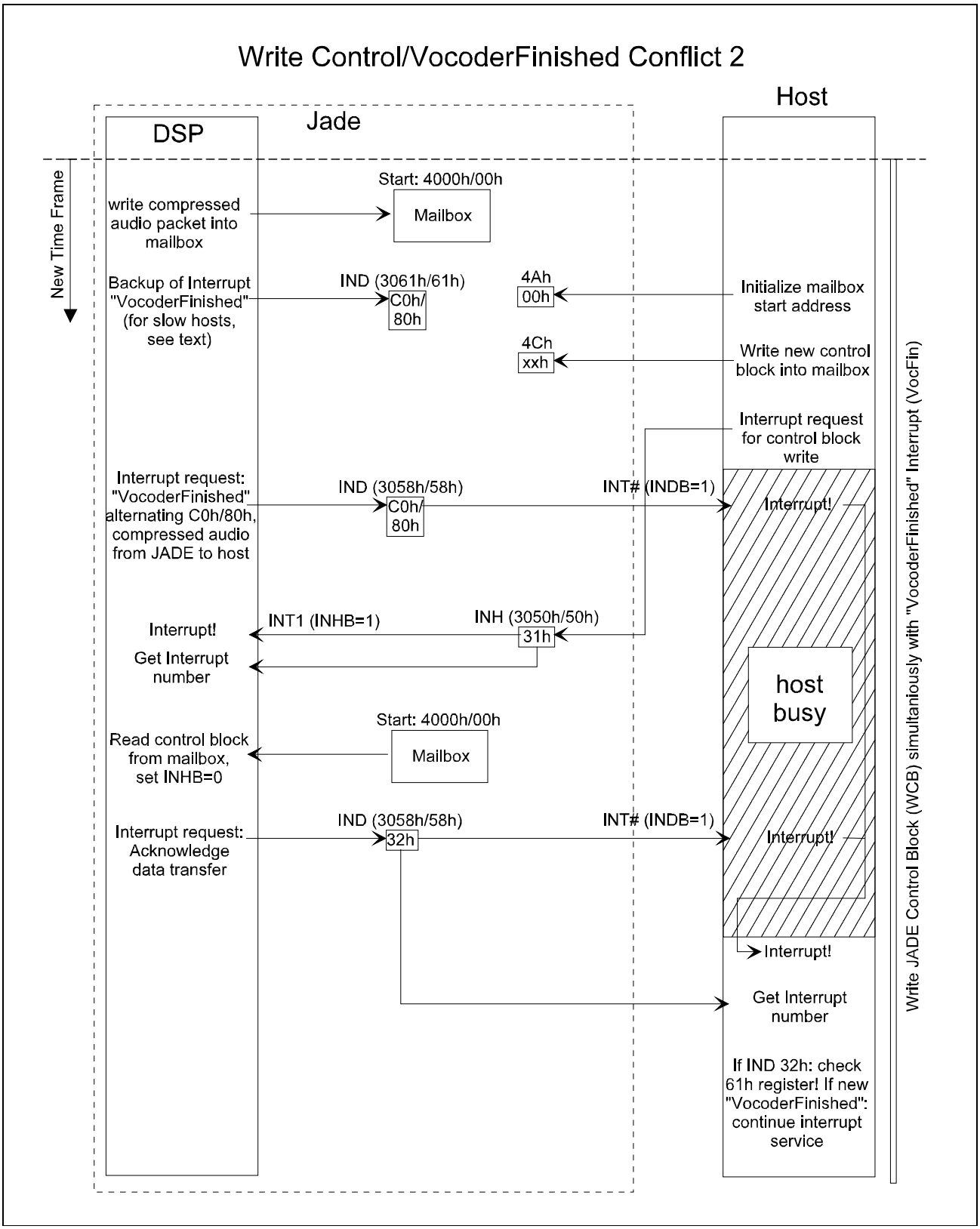

Write Control/VocoderFinished Conflict 2
Host
DSP
Jade
New Time Frame
Start: 4000h/00h
write compressed audio packet into mailbox
Mailbox
Backup of Interrupt "VocoderFinished" (for slow hosts, see text)
IND (3061h/61h)
C0h/ 80h
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write new control block into mailbox
Interrupt request for control block write
Interrupt request: "VocoderFinished" alternating C0h/80h, compressed audio from JADE to host
IND (3058h/58h)
C0h/ 80h
INT# (INDB=1)
Interrupt!
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
31h
Get Interrupt number
host busy
Start: 4000h/00h
Read control block from mailbox, set INHB=0
Mailbox
Interrupt request: Acknowledge data transfer
IND (3058h/58h)
32h
INT# (INDB=1)
Interrupt!
Interrupt!
Get Interrupt number
If IND 32h: check 61h register! If new "VocoderFinished": continue interrupt service
Write JADE Control Block (WCB) simultaniously with "VocoderFinished" Interrupt (VocFin)

Figure 51

In this case, the host generates the WCB interrupt before it has recognized the VocFin from the JADE and the JADE generates the VocFin before it has recognized the WCB from the host.

Immediately after the reception of WCB request the JADE will service that interrupt and send the corresponding acknowledge interrupt IND 32_H. The VocFin interrupt status in the IND register is overwritten by that. If the host was busy between VocFin and the acknowledge of WCB, it will only receive one interrupt and recognize the later one, which is the IND 32_H. To recognize, that it has missed one VocFin interrupt, the host should check the “VocoderFinished” backup register 61_H. If the value of this register has toggled, it knows that there has been a VocFin before the IND 32_H interrupt and must continue to service it.

Note: A parallel read/write access of the 3061/61 register is not prohibited by hardware. Thus an invalid value maybe read by the host when it reads the register at the same time as the JADE writes it. As a consequence, the host has to implement a double last look regarding this register, i.e. it has to read the contents until it has read the same value in two consecutive read-accesses, only then it is ensured that the value is valid.

3. “Read JADE Status” conflict with “VocoderFinished”, Case 1

If a “Read JADE Status” (RS) interrupt handshake is initiated by the host immediately before the next time frame starts and is not completed at the time the new VocFin interrupt should occur, the VocFin is delayed until the RS is finished.

Due to audio delay reasons, the JADE has small internal buffers for the compressed data. This leads to an overwriting of audio data very soon after a VocFin is delayed.

It is ensured that the JADE is working stable in these situations (except for the 16-kHz pass-through mode, in which two VocFin handshakes have to be done in each time frame, see above), nevertheless, a graceful degradation of speech quality has to be accepted by the user which is about proportional to the real delay time of the VocFin interrupt (the smaller the delay due to the busy host, the smaller the degradation of quality).

4. “Read JADE Status” conflict with “VocoderFinished”, Case 2

A “Read JADE Status” (RS) request from the host coming in parallel with the VocFin of the new time frame will cause the following interrupt flow:

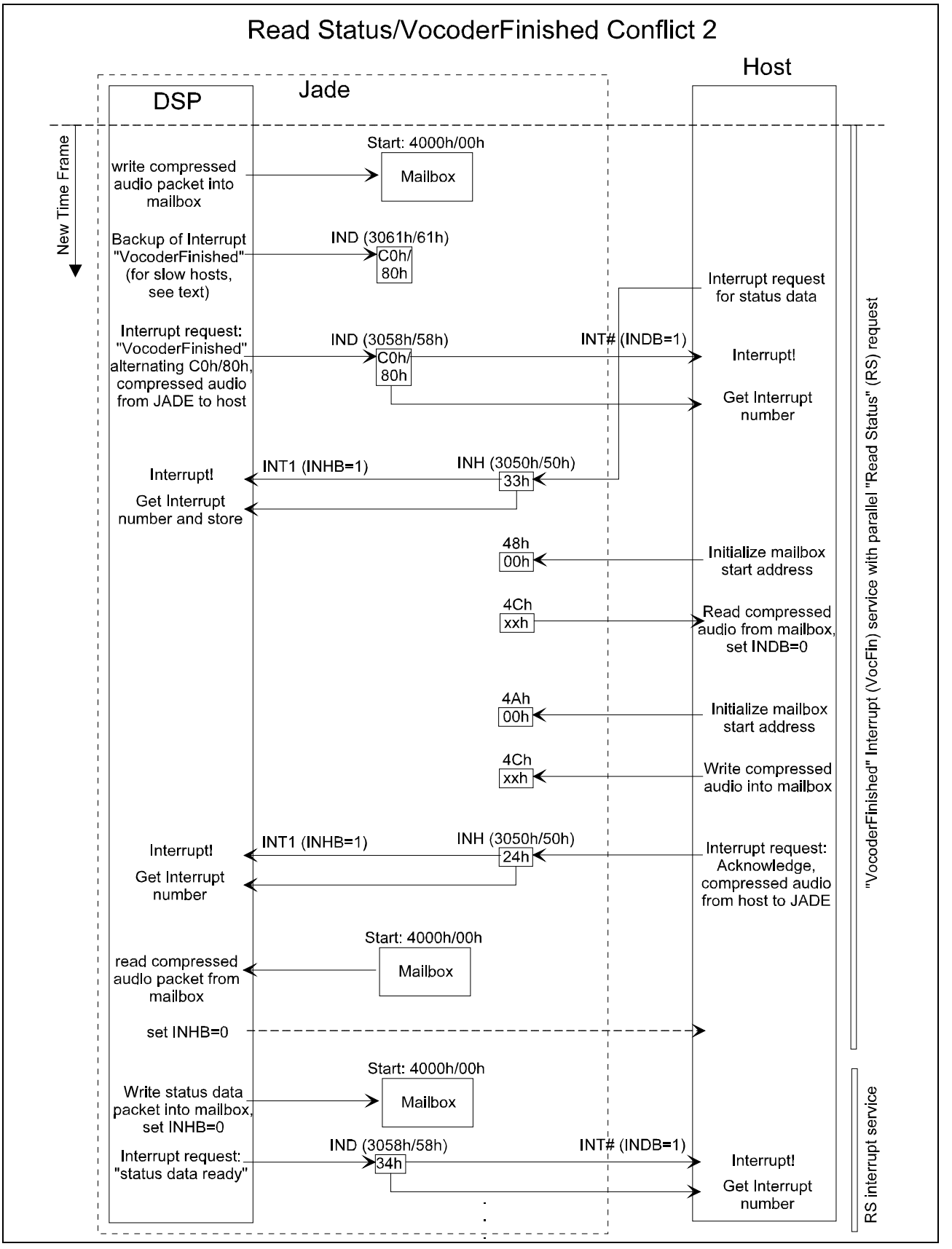

Read Status/VocoderFinished Conflict 2
Host
Jade
DSP
New Time Frame
Start: 4000h/00h
write compressed audio packet into mailbox
Mailbox
Backup of Interrupt "VocoderFinished" (for slow hosts, see text)
IND (3061h/61h)
C0h/ 80h
Interrupt request for status data
Interrupt request: "VocoderFinished" alternating C0h/80h, compressed audio from JADE to host
IND (3058h/58h)
C0h/ 80h
INT# (INDB=1)
Interrupt!
Get Interrupt number
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
33h
Get Interrupt number and store
48h
00h
Initialize mailbox start address
4Ch
xxh
Read compressed audio from mailbox, set INDB=0
4Ah
00h
Initialize mailbox start address
4Ch
xxh
Write compressed audio into mailbox
Interrupt!
INT1 (INHB=1)
INH (3050h/50h)
24h
Interrupt request: Acknowledge, compressed audio from host to JADE
Get Interrupt number
Start: 4000h/00h
read compressed audio packet from mailbox
Mailbox
set INHB=0
Start: 4000h/00h
Write status data packet into mailbox, set INHB=0
Mailbox
Interrupt request: "status data ready"
IND (3058h/58h)
34h
INT# (INDB=1)
Interrupt!
Get Interrupt number
"VocoderFinished" Interrupt (VocFin) service with parallel "Read Status" (RS) request
RS interrupt service

Figure 52

The SR request will be recognized by the JADE, but not immediately be serviced. It is stored in an internal interrupt buffer and the VocFin is handled first as the higher priority interrupt. So, the host must not wait for the SR request to be serviced, but has to be able to recognize a VocFin interrupt from the JADE after an SR request. The VocFin interrupt then is serviced as usual and only after the corresponding handshake mechanism is finished, the SR request is serviced by the JADE.

6.2.3.3 Uncompressed Data: IOM IF
Compressed Data: Serial Audio Interface (SAI)

This is the default mode of the JADE (ISEL(1-0) = 10). The complete setup of the interfaces, time slots and so on is done by the on-chip firmware after reset, so that a standalone application with a video processor using the IOM-SAI interface combination can be realized without the need of an additional host.

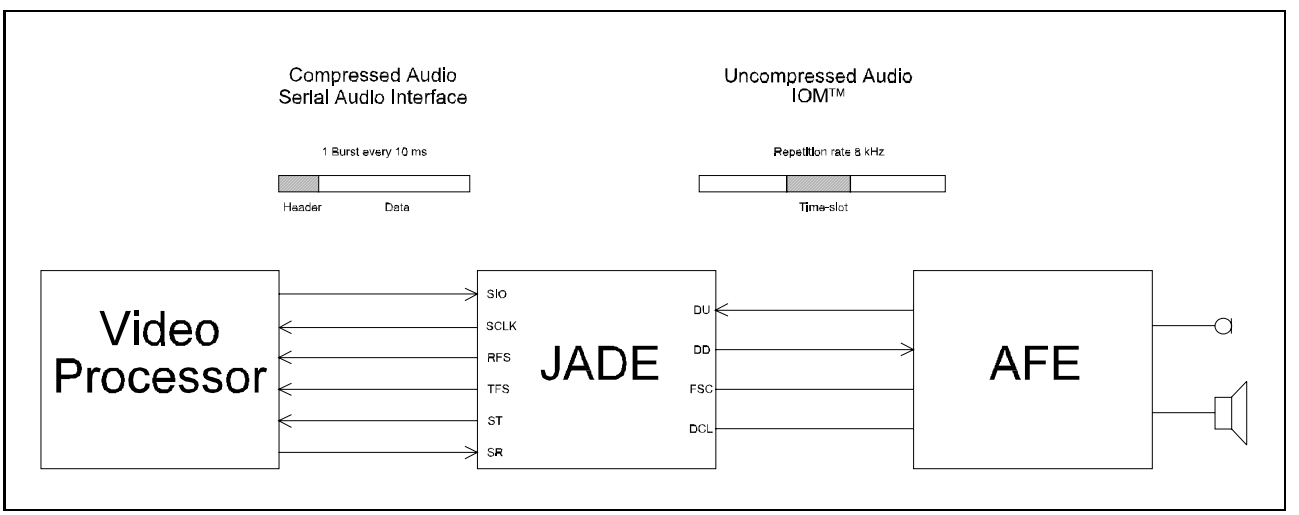


Figure 53

The on-chip firmware uses the HDLC1 controller in transparent mode for the transfer of the compressed audio data over the serial audio interface. During the initialization phase after a reset, the internal firmware programs the configuration/control registers (see **Chapter 5.3**) and the HDLC1 controller (see **Chapter 5.4**). This results in a serial clock rate of 1.23 MHz continously generated by the JADE, a 16-bit time-slot length and MSB sent/received first. The frame sync signals RFS and TFS are generated by the JADE non-continously, i.e. during one frame only the exact number of frame syncs needed for the transfer of the current packet of data is generated in one burst.

The IOM interface is in TE mode (double DCL clock) and IC1/2 channels are selected for the 16-bit linear data transfer between the JADE and the analog front end (AFE). The DD line is output of the JADE, DU is input to the JADE.

This configuration may be changed by the host by just overwriting the corresponding registers.

The timing of the JADE firmware is controlled by the video processor, which generates an interrupt every 10 ms at the SIO line. The JADE then starts generating a number of frame sync signals at RFS and TFS, depending on the length of the data packet that has to be exchanged. The RFS and TFS bursts are asynchronously, i.e. the RFS burst starts about 16 frame syncs before the TFS. After data packet transfer the JADE waits for the next SIO interrupt.

During startup procedure the uncompressed interface (IOM) must be setup before the Serial Audio Interface is started, i.e. the FSC and DCL signals must be stable before the first 10 ms interrupt is generated by the video processor.

Due to small differences in the clock of the video processor and the audio output, the JADE is able to add two uncompressed audio samples every 10 ms. That means, a skew of about 2.5% (f_S = 8 kHz) or 1.25% (f_S = 16 kHz) between the communication board's clock and the audio codec's clock is acceptable to the JADE and should be aurally imperceptible. In the following this will be called the long term skew.

In addition to the long term skew, the JADE can correct for short term variances using an internal buffer mechanism. This allows single SIO periods to be 10 ms $\pm$ 15%.

The full definition is as follows:

Long term SIO period T_L:

$$T_L = 10\ \text{ms} \pm 0.25\ \text{ms}$$

Short term SIO period T_S:

$$T_S = T_L \times 1 \pm 15\%$$

Duration of n consecutive SIO periods:

$$\sum_{i=1}^{n} T_i = n - 1 \times T_L + T_S$$

The basic clock for the definition of [ms] is the frame sync signal of the uncompressed audio interface.

Note: For maximum audio quality it is recommended to keep the skew between the IOM-2 and the SIO time base as small as possible, i.e. to adjust T_L in the above definition as close to 10 ms as possible. In an application with the VCP from 8 $\times$ 8 (formerly IIT) like in the Siemens/8 $\times$ 8 demonstration board design, the SIO interrupt period is locked to the IOM-2 time base after a call is setup, so no compensation on the uncompressed audio needs to be done by the JADE any more. This ensures the maximum possible audio quality.

7 Electrical Specification

7.1 Absolute Maximum Ratings

Table 20

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Supply voltage	V_{DD}	– 0.5 to 4.2	V
Supply voltage	V_{DDA}	– 0.5 to 4.2	V
Supply voltage	V_{DDP}	– 0.5 to 6.0	V
Voltage of pin with respect to ground: XTAL1, XTAL2	V_S	– 0.4 to $V_{DD} + 0.5$	V
Voltage of any other pin with respect to ground	V_S	If $V_{DDP} < 3$ V: – 0.4 to $V_{DD} + 0.5$ If $V_{DDP} > 3$ V: – 0.4 to $V_{DDP} + 0.5$	V V

ESD-integrity is 500 V.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Conditions

V_{DD} = 3.0 to 3.6 V, V_{DDP} = 4.5 to 5.5 V, V_{SS} = 0 V

V_{DDA} = 3.0 to 3.6 V, V_{SSA} = 0 V

V_{DDAP} = 3.0 to 3.6 V, V_{SSAP} = 0 V

Note: In the operating range the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Conditions: V_{DD} = 3.0 to 3.6 V, V_{DDP} = 4.5 to 5.5 V, V_{SS} = 0 V, T_A = 0 to + 70 °C.

All pins except XTAL1, XTAL2:

Table 21

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-level input voltage	V_{IH}	2.0		V	
Low-level input voltage	V_{IL}		0.8	V	
High-level output voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 7 mA pins for DU, DD, SR and ST (50 pF) I_{OL} = 5 mA pins CA(0:15), CD(0:15), INTN, INTRN (30pF) I_{OL} = 2 mA all others (30 pF)
Input leakage current	I_{LI}	– 1	1	µA	0 V < V_{IN} < V_{DDA} for XTAL1 0 V < V_{IN} < V_{DD} for CD(0:15) 0 V < V_{IN} < V_{DDP} for all others
Output leakage current	I_{LO}	–10	10	µA	0 V < V_{OUT} < V_{DDA} for XTAL2 0 V < V_{OUT} < V_{DD} for CA(0:15), CD(0:15), $\overline{CPS}$, $\overline{CDS}$, $\overline{CWR}$, $\overline{CRD}$ 0 V < V_{OUT} < V_{DD} for all others
V_{DD} + V_{DDA} supply current	I_{DDS}		90	mA	
V_{DDP} supply current	I_{DDPS}		1	mA	

The power supply on voltage on V_{DD} – V_{SS} and V_{DDA} – V_{SSA} **must be applied after** the power supply on V_{DDP} /V_{SSP} is applied (or at the same time as V_{DD} is applied). If this is not accomplished, the device may be damaged permanently.

Applying voltages to signal pins when power supply is not active (circuit not under bias) may cause damage – refer to paragraph “Absolute Maximum Ratings”.

When power supply is switched on, the pads do not reach their stable bias until after 2 µs (maximum).

7.4 Capacitances

Table 22

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance	C_{IN}		7	pF	
I/O capacitance	$C_{I/O}$		7	pF	
Load capacitance	C_{LD}		93/7 [1)]	pF	XTAL1,2

7.5 Oscillator Circuit

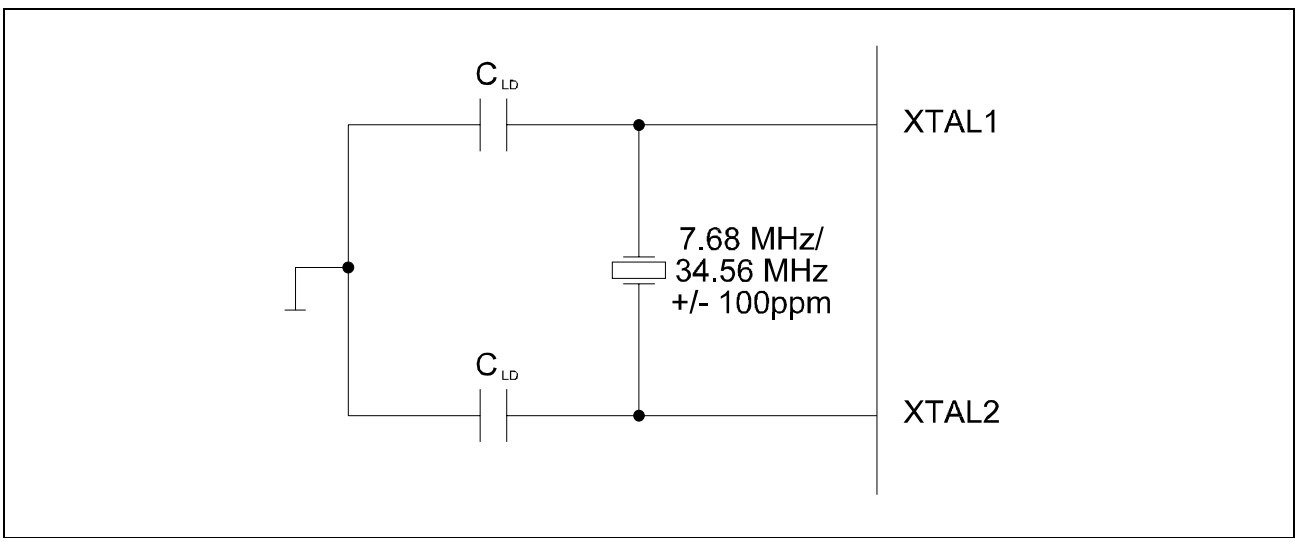


Figure 54

7.6 XTAL 1,2 Recommended Typical Crystal Parameters

Table 23

Parameter	Symbol	Limit Values	Unit
Motional capacitance	C_1	17	fF
Shunt	C_0	5	pF
Load	C_L	≤ 23/42 [1)]	pF
Resonance resistance	R_r	recommended 50/80 [1)]	Ohm

[1)] First value for 7.68 MHz crystal (using internal PLL), second value for 34.56 MHz crystal (using bypass mode).

Note: The 34.56 MHz crystal must be of the fundamental type.

7.7 AC Characteristics

7.7.1 Testing Waveform

Conditions as above (Recommended Operating Conditions) at T_A = 0 to 70 °C.

Inputs are driven to 2.4 V for a logical “1” and to 0.4 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC testing input/output waveforms are shown in **Figure 55**.

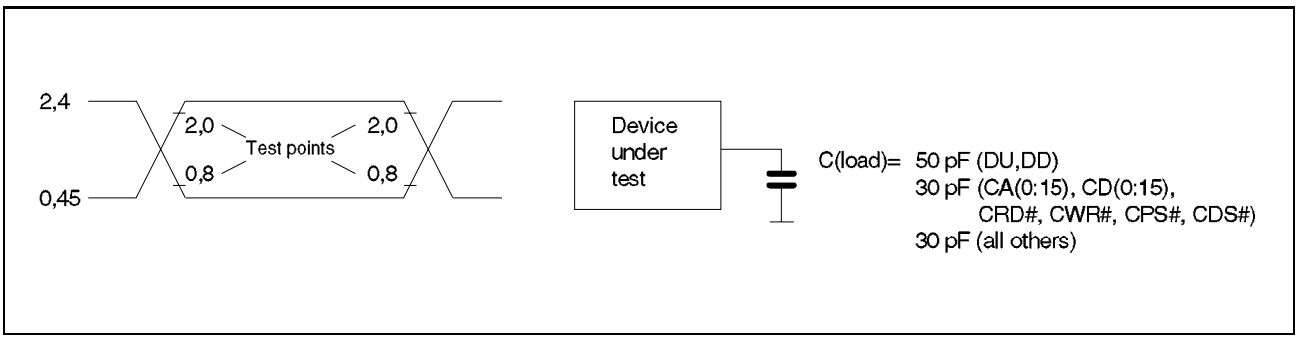


Figure 55

7.7.2 Parallel Host Interface Timing

Siemens/Intel Bus Mode

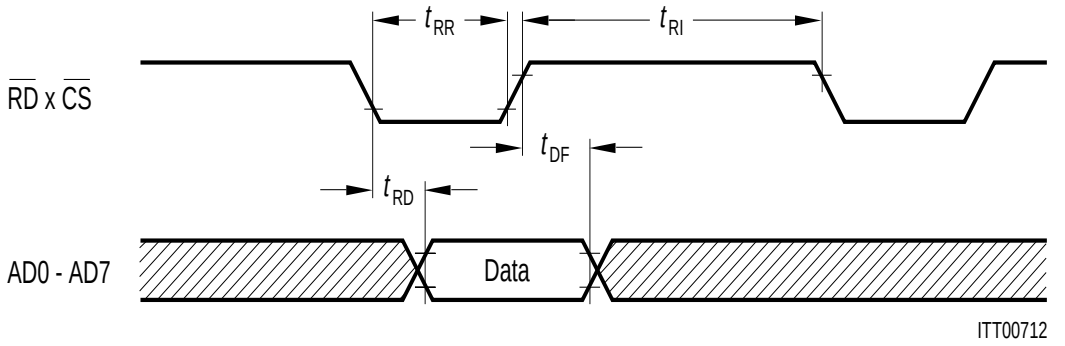


Figure 56 Microprocessor Read Timing

Figure 57 Microprocessor Write Timing

Figure 58 Multiplexed Address Timing

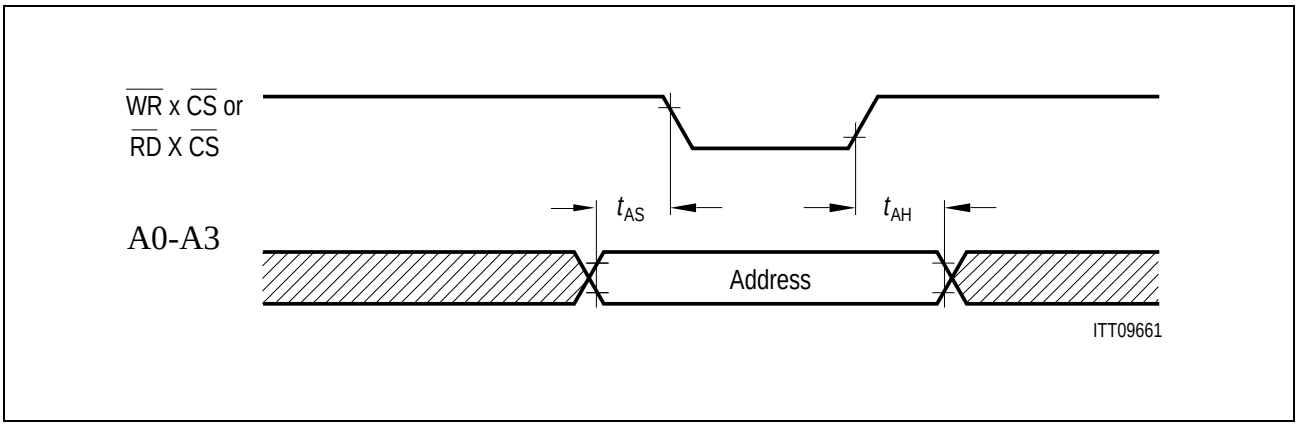


Figure 59 Non-Multiplexed Address Timing

Motorola Bus Mode

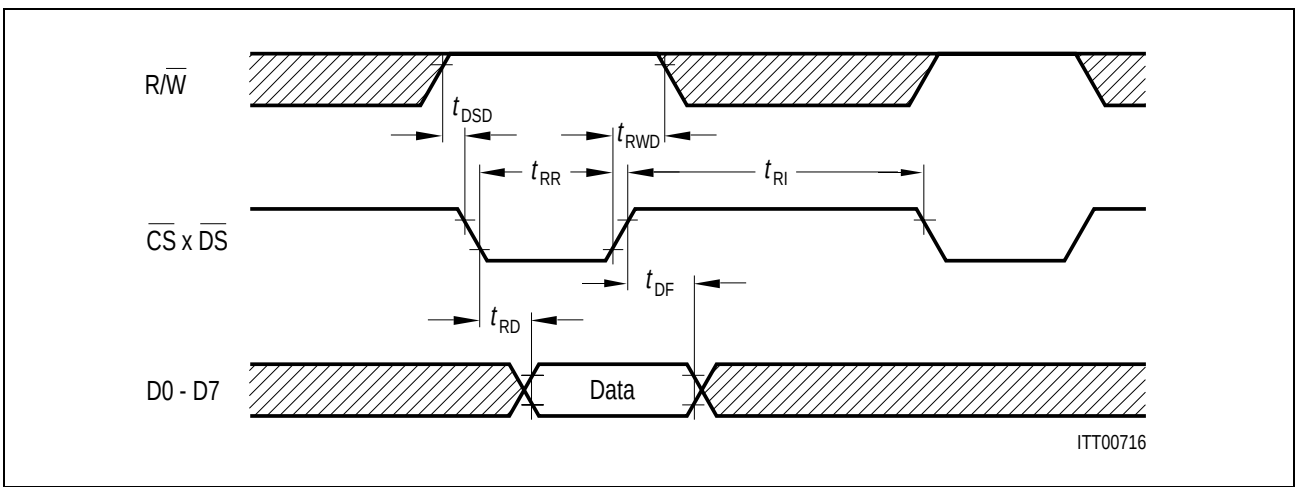


Figure 60 Microprocessor Read Timing

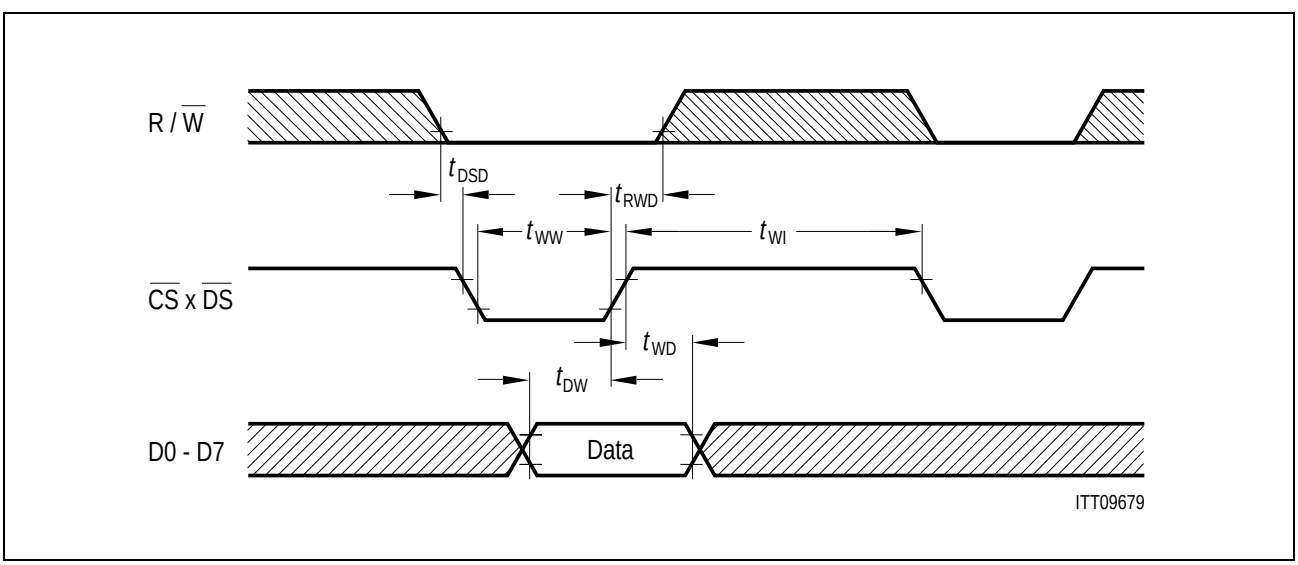


Figure 61 Microprocessor Write Timing

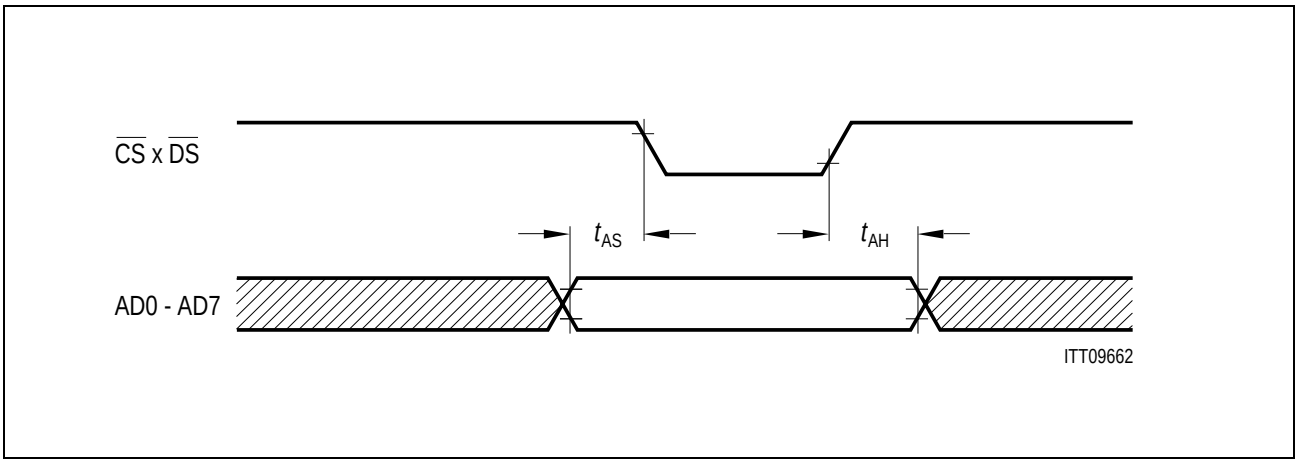


Figure 62 Non-Multiplexed Address Timing

Table 24

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time	t_{AS}	25		ns
Address hold time	t_{AH}	10		ns
ALE guard time	t_{AD}	15		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive	t_{RWD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns

Interrupt Release Timing

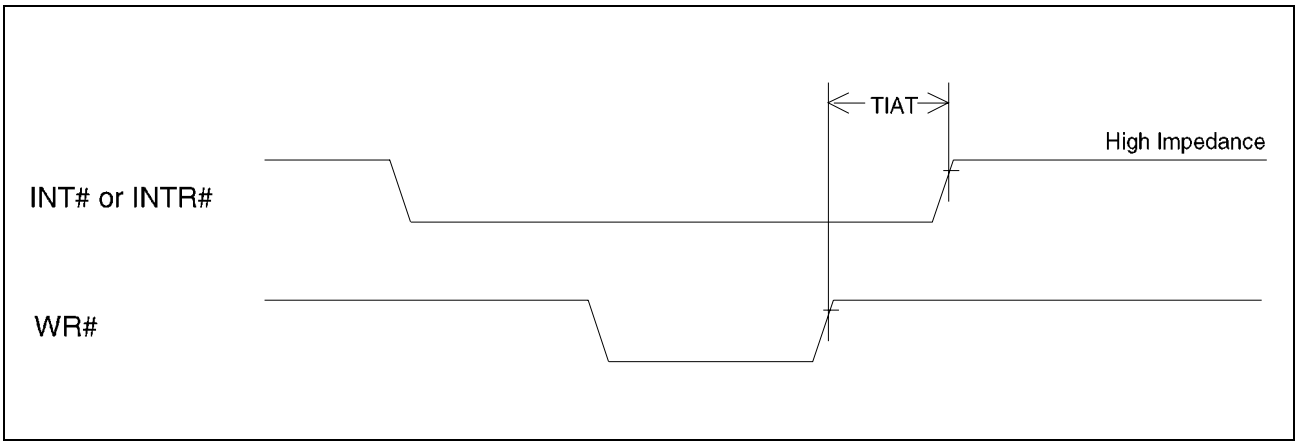


Figure 63

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Interrupt acknowledge to high-impedance	t_{IAT}		100	ns

7.7.3 IOM®-2 Interface Timing

IOM®-2 (PCM) Timing with Single Rate DCL

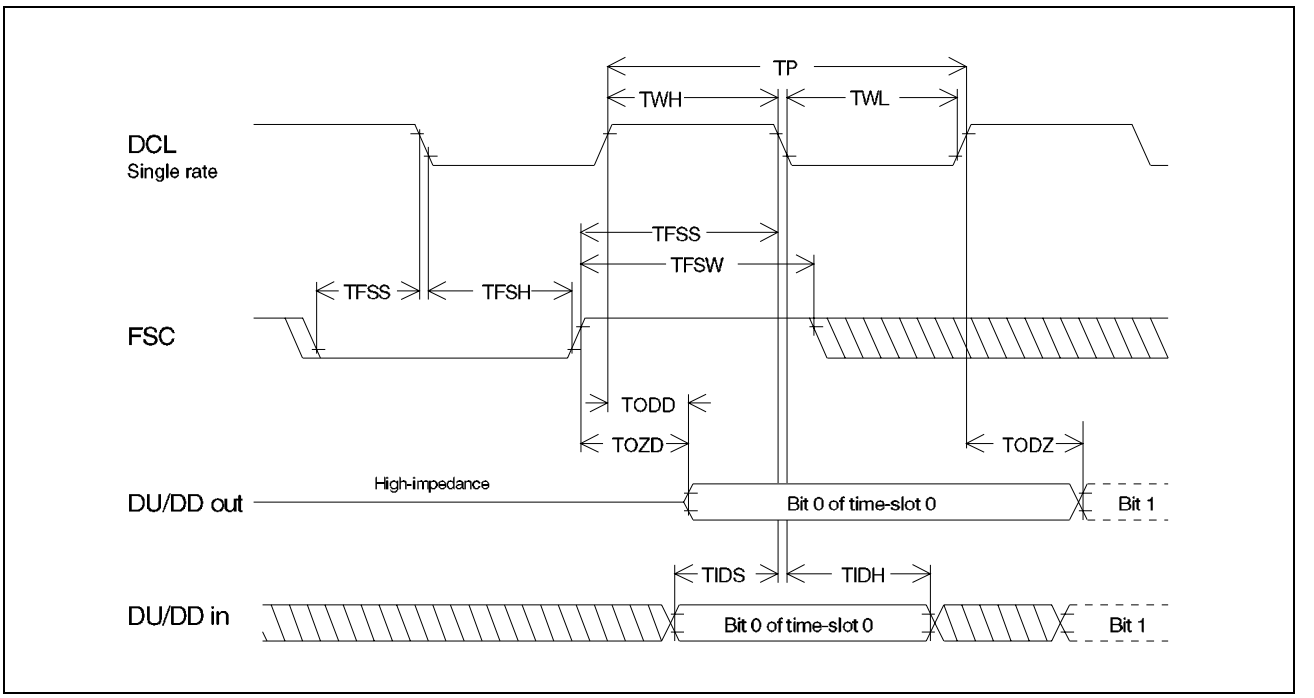


Figure 64

Table 25

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DCL period	t_P	244		ns
DCL high	t_{WH}	100		ns
DCL low	t_{WL}	100		ns
Frame sync setup	t_{FSS}	120		ns
Frame sync hold	t_{FSH}	40		ns
Frame sync width	t_{FSW}	40		ns
Output data delay from FSC (if $t_{OZD} < t_{ODD}$)	t_{OZD}		100	ns
Output data delay from DCL (if $t_{ODD} < t_{OZD}$)	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

IOM®-2 Timing with Double Rate DCL

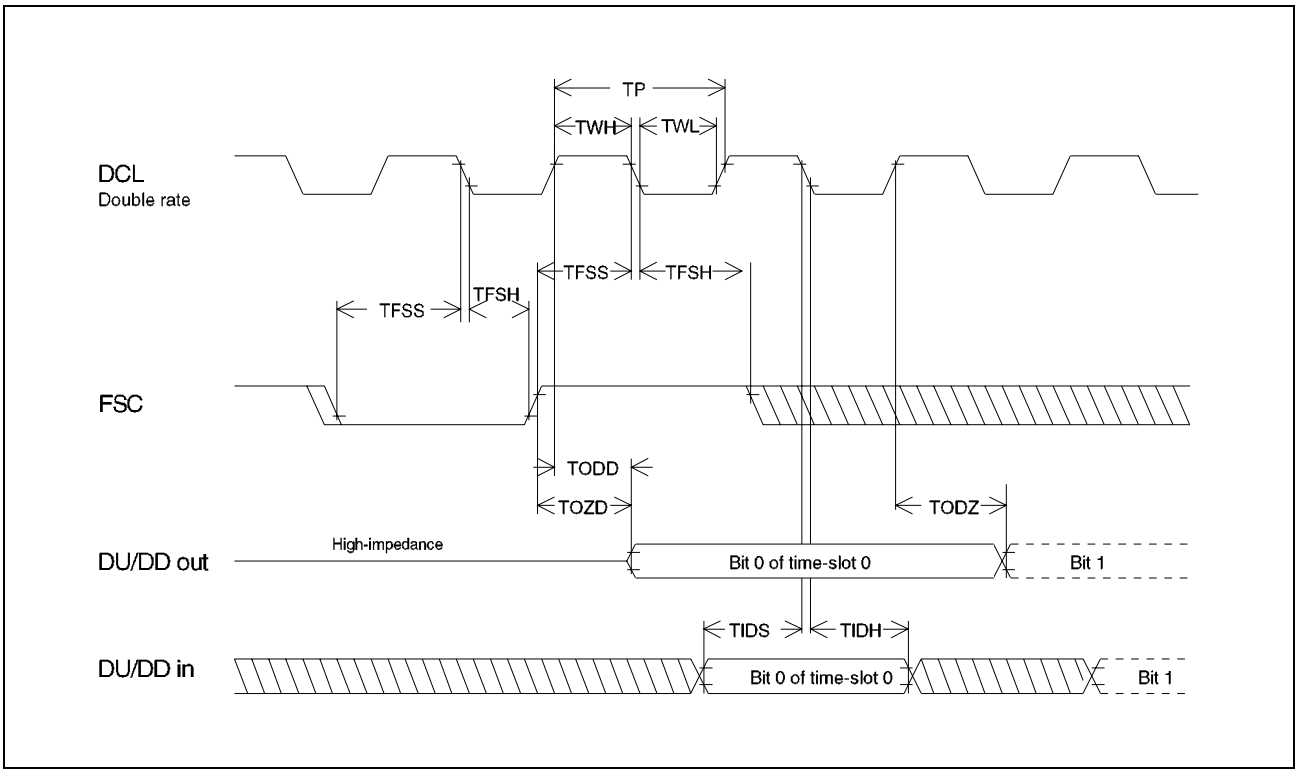


Figure 65

Table 26

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DCL period	t_P	244		ns
DCL high	t_{WH}	100		ns
DCL low	t_{WL}	100		ns
Frame sync setup	t_{FSS}	40		ns
Frame sync hold	t_{FSH}	40		ns
Output data from high impedance to active	t_{OZD}		100	ns
Output data delay from clock	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

7.7.4 Serial Audio Interface Timing

Serial Clock

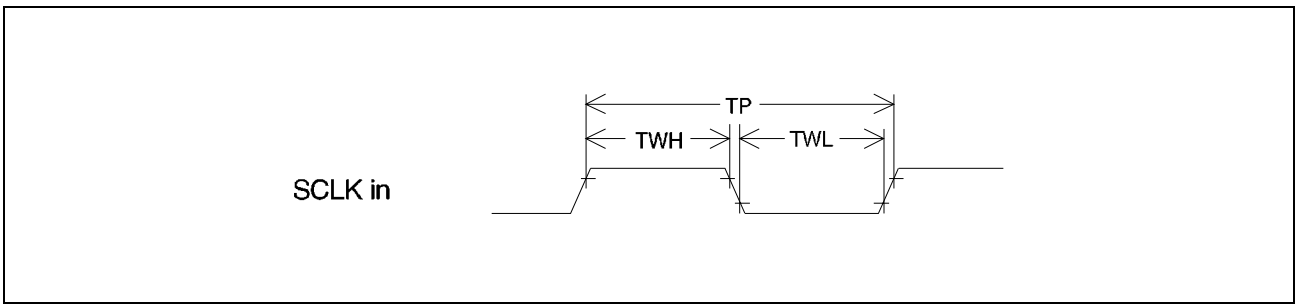


Figure 66

Table 27

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK period	t_P	244		ns
SCLK high	t_{WH}	100		ns
SCLK low	t_{WL}	100		ns

Serial Output Timing

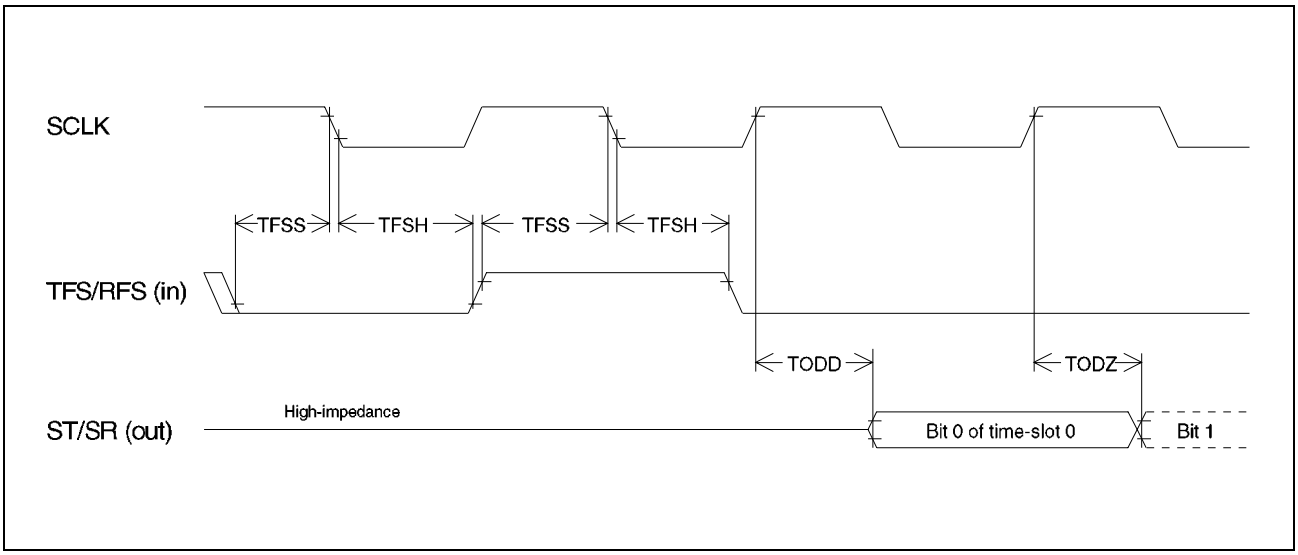


Figure 67

Table 28

Parameter	Symbol	Limit Values		Unit
		min.	max.	
TFS/RFS setup	t_{FSS}	40		ns
TFS/RFS hold	t_{FSH}	40		ns
Output data delay from clock	t_{ODD}		100	ns
Output data from active to high impedance	t_{ODZ}		80	ns

Serial Input Timing

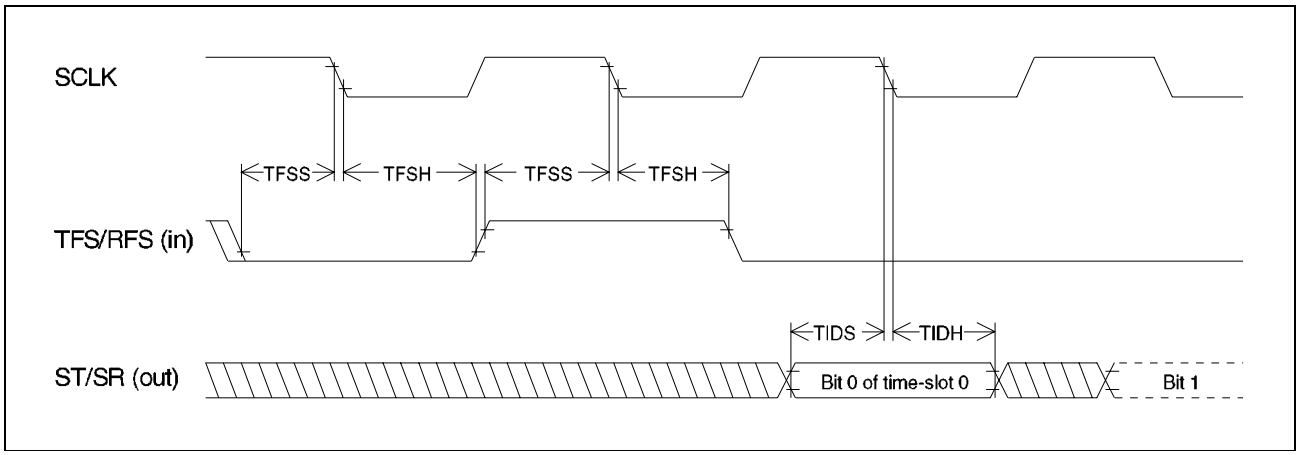


Figure 68

Table 29

Parameter	Symbol	Limit Values		Unit
		min.	max.	
TFS/RFS setup	t_{FSS}	40		ns
TFS/RFS hold	t_{FSH}	40		ns
Input data setup	t_{IDS}	20		ns
Input data hold	t_{IDH}	40		ns

TFS/RFS Output Timing

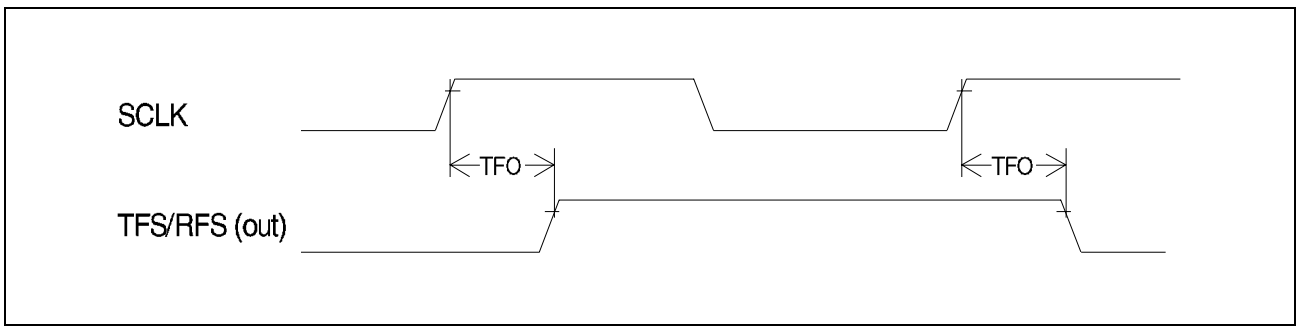


Figure 69

Parameter	Symbol	Limit Values		Unit
		min.	max.	
TFS/RFS out	t_{FO}		40	ns

7.7.5 External Memory Interface

No external SRAM needs to be connected to the JADE, since it has all memories on chip.

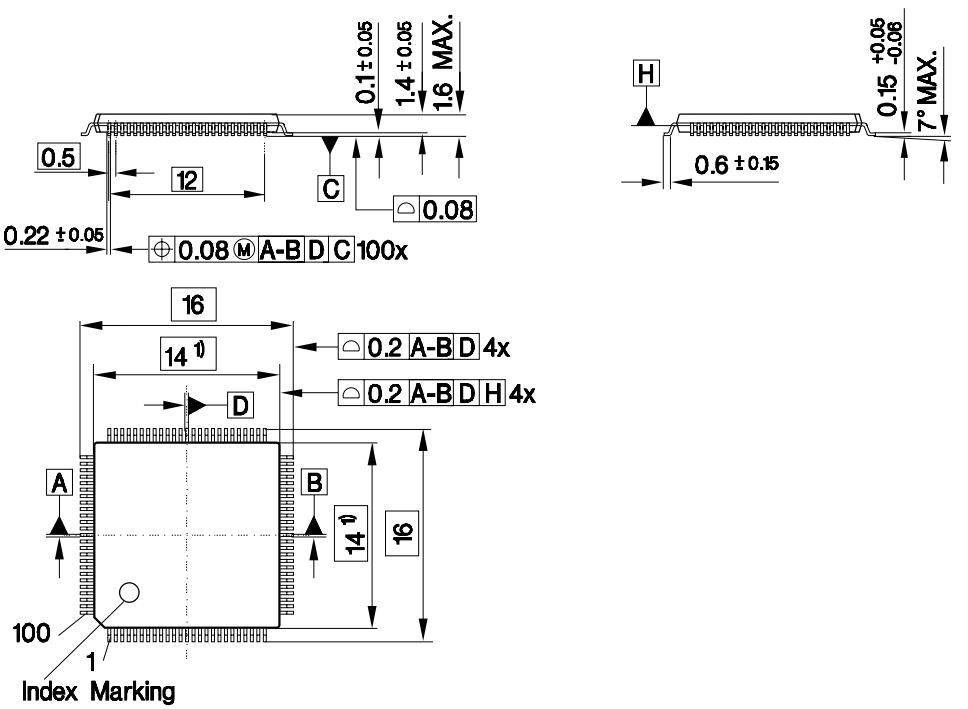
Nevertheless, an external memory interface is implemented for development purpose only.

The timing of this interface is not part of the test procedure for the JADE, and so not specified at this point. For development purpose especially tested devices (including external memory interface test) are available from Siemens on request in small quantities. These devices are working under special conditions such as e.g. higher supply voltage.

8 Package Outline

P-TQFP-100 package with size 14 × 14 mm, pitch 0.5 mm, height 1.4 mm.

P-TQFP-100
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPP05614

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm