AN1235
APPLICATION NOTE

ASD™ , IPAD™

FLIP-CHIP: PACKAGE DESCRIPTION AND RECOMMENDATIONS FOR USE

I - INTRODUCTION

The competitive market of portable equipment, notably the mobile phone market, is driven by a challenging development of highly integrated products. To allow manufacturers of portable equipment to reduce the dimension of their products, **STMicroelectronics** has developped packages with reduced size, thickness and weight in the form of the Flip-Chip.
The electrical performance of such components in Flip-Chip are improved thanks to shorter connections than the ones in standard plastic packages (as TSSOP, SSOP or BGA).

This **Flip-Chip** package family has been designed to fulfill the same quality levels and the same reliability performances as standard semiconductor plastic packages. That means these new flip-chip packages have to be considered as new surface mount devices which will be assembled on a printed circuit board without any special or additionnal process steps required. In particular this package does not require any extra underfill to increase reliability performances or to protect the device.
This package is reworkable and is compatible with existing pick and place equipment for board mounting.

The purpose of this document is to describe the Flip-Chip features and to specify how our customers can use them.

This application note addresses the following items :

- Product description
- Mechanical description
- Packing specifications and labelling description
- Recommended storage and shipping instructions
- Soldering assembly recommendations
- User responsability and returns
- Changes
- Delivery quantity
- Quality

II - PRODUCT DESCRIPTION

The Flip-Chips are manufactured with a wafer level process that **STMicroelectronics** has developed by attaching solder balls on I/Os pads of the active wafer side, thus allowing bumped dice to be produced. The I/O contact layout can be either matrix shape or set in periphery. No redistribution layer is used. This allows parasitic inductances coming from the redistribution metal tracks to be minimized.

The eutectic Sn63Pb37 bumps make this package compatible with standard reflow processes. The Bumps' dimension (315 µm bumps diameter) allows the pick and place process to be compatible with existing equipment (in particular with equipment used for BGA packages) and makes it also compatible with the PCB design rules used for standard ICs.

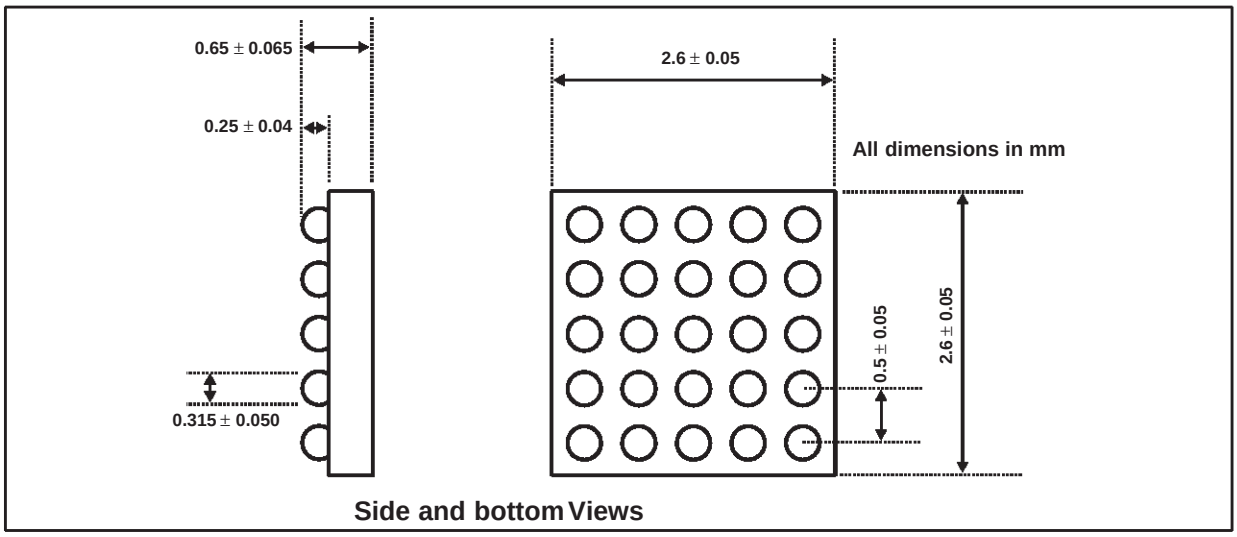
These components are delivered in tape&reel packing with the bumps turned down (placed on the bottom of the carrier tape cavity). The other face of the component is flat and allows picking as in the standard SMD packages.

Devices are 100% electrically tested before packing. The product references are marked on the flat side of the device.

III - MECHANICAL DESCRIPTION

Mechanical dimensions of Flip-Chips are provided through a product example in figure 1 below. Bumps are in Sn63Pb37 alloy with an eutectic melting point of 183°C. Die size and bump count are adapted to the connection requirements.

Fig. 1: Mechanical dimensions of a 5 x 5 bumps matrix array (sample)



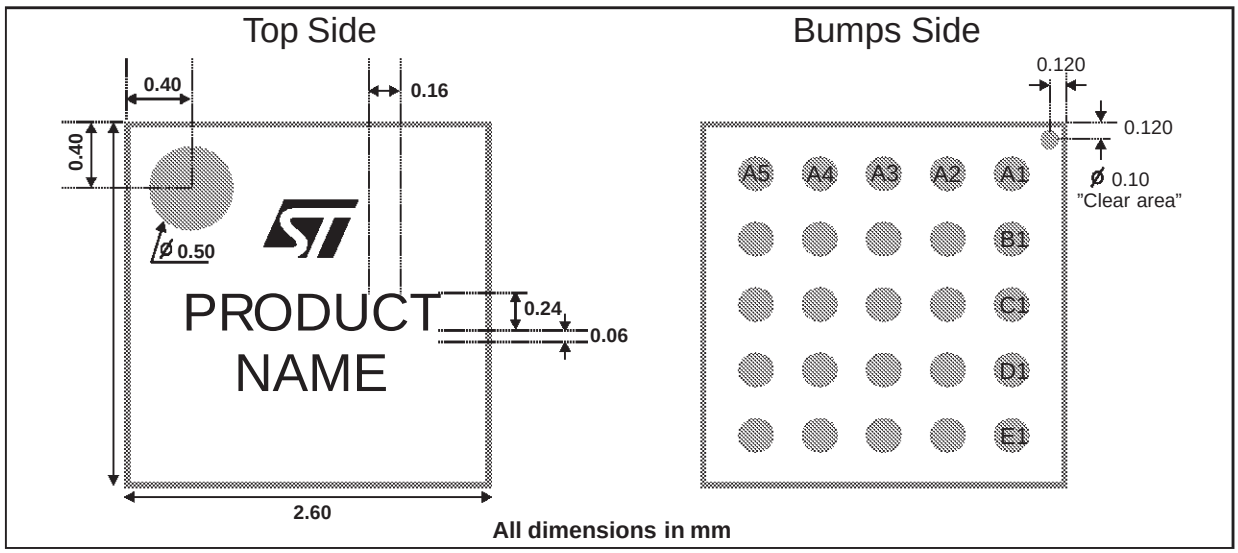
Note: The package height of 0.65mm is valid for a die thickness of 0.40mm. With a die thickness of 0.64mm the total height would be 0.89mm.

The Flip-Chip tolerance on bumps diameter and bumps height are very narrow. This constant bumps shape insures a good coplanarity between bumps. Optical measurements performed through vertical focuses show a bump plus die coplanarity below 80µm.

The product marking for both bumps side and top side is shown on figure 2 below (product example). The Flip-Chip has a pin marker (A1) on both the top and bottom sides so that the face of the component can be easily determined before and after assembly.The dots marked both on the top side and on the bumps side have been designed so that they can be detected by standard vision systems.

Marking dimensions are, of course, linked to the die size.

Fig. 2: Flip-Chip marking example for a 5x5 bumps matrix array.



IV - PACKING SPECIFICATIONS & LABELLING DESCRIPTION

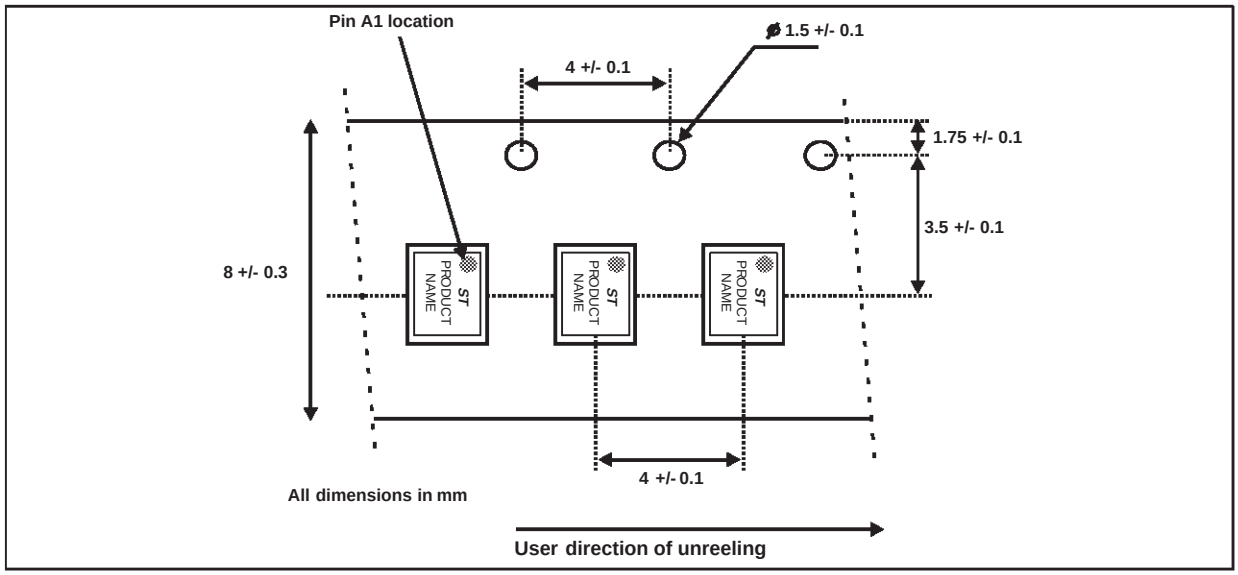
The Flip-Chip products are delivered in tape & reel to be fully compatible with standard high volume SMD components. The features of tape & reel materials are in accordance with EIA-481-1, EIA481-1-A and IEC286-3 standards. All features not specified in this section are in accordance with EIA-481-1, EIA481-1-A and IEC286-3 standards.

IV.1 - Carrier tape

The Flip-Chips are placed in carrier tape with bumps side facing the bottom of the cavity so that the components can be picked-up by their top side. No flipping of the package is necessary for mounting on PCB. The products are positionned in the carrier tape with pin A1 nearest the round sprocket hole. Carrier tape mechanical dimensions and Flip-Chip positionning is shown in figure 3 below.

Note: 12 mm carrier tape width may be used for a larger die size to be in line with EIA standards.

Fig. 3: Layout of Flip-Chips in carrier tape (8mm carrier tape sample)



The cavities in the carrier tape have been designed to avoid any damage to the components. No hole is present in the cavity in order to avoid any impact or any external contamination to the solder bumps.

For Flip-Chips larger than 2 mm x 2 mm, the 8 mm width and 4 mm pitch carrier tape is designed to allow a maximum component tilt of 5° and a maximum lateral movement of 0.3 mm.

The embossed carrier tape is in a black conductive material (surface resistivity within 10E4 and 10E8 ohm/square). Conductivity is guaranteed to be constant and not affected by shelf life or humidity. The material will neither break when bent nor will rub off, powder, flake.

The carrier tape tensile strength is higher than 40N.

IV.2 - Cover tape

The carrier tape is sealed with a transparent, antistatic (surface resistivity within 10E5 ohm/square and 10E12 ohm/square) polyester film cover tape with a heat activated adhesive. The cover tape tensile strength is higher than 10N.

The peeling force of the cover tape is between 0.1N and 0.7N by performing the testing method EIA 481-1 and IEC 286-3: cover tape is peeled back in the direction opposite to the carrier tape travel; the angle between the cover tape and the carrier tape is between 165 and 180 degrees and the test is done at a speed of 120 +/- 10 % mm/minute.

IV.3 - Reels

The sealed carrier tape with the Flip-Chip is reeled on 7 inch reels (see figure 4 for reel mechanical dimensions). These reels are compliant with EIA 481-1 standard. Each reel contains 5000 components. In compliance with the IEC286-3, each reel contains a maximum of 10 empty cavities with no more than 2 successive empty cavities. Each reel may contain components coming from 2 different wafer lots. The reel is made of an antistatic polystyrene material.

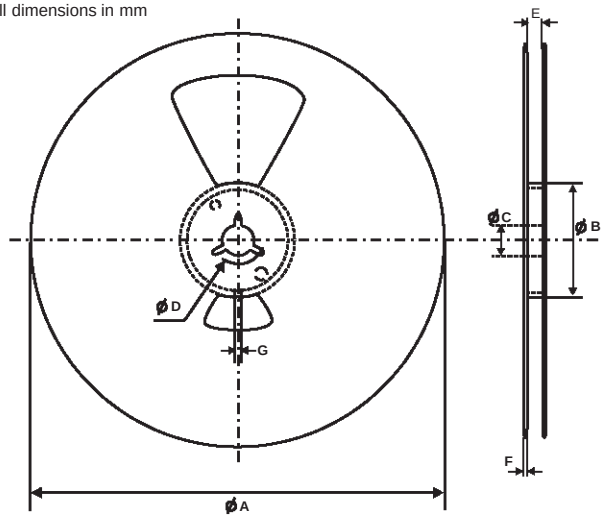
Each reel has a minimum leader of 600 mm and a minimum trailer of 160 mm (compliant with EIA 481-1 & IEC 286-3 standards). The leader makes up a portion of carrier tape with empty cavities and sealed by cover tape at the beginning of the reel (External side). The leader is affixed to the last turn of the carrier tape by using adhesive tape. The trailer is at the end of the reel and consists of empty, sealed cavities.

Fig. 4: 7” reel mechanical dimensions

Material: ANTISTATIC POLYSTYRENE

A	B	C	D	E	F	G
ø178 max	ø 60 ± 1	ø 13 ± 0.2	ø 20.2 min	8.4 ± 1.5	1.6 ± 0.5	4 ± 0.25

All dimensions in mm



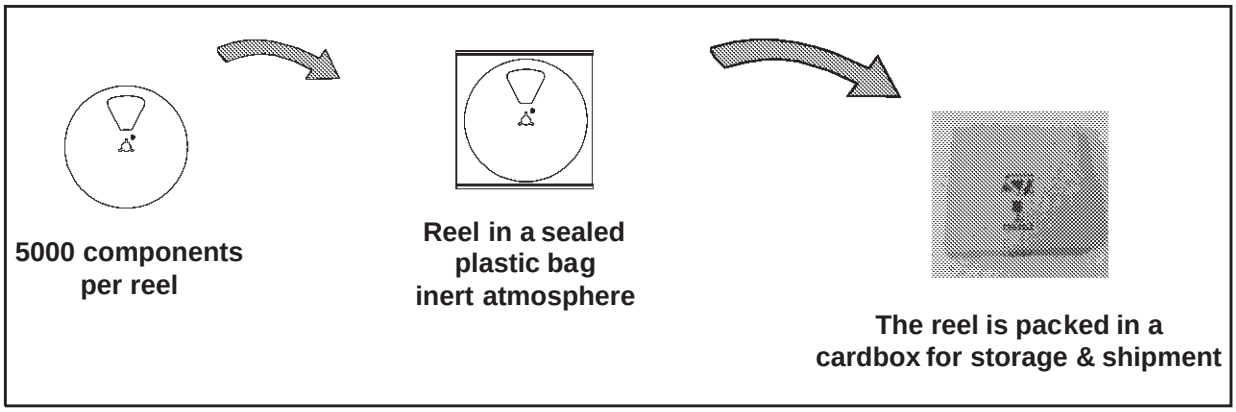
IV.4 - Final packing

Each reel is heat sealed under inert atmosphere in a transparent, recyclable and antistatic polyethylene bag (minimum of 4 mils material thickness).

Reels are then packed in cardboard boxes.

The complete description for packing is shown on figure 5.

Fig. 5: Packing flow chart



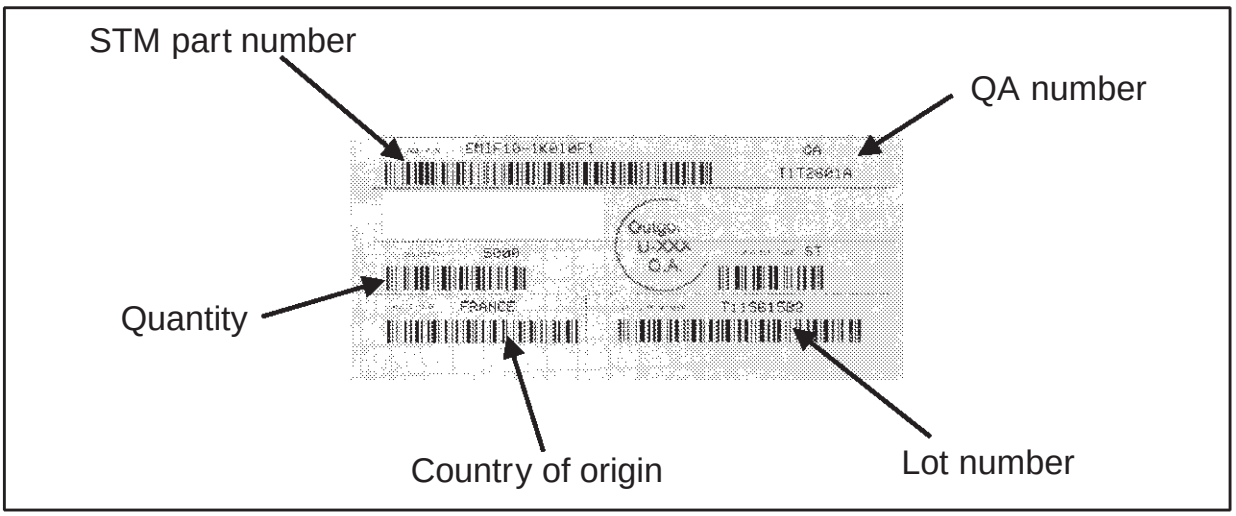
IV.5 - Labelling

To ensure components' traceability, labels are stuck on the reels and the cardboard box. The seven inch reels and the cardboard box are identified by labels including part number, shipped quantity and traceability references (Fig. 6).

The traceability is ensured for each production lot and each shipment lot through the labeling.

The QA number printed on the labels ensures backward traceability from the lot received by the customer to each step of the process: In / Out dates and quantity at diffusion, assembly, test and final store. Likewise, forward traceability is able to trace a lot history from the wafer fab to the customer's location.

Fig. 6: Example of a reel label



V- RECOMMENDED STORAGE, SHIPPING INSTRUCTIONS AND DESCRIPTIONS

Flip-Chip reels are packed under inert N2 atmosphere in a sealed bag. For shipment and handling, reels are packed in a cardboard box.

STMicroelectronics thus recommends the following shipping and storage conditions :

- relative humidity between 15% and 70%
- temperature range from -5°C to 35°C

Components in a non opened sealed bag can be stored 6 months after shipment.

Components in tape&reel must be protected from exposure to direct sunlight.

Moisture sensitivity level (MSL as per JEDEC J-STD-020A) is not applicable to Flip-Chip devices since there is no plastic encapsulation and so far no risk of moisture absorption and related possible package cracks.

VI - SOLDERING ASSEMBLY RECOMMENDATIONS

VI.1 - PCB design recommendations

For optimum electrical performance and highly reliable solder joints, **STMicroelectronics** recommends the PCB design guidelines listed in table 1.

Table. 1: PCB design recommendations

PCB pad design	Non Solder Mask Defined Micro via under bump allowed
PCB pad size	∅ = 300µm max (circular) - 250µm recommended
Solder mask opening	∅ = 340µm min (for 300µm diameter pad)
PCB pad finishing	Cu - Ni (2-6µm) - Au (0.2µm max)

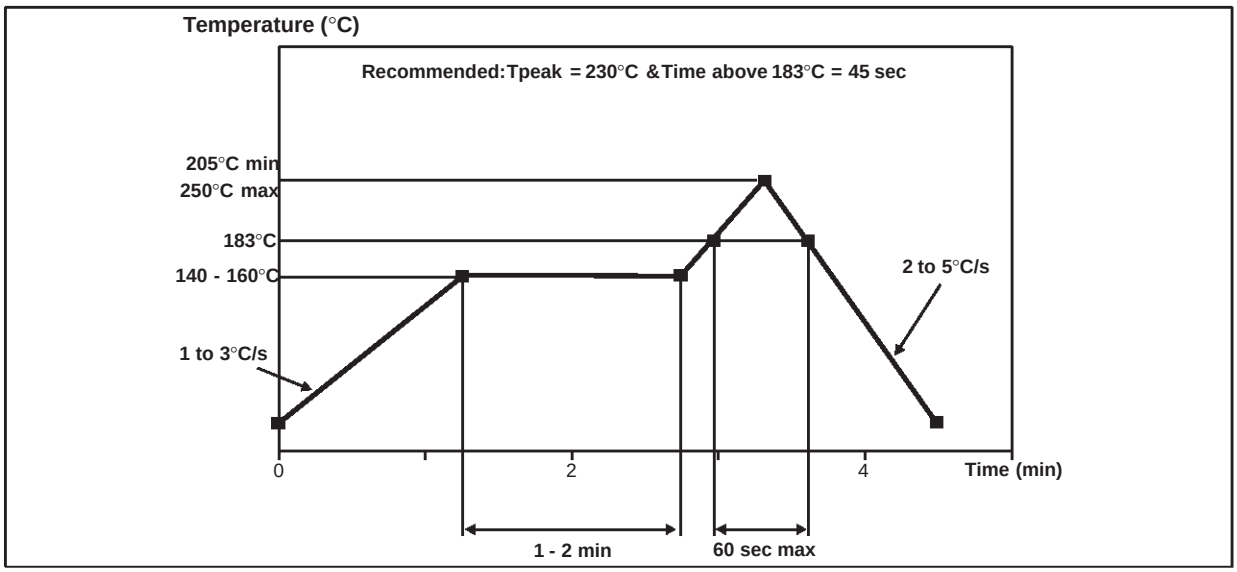
To optimize the natural self centering effect of Flip-Chips on PCB, PCB pad positioning and size have to be properly designed.

Note: a too thick gold layer finishing on the PCB pad is not recommended (low joint reliability).

VI.2 - PCB assembly guidelines

For Flip-Chip mounting on the PCB, **STMicroelectronics** recommends the use of a solder stencil aperture of 330 x 330µm maximum and a typical stencil thickness of 125µm. Flip-Chips are fully compatible with the use of eutectic Sn63Pb37 solder paste with no clean flux. ST's recommendations for Flip-Chip board mounting are illustrated on the soldering reflow profile shown in figure 7.

Fig. 7: Recommended soldering reflow profile for Flip-Chip mounting on PCB



Dwell time in the soldering zone (with temperature higher than 183°C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 250°C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, specially above 150°C.

Flip-Chips are able to withstand twice the previous recommended reflow profile in order to be compatible with a double reflow when SMDs are mounted on both sides of the PCB.
A maximum of two soldering reflows are allowed for these packages.

The use of a no clean flux is highly recommended to avoid any cleaning operation. In order to prevent any bump cracks, ultrasonic cleaning methods are not recommended.

VI.3 - Underfilling

Underfilling is not needed for Flip-Chips but the devices can withstand the dispense of an underfill if the process temperature does not exceed 175°C and if the process time is short (typically 5 minutes).

VI.4 - Manual rework

Flip-Chips are able to tolerate one repair in addition to the two reflows mentionned in section VI.2.

As for other BGA type packages, the use of laser systems is the most suitable form for Flip-Chip repair. Manual hot gas soldering is acceptable but iron soldering is not recommended.

For manual rework, the maximum temperature allowed is 250°C and dwell time must not exceed 30 seconds.
Component replacement is preferred for such packages than manual rework.

VII - USER RESPONSABILITY AND RETURNS

STMicroelectronics guarantees the excellent quality of its Flip-Chips in respect of the instructions provided in this application note. For more information, the reader can consult the “Sure 7” Quality and Reliability brochure.

In the event that parts are found defective by the customer, the parts should be returned according to the **ST** standard procedure within 60 days after the date of reception.

VIII - CHANGES

STMicroelectronics reserves the right to implement minor changes of geometry and manufacturing processes without prior notice. Such changes will not affect electrical characteristics of the die, the pad layout or the maximum die size. However for confirmed orders, no variation will be made without customer's approval.

IX - QUALITY

IX.1 - Electrical inspection

Products in Flip-Chip are 100% electrically probed according to the critical parameters of the ST product specification. The last operation before packing is 100% electrical testing. The other parameters are guaranteed by technology, design rules and by continuous monitoring systems.

IX.2 - Visual inspection

A visual control is performed on all manufacturing lots according to the MIL-STD-883 method 2010.

X - CONCLUSION

Flip-chip packages have been developped by **STMicroelectronics** for electronic applications where integration and performance are the main concerns of designers.

STMicroelectronics Flip-Chips offer :

- **remarkable board space saving** (package size equal to die size and total height less than 0.700mm)
- **enhanced electrical performance** (minimized parasitic inductance due to very short electrical paths and absence of redistribution layer)
- **high reliability** due to integration of a whole function traditionally based on discrete interconnected components.

Flip-chips are delivered in tape and reel and are fully compatible with other high volume SMD components (standard plastic packages or CSP/BGA packages) regarding existing pick and place equipment, standard solder reflow assembly equipment and standard PCB techniques.