

NVP2040 Data Sheet

CCD Camera Image Signal Processor



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Make sure to check and use an updated version of the Data sheet.**

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REV 0.1



Interlaced CCD Image Signal Processor

NVP2040 is an image signal processor(ISP) which outputs CVBS or S-Video data format after receiving color filter array(CFA) patterns from color-interlaced CCD sensor(760H), which is processed through an internal encoder and DAC. NVP2040 provides high image quality than ever by supporting 600TV lines resolution. For providing stable color reproduction, NVP2040 has functions both AE which maintains the brightness and AWB which keeps in white regardless of its color temperature. Moreover, it provides OSD without external MCU to make camera control more easily. Besides, NVP2040 supports RS-485 communication for remote control, parking line and H-mirror for rear-view camera application, lens shading correction and motion detection etc for superior camera functionality.



Features

- Input : NTSC/PAL, 760H CCD format
- Output : NTSC/PAL analog S-Video or CVBS
- Programmable GAMMA processing(16 steps)
- Supports horizontal resolution 600TV lines
- De-moire
- H/V aperture
- Video adjustment (brightness, contrast, saturation and hue)
- Horizontal MIRROR
- Blemish compensation → AUTO(64 points)
- Color rolling / Breathing suppress.
- DWDR(Digital Wide Dynamic Range)
- Motion detection (Motion size : 48 x 15)
- Lens shading
- Parking Line
- OSD(English/Chinese(Simplified))
- Communication : RS-485 (Pelco-D/P, NEXTCHIP)
- Serial interface for AFE (AD9943/HD49343HNP)
- I2C Interface
- On-chip optical detector (AE/AWB)
- On-chip CCD timing generator,
- On-chip NTSC/PAL video encoder
- On-chip 2CH DAC (S-video or CVBS and IRIS)
- On-chip 1CH ADC (2CH MUX)
- 5.0V / 3.3V operation (LDO include)

Ordering Information

Device	Package	Temperature Range
NVP2040	64-TQFP	-25°C ~ 85°C

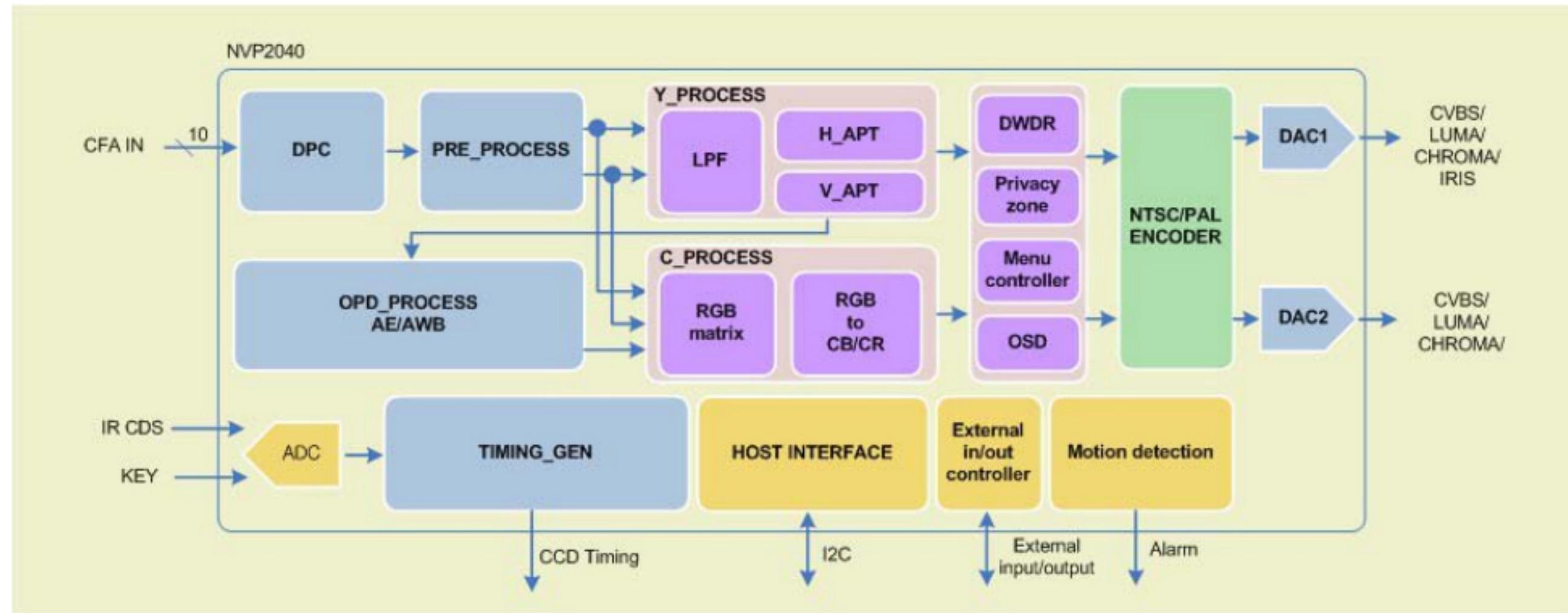
Applications

- CCD camera
- Door phone camera
- Video phone camera
- Rear-view monitoring camera

Related Products

- CCD : SONY, SHARP CCD
- AFE : AD9943/HD49343HNP
- V-Driver : NVD2014A (NEXTCHIP)

Functional Block Diagram



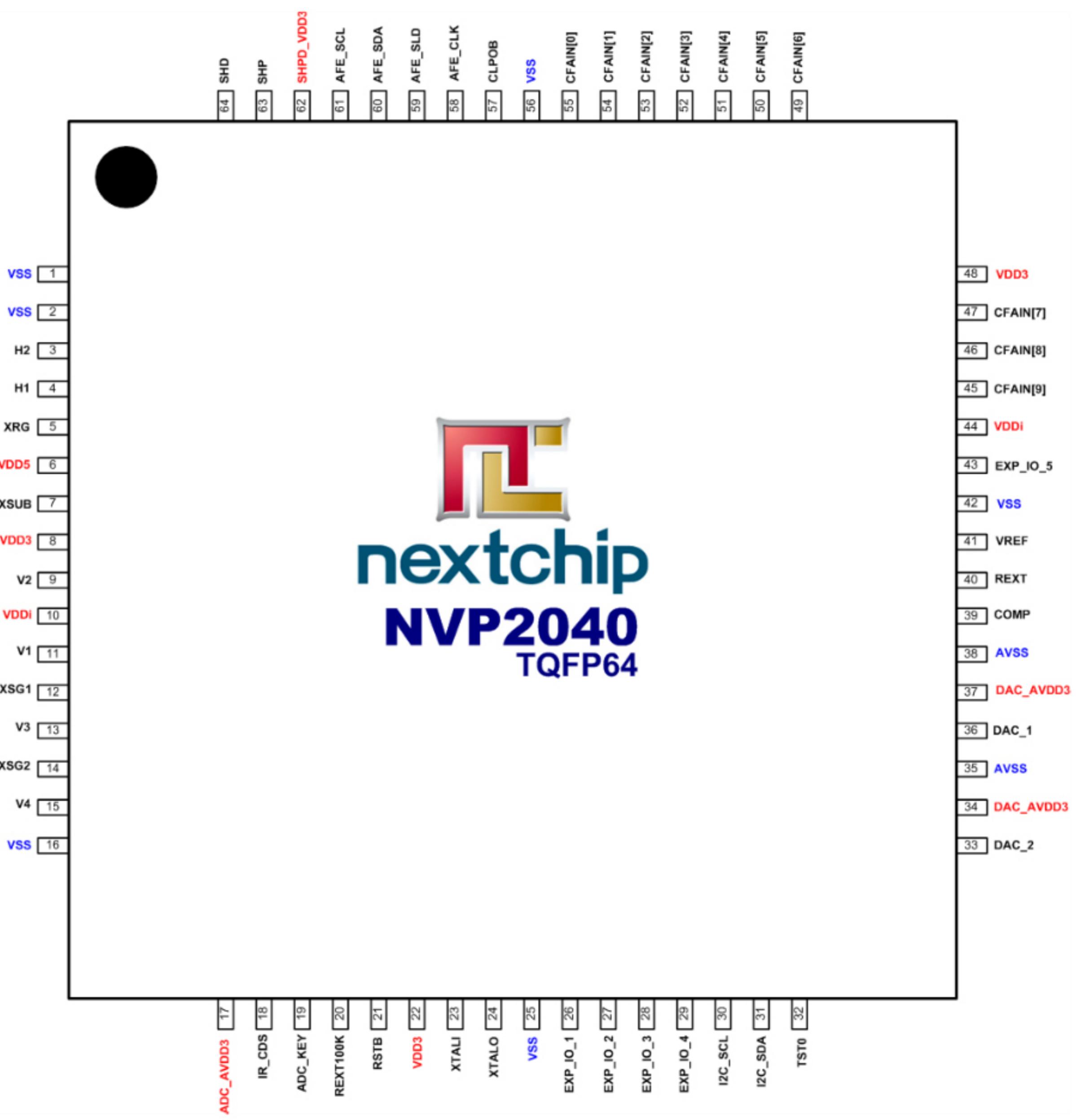
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1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	VSS	G	Digital Ground (for SHP, SHD)
2	VSS	G	Digital Ground (for XRG, H1, H2 pulse)
3	H2	O	CCD Horizontal Driving pulse 2
4	H1	O	CCD Horizontal Driving pulse 1
5	XRG	O	CCD Reset gate pulse
6	VDD5	P	5V Digital Power (for XRG, H1, H2 pulse)
7	XSUB	O	CCD shutter speed control pulse
8	VDD3	P	3.3V Digital Power
9	V2	O	CCD vertical driving pulse phase-2
10	VDDi	P	1.8V Internal Core Power(Connect to VSS via external capacitor)
11	V1	O	CCD vertical driving pulse phase-1
12	XSG1	O	CCD Read out pulse 1
13	V3	O	CCD vertical driving pulse phase-3
14	XSG2	O	CCD Read out pulse 2
15	V4	O	CCD vertical driving pulse phase-4
16	VSS	G	Digital Ground
17	ADC_AVDD3	P	ADC 3.3V Analog Power
18	IR_CDS	I	ADC IR CDS INPUT
19	ADC_KEY	I	ADC KEY INPUT
20	REXT100K	-	100Kohm external resistor
21	RSTB	I	System Reset (active low)
22	VDD3	P	3.3V Digital Power
23	XTALI	I	X-tal input(NTSC:28.6363MHz : PAL:28.375MHz)
24	XTALO	O	X-tal output
25	VSS	G	Digital Ground
26	EXP_IO_1	I/O	External input / output Pin
27	EXP_IO_2	I/O	External input / output Pin
28	EXP_IO_3	I/O	External input / output Pin
29	EXP_IO_4	I/O	External input / output Pin
30	I2C_SCL	I/O	I2C Serial Clock (EEPROM/MCU interface)
31	I2C_SDA	I/O	I2C Serial Data (EEPROM/MCU interface)
32	TST0	I	Chip Test pin
33	DAC2	O	DAC Output (LUMA/CHROMA/CVBS Output)
34	DAC_AVDD3	P	3.3V DAC Analog Power
35	VSSA	G	DAC Analog Ground
36	DAC1	O	DAC Output (LUMA/CHROMA/CVBS/IRIS Output)
37	DAC_AVDD3	P	3.3V DAC Analog Power
38	VSSA	G	DAC Analog Ground
39	COMP	-	DAC comparator reference
40	REXT	-	DAC external resistor pin($REXT(\text{ohm}) = VREFIN(V) * 7.02 / IOFS(A)$)
41	VREF	-	DAC Voltage reference
42	VSS	G	Digital Ground
43	EXP_IO_5	I/O	External input/out Pin
44	VDDi	P	1.8V Internal Core Power(Connect to VSS via external capacitor)
45	CFAIN[9]	I	CCD CFA pattern input 9
46	CFAIN[8]	I	CCD CFA pattern input 8
47	CFAIN[7]	I	CCD CFA pattern input 7

PIN NO.	SYMBOL	I/O	DESCRIPTION
48	VDD3	P	3.3V Digital Power
49	CFAIN[6]	I	CCD CFA pattern input 6
50	CFAIN[5]	I	CCD CFA pattern input 5
51	CFAIN[4]	I	CCD CFA pattern input 4
52	CFAIN[3]	I	CCD CFA pattern input 3
53	CFAIN[2]	I	CCD CFA pattern input 2
54	CFAIN[1]	I	CCD CFA pattern input 1
55	CFAIN[0]	I	CCD CFA pattern input 0
56	VSS	G	Digital Ground
57	CLPOB	O	Optical blank clamping pulse
58	AFE_CLK	O	ADC sampling clock
59	AFE_SLD	O	3-wire Serial Enable output (for AFE control)
60	AFE_SDA	O	3-wire Serial data input/output (for AFE control)
61	AFE_SCL	O	3-wire Serial interface clock output (for AFE control)
62	SHPD_VDD3	P	3.3V Digital Power
63	SHP	O	CDS sample & hold pulse for pre-charge
64	SHD	O	CDS sample & hold pulse for data

BANK 1

ADDR		REGISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0xE4	0xE4									RGB_1
0xE5	0xE5									RGB_2
0xE6	0xE6									RGB_3
0xE7	0xE7	SUC_HL_GAIN_MAX								-
0xE8	0xE8	SEL_IO_P[7:0]								
0xE9	0xE9	COLOR_OFF								SEL_IO_P[14:8]
0xEA	0xEA	AGC_MAX_SEL		-						GAMMA_SEL_USER
0xEB	0xEB									
0xEC	0xEC									
0xED	0xED				-					
0xEE	0xEE	TIM_V_OPD_OFST								-
0xEF	0xEF				-					
0xF0	0xF0				-					
0xF1	0xF1				-					
0xF2	0xF2				-					
0xF3	0xF3									AE_OFFSET_START
0xF4	0xF4									AE_OFFSET_MAX1
0xF5	0xF5									DAY_GAP
0xF6	0xF6				-					
0xF7	0xF7									LLDC_HLEDGE_TH
0xF8	0xF8									ATW1_RIGHT
0xF9	0xF9									ATW1_LEFT
0xFA	0xFA				-					
0xFB	0xFB	AWB_STA_IN								AWB_STA_OUT
0xFC	0xFC	SELI_LENS1								SELI_LENS0
0xFD	0xFD	AGC_MIDDLE								
0xFE	0xFE	AGC_ZONE								AGC_ZONE2

BANK 2

ADDR		RESISTER									DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
0xB0	0xB0									ATW2_R_MAX	
0xB1	0xB1									ATW2_B_MAX	
0xB2	0xB2									ATW2_R_MIN	
0xB3	0xB3									ATW2_B_MIN	
0xB4	0xB4									ATW2_POS_X1	
0xB5	0xB5									ATW2_POS_Y1	
0xB6	0xB6									ATW2_POS_X2	
0xB7	0xB7									ATW2_POS_Y2	
0xB8	0xB8									ATW2_DOWN	
0xB9	0xB9									ATW2_UP	
0xBA	0xBA									ATW2_RIGHT	
0xBB	0xBB									ATW2_LEFT	

3. Electrical characteristics

3.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage	-0.5	6	V
Voltage on any 3.3V input pin	3.0	3.6	V
Voltage on any 5V input pin	4.5	5.5	V
Storage temperature	-40	125	°C

3.2. Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Digital power supply voltage	VDD3 SHPD_VDD3	3.0	3.3	3.6	V
3.3V Analog power supply voltage	ADC_AVDD3 DAC_AVDD3	3.0	3.3	3.6	V
5.0V Digital power supply voltage	VDD5	4.5	5.0	5.5	V
Industrial temperature range	T _A	-25	-	85	°C

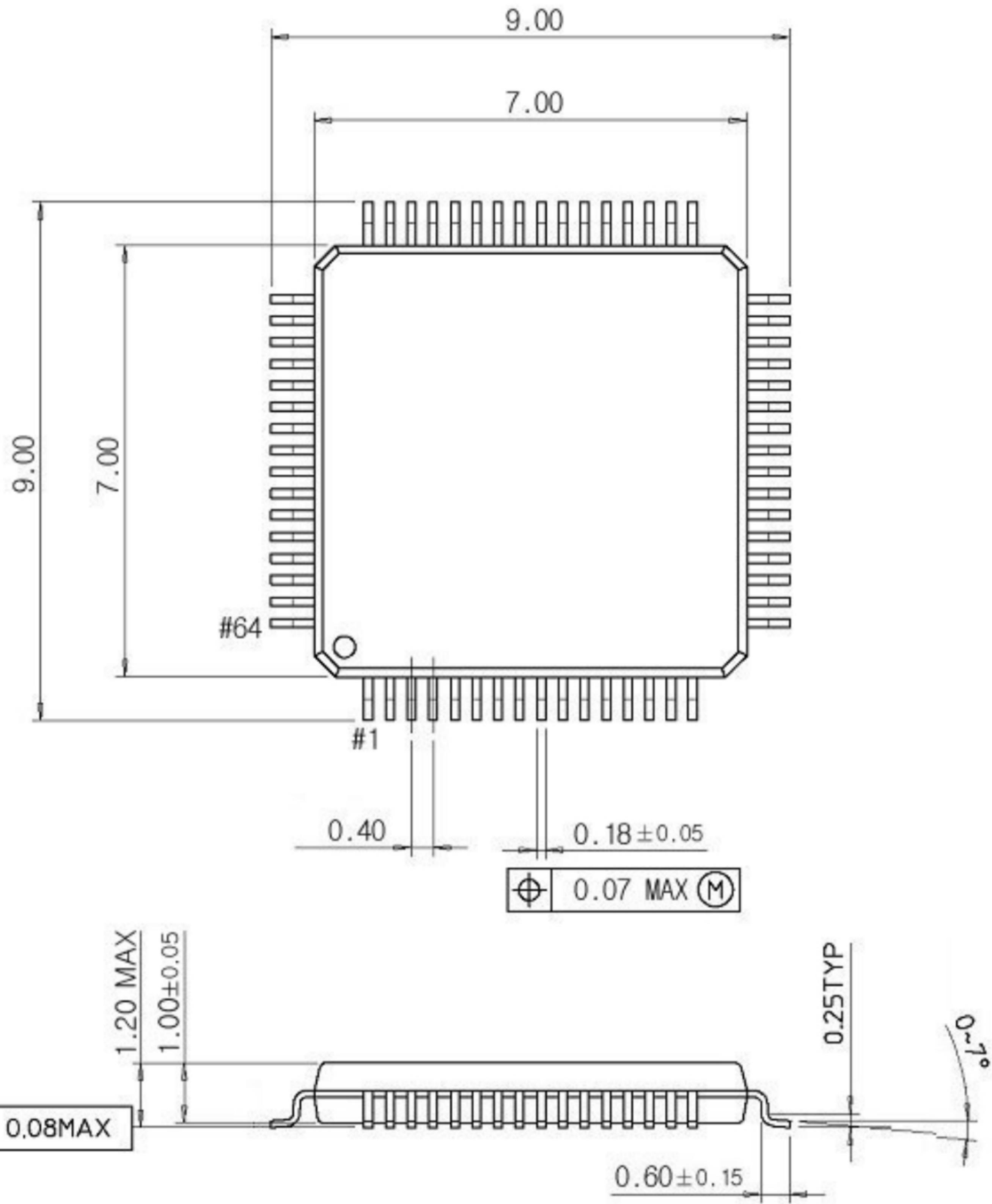
3.3 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
3.3V IO *Note1					
Input low voltage	V_{IL3}	-0.3	-	0.8	V
Input high voltage	V_{IH3}	2.0	-	5.5	V
Input Leakage current	I_{IL3}	-	-	± 10	uA
Threshold point	V_{T3}	1.35	1.47	1.60	V
Schmitt trig Low to High threshold point	V_{T3+}	1.40	1.50	1.59	V
Schmitt trig. High to Low threshold point	V_{T3-}	0.88	0.94	1.00	V
Output low voltage	V_{OL3}	-	-	0.4	V
Output high voltage	V_{OH3}	2.4	-	-	V
5.0V IO *Note2					
Input low voltage	V_{IL5}	-0.3	-	0.8	V
Input high voltage	V_{IH5}	2.0	-	5.5	V
Input Leakage current	I_{IL5}	-	-	± 10	uA
Threshold point	V_{T5}	1.33	1.44	1.48	V
Schmitt trig Low to High threshold point	V_{T5+}	1.82	1.96	2.04	V
Schmitt trig. High to Low threshold point	V_{T5-}	1.12	1.22	1.28	V
Output low voltage	V_{OL5}	-	-	0.4	V
Output high voltage	V_{OH5}	2.4	-	-	V

*Note1 : 3.3V data pins(expect 5V data pins)

*Note2 : 5V data pins(XRG, H1, H2 pins)

4. Package Information



Package	Type	Pin pitch	Size(WxD)
	64 - TQFP	0.40mm	7x7mm

5. Revision History

REVISION	DATE	DESCRIPTION
rev 0.1	2010.07.12	• Generated