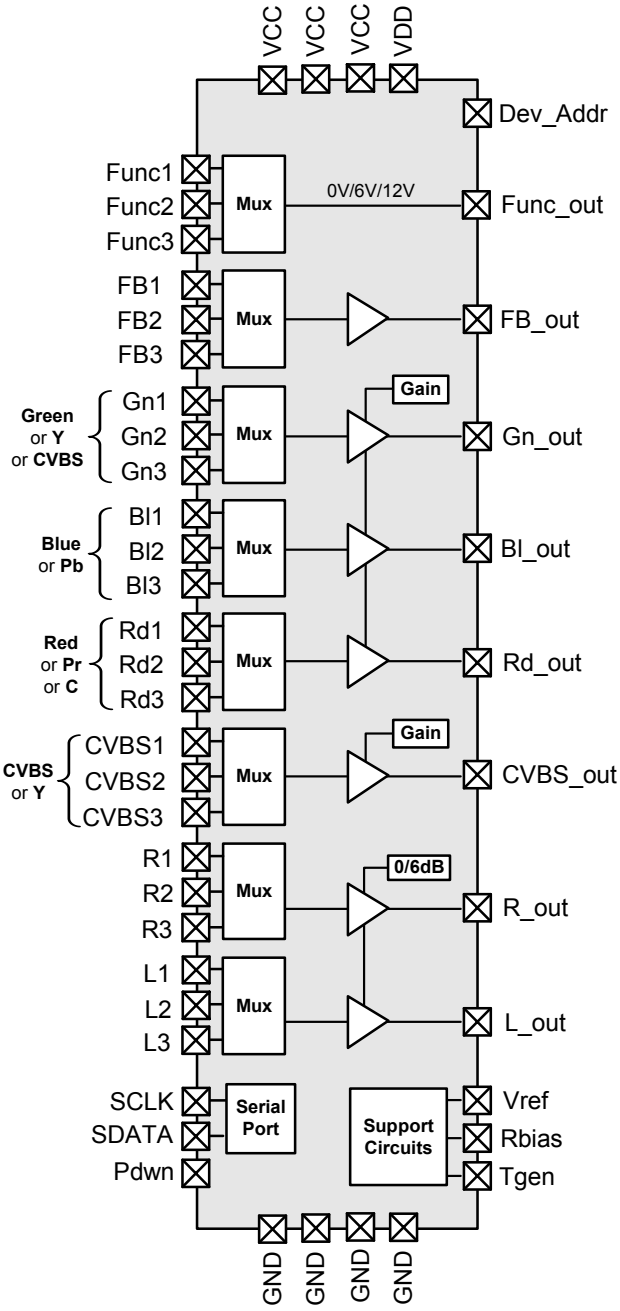
AVPro® 5303B
Universal 3-Input A/V Switch Interface

DATA SHEET

DECEMBER 2005

DESCRIPTION

The AVPro® 5303B device is a universal three input A/V switch interface IC designed for TV and general-purpose A/V applications. The device provides interfaces for three full sets of TV SCART input signals (Red, Green, Blue, CVBS, R, L, Fast Blanking, and TV Function) and also supports SCART SVHS video mode. In addition, the 5303B can be configured to support general-purpose A/V interface (YPrPb, SVHS, and CVBS) for TVs, DVD recorders, digital set-top boxes, and PVRs. Video and audio gains are programmable. All switching and function settings are controlled via I²C.



FEATURES

Three Input A/V Interface

- *3:1 video and audio mux*
- *Programmable gain video drivers*
- *0/6 dB audio drivers*
- *TV SCART Interface*
  - *RGB+FB, SVHS and CVBS video modes*
  - *12V TV Function pins mux*
- *General Purpose A/V Interface*
  - *YPrPb, SVHS and CVBS video modes*

I²C Control

Power Down Mode

Configurable Device Address

- *Picture-in-Picture Application*
- *Expandable Multi-function Inputs (up to 6 channels)*

Power Supply

- *+5V, +12V*

Package

- *48-QFN*

APPLICATIONS

- ✓ TV 3-SCART Interface
- ✓ TV A/V Interface (YPrPb/SVHS/CVBS)
- ✓ DVD Recorder A/V Interface
- ✓ Digital Set-Top Box A/V Interface
- ✓ PVR A/V Interface

Functional Description

The 5303B is an analog A/V interface IC designed for TV and general-purpose A/V applications. The device accepts up to three sets of SCART input signals (Red, Green, Blue, CVBS, R, L, Fast Blanking, and TV Function). By way of 3:1 mux, SCART 1, 2, or 3 signals can be selected at the device's output pins. The 5303B supports four SCART video modes: RGB/CVBS, RGB-only, CVBS-only and SVHS. The RGB and CVBS video driver gains are programmable from 2 to 1.4 in 0.2 steps, and the R/L audio driver gain can be 0dB or 6dB. The R/L audio drivers can accept signals from 0.5Vrms to 2Vrms.

For general-purpose A/V applications, video switches and drivers can be configured to support component video (YPrPb), S-Video (SVHS), and composite video (CVBS) signals.

All switching and programmable functions of the device are controlled through a standard I^2C serial interface

DC Restore for RGB, Y, and CVBS: The device will generate a DC restore level on each video output based on timing referenced to a horizontal sync pulse. When the sync pulse is detected, the DC restore circuit will act to position the blank level to 1.2V at the respective RGB, Y, or CVBS output pin(s).

DC Restore for SVHS and YPrPb: In the SVHS mode, the CVBS pin is used as Luma input and the Red pin is used as Chroma input. The DC restore function for Luma signal is equivalent to CVBS signal. The DC restore circuit will position the output blank level to 1.2V at the respective Luma output pin. For the Chroma input, the on-chip clamp circuit will be used to position the output mid-scale DC level to 1.8V. In the YPrPb mode, the mid-scale DC level for Pr and Pb outputs will also be at 1.8V.

A/V Input Source Selection

The device accepts up to three sets of A/V input signals. Bits 0 & 1 of Register 0 determine which of the sets will be present at the device's output pins.

Video Mode Selection

The device supports four video modes for TV SCART applications: RGB/CVBS, RGB-only, CVBS-only, and SVHS. Bits 2, 3, & 4 set the active video mode. RGB/CVBS video mode is a default mode. For general-purpose A/V applications, the device supports YPrPb/CVBS and CVBS/SVHS video modes.

RGB Gain

The gain of the RGB outputs can be adjusted to one of four different levels. Bits 0 & 1 Register 1 set the gain of the RGB output amplifiers according to the following table:

Bit 1	Bit 0	RGB Amplifier Gain
0	**0**	**Gain = 2 V/V**
0	1	Gain = 1.8 V/V
1	0	Gain = 1.6 V/V
1	1	Gain = 1.4 V/V

CVBS Gain

The gain of the CVBS output can be adjusted to one of four different levels. Bits 2 & 3 Register 1 set the gain of the CVBS output amplifier according to the following table:

Bit 3	Bit 2	CVBS Amplifier Gain
0	**0**	**Gain = 2 V/V**
0	1	Gain = 1.8 V/V
1	0	Gain = 1.6 V/V
1	1	Gain = 1.4 V/V

Audio Gain

The gain of the R/L audio amplifiers can be set to either 0dB or 6dB. Bit 4 of Register 1 sets the gain of the amplifiers according to the following table:

Bit 4	R/L Amplifier Gain
0	**Gain = 0 dB**
1	Gain = 6 dB

TV Function Input

The TV Function feature generally supports three-level logic signal required for SCART TV Function Switching:

Input Voltage	TV Function Switching Mode
0-2V	Broadcast TV
4.5-7V	16:9 Peritelevision Reproduction
9.5-12V	Normal Peritelevision Reproduction

In the AVPro® 5303B device, the TV Function feature works in pass through mode only. The three inputs, Func1, Func2 and Func3 support the pass through mode of the TV Function feature. A 100kΩ load is recommended for typical operation at the Func_out pin.

Fast Blanking (FB) Input

The FB1, FB2 and FB3 inputs support two-level logic signal required for SCART Fast Blanking:

Logic	Input Voltage	Fast Blanking Mode
0	0-0.4V	CVBS Active
1	1-3V	RGB Active

Following a 3:1 input mux stage is a unity-gain FB video driver. The FB video driver is designed to match the video drivers of RGB in bandwidth and time delay and can support a minimum load of 300Ω.

Chip Power Down

The whole chip (except negligible on-chip biasing circuit) can be powered down by setting Pdwn pin to high (5V).

Configurable Device Address

Dev_Addr pin sets the address of the 5303B device. There are two possible device addresses that the 5303B can have:

Device Address	Description
10**01**000x	Dev_Addr pin left OPEN (Default)
10**10**000x	Dev_Addr pin connected to GND

In the case of picture-in-picture or 6-channel inputs application, a second device is required to have a different address from the first or original device. This can be done by connecting the Dev_Addr pin of the second device to GND while leaving the Dev_Addr pin of the first device OPEN or unconnected.

Serial Port Definition

Internal functions of the device are monitored and controlled by a standard inter-IC (I^2C)bus with data being transferred MSB first on the rising edge of the clock. The serial port operates in a slave mode only and can be written to or read from. The device uses 7-bit addressing, and does not support 10-bit addressing mode. The write register data is sent sequentially, such that if register 1 is to be programmed, then registers 0 and 1 need to be sent. If only register 0 needs to be programmed, then only registers 0 data needs to be sent. It will support standard and fast bus speed. The default address of the device is 1001000x (1001000 for Write and 10010001 for Read).

The 5303B includes a read register in which the upper four bits identify the specific chip within the AVPro® family. This allows a single application platform and software to work with a wide variety of AVPro® chips. The ID code for the 5303B is 0010.

Data Transfers

A data transfer starts when the *SDATA* pin is driven from HIGH to LOW by the bus master while the *SCLK* pin is HIGH. On the following eight clock cycles, the device receives the data on the *SDATA* pin and decodes that data to determine if a valid address has been received. The first seven bits of information are the address with the eighth bit indicating whether the cycle is a read (bit is HIGH) or a write (bit is LOW). If the address is valid for this device, on the falling *SCLK* edge of the eighth bit of data, the device will drive the *SDATA* pin low and hold it LOW until the next rising edge of the *SCLK* pin to acknowledge the address transfer. The device will continue to transmit or receive data until the bus master has issued a stop by driving the *SDATA* pin from LOW to HIGH while the *SCLK* pin is held HIGH

Write Operation: When the read/write bit (LSB) is LOW and a valid address is decoded, the device will receive data from the *SDATA* pin. The device will continue to latch data into the registers until a stop condition is detected. The device generates an acknowledge after each byte of data written.

Read Operation: When the read/write bit (LSB) is HIGH and a valid address is decoded, the device will transmit the data from the internal register on the following eight *SCLK* cycles. Following the transfer of the register data and the acknowledge from the master, the device will release the data bus.

Reset: At power-up the serial port defaults to the states indicated in boldface type. The device also responds to the system level reset that is transmitted through the serial port. When the master sends the address 00000000 followed by the data 00000110, the device resets to the default condition.

SERIAL PORT REGISTER TABLES

Read register Device Address = 10010001 (10100001 when Dev_Addr = 0)

Function	Bits	Description
Not Used	xxxx0000	**Not Used**
Device ID Code	0010xxxx	This code identifies the device type as the 5303B.

Write Registers: Device Address = 10010000 (10100000 when Dev_Addr = 0). **Bold** indicates default setting.

Register 0: Signal Source Selection

Register 0:

Video Mode	Bits	Description
BLUE Chroma/Pr/Pb enable	xxxxxxx**0**	Blue input set for Chroma/Pr/Pb
	xxxxxxx1	Blue input set for Y or Blue(DC Restore)
RED Chroma/Pr/Pb enable	xxxxxx**0**x	Red input set for Chroma/Pr/Pb
	xxxxxx1x	Red input set for Y or Red(DC Restore)
FB_OUT set to 0V	xxxxx**0**xx	FB_OUT for normal operation
	xxxxx1xx	FB_OUT SET TO 0V
GN_OUT set to 0V	xxxx**0**xxx	GN_OUT for normal operation
	xxxx1xxx	GN_OUT SET TO 0V

Audio/FUNC Source Selection	Bits	ROUT	LOUT	FUNC_OUT
	00xxxxxx	R1	L1	FUNC1
	01xxxxxx	R2	L2	FUNC2
	10xxxxxx	R3	L3	FUNC3
	11xxxxxx	Not Used	Not Used	Not Used

Register 1: Audio/Video Gain Control

Function	Bits	Description
RBG Gain	xxxxxx**00**	2
	xxxxxx01	1.8
	xxxxxx10	1.6
	xxxxxx11	1.4
Function	**Bits**	**Description**
CVBS Gain	xxxx**00**xx	2
	Xxxx01xx	1.8
	Xxxx10xx	1.6
	Xxxx11xx	1.4
Function	**Bits**	**Description**
Audio Gain	xxx**0**xxxx	0 dB
	xxx1xxxx	6 dB

Register 2: XXXX XXXX. User must write to register 2 (contents written are a don't care) prior to writing to register 3.

Register 3: Video Signal Source Selection

Video Mode	Bits	RED_OUT
RED Source Selection	xxxxx**x00**	RD1
	xxxxxx01	RD2
	xxxxxx10	RD3
	xxxxxx11	0V
Video Mode	**Bits**	**CVBS_OUT**
CVBS Source Selection	xxxx**00**xx	CVBS1
	xxxx01xx	CVBS2
	xxxx10xx	CVBS3
	xxxx11xx	0V
Video Mode	**Bits**	**BLUE_OUT**
BLUE Source Selection	xx**00**xxxx	BL1
	xx01xxxx	BL2
	xx10xxxx	BL3
	xx11xxxx	0V

Video Mode	Bits	GN_OUT	FB_OUT
GREEN Source Selection	**00**xxxxxx	GN1	FB1
	01xxxxxx	GN2	FB2
	10xxxxxx	GN3	FB3
	11xxxxxx	Not Used	Not Used

PIN DESCRIPTIONS

Name	Pin	Type	Description
Analog Pins			
Func1	25	I	TV Function Input 1
Func2	24	I	TV Function Input 2
Func3	23	I	TV Function Input 3
FB1	48	I	Fast Blanking Input 1
FB2	5	I	Fast Blanking Input 2
FB3	36	I	Fast Blanking Input 3
Gn1	2	I	Green Input 1
Gn2	7	I	Green Input 2
Gn3	38	I	Green Input 3
Bl1	3	I	Blue Input 1
Bl2	8	I	Blue Input 2
Bl3	39	I	Blue Input 3
Rd1	1	I	Red Input 1
Rd2	6	I	Red Input 2
Rd3	37	I	Red Input 3
CVBS1	47	I	CVBS Input 1
CVBS2	4	I	CVBS Input 2
CVBS3	35	I	CVBS Input 3
R1	14	I	Right Audio Input 1
R2	16	I	Right Audio Input 2
R3	18	I	Right Audio Input 3
L1	15	I	Left Audio Input 1
L2	17	I	Left Audio Input 2
L3	19	I	Left Audio Input 3
Func_out	22	O	TV Function Output
FB_out	45	O	Fast Blanking Output
Gn_out	41	O	Green Output
Bl_out	40	O	Blue Output
Rd_out	44	O	Red Output
CVBS_out	46	O	CVBS Output
R_out	21	O	Right Audio Output
L_out	13	O	Left Audio Output

PIN DESCRIPTIONS (Continued)

Name	Pin	Type	Description
Digital Pins			
Dev_Addr	29	I	Device Address Input
Pdwn	28	I	Chip Power Down
SCLK	30	I	Serial Clock Input: This pin accepts a serial port clock input signal.
SDATA	31	I/O	Serial Data Input/Output that can receive or transmit serial data.
Power/Ground Pins			
VCC	9, 33, 43	-	+5 VDC power supply pins.
VDD	27	-	+12 VDC power supply pin for function switching circuits.
Vref	20	-	Internal voltage reference, bypass pin. Add capacitor 0.1µF(1.0 µF for better PSRR) to ground.
GND	20, 26, 34, 42	-	Ground for all blocks.
Rbias	11	-	Bias point of internal current generator. Add resistor 10.0kΩ(± 1%) to ground.
Tgen	32	-	Reference point for internal timing circuit. Add capacitor 470pF to ground.
N/C	12	-	No connect.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

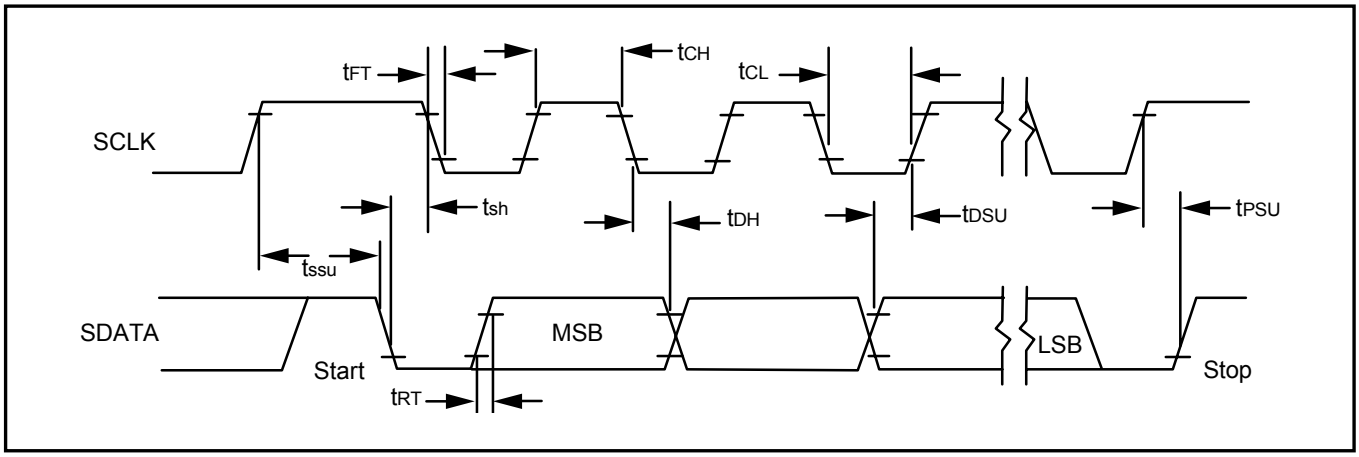
PARAMETER	RATING
Storage temperature	-55 to 150 °C
Junction operating temperature	+125 °C
5V supply voltage pins	-0.3 V < VCC < 6V
12V supply pin	-0.3 V < VDD < 13V
Voltage applied to Digital and Video Inputs	-0.3V to VCC+0.3 V
Voltage applied to video pins	-0.3V to VCC+0.3 V
Voltage applied to audio pins	-0.3 V < VDD < 13V
Voltage applied to FNC pin (input)	-0.3 V < VDD < 13V

SPECIFICATIONS: Unless otherwise specified: 0° < Ta < 70 °C; power supplies VCC = +5.0 V ±5%, VDD = 12.0 V ±5%.

Parameter	CONDITION	MIN	NOM	MAX	UNIT
Operating Characteristics					
Power Supply Currents (Default register setting)	All outputs not loaded VCC (+5 VDC) VDD (+12 VDC)		 16.5 4	 20 5	 mA mA
Power Supply Currents (Default register setting)	Pdwn = 1 VCC (+5 VDC) VDD (+12 VDC)		 2.3 10	 3 100	 mA µA
PSRR	f_{in} = 100 Hz, 0.3 Vpp on VCC/ VDD	40			dB
Switch time	From serial data acknowledge		2.0		µs
Wake time	From Power Down Condition		5		µs
Serial Port Timing (Set by I^2C controller)					
SCLK Input Frequency				400	kHz
SCLK LOW time (t_{CL})		1.3			µs
SCLK HIGH time (t_{CH})		0.6			µs
Rise time (t_{RT})	*SCLK* and *SDATA*			300	ns
Fall time (t_{FT})	*SCLK* and *SDATA*			300	ns
Data set-up time* (t_{DSU})	*SDATA* change to *SCLK* HIGH	100			ns
Data hold time* (t_{DH})	*SCLK* LOW to *SDATA* change	30			ns
Start set-up time (t_{SSU})		0.6			µs
Start hold time (t_{SH})		0.6			µs
Stop set-up time (t_{PSU})		0.6			µs
Glitch rejection	maximum pulse on *SCLK* and/or *SDATA*			50	ns
* These specifications also apply to an acknowledge generated by the device.					

SPECIFICATIONS (continued)

Digital I/O Characteristics (SCLK, SDATA, Pdwn, Dev_Addr)					
Parameter	**CONDITION**	MIN	NOM	MAX	UNIT
High level input voltage		0.7* VCC		VCC+0.3	V
Low level input voltage		GND-0.3		0.3* VCC	V
High level input current (SCLK, Pdwn, Dev_Addr)	Vin = Vcc - 1.0V	-10		10	µA
High level input current (SDATA)	Vin = Vcc - 1.0V	-50		50	µA
Low level input current (SCLK, Pdwn)	Vin = 1.0V	-10		10	µA
Low level input current (Dev_Addr)	Vin = 1.0V	-300		10	µA
Low level input current (SDATA)	Vin = 1.0V	-50		50	µA
Low level output voltage (SDATA)	I_{OL} = 3 mA			0.4	V
Fall time (t_{FT}) V_{Ihmin} to V_{ILmax} (SDATA)	Acknowledge or read with C_L = 400pF			250	ns



Serial Port Timing (Typical)

Video Characteristics - Unless otherwise noted, typical output loading on all video outputs is 150Ω. All video outputs are capable of withstanding a sustained 75Ω load to ground without damage.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Impedance	All video inputs	100			kΩ
Input Dynamic Range	f_{in} = 100 kHz, THD < 0.15%		1.5		Vpp
RGB Gain Control A_0 = reading xx00xxxx gain	1.0 Vpp input, f_{in} = 100 kHz; Register 1 = xxxxxx00 Register 1 = xxxxxx01 Register 1 = xxxxxx10 Register 1 = xxxxxx11	 1.9 A_0 –12% A_0 –22% A_0 –33%	 2.0 A_0 –10% A_0 –20% A_0 –30%	 2.1 A_0 –8% A_0 –18% A_0 –27%	 V/V V/V V/V V/V
CVBS Gain Control A_0 = reading xx00xxxx gain	1.0 Vpp input, f_{in} = 100 kHz; Register 1 = xxxx00xx Register 1 = xxxx01xx Register 1 = xxxx10xx Register 1 = xxxx11xx	 1.9 A_0 –12% A_0 –22% A_0 –33%	 2.0 A_0 –10% A_0 –20% A_0 –30%	 2.1 A_0 –8% A_0 –18% A_0 –27%	 V/V V/V V/V V/V
Output Gain Inequality	RGB or SVHS output channel to channel	-2.5		2.5	%
Video Bandwidth	Amplitude loss measured at 10MHz, A_0 = 2V/V	1.0	0.7		dB
	3dB, A_0 = 2V/V		25		MHz
Output DC Level Blank level clamp voltage	RGB, CVBS or Luma output		1.2		V
Average level	Chroma, Pr or Pb output		1.8		V
Signal to Noise Ratio	1 Vpp input	58	75		dB
Cross Talk	f_{in} = 4.43 MHz, 1 Vpp		-65		dB
Output to Output Differential Delay	RGB signals, f_{in} = 100 kHz	-20		20	ns
Differential Phase	CVBS output	-2.5		2.5	Deg.
Differential Gain	CVBS output	-2.5		2.5	%

Audio Characteristics - Unless otherwise noted, all audio outputs shall drive a load of 10.3 kΩ. All audio outputs will withstand a sustained 300Ω to ground without damage.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Impedance		110	160	210	kΩ
Output Impedance			1.6	5	Ω
Audio Gain Control	f_{in} = 1.0 kHz Register 1 = xxx0xxxx Register 1 = xxx1xxxx		 0 6		 dB dB
Frequency Response	0.5 Vrms input, Flat within ± 0.3 dB	20			kHz
	Measured -3 dB point	100			kHz
Dynamic Range A Weighting filter	f_{in} = 1.0 kHz, 2.0 Vrms	90	100		dB
Signal to Noise ratio A Weighting filter	f_{in} = 1.0 kHz, 2.0 Vrms	90	100		dB
Distortion (THD)	0.5 Vrms output			0.03	%
	2 Vrms output			0.1	%
DC Offset		-250		250	mV
Output Phase Matching	f_{in} = 1.0 kHz, 0.5 Vrms		0.5		Deg.
Cross Talk	f_{in} = 1.0 kHz, 2.0 Vrms	75	100		dB
Audio to video path skew	Video input = 1.0 Vpp @ 100 kHz Audio input = 0.5 Vrms @ 1.0 kHz		150		ns

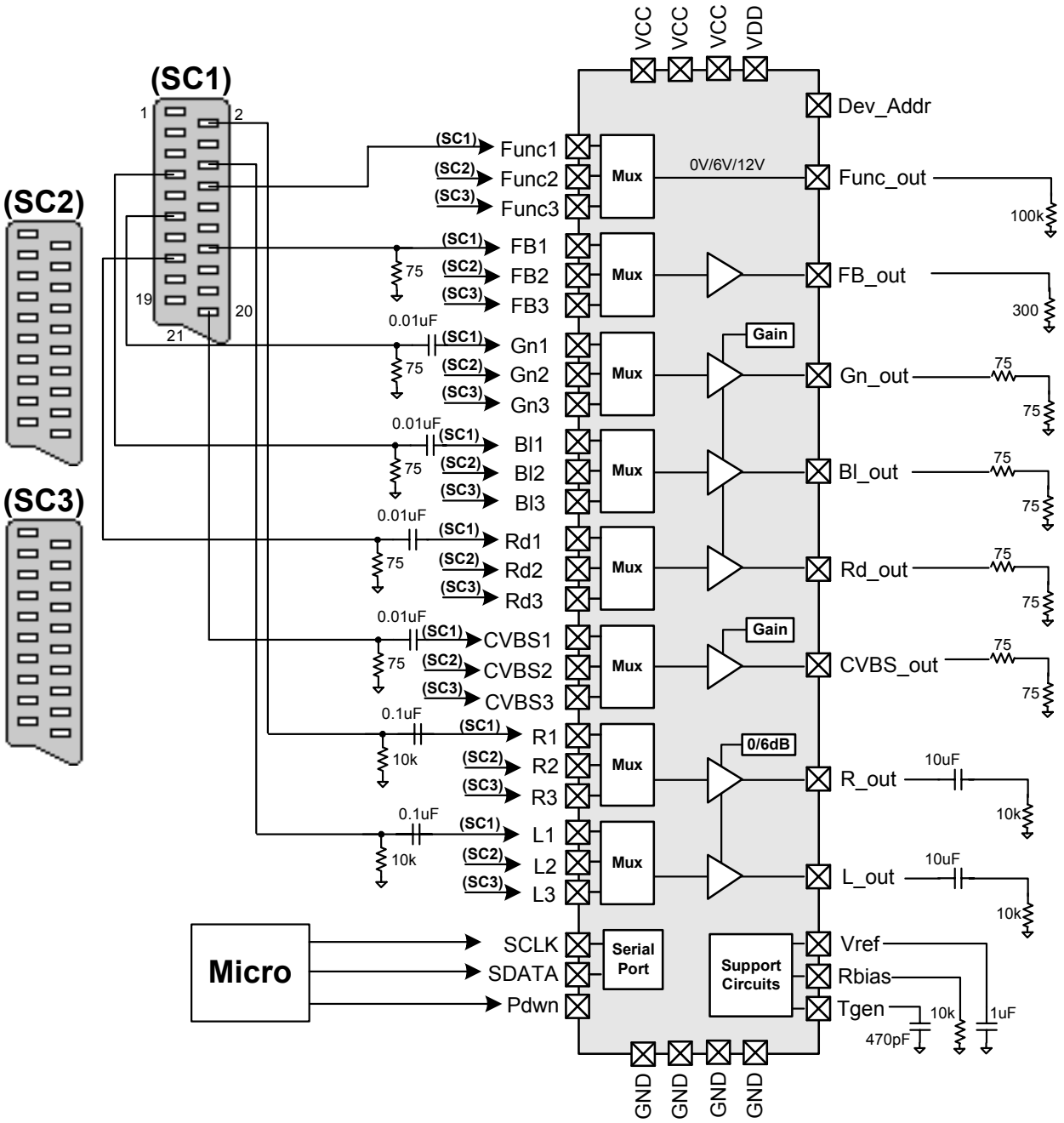
TV Function Pin Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Load	@ Func_out	10			kΩ
Series Resistance	With Output Load, 10kΩ, Vin = 12V		290	500	Ω
	With Output Load, 10kΩ, Vin = 9.5V		350	500	Ω
	With Output Load, 10kΩ, Vin = 7V		220	500	Ω

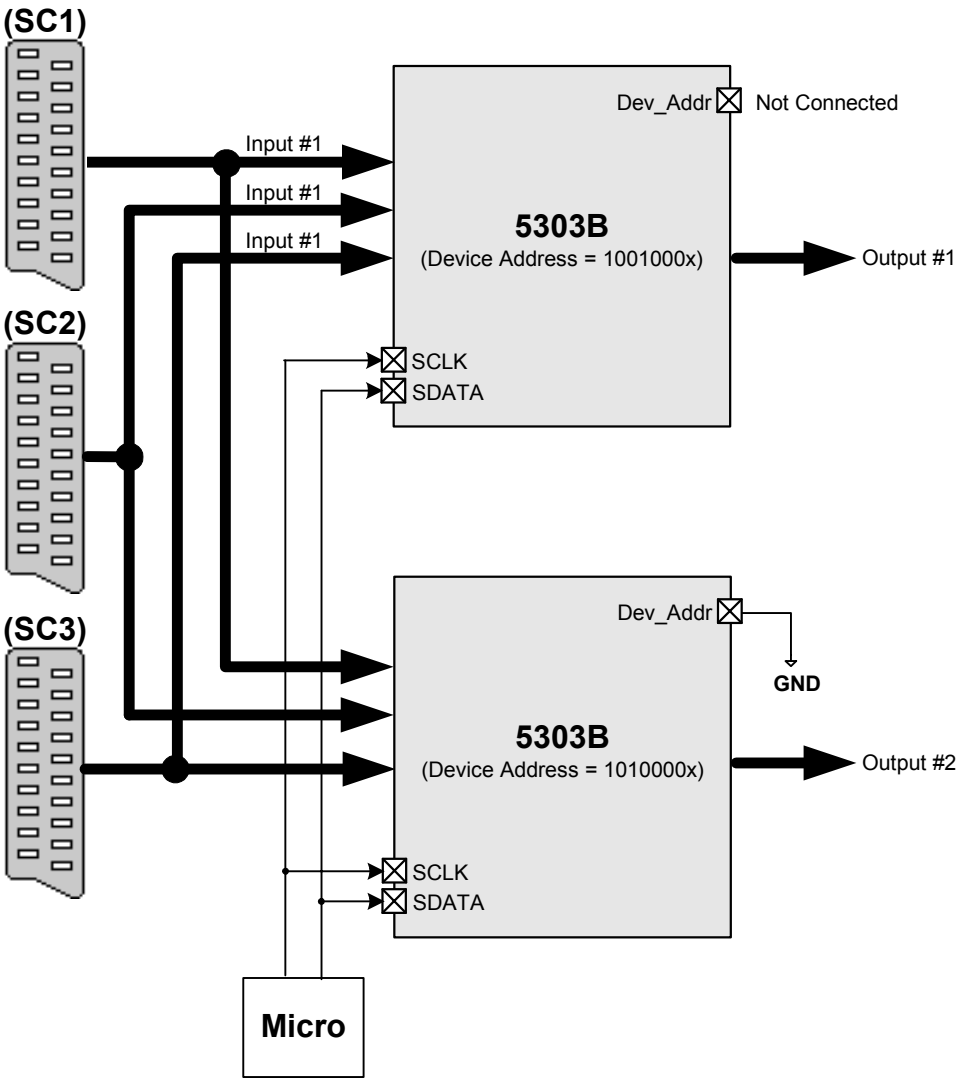
Fast Blanking (FB) Pin Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Impedance	FB1, FB2, FB3	100			kΩ
Blanking Input Level	Input Logical "0"	0.0		0.4	V
	Input Logical "1"	1.0		3.0	V
Blanking Delay	FB to RGB Signals	-50		50	ns
Output Load	@ FB_out	300			Ω
FB Gain			1.0		V/V

Application Diagram: (For TV 2/3-SCART Application)

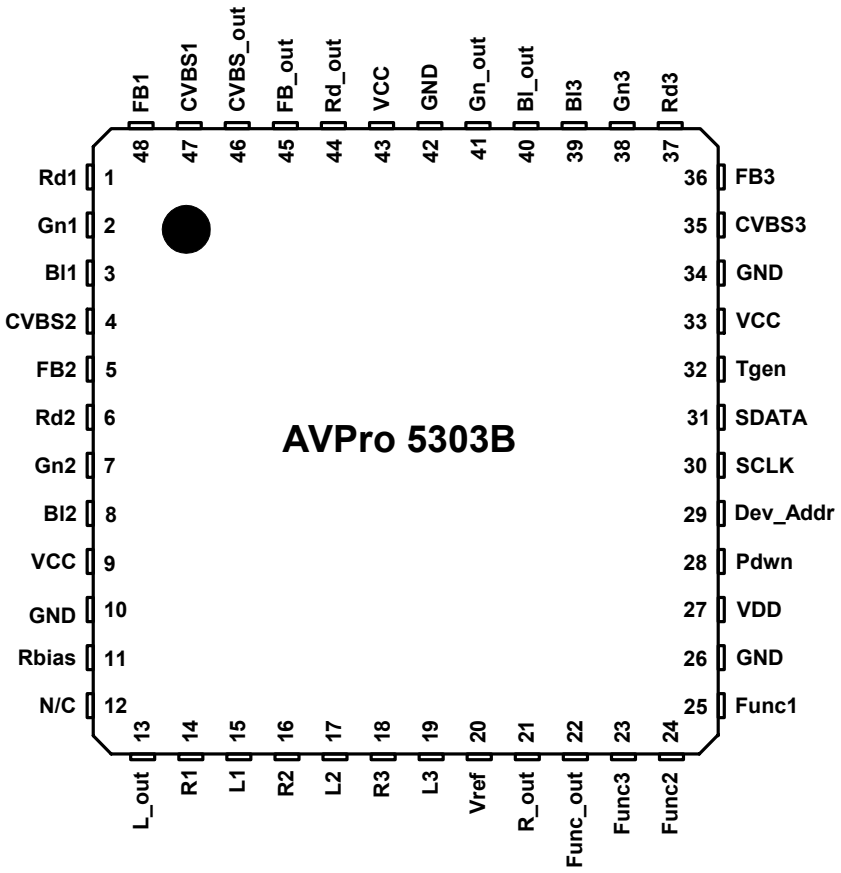


Application Diagram: (Dual AVPro® 5303B Application)

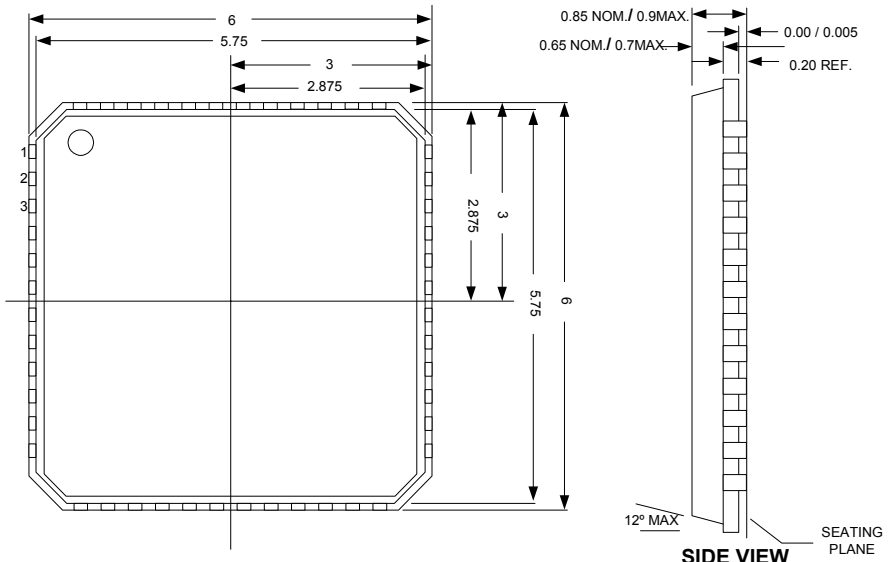


PACKAGE PIN DESIGNATION

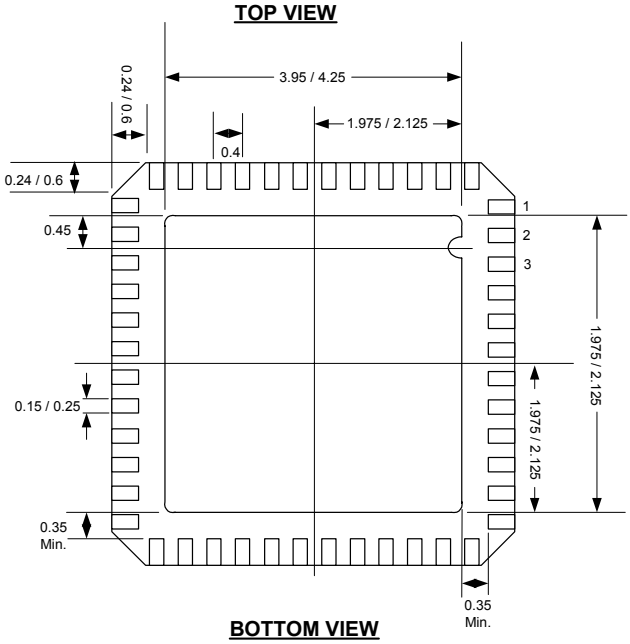
(Top View)



MECHANICAL DRAWING 48QFN Package



TOP VIEW **SIDE VIEW**



BOTTOM VIEW

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
AVPro® 5303B Universal 3-Input A/V Switch Interface (48 QFN)	AVPro® 5303B-CM	AVPro® 5303B-CM
AVPro® 5303B Universal 3-Input A/V Switch Interface (48 QFN) Tape and Reel	AVPro® 5303B-CMR	AVPro® 5303B-CM
AVPro® 5303B Universal 3-Input A/V Switch Interface (48 QFN) Lead Free	AVPro® 5303B-CM/F	AVPro® 5303B-CM
AVPro® 5303B Universal 3-Input A/V Switch Interface (48 QFN) Lead Free, Tape and Reel	AVPro® 5303B-CMR/F	AVPro® 5303B-CM

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