CHRONTEL

Video Genlock Pixel Clock Generator

Features

- On-chip PLL for clock synchronization
- On-chip loop filter for clock generation
- Built-in power supply conditioning circuitry for low phase jitter
- Tristate and output enable feature to revert pixel clock control to the system clock when not in genlock mode
- 15 kHz to 1 MHz reference clock range
- 1.25 MHz to 50 MHz output clock range
- Drop-in replacement for AV9173
- CMOS technology in 8-pin PDIP (300 mil) and SOIC (150 mil)
- 5V power supply

Description

CH9073 is a PLL clock generator designed to provide the necessary implementation of a video genlock pixel clock generator. It consists of a phase detector, a charge pump, a loop filter, and a voltage-controlled oscillator (VCO) grouped into a single low cost, high performance integrated circuit.

CH9073 generates a pixel clock from a video horizontal synchronization (HSYNC) signal and uses an external clock feedback divider to function as a frequency synthesizer. A selectable VCO output divider input, FS0, is also available, providing four distinct clock output frequency ranges. In addition, CH9073 can be used for other clock recovery applications such as in the area of data communications.

CH9073 uses high performance, low power CMOS technology available in 8-pin PDIP and SOIC packages.
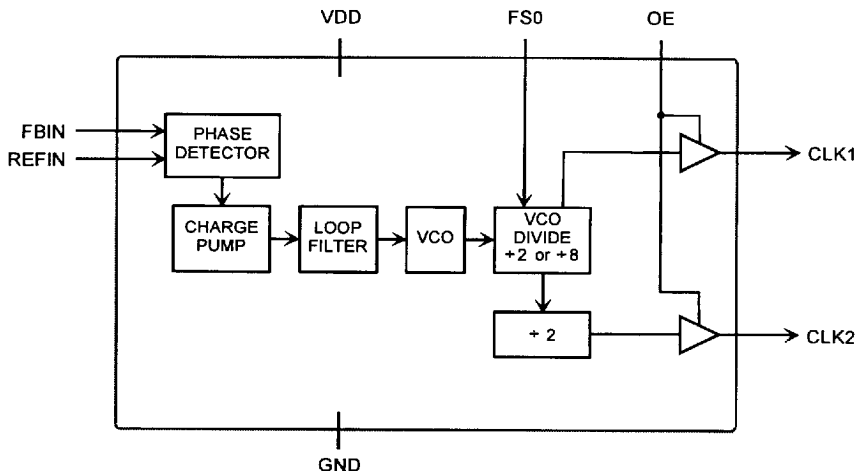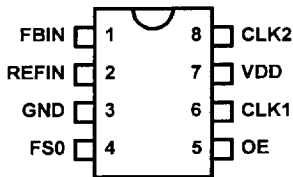
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Figure 1: Block Diagram

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      FBIN  ▢ 1      8 ▢ CLK2
      REFIN ▢ 2      7 ▢ VDD
      GND   ▢ 3      6 ▢ CLK1
      FS0   ▢ 4      5 ▢ OE
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Figure 2: CH9073A

Table 1 • Pin Description CH9073A

Pin	Type	Symbol	Description
1	In	FBIN	Feedback input
2	In	REFIN	Reference clock input
3	Power	GND	Ground
4	In	FS0	VCO output divider ($\div$ 2 or $\div$ 8) select input
5	In	OE	Output enable (active high, internal pull-up)
6	Out	CLK1	Clock1 output
7	Power	VDD	5V supply
8	Out	CLK2	Clock2 output

Note: The frequency of CLK1 is always twice the frequency of CLK2.
When FS0 = 0, the VCO output is divided by 2; when FS0 = 1, the VCO output is divided by 8.

Table 2 • Clock Output Frequency Ranges for CH9073A

FS0	Output Used	Frequency Range
0	CLK1	10 MHz – 50 MHz
0	CLK2	5 MHz – 25 MHz
1	CLK1	2.5 MHz – 12.5 MHz
1	CLK2	1.25 MHz – 6.25 MHz

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Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	−0.5 to +7.0	V
VIN	Input voltage on any pin with respect to GND	−0.5 to VDD+0.5	V
TSTOR	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 5V, IOH = −1mA	VDD −0.4			V
VOH	Output high voltage	VDD = 5V, IOH = −4mA	VDD −0.8			V
VOH	Output high voltage	IOH = −8mA	2.4			V
VOL	Output low voltage	IOL = 8mA			0.4	V
VIH	Input high voltage	VDD = 5V	2.0			V
VIL	Input low voltage	VDD = 5V			0.8	V
IIL	Input low current	VIN = 0V	−5		5	µA
IIH	Input high current	VIN = VDD	−5		5	µA
CI	Input capacitance				10	pF
IDD	Operating current	VDD = 5V, No load, 50 MHz		20	50	mA

Table 5 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
TIR	Input clock rise time	Note 1			10	ns
TIF	Input clock fall time	Note 1			10	ns
TR	Output rise time, 0.8V − 2.0V	15 pF load		1	2	ns
TR	Rise time, 20% − 80% VDD	15 pF load		2	4	ns
TF	Output fall time, 2.0V − 0.8V	15 pF load		1	2	ns
TF	Fall time, 80% − 20% VDD	15 pF load		2	4	ns
TDC	Output duty cycle	15 pF load. **Note 2**	40	48 / 52	60	%
T1S	Cycle-to-cycle jitter, 1 sigma			120	300	ps
TABS	Cycle-to-cycle jitter, absolute		−500	±250	500	ps
TLABS	Line-to-line jitter, absolute	Note 3		±4		ns
FIN	Input frequency, REFIN or FBIN	Note 1	15		1000	kHz
FVCO	VCO frequency	Note 1	20		100	MHz

Notes: 1. It may be possible to operate CH9073 outside these ranges. Consult Chrontel for details.
  2. Duty cycle measured at 1.5V.
  3. Input Reference Frequency = 15 kHz, Output Frequency = 25 MHz.
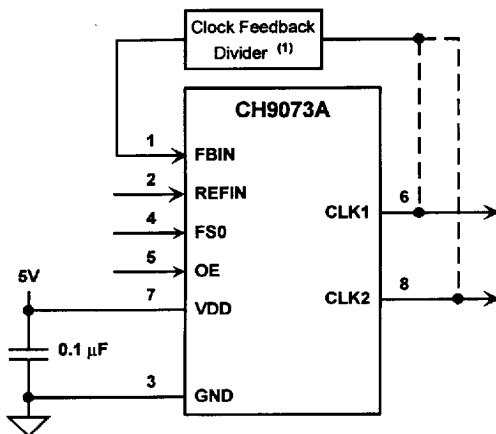   Jitter specification is measured between adjacent vertical pixels.

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Figure 3: Application Schematic
(1) Clock feedback divider is connected to
either CLK1 or CLK2, not both

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9073A-N	300 mil PDIP	8	5V
CH9073A-S	150 mil SOIC	8	5V

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