MC10E445, MC100E445

5V ECL 4-Bit Serial/Parallel Converter

The MC10/100E445 is an integrated 4-bit serial to parallel data converter. The device is designed to operate for NRZ data rates of up to 2.0 Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q0, the second to Q1 etc.

Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel to serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse applied asynchronously for at least two input clock cycles shifts the start bit for conversion from Qn to Qn–1. For each additional shift required an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Qn to the Qn–1 output (see Timing Diagram B).

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the data on the output will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E445's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 2.0 Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

Upon power-up the internal flip-flops will attain a random state. To synchronize multiple E445's in a system the master reset must be asserted.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- On-Chip Clock ÷4 and ÷8
- 2.0 Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-Ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8-Bits
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8″,
  Oxygen Index 28 to 34
- Transistor Count = 528 devices

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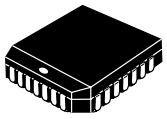
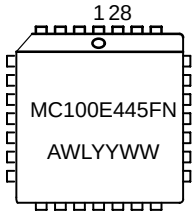
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

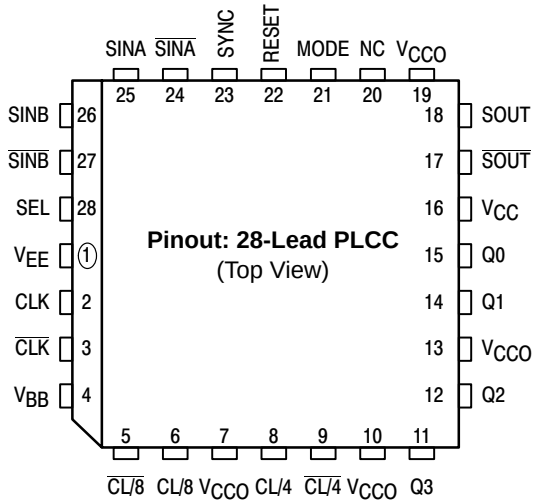
Device	Package	Shipping
MC10E445FN	PLCC–28	37 Units/Rail
MC10E445FNR2	PLCC–28	500 Units/Reel
MC100E445FN	PLCC–28	37 Units/Rail
MC100E445FNR2	PLCC–28	500 Units/Reel

PIN DESCRIPTION

PIN	FUNCTION
SINA, $\overline{\text{SINA}}$	ECL Differential Serial Data Input A
SINB, $\overline{\text{SINB}}$	ECL Differential Serial Data Input B
SEL	ECL Serial Input Selector Pin
Q0–Q3	ECL Parallel Data Outputs
CLK, $\overline{\text{CLK}}$	ECL Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	ECL Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	ECL Differential ÷8 Clock Output
MODE	ECL Conversion Mode 4-Bit/8-Bit
SYNCH	ECL Conversion Synchronizing Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLES

Mode	Conversion	SEL	Serial Input
L	4-Bit	H	A
H	8-Bit	L	B



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout Assignment

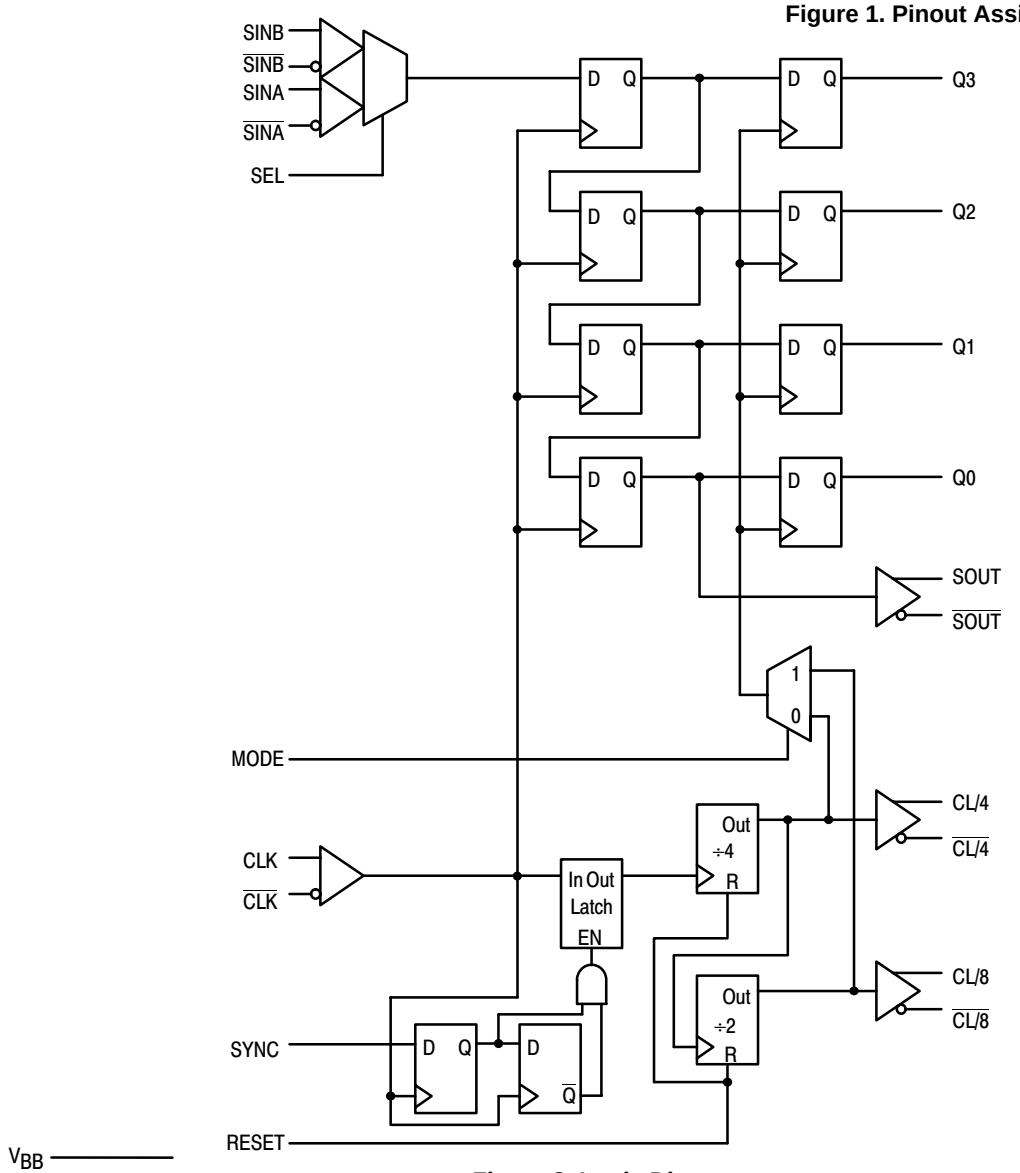


Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		154	185		154	185		154	185	mA
V_{OH}	Output HIGH Voltage (Note 3)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single–Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC}–2 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 5)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		154	185		154	185		154	185	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1025		–830	–1025		–830	–1025		–830	mV
V_{OL}	Output LOW Voltage (Note 6)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC}–2 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 8)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		154	185		154	185		177	212	mA
V_{OH}	Output HIGH Voltage (Note 9)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 9)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single–Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
9. Outputs are terminated through a 50 Ω resistor to V_{CC}–2 volts.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 11)

Symbol	Characteristic	0°C5			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		154	185		154	185		177	212	mA
V_{OH}	Output HIGH Voltage (Note 12)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1025		–830	–1025		–830	–1025		–830	mV
V_{OL}	Output LOW Voltage (Note 12)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
12. Outputs are terminated through a 50 Ω resistor to V_{CC}–2 volts.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 14)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Conversion Frequency	2.0			2.0			2.0			Gb/s NRZ
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q, Reset to Q CLK to SOUT (Diff) CLK to CL/4(Diff) CLK to CL/8(Diff)	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	ps
t_S	Setup Time SINA, SINB SEL	 –100 0	 –250 –200		 –100 0	 –250 –200		 –100 0	 –250 –200		ps
t_h	Hold Time SINA, SINB, SEL	 450	 300		 450	 300		 450	 300		ps
t_{RR}	Reset Recovery Time	500	300		500	300		500	300		ps
t_{PW}	Minimum Pulse Width CLK, MR	 400			 400			 400			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times 20%–80% SOUT Other	 100 200	 225 425	 350 650	 100 200	 225 425	 350 650	 100 200	 225 425	 350 650	ps

14. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
100 Series: V_{EE} can vary +0.46 V / –0.8 V.

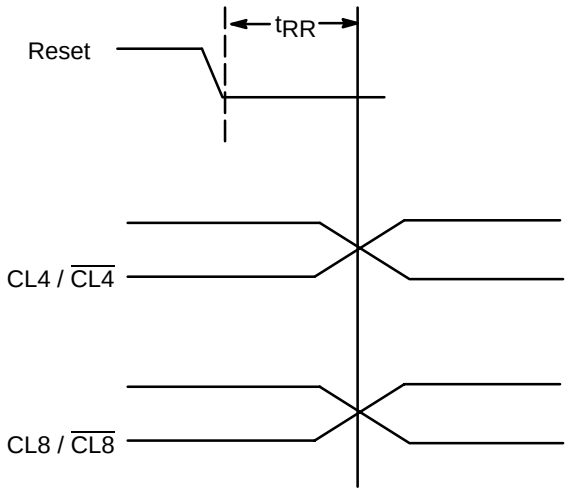
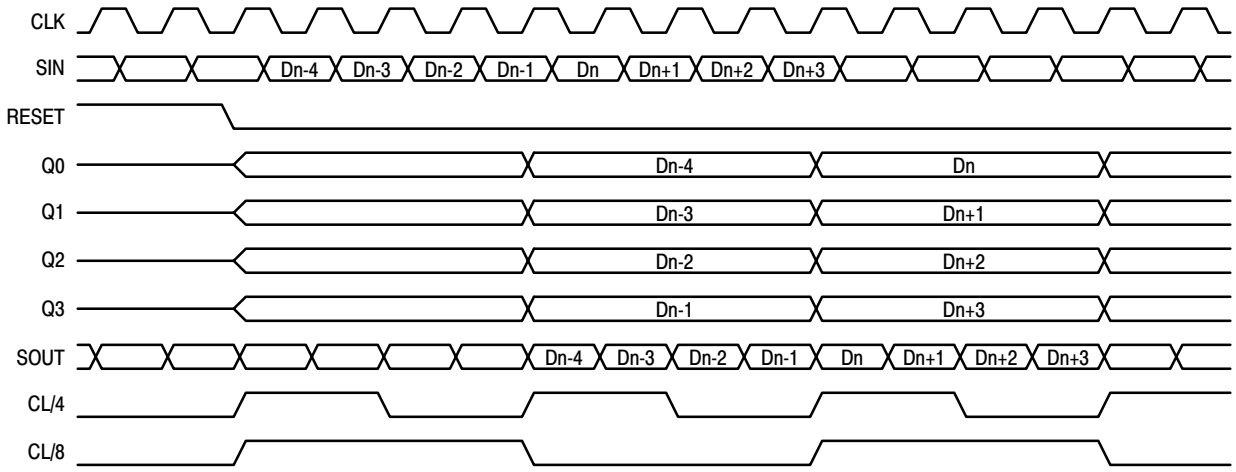
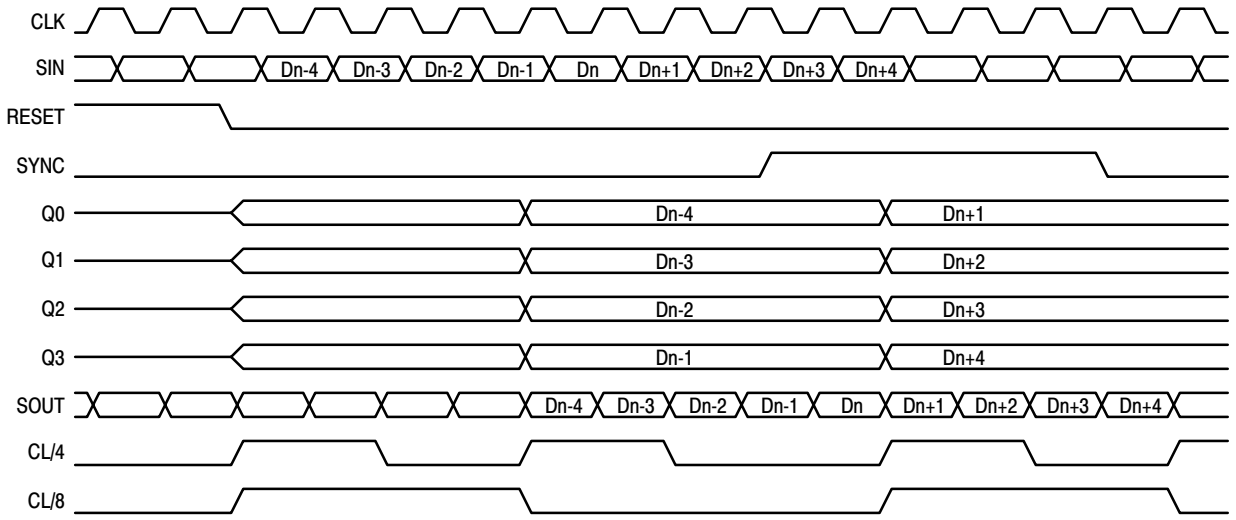


Figure 3.



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion With SYNC Pulse

Figure 4. Timing Diagrams

APPLICATIONS INFORMATION

The MC10E/100E445 is an integrated 1:4 serial to parallel converter. The chip is designed to work with the E446 device to provide both transmission and receiving of a high speed serial data path. The E445, can convert up to a 2.0Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide by four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 5 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and thus should be used as the loop back serial input.

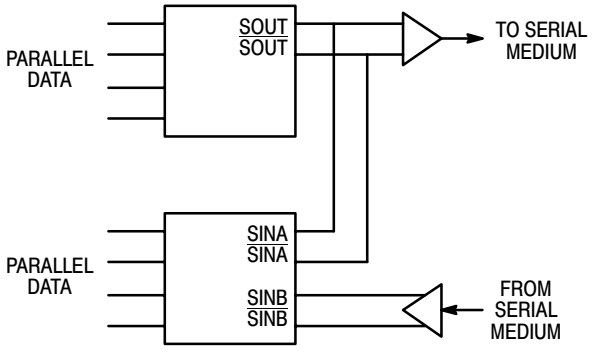


Figure 5. Loopback Test Architecture

The E445 features a differential serial output and a divide by 8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 6 illustrates the architecture for a 1:8 demultiplexer using two E445's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1150ps and tS for SIN = –100ps, yields a minimum period of 1050ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445 the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of clock to serial out would potentially cause a serial bit to be swallowed (Figure 7).

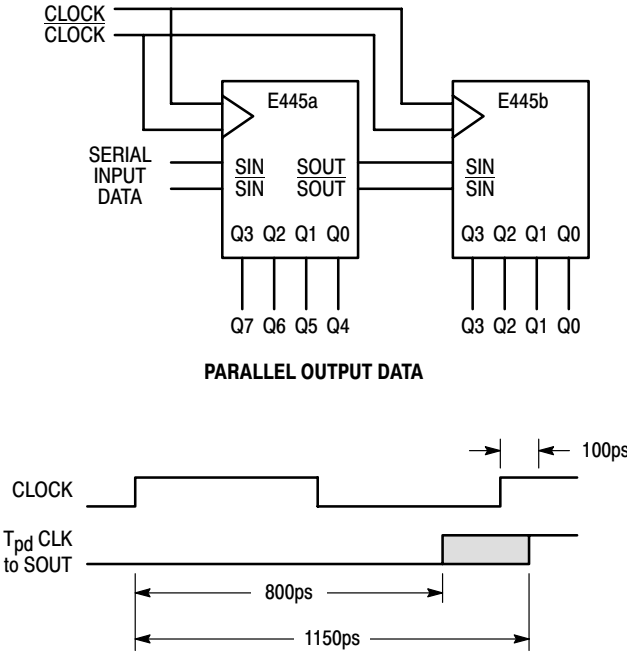


Figure 6. Cascaded 1:8 Converter Architecture

With a minimum delay of 800ps on this output the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the setup time on the serial input pin is negative coincident excursions on the data and clock inputs of the E445 will result in correct operation.

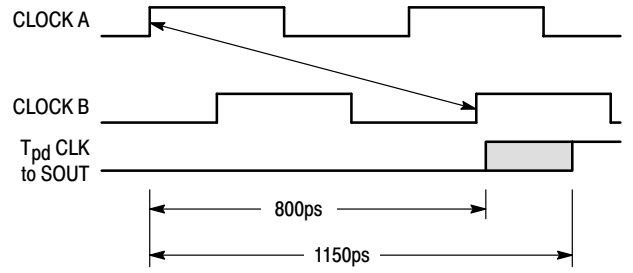


Figure 7. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin the device will clock a half a clock period after the first E445 (Figure 8). Utilizing this simple technique will raise the potential conversion frequency up to 1.4GHz. The divide by eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445's will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

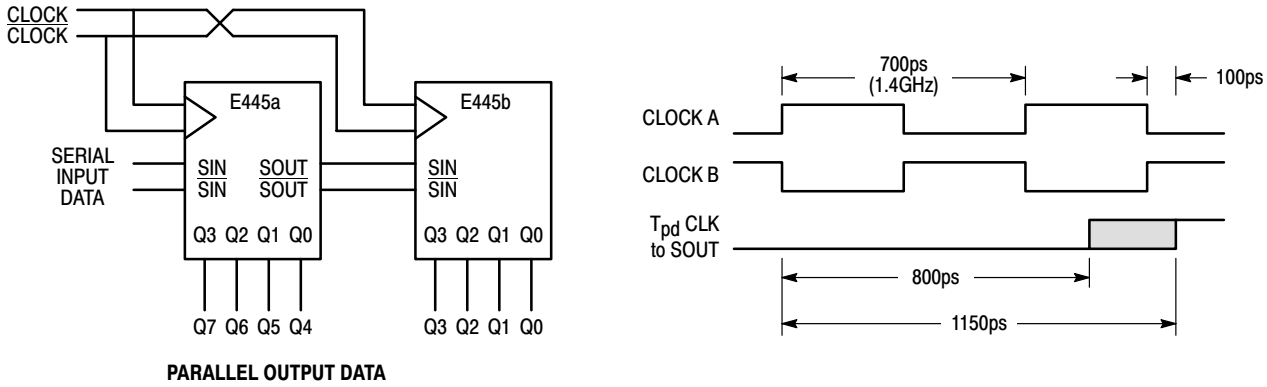


Figure 8. Extended Frequency 1:8 Demultiplexer

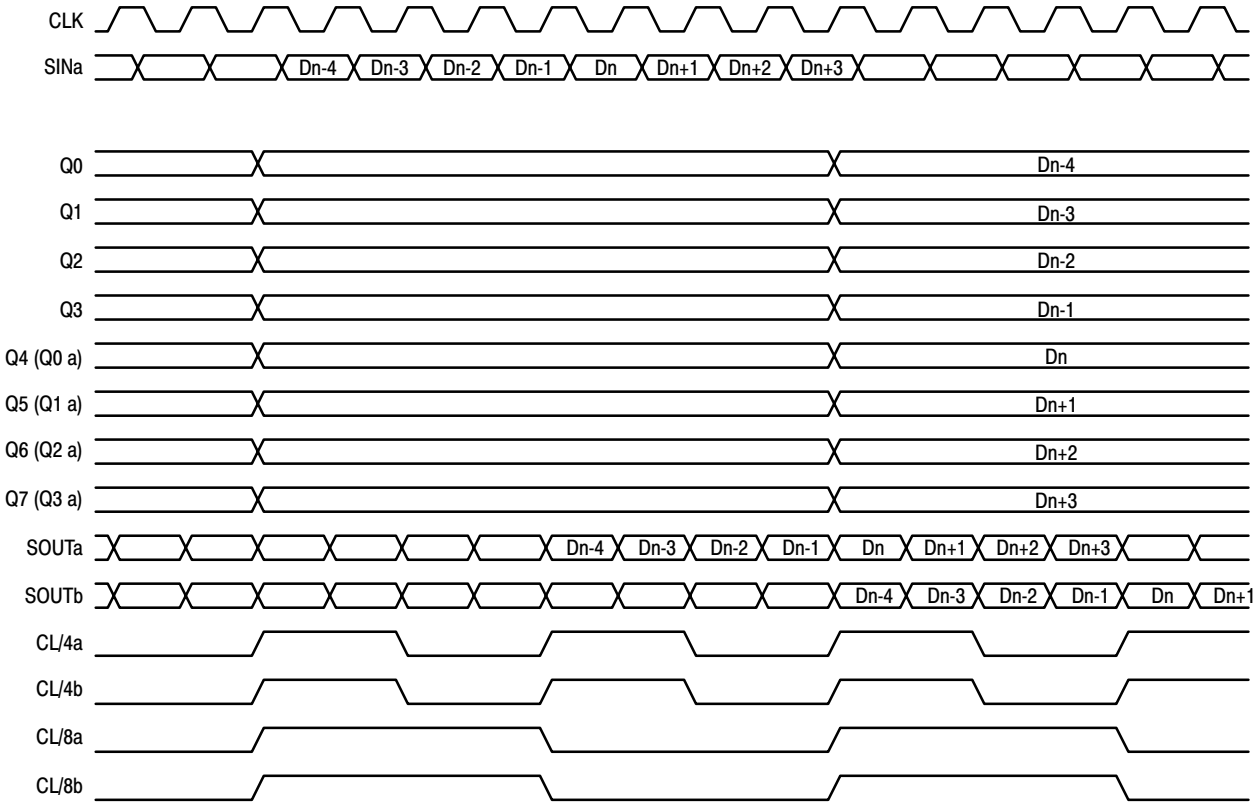
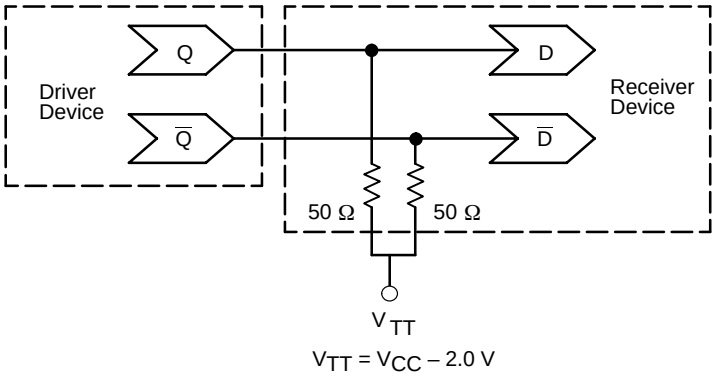


Figure 9. Timing Diagram A. 1:8 Serial to Parallel Conversion



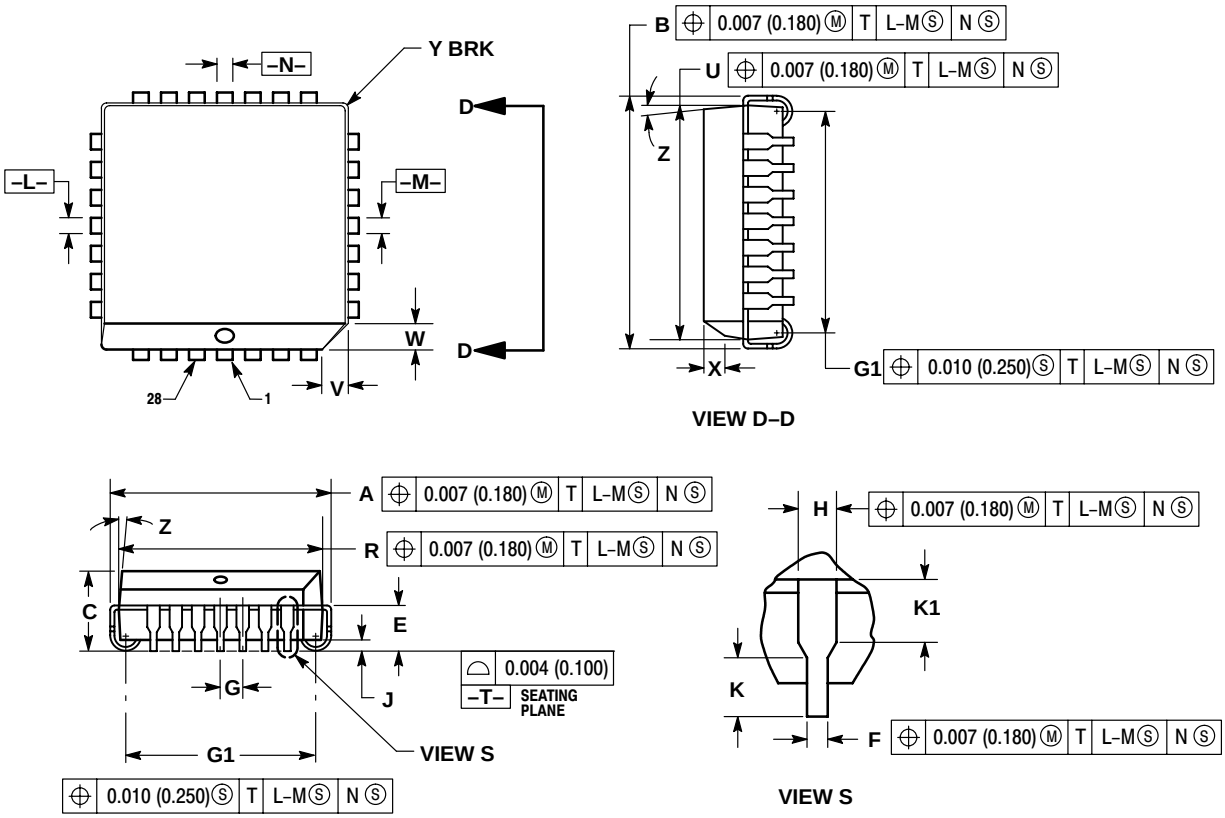
Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

Notes

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