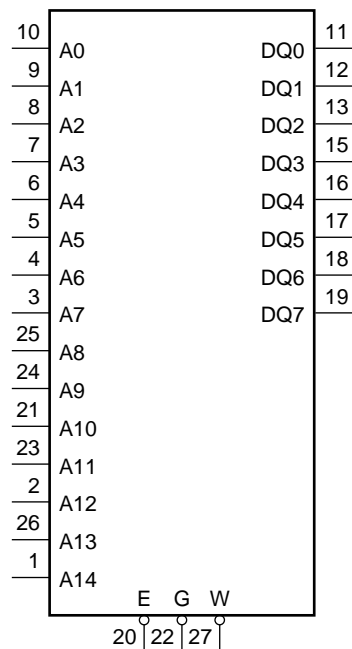
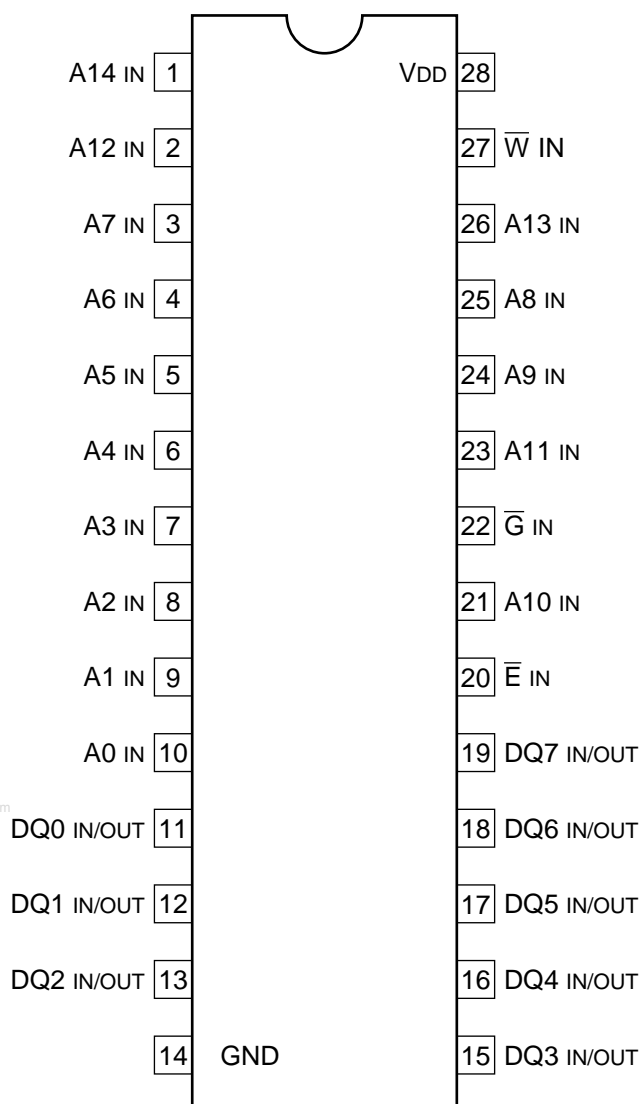


## C-MOS 256 K (32,768 × 8)-BIT SRAM

—TOP VIEW—



A0 - A14 ; ADDRESS INPUTS  
 DQ0 - DQ7 ; DATA INPUTS/OUTPUTS  
 $\bar{E}$  ; CHIP ENABLE  
 $\bar{G}$  ; OUTPUT ENABLE  
 $\bar{W}$  ; WRITE ENABLE

MODE	E	G	W	DQ0-DQ7	POWER
READ	0	1	1	HI-Z	ACTIVE
READ	0	1	0	DOUT	ACTIVE
WRITE	0	0	X	DIN	ACTIVE
DESELECT	1	X	X	HI-Z	STANDBY

1 ; HIGH LEVEL  
 0 ; LOW LEVEL  
 X ; DON'T CARE  
 HI-Z ; HIGH IMPEDANCE

