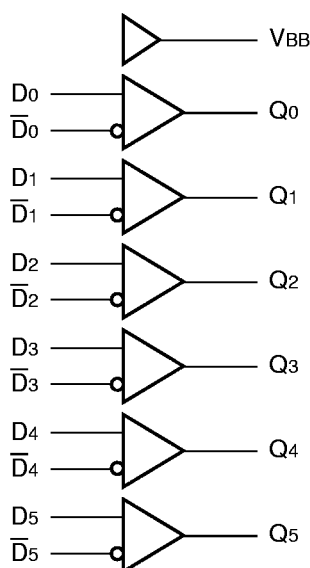


FEATURES

- Max. propagation delay of 3.7ns
- IEE min. of -37mA
- TTL outputs
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- 25% faster than National's 325
- Differential inputs with built-in offset
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- Internal 75K Ω input pull-down resistors
- Function and pinout compatible with National and Signetics (F100K)
- ESD protection of 2000V
- Available in 24-pin CERPDP, 24-pin CERPDP and 28-pin PLCC packages

BLOCK DIAGRAM



PIN NAMES

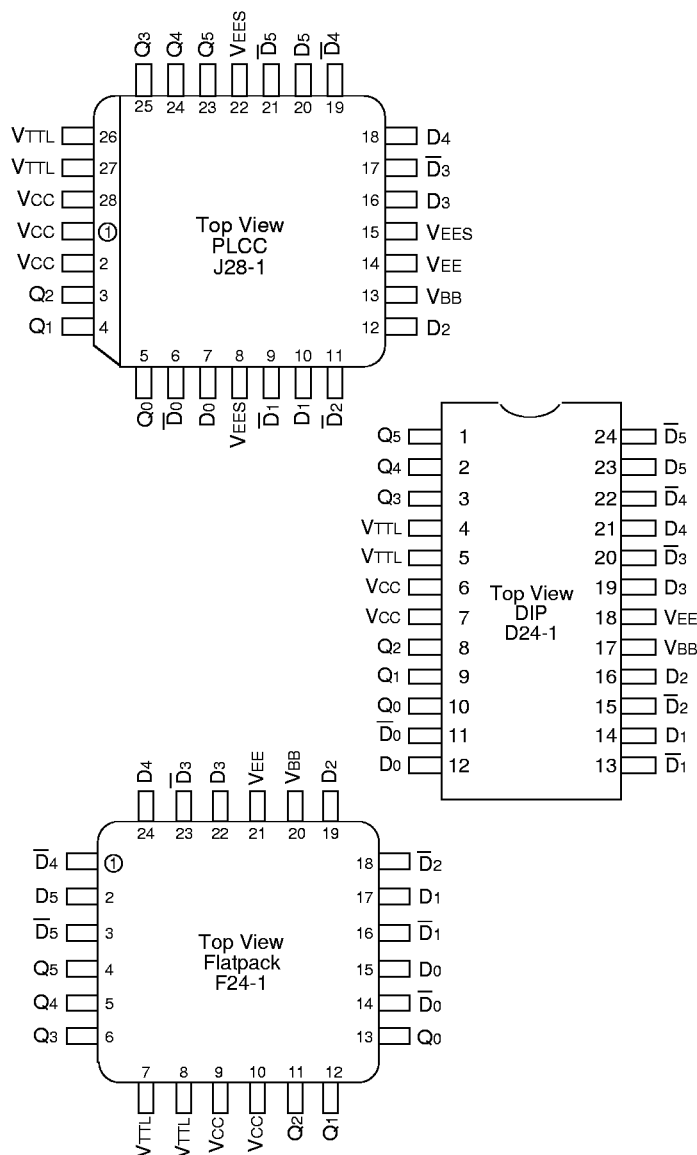
Pin	Function
D0-D5	Data Inputs
D0-D5	Inverting Data Inputs
Q0-Q5	Data Outputs
VEES	VEE Substrate
VTTL	TTL Vcc Power Supply
VCCA	Vcco for ECL Outputs

DESCRIPTION

The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75K Ω pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The VTTL and VEE power may be applied in either order.

PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5	—	—	V	$I_{OH} = -2.0mA$	$V_{IN} = V_{IH} (Max.)$
V_{OL}	Output LOW Voltage	—	—	0.5	V	$I_{OL} = 24mA$	$V_{IN} = V_{IL} (Min.)$
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible $\pm V_{CM}$ with Respect to V_{BB}	
I_{IH}	Input HIGH Current	—	—	350	μA	$V_{IN} = V_{IH} (Max.)$, $D_0-D_5 = V_{BB}$, $\underline{D_0-D_5} = V_{IL} (Min.)$	
I_{IL}	Input LOW Current	0.5	—	—	μA	$V_{IN} = V_{IH} (Min.)$, $D_0-D_5 = V_{BB}$	
I_{OS}	Output Short Circuit Current	-150	-80	-60	mA	$V_{OUT} = GND$	
I_{EE}	V_{EE} Power Supply Current	-37	-24	-17	mA	$D_0-D_5 = V_{BB}$	
I_{TTL}	V_{TTL} Power Supply Current	—	42	65	mA	$D_0-D_5 = V_{BB}$	
V_{BB}	Output Reference Voltage	-1380	-1320	-1260	mV	$I_{VBB} = -2.1mA$	
V_{IH}	Single-Ended Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V_{BB})	

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	2.2	3.0	ns	$C_L = 15pF$, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	3.2	3.8	ns	$C_L = 50pF$, Figure 2

PLCC/FLATPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	$C_L = 15pF$, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	$C_L = 50pF$, Figure 2

SWITCHING WAVEFORM

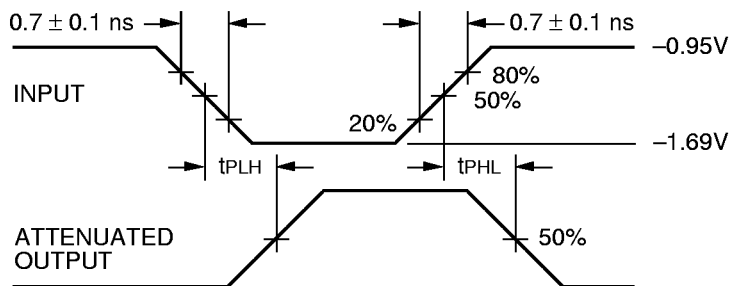


Figure 1. Propagation Delay

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

TEST CIRCUITS

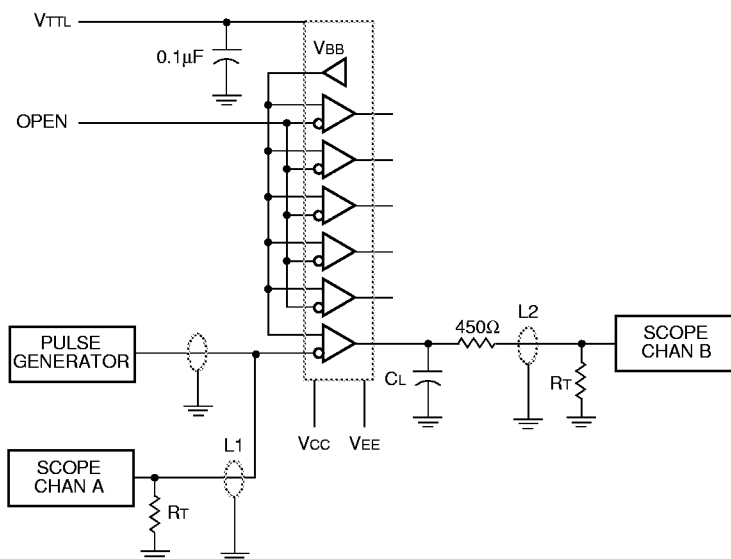


Figure 2. AC Test Circuit for 15pF Loading

NOTES:

$V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1μF from GND to V_{CC} , V_{EE} and V_{TTL}

All unused outputs are loaded with 500Ω to GND

C_L = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

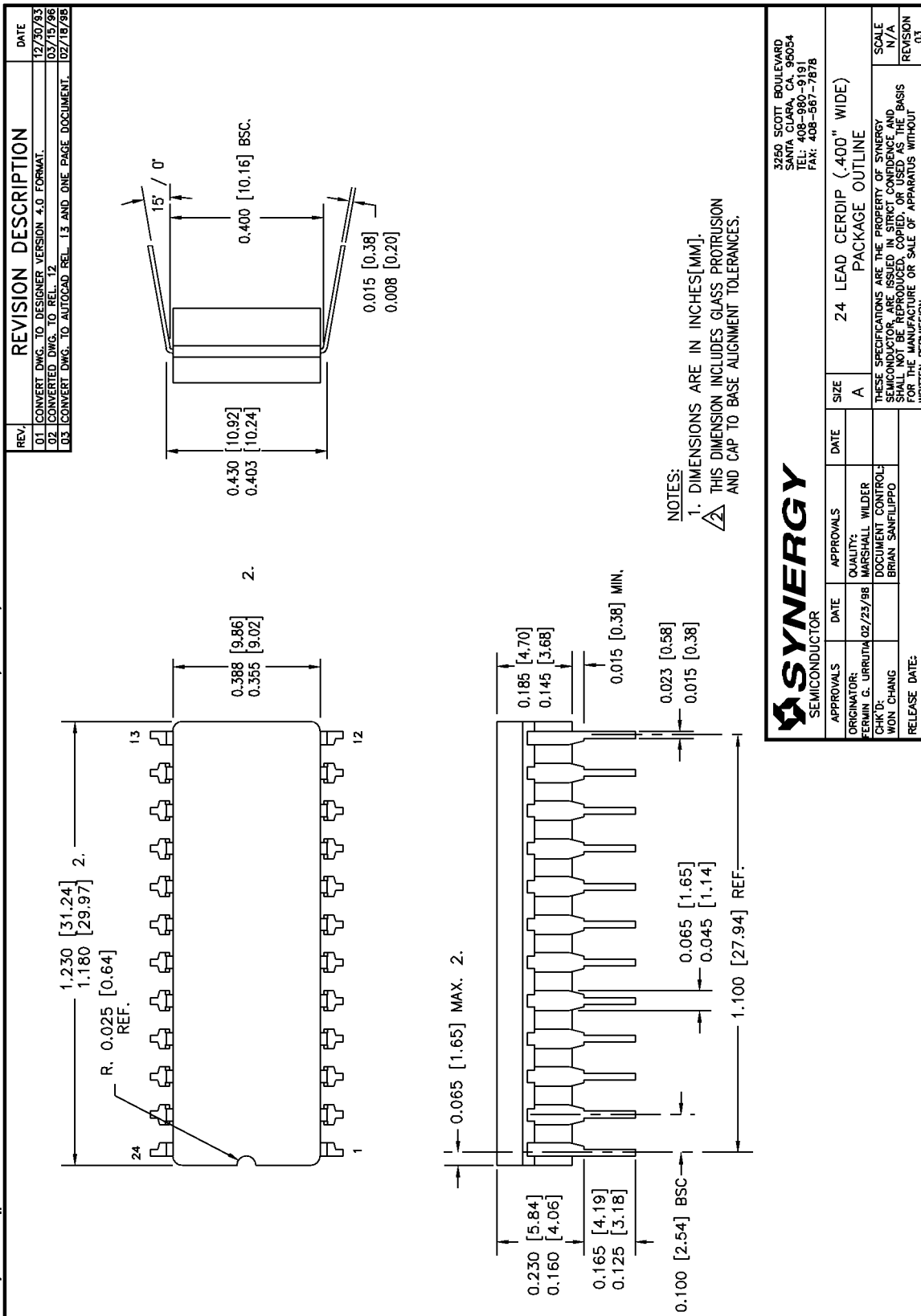
Ordering Code	Package Type	Operating Range
SY100S325DC	D24-1	Commercial
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial
SY100S325JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1



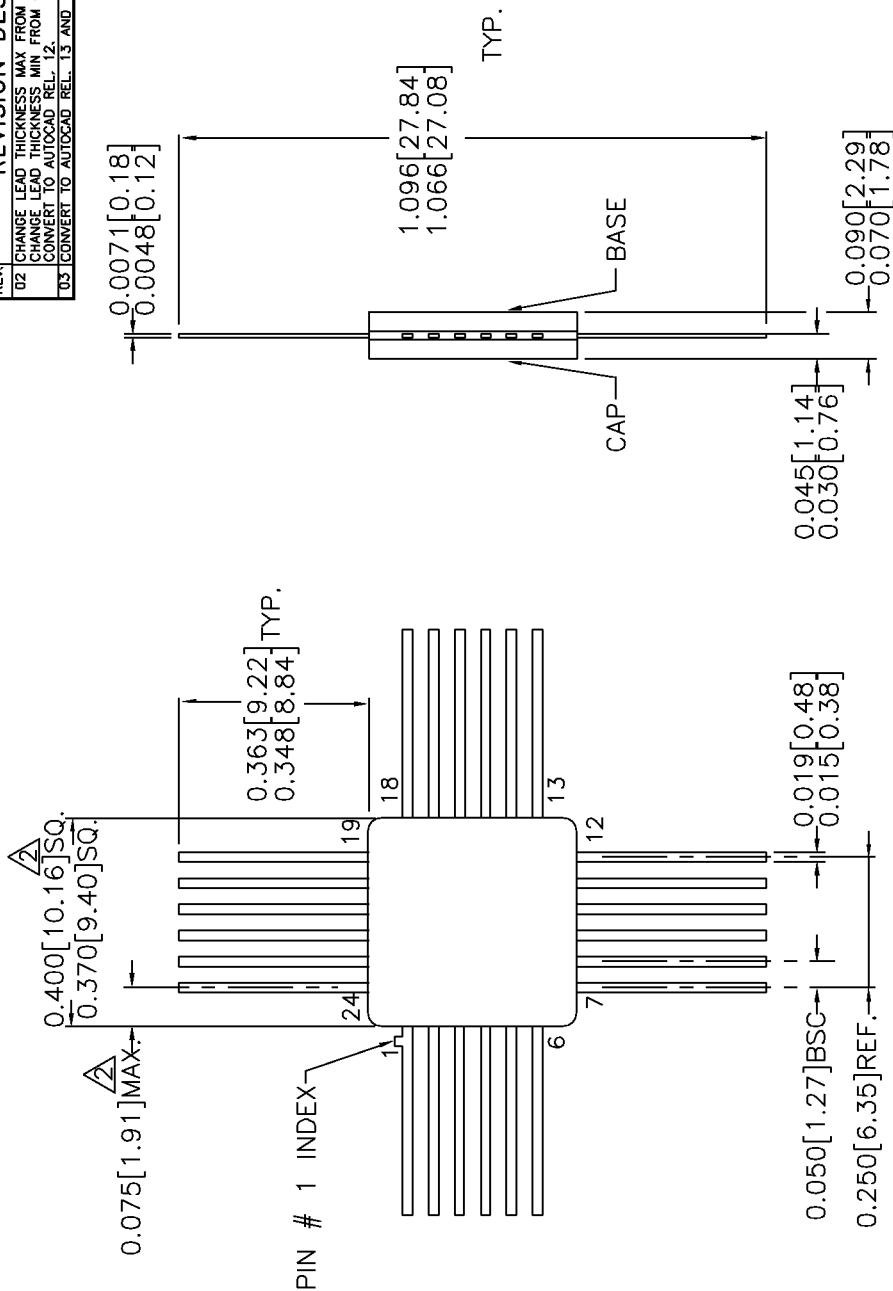
24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006[0.15] TO 0.0071[0.18] CHANGE LEAD THICKNESS MIN FROM 0.004[0.10] TO 0.0048[0.12] CONVERT TO AUTOCAD REL. 12.	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

SCALE
N/A

REVISION
03

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

FILE/REV #: PD0008A03

PD/0008/ASCORP

PAGE 1 OF 1

