U 4223 B

Time code receiver

Description

The U 4223 B is a bipolar integrated straight through receiver circuit in the frequency range of 40 to 80 kHz. The device is designed for radio controlled clock applications.

Features

- Very low power consumption
- Very high sensitivity
- High selectivity by using two crystal filters
- Power down mode available
- Only a few external components necessary
- 4 bit digital output
- AGC hold mode

Block Diagram

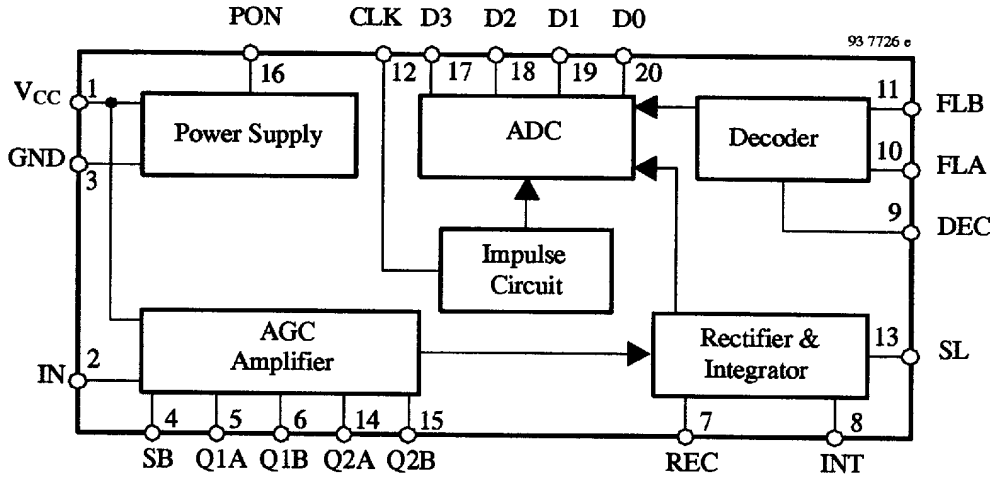
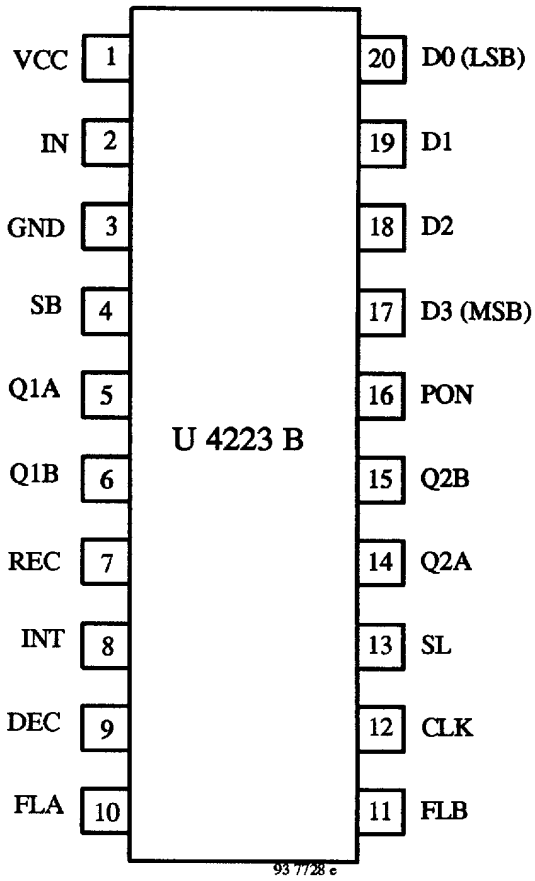


Figure 1

U 4223 B

Pin Description

Pin SO 20 L	Pin SSO 20	Symbol	Function
1	1	V_{CC}	Supply voltage
2	2	IN	Amplifier – Input
3	3	GND	Ground
4	4	SB	Bandwidth control
5	5	Q1A	Crystal filter 1
6	6	Q1B	Crystal filter 1
7	7	REC	Rectifier output
8	8	INT	Integrator output
9	9	DEC	Decoder input
10	10	FLA	Low pass filter
11	11	FLB	Low pass filter
12	12	CLK	Clock input for ADC
13	13	SL	AGC hold mode
14	14	Q2A	Crystal filter 2
15	15	Q2B	Crystal filter 2
16	16	PON	Power ON/OFF control
17	17	D3	Data out MSB
18	18	D2	Data out
19	19	D1	Data out
20	20	D0	Data out LSB

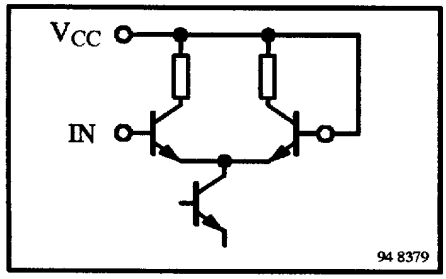


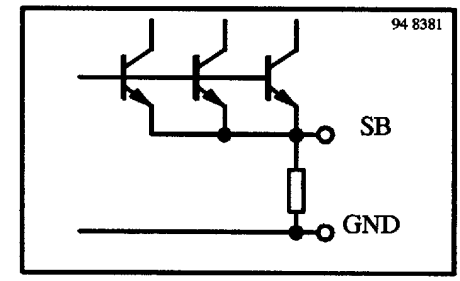
IN

A ferrite antenna is connected between IN and V_{CC}. For high sensitivity the Q of the antenna circuit should be as high as possible, but a high Q often requires temperature compensation of the resonant frequency. Specifications are valid for Q>30. An optimal signal to noise ratio will be achieved by a resonant resistance of 50 to 200 kΩ.

SB

A resistor R_{SB} is connected between SB and GND. It controls the bandwidth of the crystal filters. It is recommended: R_{SB} = 0 Ω for DCF 77.5 kHz and WWVB 60 kHz applications and R_{SB} = 22 kΩ for JG2AS 40kHz.

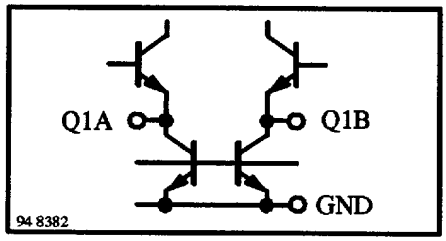




Q1A, Q1B

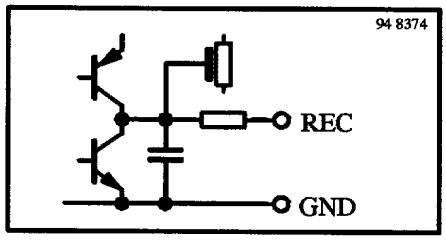
In order to achieve a high selectivity, a crystal is connected between the pins Q1A and Q1B. It is used with the serial resonance frequency of the time code transmitter (e.g. 60 kHz WWVB, 77.5 kHz DCF or 40kHz JG2AS).

The equivalent parallel capacitor of the filter crystal is internally compensated. The compensated value is about 0.7 pF. If the full sensitivity and selectivity is not needed, the crystal filter can be substituted by a capacitor of 82 pF.



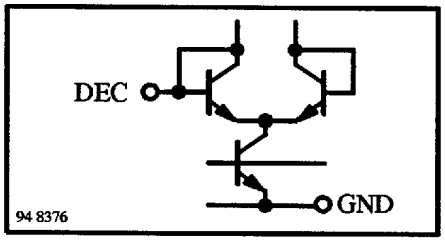
REC

Rectifier output and integrator input: The capacitor C1 between REC and INT is the lowpass filter of the rectifier and at the same time a damping element of the gain control.



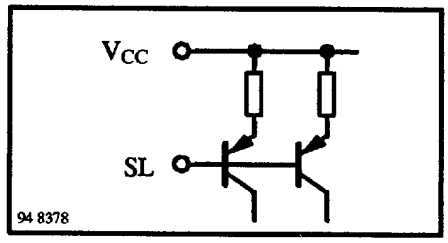
DEC

Decoder input: Senses the current through the integration capacitor C2. The dynamic input resistance has a value of about 420kΩ and is low compared to the impedance of C2.



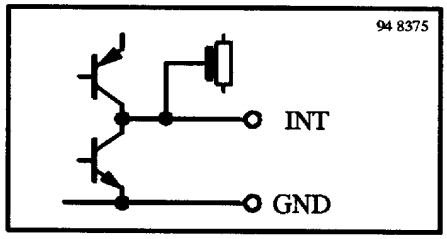
SL

AGC hold mode: SL high (V_{SL} = V_{CC}) sets normal function, SL low (V_{SL} = 0) disconnects the rectifier and holds the voltage V_{INT} at the integrator output and also the AGC amplifier gain.



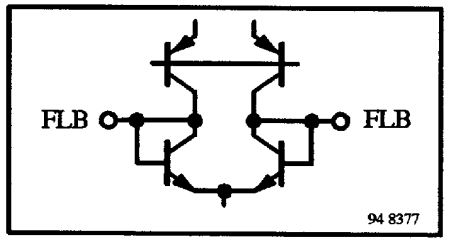
INT

Integrator output: The voltage V_{INT} is the control voltage for the AGC. The capacitor C2 between INT and DEC defines the time constant of the integrator. The current through the capacitor is the input signal of the decoder.



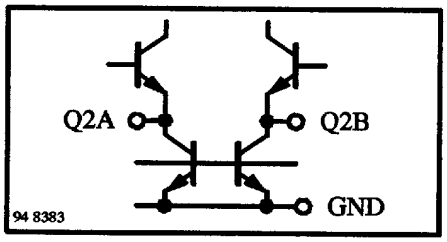
FLA, FLB

Lowpass filter: A capacitor C3 connected between FLA and FLB supresses higher frequencies at the trigger circuit of the decoder.



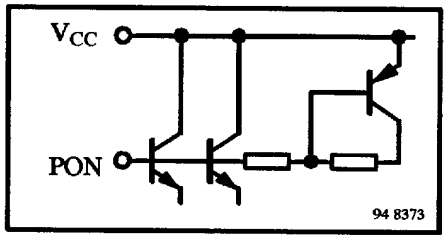
Q2A, Q2B

According to Q1A, Q1B a crystal is connected between the pins Q2A and Q2B. It is used with the serial resonance frequency of the time code transmitter (e.g. 60 kHz WWVB, 77.5 kHz DCF or 40 kHz JG2AS). The equivalent parallel capacitor of the filter crystal is internally compensated. The value of the compensation is about 0.7 pF.



PON

If PON is connected to GND, the U 4224 B receiver IC will be activated. The set-up time is typical 0.5s after applying GND at this pin. If PON is connected to V_{CC}, the receiver will go into power down mode.

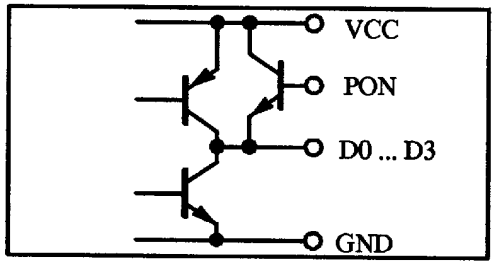


D0, D1, D2, D3

The outputs of the ADC consist of pnp-npn push-pull stages and can be directly connected to a microcomputer. In order to avoid any interference of the output into the antenna circuit we recommend terminating each digital output with a capacitor of 10 nF. The digitalized signal of the ADC is Gray coded (see table). It should be taken into account that in the power down mode (PON = high) D0, D1, D2 and D3 will be high.

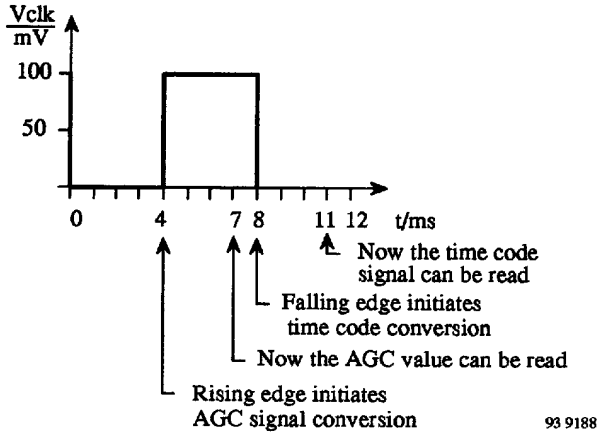
A sequence of the digitalized time code signal can be analysed by a special noise suppressing algorithm in order to increase the sensitivity and the signal to noise ratio (more than 10 dB compared to a conventional decoding). Details about the time code format are described separately.

Decimal	Gray
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

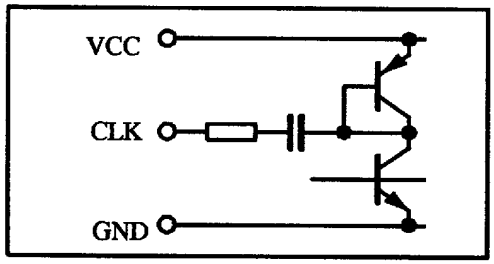


CLK

The input of the ADC is switched to the AGC voltage by the rising edge of the clock. After the conversion time (about 1.8 ms at 25°C) the digitalized field strength signal is stored in the output registers D0 to D3 as long as the clock is high and can be read by a microcomputer. The falling edge of the clock switches the input of the ADC to the time code signal. After the conversion time the digitalized time code signal is stored in the output registers D0 to D3 as long as the clock is low (see figure below).



In order to minimize interferences we recommend a voltage swing of about 100 mV. A full supply voltage swing is possible but it reduces the sensitivity.

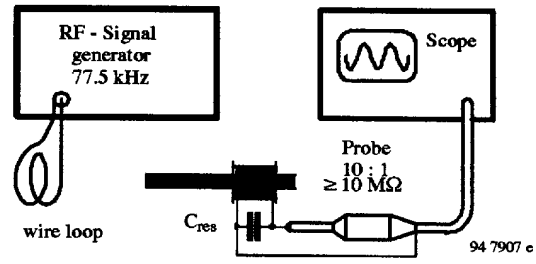


Please note:
The signals and voltages at the pins REC, INT, FLA, FLB, Q1A, Q1B, Q2A and Q2B cannot be measured by standard measurement equipment due to very high internal impedances. For the same reason the PCB should be protected against surface humidity.

Design Hints for the Ferrite Antenna

The bar antenna is a very critical device of the complete clock receiver. But by observing some basic RF design knowledge, no problem should arise with this part. The IC requires a resonance resistance of 50 kΩ to 200 kΩ. This can be achieved by a variation of the L/C-relation in the antenna circuit. But it is not easy to measure such high resistances in the RF region. It is much more convenient to distinguish the bandwidth of the antenna circuit and afterwards to calculate the resonance resistance.

Thus the first step in designing the antenna circuit is to measure the bandwidth. Figure 4 shows an example for the test circuit. The RF signal is coupled into the bar antenna by inductive means, e.g. a wire loop. It can be measured by a simple oscilloscope using the 10:1 probe. The input capacitance of the probe, typically about 10 pF, should be taken into consideration. By varying the frequency of the signal generator, the resonance frequency can be determined.



Afterwards, the two frequencies where the voltage of the rf signal at the probe drops 3 dB down can be measured. The difference between these two frequencies is called the bandwidth BW_A of the antenna circuit. As the value of the capacitor C_{res} in the antenna circuit is well known, it is easy to compute the resonance resistance according to the following formula:

$$R_{res} = \frac{1}{2 \cdot \pi \cdot BW_A \cdot C_{res}}$$

whereas
R_{res} is the resonance resistance,
BW_A is the measured bandwidth (in Hz)
C_{res} is the value of the capacitor in the antenna circuit (in Farad)

If high inductance values and low capacitor values are used, the additional parasitic capacitances of the coil must be considered. It may reach up to about 20 pF. The Q-value of the capacitor should be no problem if a high Q-type is used. The Q-value of the coil is more or less distinguished by the simple DC-resistance of the wire. Skin effects can be observed but do not dominate.

Therefore it shouldn't be a problem to achieve the recommended values of resonance resistance. The use of thicker wire increases Q and accordingly reduces bandwidth. This is advantageous in order to improve reception in noisy areas. On the other hand, temperature compensation of the resonance frequency might become a problem if the bandwidth of the antenna circuit is low compared to the temperature variation of the resonance frequency. Of course, Q can also be reduced by a parallel resistor.

Temperature compensation of the resonance frequency is a must if the clock is used at different temperatures. Please ask your dealer of bar antenna material and of capacitors for specified values of temperature coefficient.

Furthermore some critical parasitics have to be considered. These are shortened loops (e.g. in the ground line of the PCB board) close to the antenna and undesired loops in the antenna circuit. Shortened loops decrease Q of the circuit. They have the same effect like conducting plates close to the antenna. To avoid undesired loops in the antenna circuit it is recommended to mount the capacitor C_{res} as close as possible to the antenna coil or to use a twisted wire for the antenna coil connection. This twisted line is also necessary to reduce feedback of noise from the microprocessor to the IC input. Long connection lines must be shielded.

A final adjustment of the time code receiver can be done by pushing the coil along the bar antenna. The maximum of the integrator output voltage V_{INT} at pin INT indicates the resonant point. But attention: The load current should not exceed 1 nA, that means an input resistance $\geq$ 1 GΩ of the measuring device is required. Therefore a special DVM or an isolation amplifier is necessary.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	5.25	V
Ambient temperature range	T_{amb}	–25 to +75	°C
Storage temperature range	R_{stg}	–40 to +85	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883 C), excepted pins 2, 5, 6, 14 and 15	$\pm V_{ESD}$	2000	V

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Thermal resistance	R_{thJA}	70	K/W

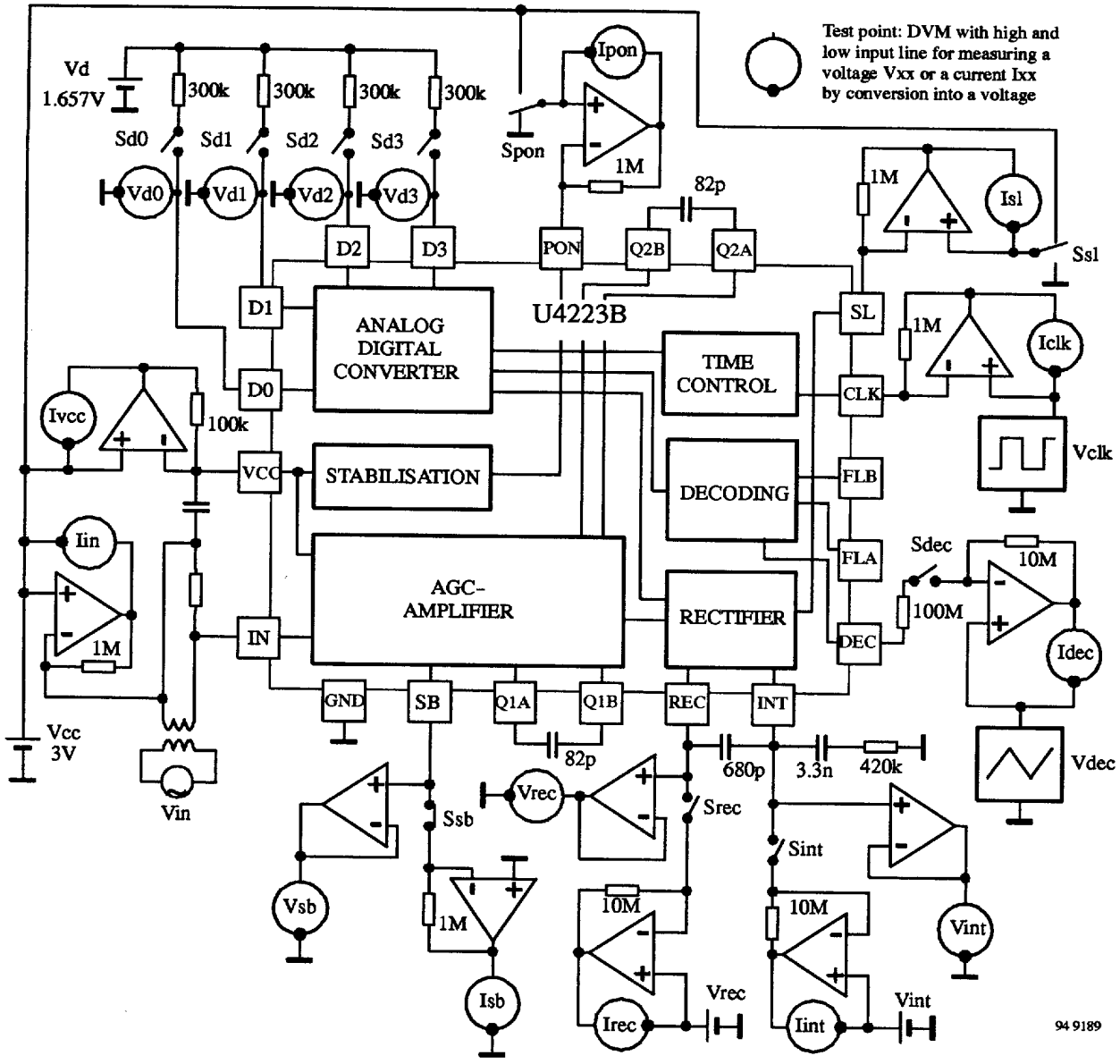
Electrical Characteristics

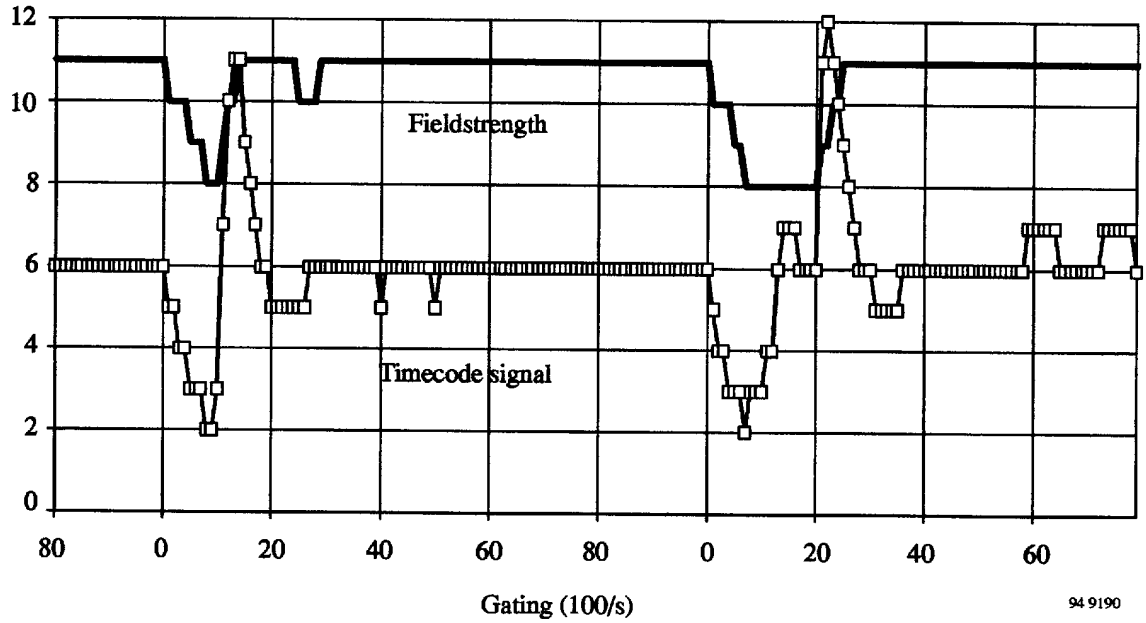
V_{CC} = 3 V, reference point pin 3, input signal frequency 80 kHz, T_{amb} = 25 °C, unless otherwise specified

Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
Supply voltage range	pin 1	V_{CC}	1.2		5.25	V
Supply current	pin 1 without reception signal with reception signal = 200µV OFF-mode	I_{CC}		 15	 30 25 0.1	 µA µA µA
Set-up time after V_{CC} ON	V_{CC} = 1.5 V	t		2		s
AGC AMPLIFIER INPUT; IN	pin 2					
Reception frequency range		f_{in}	40		80	kHz
Minimum input voltage	R_{res} = 100 kΩ, Q_{res} > 30	V_{in}		1	1.5	µV
Maximum input voltage		V_{in}	40	80		mV
Input capacitance to ground		C_{in}		1.5		pF
ADC; D0, D1, D2, D3	pin 17, 18, 19, 20					
Output voltage HIGH LOW	 R_{LOAD} = 870 kΩ to GND R_{LOAD} = 650 kΩ to V_{CC}	 V_{OH} V_{OL}	 V_{CC}-0.4		 0.4	 V V
Output current HIGH LOW	 V_{TCO} = V_{CC}/2 V_{TCO} = V_{CC}/2	 I_{SOURCE} I_{SINK}	 3 4	 10 12		 µA µA
Input current into DEC (first bit)	falling edge of CLK	I_{decs}	-32	-25	-18	nA
Input current into DEC (last bit)	falling edge of CLK	I_{dece}	28	35	42	nA
Input current into DEC (step range)	falling edge of CLK	I_{decst}	1.75	4	7	nA
Input voltage at IN (first bit)	RF generator at IN, without modulation rising edge of CLK	V_{min}		-10		dBµV
Input voltage at IN (last bit)	RF generator at IN, without modulation rising edge of CLK	V_{max}		60		dBµV
Input voltage at IN (step range)	RF generator at IN, without modulation rising edge of CLK	V_{step}		4.7		dBµV
CLOCK INPUT; CLK	pin 12					
Input voltage swing		V_{swing}	50	100	V_{CC}	mV
Clock frequency		f_{clk}		100	125	Hz
Dynamical input resistance		$R_{dyn.}$		100		kΩ
POWER ON/OFF CONTROL; PON	pin 16					
Input voltage HIGH LOW	Required I_{IN} ≧ 0.5 µA		 V_{CC}-0.2		 V_{CC}-1.2	 V V
Input current	V_{CC} = 3V V_{CC} = 1.5 V V_{CC} = 5 V	I_{IN}	1.4	1.7 0.7 3	2	µA µA µA
Set-up time after PON		t		0.5	2	s

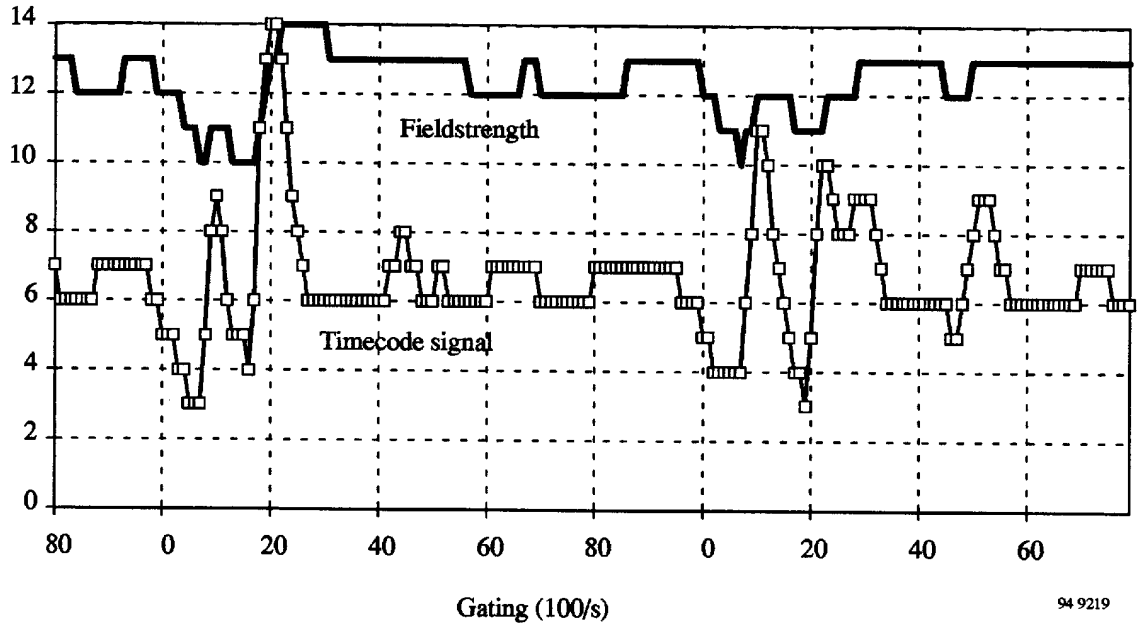
Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
AGC HOLD MODE; SL	pin 13					
Input voltage HIGH LOW	Required $I_{IN} \geqq 0.5\ \mu A$		V_{CC}-0.2		 V_{CC}-1.2	 V V
Input current	Vin = V_{CC} Vin = GND			 2.5	0.1	µA µA
Attenuation of undesired signal	$\lvert f_d - f_{ud} \rvert$ = 625 Hz V_d = 3 µV, f_d = 77.5 kHz using 2 crystal filters using 1 crystal filter	 a_f a_f		 43 22		 dB dB

Test Circuit (for fundamental function)



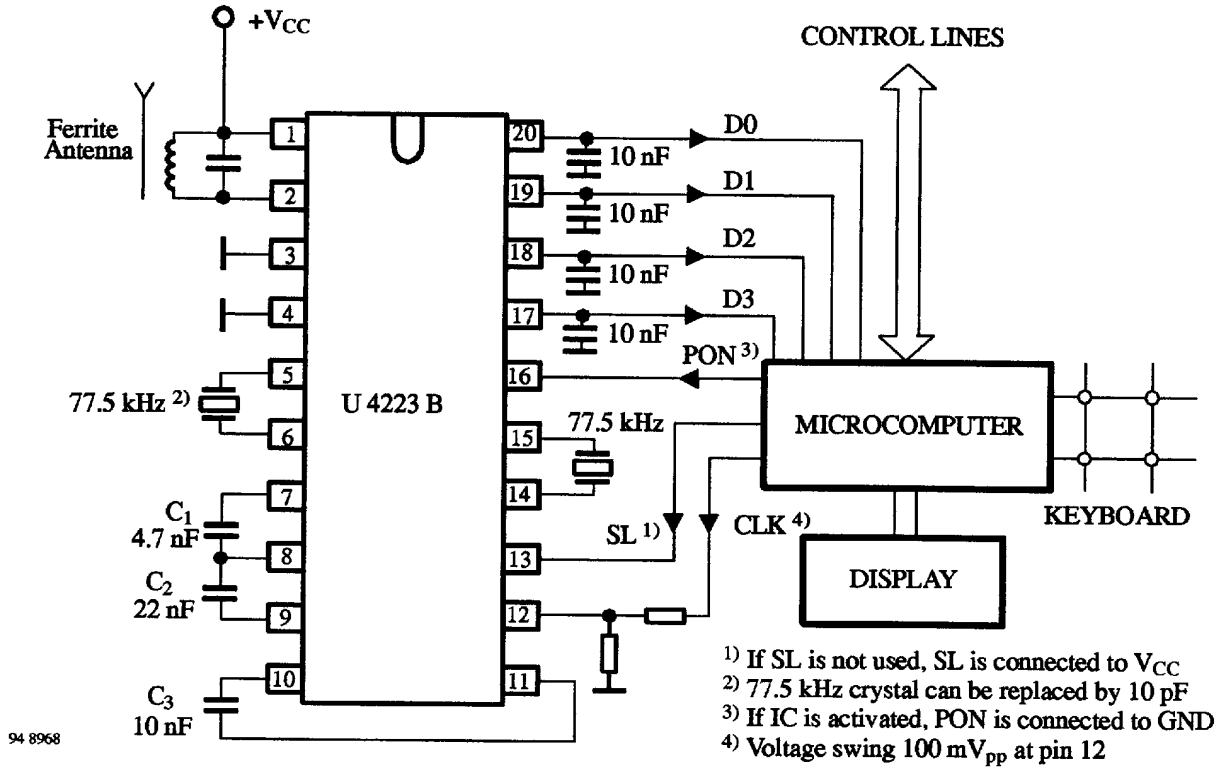


Example of a normal DCF signal



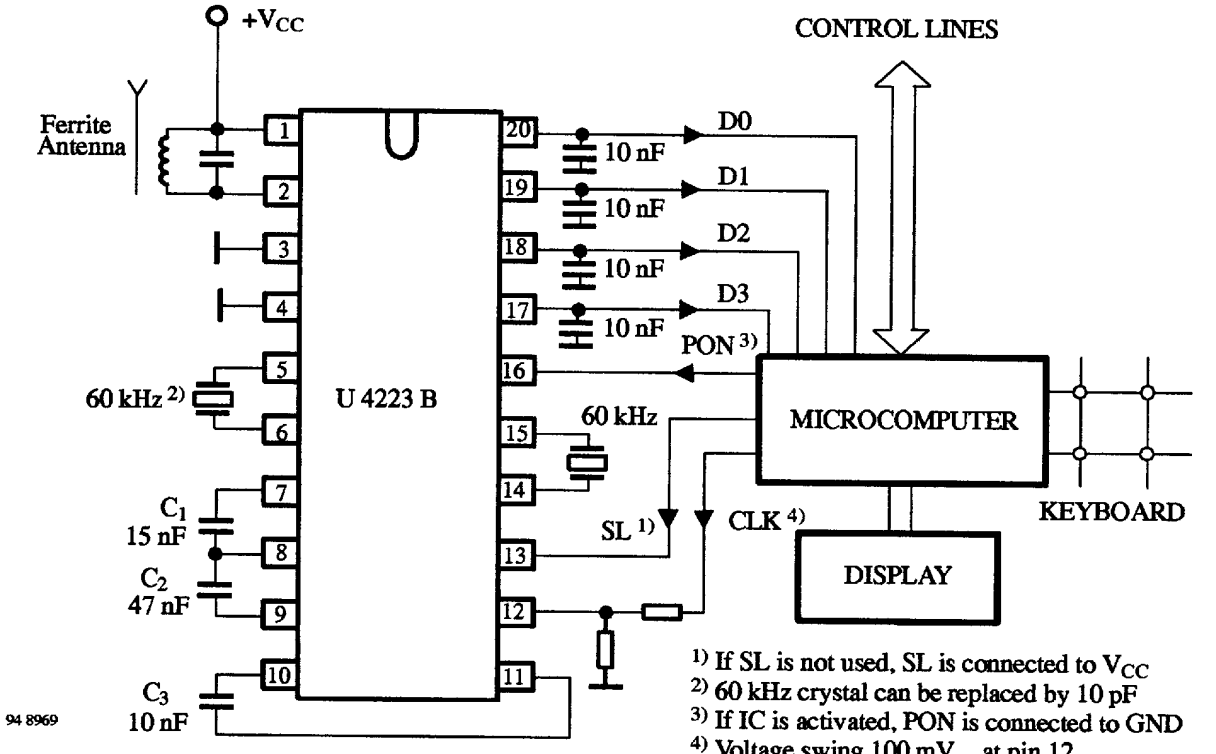
Example of a disturbed DCF signal

Application Circuit for DCF 77.5 kHz



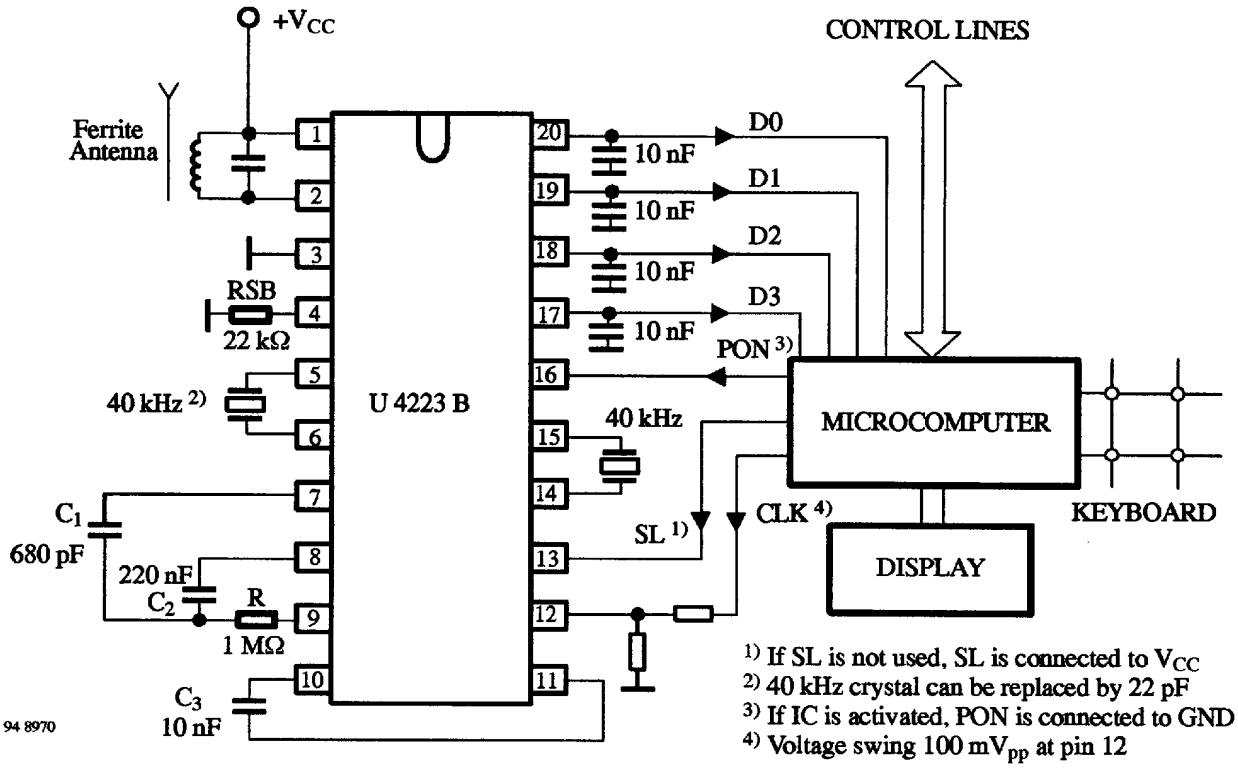
1) If SL is not used, SL is connected to V_{CC}
2) 77.5 kHz crystal can be replaced by 10 pF
3) If IC is activated, PON is connected to GND
4) Voltage swing 100 mV_{pp} at pin 12

Application Circuit for WWVB 60 kHz



1) If SL is not used, SL is connected to V_{CC}
2) 60 kHz crystal can be replaced by 10 pF
3) If IC is activated, PON is connected to GND
4) Voltage swing 100 mV_{pp} at pin 12

Application Circuit for JG2AS 40 kHz



1) If SL is not used, SL is connected to V_{CC}
2) 40 kHz crystal can be replaced by 22 pF
3) If IC is activated, PON is connected to GND
4) Voltage swing 100 mV_{pp} at pin 12

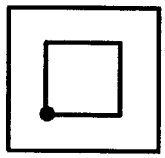
PAD Coordinates

The T 4223 B is also available as die for "Chip on board" mounting.
DIE size: 2.26 x 2.09 mm
PAD size: 100 x 100 µm (contact window 88 x 88 µm)
Thickness: 200 µm ± 20 µm

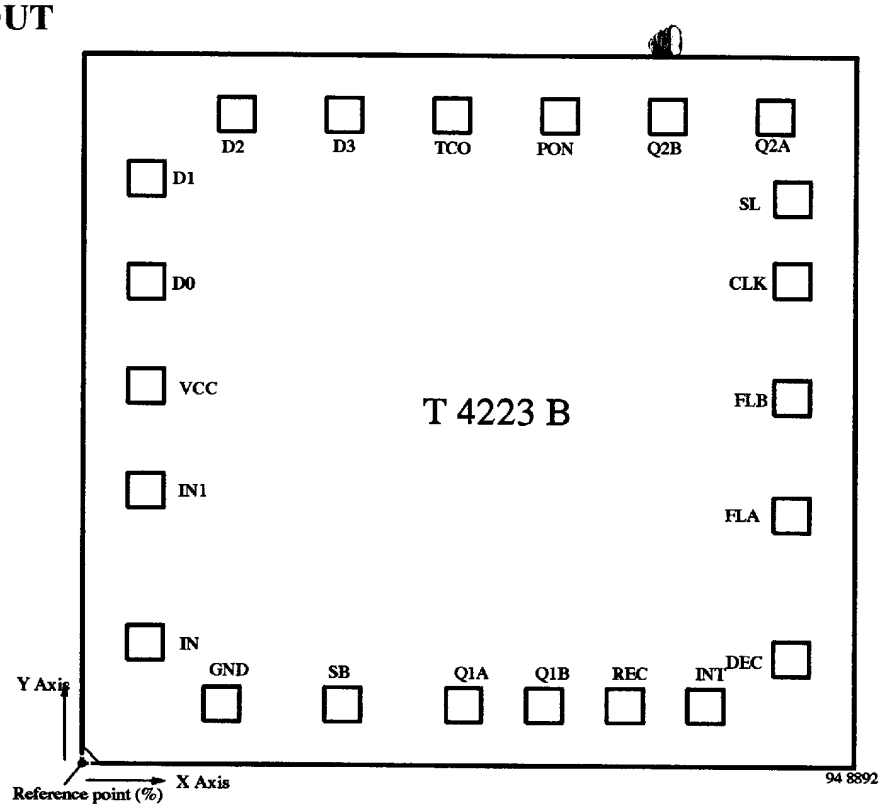
SYMBOL	X-Axis/µm	Y-Axis/µm
IN1	128	758
IN	128	310
GND	354	124
SB	698	128
Q1A	1040	128
Q1B	1290	128
REC	1528	128
INT	1766	128
DEC	2044	268
FLA	2044	676
FLB	2044	1012

SYMBOL	X-Axis/µm	Y-Axis/µm
CLK	2044	1372
SL	2044	1624
Q2A	1980	1876
Q2B	1634	1876
PON	1322	1876
TCO	1008	1876
D3	696	1876
D2	384	1876
D1	128	1682
D0	128	1368
VCC	128	1098

The PAD coordinates are referred to the left bottom point of the contact window.



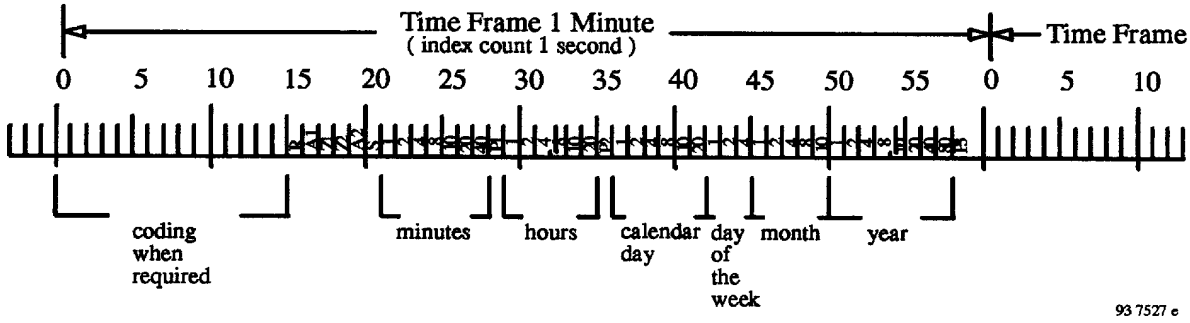
PAD LAYOUT

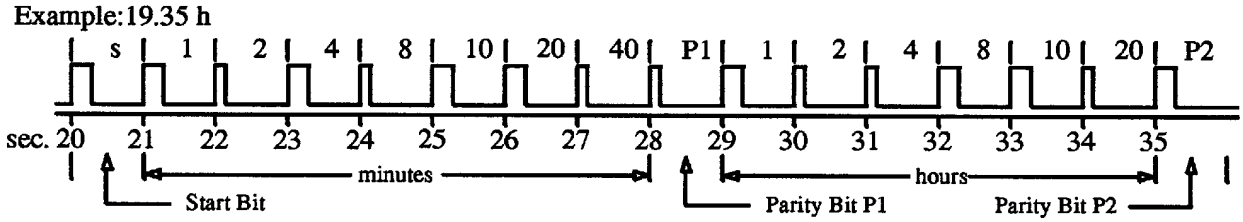


Information regarding German transmitter

Station: DCF 77,
Frequency 77.5 kHz,
Transmitting power 50 kW

Location: Mainflingen/Germany,
Geographical coordinates: 50° 0.1'N, 09° 00'E
Time of transmission: permanent





Modulation:

The carrier amplitude is reduced to 25 % at the beginning of each second for 100 ms (binary zero) or 200 ms (binary one) duration, excepting the 59th second.

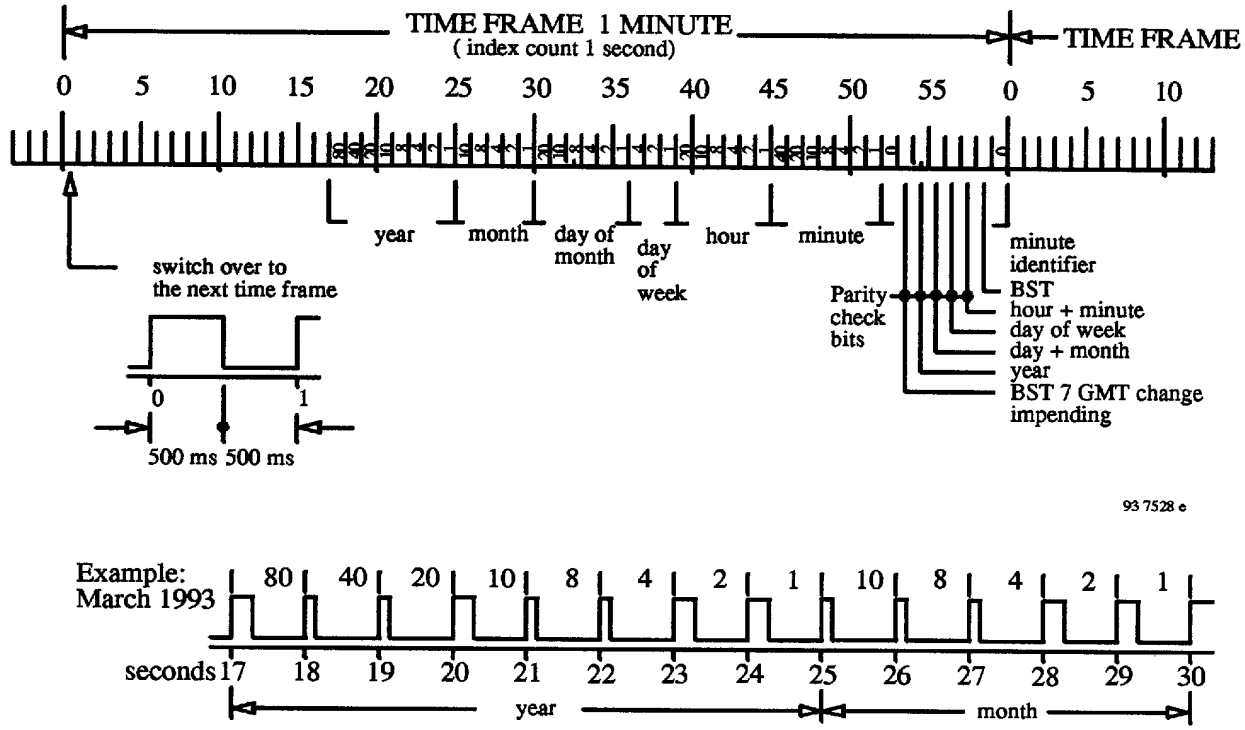
Time Code Format: (based on information of Deutsche Bundespost)

It consists of 1 minute time frames. No modulation at the beginning of the 59th second to recognize the switch over to the next 1 minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Further there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to the summer time), Z1 (during the summer time 200 ms, otherwise 100 ms), Z2 (during standard time 200 ms otherwise 100 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

Information regarding British transmitter

Station: MSF
Frequency 60 kHz
Transmitting power 50 kW
Location: Teddington, Middlesex

Geographical coordinates: 52° 22'N, 01° 11'W
Time of transmission: permanent, excepting the first tuesday of each month from 10.00 h to 14.00 h.



Modulation:

The carrier amplitude is switched off at the beginning of each second for the time of 100 ms (binary zero) or 200 ms (binary one).

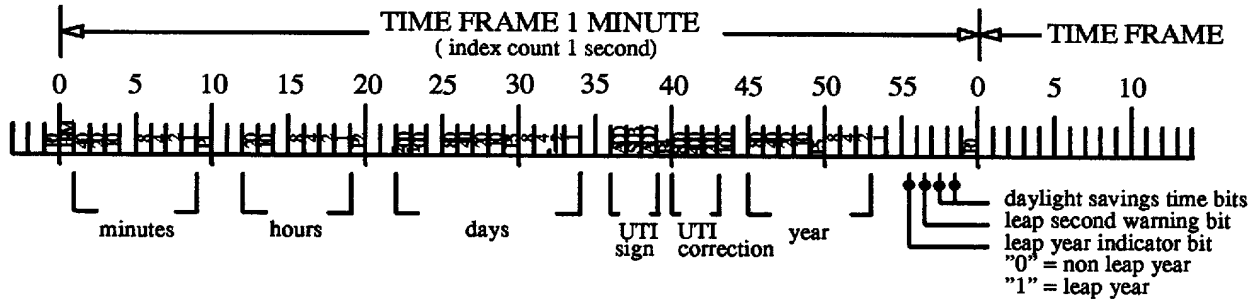
Time Code Format:

It consists of 1 minute time frames. A time frame contains BCD-coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is reduced for 500 ms duration.

Information regarding US transmitter

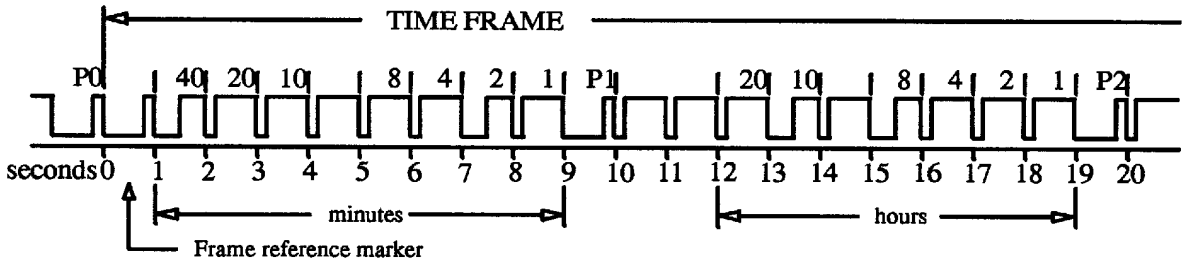
Station: WWVB
Frequency 60 kHz
Transmitting power 10 kW

Location: Fort Collins
Geographical coordinates: 40° 40'N, 105° 03'W
Time of transmission: permanent.



93 7529 e

Example: UTC 18.42 h



Modulation:

The carrier amplitude is reduced 10 dB at the beginning of each second and is restored in 500 ms (binary one) or in 200 ms (binary zero).

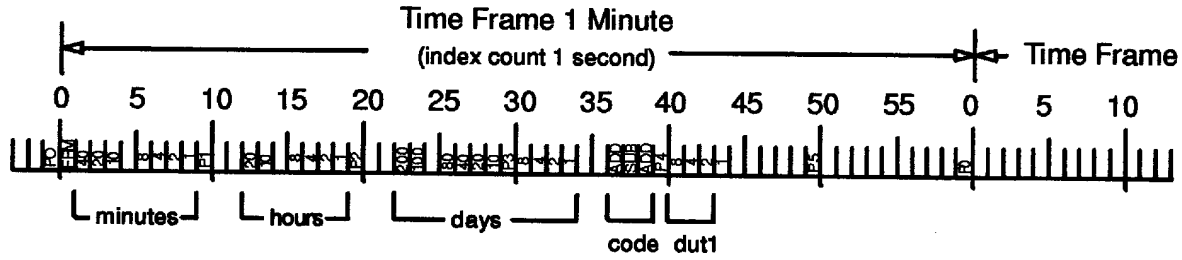
Time Code Format:

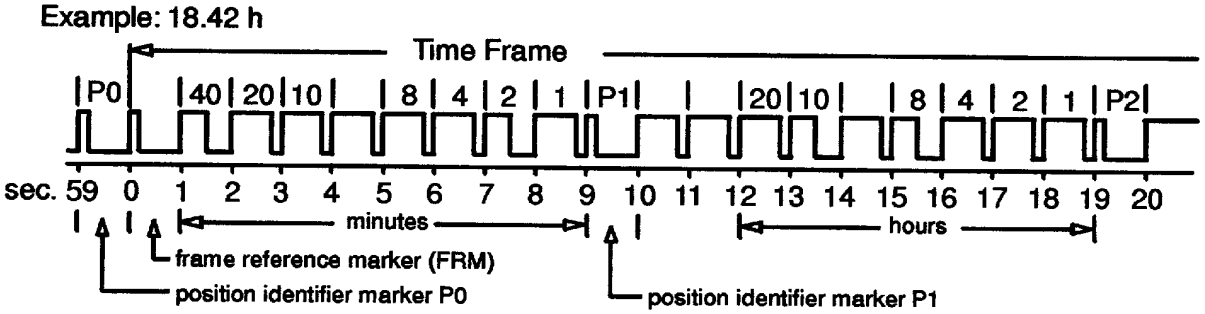
It consists of 1 minute time frames. A time frame contains BCD-coded information of minutes, hours, days and year. In addition there are 6 position identifier markers (P0 thru P5) and 1 frame reference marker with reduced carrier amplitude of 800 ms duration.

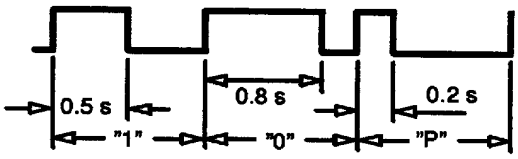
Information regarding Japanese transmitter

Station: JG2AS
Frequency 40 kHz
Transmitting power 10 kW

Location: Sanwa, Ibaraki
Geographical coordinates: 36° 11' N, 139° 51' E
Time of transmission: permanent







0.5 second: Binary one
0.8 second: Binary zero
0.2 second: Identifier markers P0...P5

93 7508 e

Modulation:

The carrier amplitude is 100% at the beginning of each second and is switched off after 500 ms (binary one) or after 800 ms (binary zero).

Time code format:

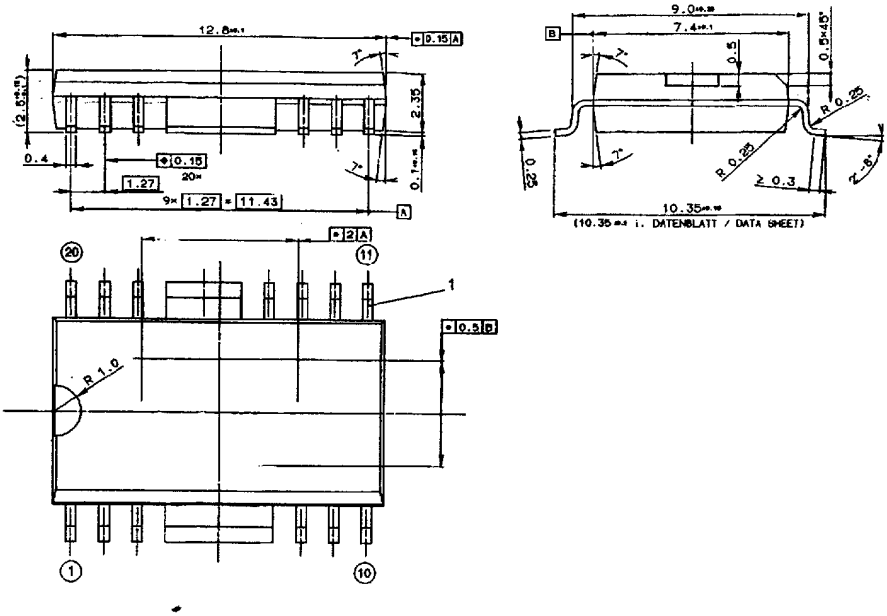
It consists of one minute time frame. A time frame contains BCD-coded information of minutes, hours and days. In addition there are 6 position identifier markers (P0 thruP5) and one frame reference markers (FRM) with reduced carrier amplitude of 800 ms duration.

Ordering and Package Information

Extended type number	Package	Remarks
U 4223 B-BFL	SO 20 plastic	
U 4223 B-BFLG3	SO 20 plastic	Taping according to IEC-286-3
U 4223 B-BFS	SSO 20 plastic	
U 4223 B-BFSG3	SSO 20 plastic	Taping according to IEC-286-3
T 4223 B-BF	no	die on foil
T 4223 B-BC	no	die on carrier

Dimensions in mm

Package: SO 20



Package: SSO 20