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# Implementing FDDI Over Copper; The ANSI X3T9.5 Standard

*Application Note*

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*The American National Standards Institute (ANSI) X3T9 Committee is developing the standard for the implementation of FDDI links (PMD layer) on copper-shielded and unshielded twisted-pair cables.*

*The content of this application note is consistent with the existing trends for specifying link parameters.*

*However, at the time of this application note release, the standard is not complete and could introduce either new specifications, or changes in the existing specifications, neither of which would not be reflected in this paper.*

# Implementing FDDI Over Copper; The ANSI X3T9.5 Standard

## *Application Note*

*by Advanced Micro Devices, Inc., Micro Linear, and Pulse Engineering, Inc.*

## OVERVIEW

The proposed ANSI TP-PMD standard has been demonstrated in Interop tests and the X3T9.5 committee is progressing quickly in preparing a final standard. The use of copper media significantly reduces the node cost by eliminating the need for expensive optical transceivers. Both Shielded Twisted Pair cable (STP) and data grade (category 5) Unshielded Twisted Pair cable (UTP-5) are covered in the new specification. Although transmission distance is limited to 100 meters, the new TP-PMD is an important step in reducing the overall cost of FDDI and bringing it to the desktop.

To enable FDDI transmission over copper, both analog and digital signal processing are required. Advanced Micro Devices, Micro Linear and Pulse Engineering have worked together to provide a simple implementation for the proposed TP-PMD specification. AMD's SUPERNET® 2 chipset can be used for copper transmission by removing the Optical Data Links (ODL) on existing adapter cards and concentrator boards and replacing them with a Copper Data Link (CDL). The PHY/PMD interface at the Am79865 PDT and Am79866A PDR remain intact. A high-performance CDL can be implemented using an integrated transceiver made by Micro Linear and a Filter/Magnetics module made by Pulse Engineering for under $30.

### Copper Interface

The TP-PMD standard introduces three main functional changes in the way the signal is processed: data scrambling, MLT-3 format (encoding) for the line signal and adaptive equalization at the receiver. Figure 1 depicts the signal characteristics at various points within the TP-PMD interface. AMD's Physical Layer Controller with Scrambler (PLC-S) device, the Am79C864A, provides the Scrambling/De-scrambling function, while Micro Linear's ML6671 provides MLT-3 Encoding/Decoding and Adaptive Equalization. Pulse Engineering provides the filter/magnetics interface to the cable.

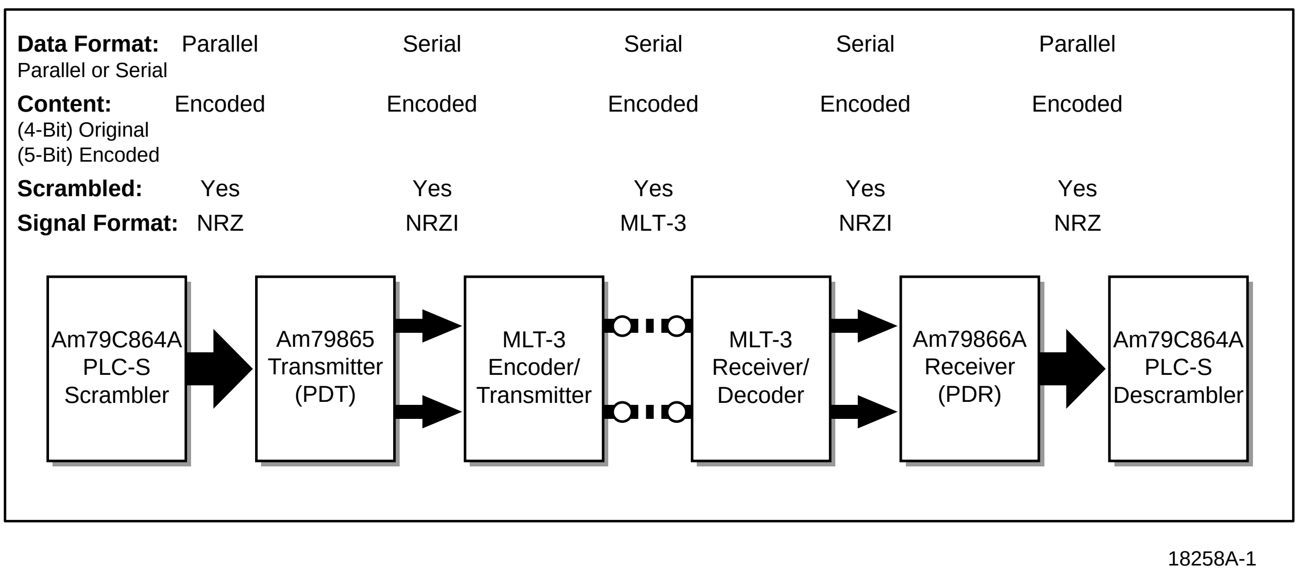


**Figure 1. TP-PMD Interface Signal Flow**

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Figure 2 shows a block diagram of the TP-PMD interface. Note that the PHY/PMD interface is the same, regardless of whether an ODL or CDL is used. Both utilize serial 4B/5B encoded NRZI data. The only difference is that the data pattern is scrambled when using a CDL. The scrambling function can be enabled and disabled in the PLC-S to accommodate both cases.

## MLT-3 Encoding

NRZI and MLT-3 line signals are shown in Figure 3. MLT-3 is an extension of NRZI: “ones” are represented by transitions and “zeroes” by the lack of transitions. The distinctive features of MLT-3 are: the signal has three possible voltage levels and the transitions are always between two adjacent levels.

MLT-3 encoding is used to control Electro Magnetic Interference (EMI). The conversion from NRZI to MLT-3 shifts much of the spectral energy below 30 MHz. Most importantly, it reduces the spectral energy between 40 MHz and 70 MHz, a region where NRZI transmission has trouble meeting governmental emission requirements. Figure 4 shows the MLT-3 spectrum. The proposed TP-PMD specification calls for a 2 V peak-to- peak transmitter output signal, which was used for this plot. Ninety percent of the spectral energy lies below 40 MHz. However, to prevent Inter-Symbol-Interference (ISI) and for proper operation of the adaptive equalization, the data channel requires at least 90 MHz of bandwidth.

## Scrambling/Descrambling

Scrambling is required to avoid energy peaks in the spectrum of the line signal. FDDI allows for some repetitive data patterns which concentrate spectral energy. Scrambling tends to randomize these patterns. Thus, scrambling tends to average out the signal spectrum and reduce EMI. ANSI has selected Stream-Cipher scrambling, mainly because its output spectral characteristics are essentially independent of the input pattern, which makes it less likely to lock-up, as compared to other scrambling techniques. The Stream-Cipher Scrambling/ Descrambling function has been included in the Am79C864A PLC-S device and may be enabled/disabled either through software or through hardware. Note, the PLC-S supports both copper and fiber designs as the scrambler is selectable. A theoretical description of Stream-Cipher scrambling may be found in Appendix A.

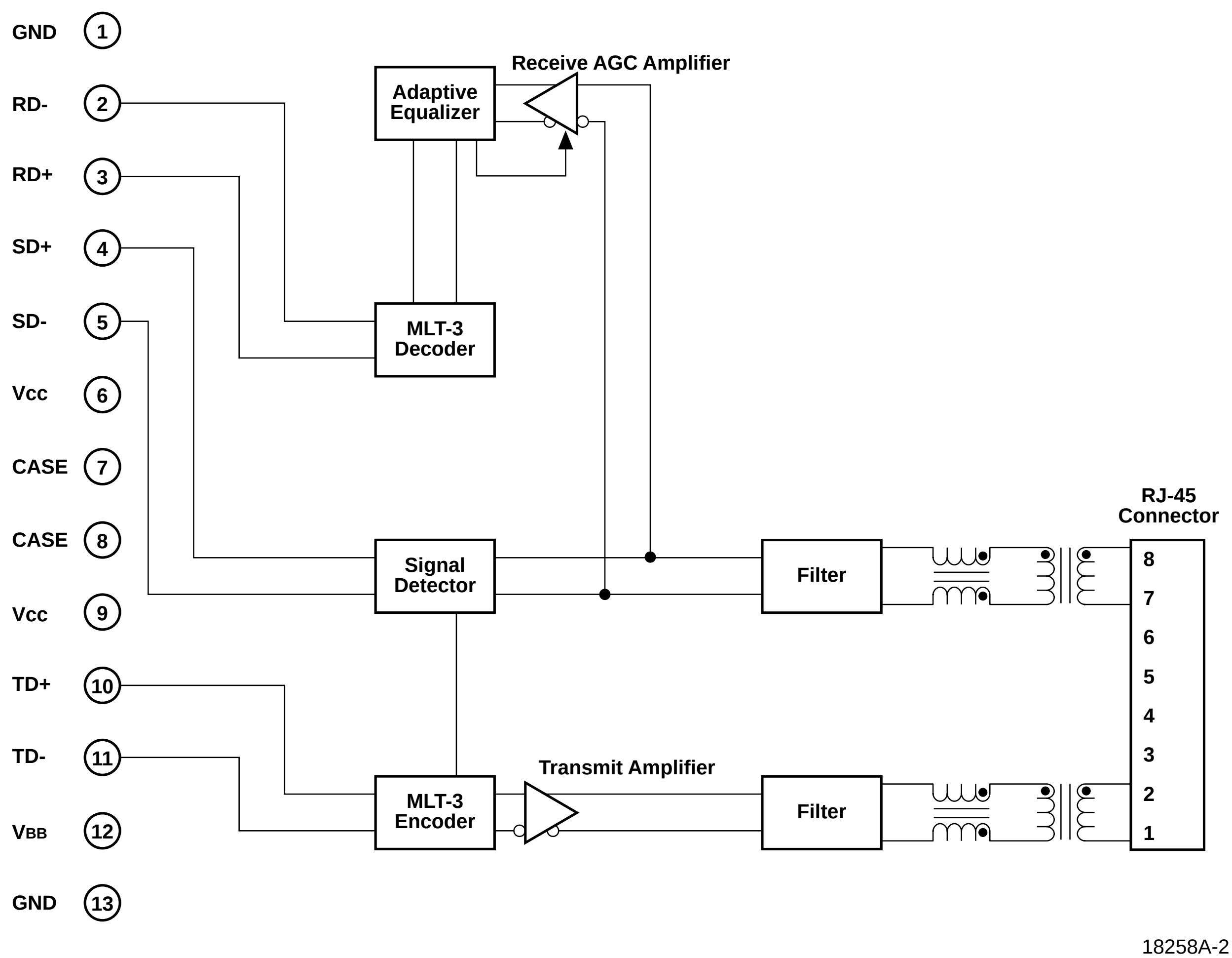



**Figure 2. Copper Data Link Block Diagram**

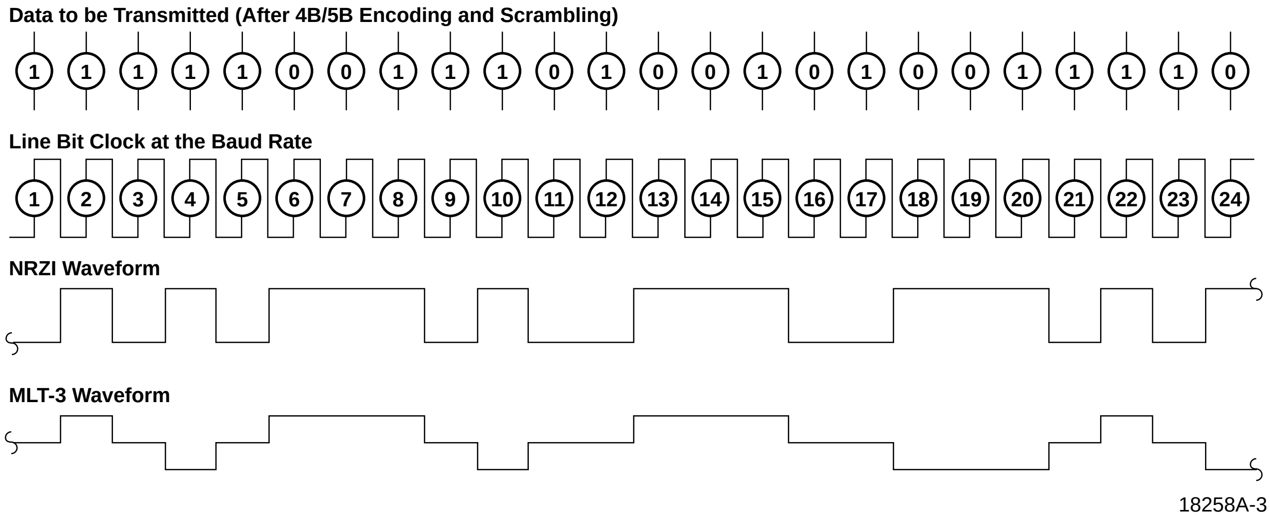



**Figure 3. Waveforms of NRZI and MLT-3 Line Signals**

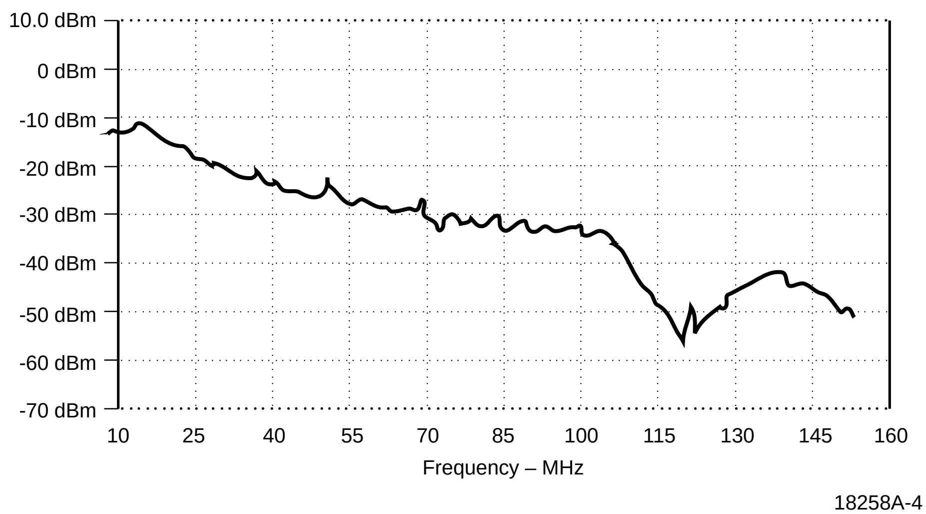


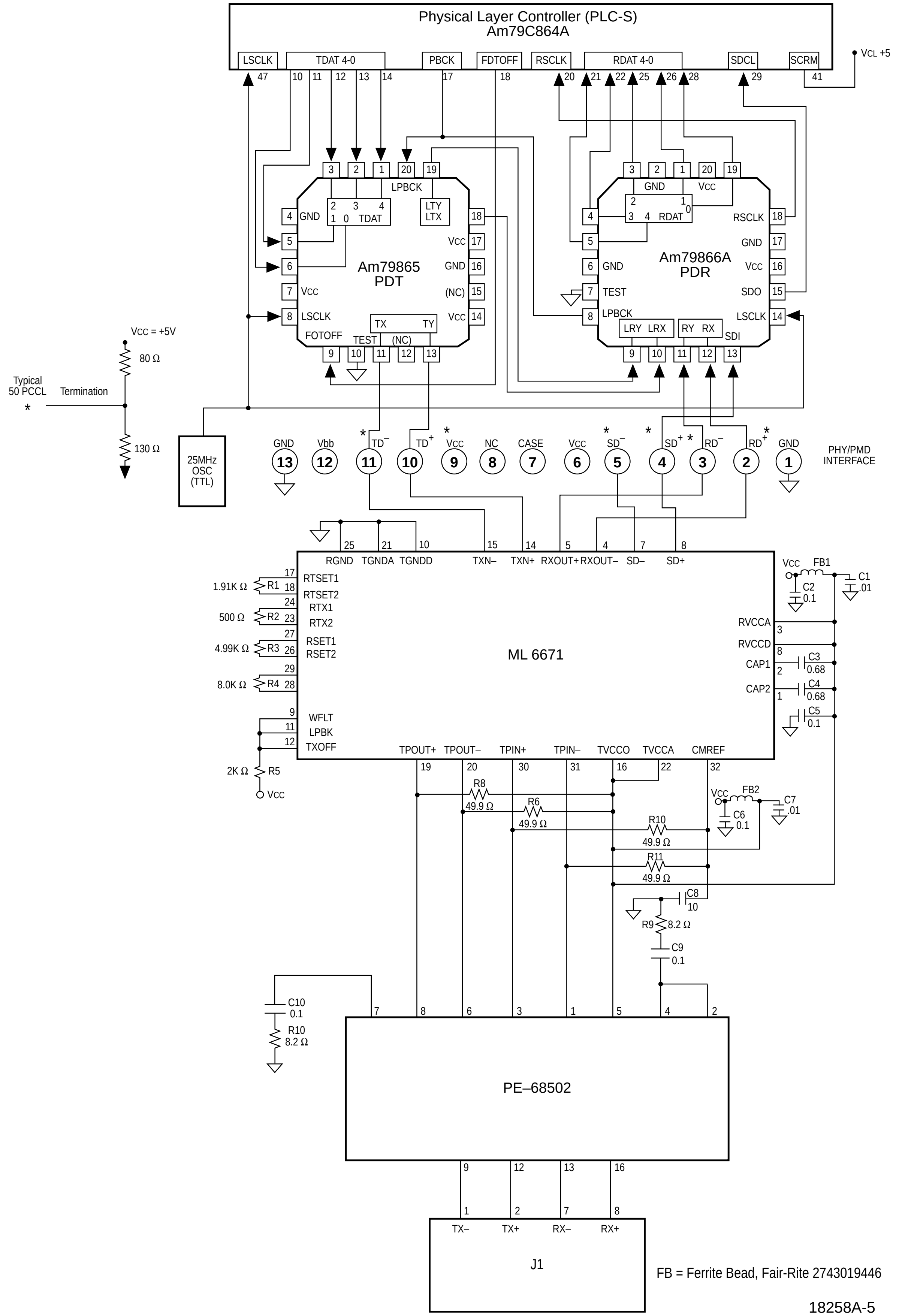

**Figure 4. Typical MLT-3 Spectrum at the Transmitter Output**

## Adaptive Equalization

Adaptive equalization is necessary to compensate for the cable attenuation and phase distortion that is encountered at various lengths of STP and UTP cable. STP cable has a characteristic impedance of 150 Ω. 100 meters of this cable will attenuate a transmitted signal by 12 dB (a factor of 4) at 62.5 MHz. 100 meters of UTP-5 cable, such as AT&T 1061 ($Z_O$ = 100 Ω), attenuates the signal by 18 dB at 62.5 MHz. Should the channel be equalized for the maximum length of either cable, it would be over-equalized for the shorter and intermediate lengths. Over-equalization results in excessive signal jitter. With adaptive equalization, the receiver frequency response is optimized for any given segment of cable. In order to achieve this, the equalizer is constantly adjusted by a feedback loop.

## TP-PMD Circuit

The copper solution described in this application note has been based on three functional blocks: AMD's SUPERNET® 2 PHY (Am79C864A PLC-S, Am79865 PDT and Am79866A PDR), Micro Linear's MLT-3 Transceiver (ML6671) and Pulse Engineering's Filter/Magnetic Module (PE68502). An application circuit of the TP-PMD is shown in Figure 5. This is a UTP-5 implementation utilizing an RJ-45 connector at the media interface. A 13-pin connection is shown at the PHY-PMD interface which is pin compatible with the footprint of the Sumitomo ODL. A 9- or 22-pin footprint could also be used for compatibility with other common ODL configurations from AT&T, Siemens and HP.




FB = Ferrite Bead, Fair-Rite 2743019446

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**Figure 5. Application Circuit for the TP-PMD**

## Transmit Circuit

The Am79865 PDT sends scrambled NRZI data to the CDL at PECL signal levels. The ML6671 converts the NRZI data to three level, MLT-3 code. In MLT-3 coding, ones are represented by transitions and zeros are represented by a lack of transitions. The transitions are always between two adjacent levels.

The transmit level is set to 2 V peak-to-peak by placing a 2 KΩ resistor between pins 17 and 18 of the ML6671. The rise time between adjacent levels (10% to 90%) out of the ML6671 is less than 1.0 ns. A low pass filter on the PE68502 increases the rise time to 3.0 ns, prior to launching the signal onto the cable. A fast rise time maintains a clean eye pattern, but it also creates unnecessary overshoot and EMI that can develop when the signal encounters punch down blocks in the wiring closet and cable imbalances. The 3.0 ns rise time has been found empirically to be the optimum value for the application. The Filter/Magnetics module also provides AC Coupling, Ground Isolation and reduces radiated emissions by providing Common Mode Filtering. In the transmit channel, it is recommended that the transformer center tap be AC coupled to ground for added Common Mode Filtering. Figure 6 shows the MLT-3 eye pattern at the transmitter output into a 100 Ω resistive load. The output jitter of the transmitter is typically less than 2.5 ns.

## Receive Circuit

The receive section consists of a differential Equalization Amplifier, Signal Detect Circuitry and an MLT-3 to NRZI Decoder. Again, the signal is AC coupled from the media through a transformer in the PE68502 module. Two 50 Ω resistors from pins 1 and 3 of the PE68502 to CMREF (pin 32 of the ML6671) are part of the cable termination and also set a DC bias for the receive amplifier input. Pin 4 of the module should also be connected to CMREF. As with the transmit channel, AC coupling the center tap (pin 4) of the Filter/Magnetics module to ground improves common mode rejection of the channel and reduces noise susceptibility.

It was found in early implementations of MLT-3 over UTP-5 that fixed equalization cannot be optimized for all combinations of distances and cable performance. Adaptive equalization changes the receiver gain and frequency response as a function of the received signal. The receiver amplifier has a dynamic range of 20:1, from 100 $mV_{PP}$ to 2.0 $V_{PP}$. The equalizer boosts the high frequency content of the signal in order to compensate for cable filtering and/or distortion. Equalization is adaptive and the receiver can compensate for lengths of UTP-5 between 0 and 100 meters.

Figures 7 and 8 show the typical eye patterns of the NRZI signal recovered by the receiver (at RD+/–) after 10 and 100 meters of UTP-5, respectively. In both cases, the jitter is held below 3.0 ns. Figure 9 shows the jitter at the PHY/PMD interface plotted as a function of cable length.

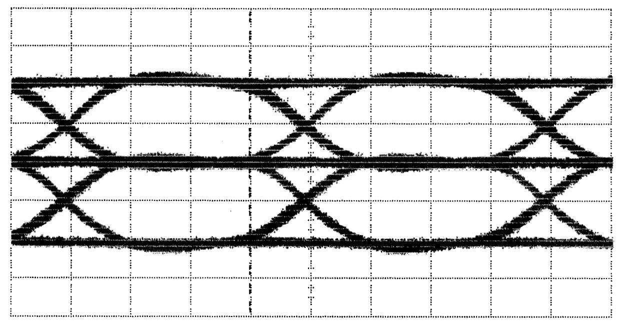


**Figure 6. MLT-3 Eye Pattern of the Transmitter**

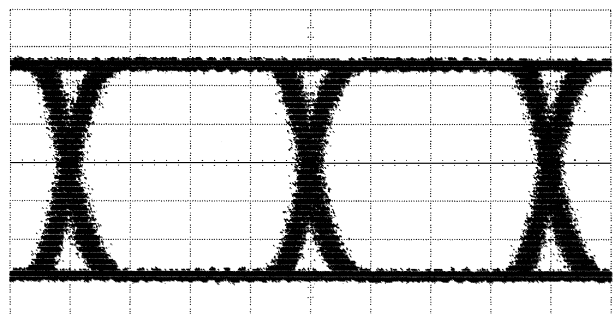


**Figure 7. NRZI Eye Pattern Out of the Receiver, 10 Meters UTP-5 Cable**

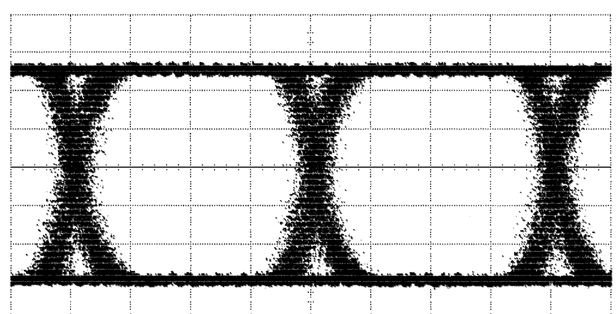


**Figure 8. NRZI Eye Pattern Out of the Receiver, 100 Meters UTP-5 Cable**

## Signal Detect

Voltage amplitude of the received signal is used as an indication of a working PHY and PMD link. If the signal at the receiver input is greater than 100 mV the received signal is interpreted as data, and the SD+ logic signal out of the ML6671 is asserted high (>3.8 Vdc). The PLC-S acknowledges that there is an active signal and monitors the line for data. If the signal amplitude is less than 100 $mV_{PP}$, SD+ is asserted low (<3.5 Vdc) and the PLC-S is free for transmission.

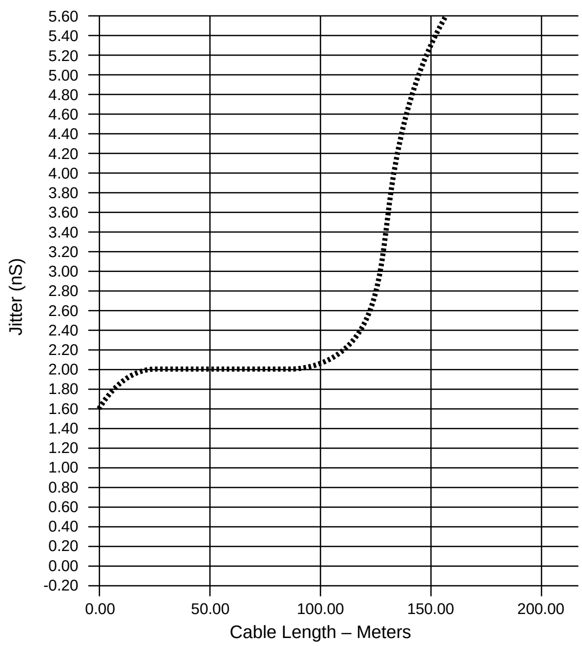


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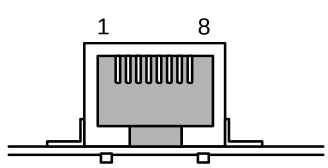
**Figure 9. Jitter vs. UTP-5 Cable Length**

## Layout Considerations

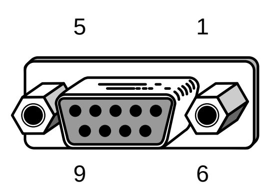
In laying out the TP-PMD PC Board, it is important to keep the TX+/TX– and RD+/RD– signal lines as short (direct) as possible. The Transmit and Receive power planes should be isolated from one another with LC filter networks. Surface mount ferrite beads are suitable for the inductive elements of these filters. A ground plane should also be used. However, the ground plane should not extend to within 0.150″ of the output of the Filter/Magnetics Module or the RJ-45 connector. This separation should prevent common mode noise, that may develop on the ground, from coupling onto the media. Grounds on connector shields should be attached to chassis ground. The shields should not be connected to Analog or Digital ground. Since FCC compliance depends on both the circuit characteristics and the system layout, test results will vary from implementation to implementation.

Three different MIC connectors are specified in the X3T9.5 TP-PMD document. The RJ-45 is used for UTP-5 while a DB-9 Plug is used for the STP M-Port and a DB-9 socket is used for the STP A, B, or S-Port. Pin assignments for the three connectors are shown in Figure 10.



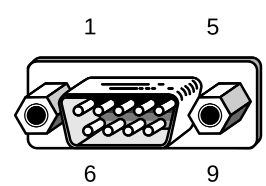

RJ-45 Receptacle For S-Port

| Pin # | Signal |
|---|---|
| 1 | Transmit (TX+) |
| 2 | Transmit (TX–) |
| 3 | Not Used |
| 4 | Not Used |
| 5 | Not Used |
| 6 | Not Used |
| 7 | Receive (RX+) |
| 8 | Receive (RX–) |




MIC Receptacle For A, B, or S-Port

| Pin # | Signal |
|---|---|
| 1 | Receive (RX+) |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Not Used |
| 5 | Transmit (TX+) |
| 6 | Receive (RX–) |
| 7 | Not Used |
| 8 | Not Used |
| 9 | Transmit (TX–) |
| Shell | Chassis GND |




MIC Plug For M-Port

| Pin # | Signal |
|---|---|
| 1 | Transmit (TX+) |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Not Used |
| 5 | Receive (RX+) |
| 6 | Transmit (TX–) |
| 7 | Not Used |
| 8 | Not Used |
| 9 | Receive (RX–) |
| Shell | Chassis GND |

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**Figure 10. MIC Connectors and Pin Out**

# Description of Stream Cipher Scrambling

## About Stream-Cipher Scrambling

Stream-cipher scrambling was selected by the XT3.9 standards committee mostly because its output spectral characteristic is essentially independent of the input pattern. The selection was between a stream-cipher algorithm and a self-synchronizing algorithm. The former seems to be more reliable in avoiding lock-up conditions but requires more components, especially on the receiver side, where the scrambled serial data need to be reframed.

The stream-cipher scrambler and stream-cipher descrambler described below are implemented in the Physical Layer Controller chip with Scrambler (PLC-S). The design is based on a stream-cipher version presented at the standards committee.

## Background

Scramblers modify data by mixing the output of a random generator with the original data. The mixing is performed by logic exclusive-OR operations. At the receiver end, the descrambler adds the same random pattern (using the XOR function) to the scrambled data. Because the scrambler and descrambler patterns are the same, they cancel each other out and the descrambled data equal the original data.

Given the following patterns:

Original data = A
Random (scrambler and descrambler) = B
Descrambled output = C

$$C = A \oplus B \oplus B$$

Because of the XOR operation:

$$B \oplus B = 0,$$
$$C = A \oplus B \oplus B = A \oplus 0 = A$$

The random generators used on both sides are shift registers with XOR feedback. The function can be expressed as the polynomial $x^J + x^K$. The output of the random generator is bit J XORed with bit K. This is also fed back to the input. The scrambler selected by the XT3.9 committee has J=11 and K=9. The polynomial is $x^{11} + x^9$.

Proper operation requires that the scrambler and descrambler generate the same random pattern and be synchronized. At any given instant, they must be in the same state and have the same output. In the case of the stream-cipher, the descrambler's random generator operates independently of the scrambler's random generator. Therefore, the descrambler must be synchronized to the scrambler before it can reliably decode data.

In the FDDI protocol, user data are preceded by line state patterns such as HLS, MLS, ILS and QLS. These patterns are repetitive and during their transmission, the incoming scrambled data are predictable. The following formula allows us to use the line states to synchronize the descrambler.

H(n) = SCRMData(n) ⊕ SCRMData(n-11) ⊕ SCRMData(n-9) = Data(n)

Where:
H(n) is a test bit
SCRMData(n) is scrambled data
SCRMData(n-11), SCRMData(n-9) are the eleventh and ninth bits of scrambled data.
Data(n) is unscrambled data

This relationship is true when Data(11) equals Data(9). Three rules, based on the above formula, synchronize the descrambler:

1. If SCRMData(n) = SCRMData(n-11) and SCRMData(n) = SCRMData(n-9) then set descrambler input to SCRMData(n).
2. If SCRMData(n) = SCRMData(n-11) = 1 and SCRMData(n-1) = SCRMData(n-2) = SCRMData(n-2) = SCRMData(n-4) = SCRMData(n-6) = SCRMData(n-7) = SCRMData(n-8) = SCRMData(n-9) = 0, then set the descrambler to SCRMData(n).
3. Otherwise DESCRM(n) = DESCRM(n-j) ⊕ DESCRM(n-k).

Table A-1 below shows the line states and the corresponding detected test signals.

**Table A-1. FDDI Line States and Detected Test Signals**

| Line State | Data Bits | Test Bits H(n) |
|---|---|---|
| HLS | 0010000100 | 0111001110 |
| QLS | 0000000000 | 0000000000 |
| MLS | 0000000100 | 0000001110 |
| ILS | 1111111111 | 1111111111 |

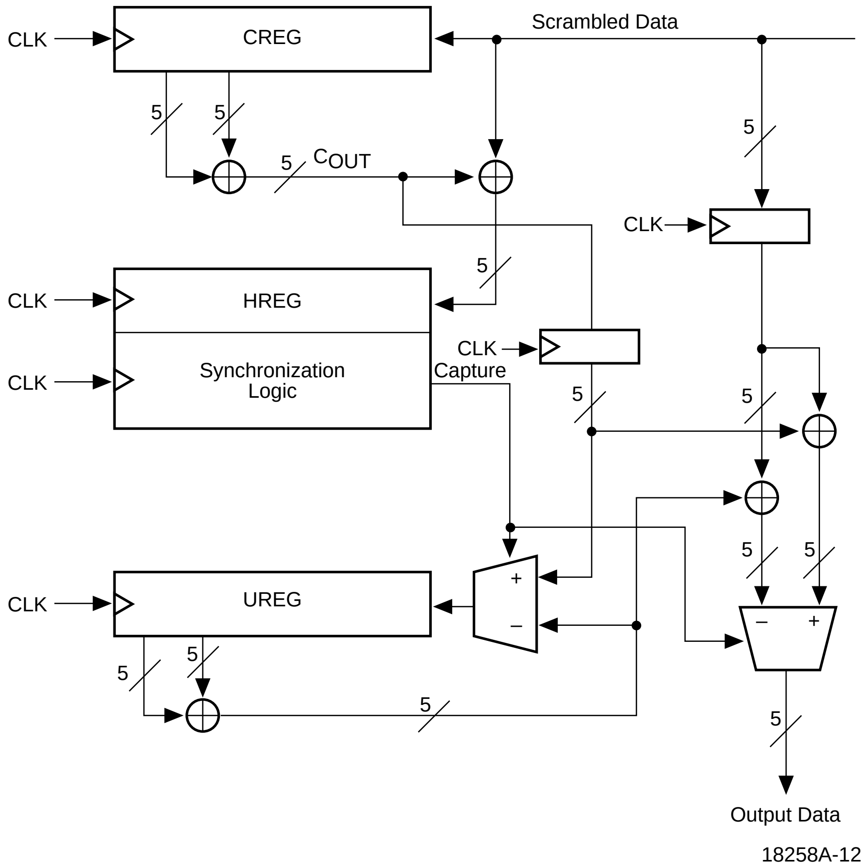


**Figure A-1. PLC-S Descrambler Logic Diagram**

## PLC-S Implementation

The PLC-S Scrambler is a 5-bit parallel version of the serial data scrambler. The main functional pieces are:

1. sreg: scrambler shift register
2. creg: cipher shift register—records 10 bits of the scrambled data.
3. hreg: implements the formula c(n) ⊕ c(n-11) ⊕ c(n-9)
4. ureg: the descrambler shift register

The descrambler is shown in Figure A-1. It has two modes of operation: sample and normal. In the sample mode, ureg is not synchronized with sreg. The hreg portion monitors creg for the line states. When it detects one, it generates a signal called “Capture”. Capture forces ureg into a predetermined state. In normal operation ureg is synchronized to sreg. Capture cannot be generated in this mode.

## Synchronization

The objective of synchronization is to set the descrambler shift register to the same state as the scrambler shift register. Once the scrambler is synchronized, it will maintain synchronization because both devices implement the same function.

Hreg monitors 20 bits of data for a line state. The reason such a large number of bits are monitored is that the byte boundary is unpredictable. There are ten possible inputs for each line state. The repetitive nature of the line states reduces the possible inputs to one for QLS and ILS, and five for HLS.

When hreg detects a line state, the output data are set to the corresponding value. The input bits to ureg are set to the data value XORed with the scrambled data input.

# Recommended CDL Test Circuit

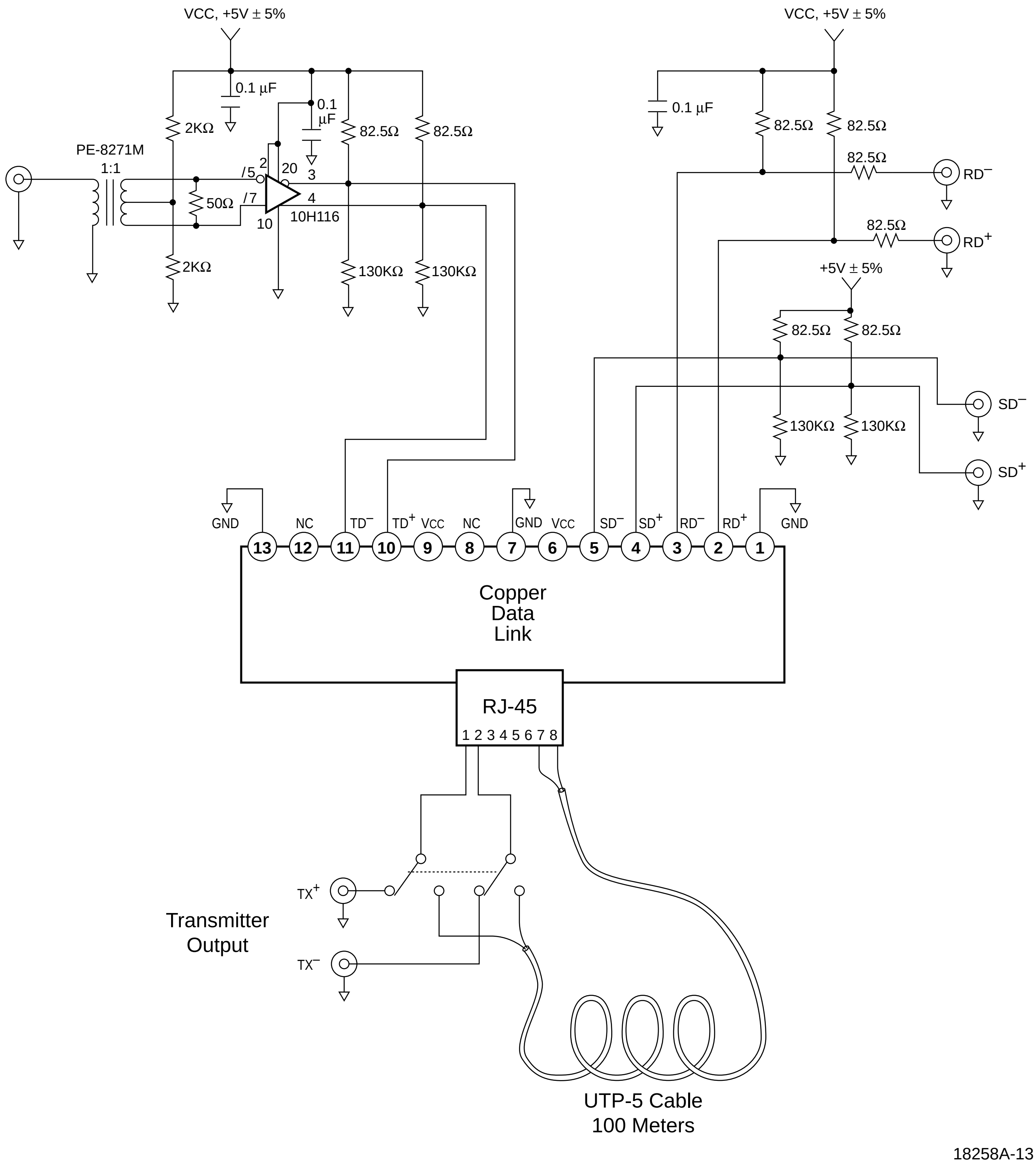


**Figure B-1.**

## FURTHER APPLICATION DETAILS

For further application details, refer to the following documents:

**AMD**
SUPERNET® 2 Family for FDDI, 1994 Data Book, PID #15502C
901 Thompson Place
Sunnyvale, CA 94088-3453
800-222-9323
408-749-5703

**Micro Linear**
MLT-3 Transceiver Application Note
2092 Concourse Drive
San Jose, CA 95131
408-433-5200

**Pulse Engineering**
TP-FDDI Filter/Magnetic Modules, Data Sheet
12220 World Trade Drive
San Diego, CA 92128
619-674-8100