FS781/82/84

LOW EMI SPECTRUM SPREAD CLOCK

Features

- Spread Spectrum Clock Generator (SSCG) with 1x, 2x and 4x Outputs
- 6 to 82 MHz operating frequency range.
- Modulates external clocks including crystals, crystal oscillators and ceramic resonators.
- Programmable modulation with simple R-C external loop filter (LF)
- Center Spread Modulation.
- 3 - 5 Volt power supply.
- TTL/CMOS compatible outputs.
- Low short term jitter.
- Low Power Dissipation;
  - 3.3 VDC = 37 mw - typical
  - 5.0 VDC = 115 mw - typical
- Available in 8 pin SOIC and TSSOP packages.

Applications

- Desktop/Notebook Computers
- Printers, Copiers and MFP
- Scanners and Fax
- LCD Displays and Monitors
- CD-ROM, VCD and DVD
- Automotive and Embedded Systems
- Networking, LAN/WAN
- Digital Cameras and Camcorders
- Modems

Benefits

- Programmable EMI Reduction
- Fast Time to Market
- Lower cost of compliance
- No degradation in Rise/Fall times
- Lower component and PCB layer count

Product Description

The Cypress FS781/2/4 are Spread Spectrum Clock Generator ICs (SSCG) designed for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital systems.

The FS781/2/4 SSCG clocks use an IMI proprietary technology to modulate the input clock frequency, FSOUT by modulating the frequency of the digital clock. By modulating the reference clock the measured EMI at the fundamental and harmonic frequencies of FSOUT is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The Cypress FS781/2/4 clocks are very simple and versatile devices to use. By programming the two range select lines, S0 and S1, any frequency from 6 to 82 MHz operating range can be selected. The FS781/2/4 are designed to operate over a very wide range of input frequencies and provides 1x, 2x and 4x modulated clock outputs.
The FS78x devices have a simple frequency selection table that allows operation from 6 MHz to 82 MHz in four separate ranges. The bandwidth of the frequency spread at FSOUT is determined by the values of the loop filter components. The modulation rate is determined internally by the input frequency and the selected input frequency range.

The Bandwidth of these products can be programmed from as little as 0.6% up to as much as 4.0% by selecting the proper loop filter value. Refer to the Loop Filter Selection chart on page 6 for recommended values. Due to a wide range of application requirements, an external loop filter (LF) is used on the FS78x products. The user can select the exact amount of frequency modulation suitable for the application. Using a fix internal loop filter would severely limit the use of a wide range of modulation bandwidths (Spread %) to a few discrete values.

Refer to FS791/2/4 products for applications requiring 80 to 140 MHz frequency range.

Block Diagram

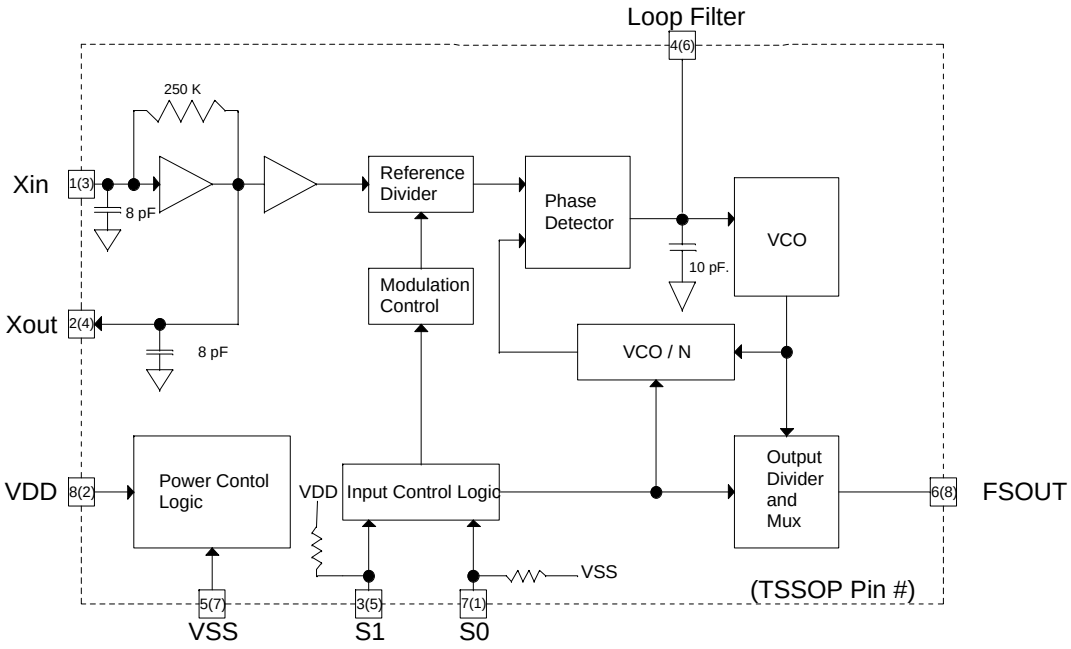


Figure 1. Block Diagram

Ordering Information

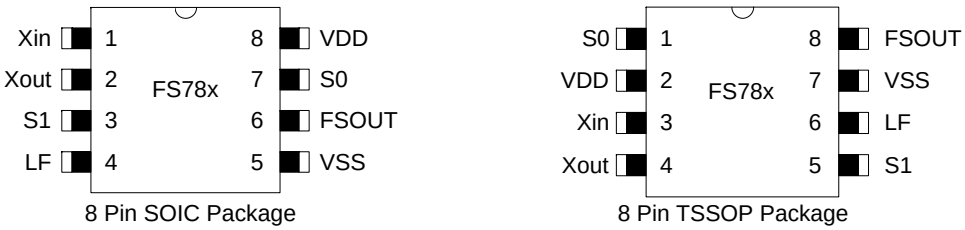
Product Number	FM-OUT Scaling	Package Type	Production Flow
FS781BZB	1xFin	8 Pin 150 mil SOIC	Commercial, 0 to 70°C
FS782BZB	2xFin	8 Pin 150 mil SOIC	Commercial, 0 to 70°C
FS784BZB	4xFin	8 Pin 150 mil SOIC	Commercial, 0 to 70°C
FS781BT	1xFin	8 Pin 169 mil TSSOP	Commercial, 0 to 70°C
FS781BT	2xFin	8 Pin 169 mil TSSOP	Commercial, 0 to 70°C
FS781BT	4xFin	8 Pin 169 mil TSSOP	Commercial, 0 to 70°C

Marking Example: Date Code
FS781BZB
Lot Number

FS78xBZB

- Flow
  (“B” Flow not indicated on TSSOP package)
- Packages
  Z = SOIC (150 Mil)
  T = TSSOP (169 Mil)
- Revisions
- Device Number

Pin Configuration



8 Pin SOIC Package

8 Pin TSSOP Package

Pin Description

Pin No.	Pin Name	I/O	TYPE	Description
1/2	Xin / Xout	I/O	Analog	Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Xin may be connected to TTL/CMOS external clock source. If Xin connected to external clock other than crystal, leave Xout (pin 2) unconnected.
7/3	S0 / S1	I	CMOS/TTL	Digital control inputs to select input frequency range and output frequency scaling. Refer to Tables 7 & 8 for selection. S0 has internal pulldown. S1 has internal pullup.
4	LF	I	Analog	Loop Filter. Single ended tri-state output of the phase detector. A two-pole passive loop filter is connected to Loop Filter (LF).
6	FSOUT	O	CMOS/TTL	Modulated Clock Frequency Output. The center frequency is the same as the input reference frequency for FS781. Input frequency is multiplied by 2x and 4x for FS782 and FS784 respectively.
8	VDD	P	Power	Positive Power Supply.
5	VSS	P	Power	Power Supply Ground

Table 1

Output Frequency Selection

Product Number	FSOUT Frequency Scaling	Description
FS781	1x	1x Modulated Frequency of Input Clock
FS782	2x	2x Modulated Frequency of Input Clock
FS784	4x	4x Modulated Frequency of Input Clock

Table 2. FSOUT SSCG (Modulated Output Clock) Product Selection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range, VSS < (Vin or Vout) < VDD. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

Absolute Maximum Ratings

Item	Symbol	Min	Max	Units
Operating Voltage	VDD	3.0	6.0	VDC
Input, relative to VSS	VIRvss	-0.3	VDD +0.3	VDC
Output, relative to VSS	VORvss	-0.3	VDD +0.3	VDC
AVDD relative to DVDD	ΔVpp	-100	+100	mV
AVSS relative to DVSS	ΔVss	-100	+100	mV
Temperature, Operating	TOP	0	+ 70	^{0} C
Temperature, Storage	TST	- 65	+ 150	^{0} C

Table 3

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	VIL	-	-	0.3 * VDD	VDC
Input High Voltage	VIH	0.7 * VDD	-	-	VDC
Input Low Current	IIL	-	-	100	µA
Input High Current	IIH	-	-	100	µA
Output Low Voltage IOL= 10mA, VDD = 5V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 10mA, VDD = 5V	VOH	VDD-1.0	-	-	VDC
Output Low Voltage IOL= 6mA, VDD = 3.3V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 5mA,VDD = 3.3V	VOH	2.4	-	-	VDC
Resistor, Pull Down (Pin-7)	Rpd	60K	125K	200K	Ω
Resistor, Pull Up (Pin-3)	Rpu	60K	125K	200K	Ω
Input Capacitance (Pin-1)	C_{xin}	-	8	-	pF
Output Capacitance (Pin-2)	C_{xout}	-	10	-	pF
5 Volt Dynamic Supply Current (C_L = No Load)	ICC	-	38	-	mA
3.3 Volt Dynamic Supply Current (C_L = No Load)	ICC	-	20	-	mA
Short Circuit Current (FSOUT)	ISC	-	25	-	mA
BW% Variations, 3.30V**	BW	-20	0	+20	%
BW% Variations, 5.00V**	BW	-30	0	+30	%
Test measurements performed at VDD = 3.3V and 5.0V ±10%, Xin = 48 MHz, Ta = 0°C to 70°C **BW% Variations in % from the BW% values give in Loop Filter Value Tables.					

Table 4

Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise Time Measured at 10% - 90% @ 5 VDC	tTLH	2.0	2.2	2.5	ns
Output Fall Time Measured at 10% - 90% @ 5 VDC	tTHL	1.7	2.0	2.2	ns
Output Rise Time Measured at 0.8V - 2.0V @ 5 VDC	tTLH	0.50	0.65	0.75	ns
Output Fall Time Measured at 0.8V - 2.0 V @ 5 VDC	tTHL	0.50	0.65	0.75	ns
Output Rise Time Measured at 10% - 90% @ 3.3 VDC	tTLH	2.6	2.65	2.9	ns
Output Fall Time Measured at 10% - 90% @ 3.3 VDC	tTHL	2.0	2.1	2.2	ns
Output Rise Time Measured at 0.8V - 2.0V @ 3.3 VDC	tTLH	0.8	0.95	1.1	ns
Output Fall Time Measured at 0.8V - 2.0 V @ 3.3 VDC	tTHL	0.78	0.85	0.9	ns
Output Duty Cycle	TsymF1	45	50	55	%
FSOUT, Cycle to Cycle Jitter, 48 MHz @ 3.30 VDC (Pin 6)	CCJ	-	320	370	pS
FSOUT, Cycle to Cycle Jitter, 48 MHz @ 5.0 VDC (Pin 6)	CCJ	-	310	360	pS
FSOUT, Cycle to Cycle Jitter, 72 MHz @ 3.30 VDC (Pin 6)	CCJ	-	270	325	pS
FSOUT, Cycle to Cycle Jitter, 72 MHz @ 5.0 VDC (Pin 6)	CCJ	-	390	440	pS
Measurements performed at VDD = 3.3 and 5.0V ± 10%, Ta = 0°C to 70°C, CL = 15pF, Xin = 48 MHz.					

Table 5

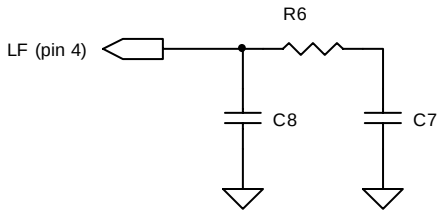
Range Selection Table

S1 (pin 3)	S0 (pin 7)	Fin (MHz) (pin 2/3)	Modulation Rate	FS781 FSOUT (pin 6)	FS782 FSOUT (pin 6)	FS784 FSOUT (pin 6)
0	0	6 - 16	Fin/120	6 – 16 MHz	12 – 32 MHz	32 – 64 MHz
0	1	16 - 32	Fin/240	16 – 32 MHz	32 – 64 MHz	64 – 82 MHz
1	0	32 - 66	Fin/480	32 – 66 MHz	64 – 82 MHz	N/A
1	1	66 - 82	Fin/720	66– 82 MHz	N/A	N/A

Table 6

Loop Filter Selection Chart

The following table provides a list of recommended loop filter values for the FS781/2/4. The FS78x is divided into 4 ranges and operates at both 3.3 and 5.0 VDC. The loop filter at the right is representative of the loop filter components in the table below.



FS781/2/4 Recommended Loop Filter Values.

			C7 (pF.) @ +3.3 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**S 1**	**S 0**	**BW = 1.0% (note 3)**	**BW = 1.5% (note 3)**	**BW = 2.0% (note 3)**	**BW = 2.5% (note 3)**	**BW = 3.0% (note 3)**	**BW = 3.5% (note 3)**	**BW = 4.0% (note 3)**
6	0	0	10,000/1000	1550	910	780	700	640	560
8	0	0	10,000/330	990	820	640	520	450	400
10	0	0	1040	680	460	360	300	240	210
12	0	0	830	420	300	220	200	190	170
14	0	0	580	230	200	160	140	100	80
16	0	1	10000	980	760	580	470	410	385
20	0	1	1000	730	470	390	320	220	190
22	0	1	960	640	410	270	230	200	180
24	0	1	920	400	250	210	180	160	150
26	0	1	660	300	220	180	150	140	120
28	0	1	470	230	180	150	130	100	70
30	0	1	470	180	140	120	100	80	60
32	0	1	330	170	120	100	82	68	47
34	1	0	10000	860	640	520	430	380	330
36	1	0	2200	820	620	470	400	330	290
38	1	0	1500	690	520	410	340	290	240
40	1	0	960	600	420	340	280	220	160
42	1	0	940	620	380	275	230	210	180
44	1	0	950	680	400	250	210	190	170
46	1	0	900	580	270	220	190	180	165
48	1	0	790	440	260	210	180	160	140
52	1	0	470	325	220	185	155	135	120
54	1	0	470	270	200	170	140	130	100
56	1	0	445	250	185	150	120	85	47
58	1	0	430	210	165	130	100	65	33
60	1	0	295	185	150	120	100	90	82
62	1	0	270	220	150	120	100	82	68
64	1	1	1180	860	560	410	340	290	230
66	1	1	1180	760	560	350	260	220	210
68	1	1	1180	750	500	320	260	230	210
70	1	1	1120	740	470	370	300	240	170
72	1	1	1160	780	470	300	250	220	190
74	1	1	1110	770	470	280	230	210	190
76	1	1	1000	720	440	240	210	190	170
78	1	1	910	670	270	210	190	170	160
80	1	1	900	620	260	210	190	170	156
82	1	1	900	540	250	210	190	170	150

Notes:

1. If the value selected from the above chart is not a standard, use the next available larger value.
2. All Bandwidth's indicated above are total peak-to-peak spread. 1% = +0.5% to –0.5%. 4% = +2.0% to –2.0%.
3. If C8 is not listed in the chart for a particular BW and Freq., it is not used in the loop filter.
4. Contact factory for LF (Loop Filter) values less than 1.0 % BW.

Table 7

FS781/2/4 Recommended Loop Filter Values.

			C7 (pF.) @ +5.0 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**S 1**	**S 0**	**BW = 1.0% (note 3)**	**BW = 1.5% (note 3)**	**BW = 2.0% (note 3)**	**BW = 2.5% (note 3)**	**BW = 3.0% (note 3)**	**BW = 3.5% (note 3)**	**BW = 4.0% (note 3)**
6	0	0	1140	1030	930	830	710	610	510
8	0	0	1170	970	740	570	460	400	280
10	0	0	1030	660	430	350	280	210	130
12	0	0	760	340	230	200	180	160	130
14	0	0	450	240	180	140	100	70	50
16	0	1	2490	970	730	590	480	430	370
20	0	1	1360	680	480	370	280	190	250
22	0	1	990	560	330	260	230	200	190
24	0	1	820	360	250	200	180	160	150
26	0	1	530	270	210	170	150	110	90
28	0	1	430	230	180	150	110	100	90
30	0	1	250	200	150	110	100	90	80
32	1	0	Note 4.	1000	740	570	470	410	370
36	1	0	Note 4.	970	670	480	380	310	230
38	1	0	Note 4.	880	560	380	310	270	220
40	1	0	Note 4.	800	460	290	240	230	220
42	1	0	1030	680	360	260	220	200	190
44	1	0	790	560	260	220	200	190	170
46	1	0	1110	420	280	210	180	170	140
48	1	0	1110	280	200	190	170	140	120
50	1	0	830	330	200	180	160	130	110
52	1	0	560	340	205	170	140	120	90
54	1	0	510	280	180	140	110	110	90
56	1	0	470	210	160	120	100	90	90
58	1	0	450	220	250	110	90	80	80
60	1	0	430	240	120	90	80	80	70
62	1	1	Note 4.	800	580	430	330	250	180
66	1	1	Note 4.	630	400	320	240	150	100
68	1	1	Note 4.	690	365	285	225	170	140
70	1	1	Note 4.	650	330	250	210	190	180
72	1	1	Note 4.	575	340	250	210	190	170
74	1	1	Note 4.	500	355	245	205	180	165
76	1	1	Note 4.	550	330	230	200	175	160
78	1	1	Note 4.	600	290	220	190	170	155
80	1	1	Note 4.	570	240	210	185	165	150
82	1	1	Note 4.	540	250	200	180	160	140

Notes:

1. If the value selected from the above chart is not a standard value, use the next available larger value.
2. All bandwidths indicated are total peak-to-peak spread. 1% = +0.5% to –0.5%. 4% = +2.0% to –2.0%.
3. If C8 is not listed in the chart for a particular BW and Freq., it is not used in the loop filter.
4. Contact Factory for these Loop Filter values and bandwidths less than 1.0%.

Table 8

SSCG Modulation Profile

The digital control inputs S0 and S1 determine the modulation frequency of FS781/2/4 products. The input frequency is divided by a fixed number, depending on the operating range that is selected. The modulation frequency of the FS78x can be determined from the Table 8. To compute the modulation frequency enter to Table 8 with selected S0 and S1 values to obtain Modulation Divider Number, and divide the input frequency by this fix number.

S1	S0	Input Frequency Range (MHz)	Modulation Divider Number
0	0	6 to 16	120
0	1	16 to 32	240
1	0	32 to 66	480
1	1	66 to 82	720

Table 9

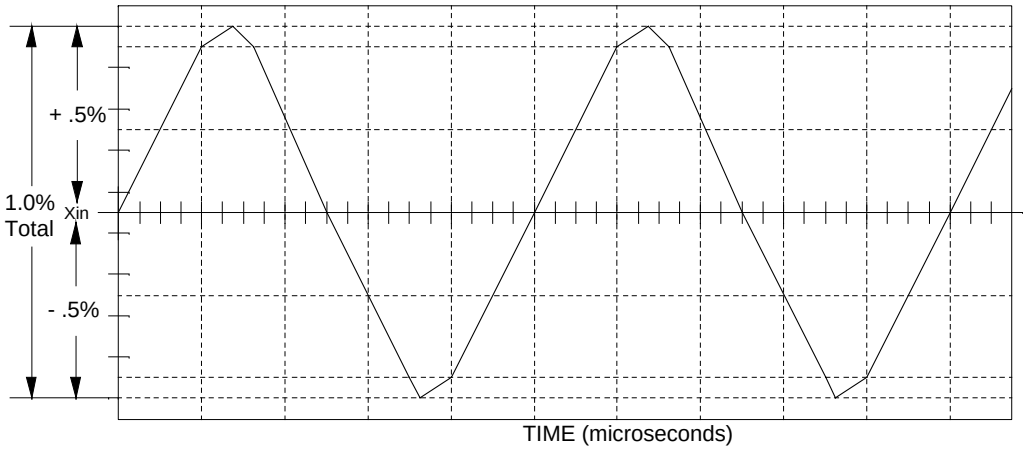


Figure 5. Frequency Profile in Time Domain

With the correct loop filter connected to pin 4, the following profile will provide the best EMI reduction. This profile can be seen on a Time Domain Analyzer.

Theory of Operation

The FS781/2/4 devices are Phase Lock Loop (PLL) type clock generators using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the FS781/2/4 products become a Low EMI clock generator. The theory and detailed operation of these products will be discussed in the following sections.

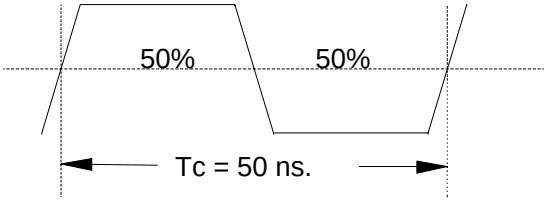
EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 %. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital

clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the Amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. These FS781/2 and 4 use the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q of the clock.

SSCG

The FS781/2/4 products use a unique method of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak to peak and cycle to cycle. The FS78x products take a narrow band digital reference clock in the range 6 - 82 MHz and produce a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 20 MHz clock with a 50 % duty cycle. From a 20 MHz clock we know the following;



20 MHz Unmodulated Clock

Figure 6.

Clock Frequency = Fc = 20 MHz.
Clock Period = Tc = 1/20 MHz=50 ns

Consider that this 20 MHz clock is applied to the Xin input of the FS78x, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the FS78x. Also consider that the products are operating from a 5-volt DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to table 6 on page 6.
From the above parameters, the output clock at FSOUT will be sweeping symmetrically around a center frequency of 20 MHz.
The minimum and maximum extremes of this clock will be +200 kHz and -200 kHz. So, we have a clock that is sweeping from 19.8 MHz to 20.2 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in figure 7. Keep in mind that this is a drawing of a perfect clock with no noise.

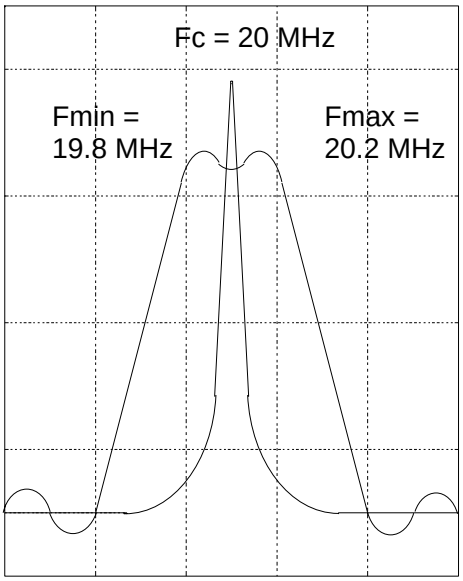


Figure 7.

We see that the original 20 MHz reference clock is at the center Frequency, Cf, and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called **Center-Spread**. Figure 8 shows a 20 MHz clock, as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock,. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The Tc measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this figure would show the clock going from minimum extreme back to the high extreme.

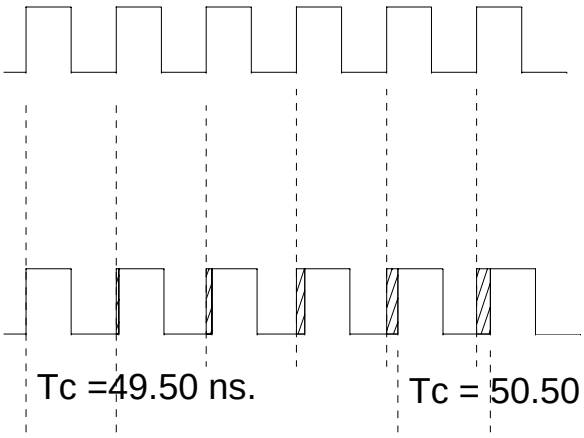


Figure 8. Period Comparison Chart

Looking at figure 7, you will note that the peak amplitude of the 20 MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This figure refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the fundamental frequency is multiplied by the harmonic number. In other words, if the bandwidth of a 20 MHz clock is 200 kHz, the bandwidth of the 3rd harmonic will be 3 times 200, or 600 kHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of a 20 MHz clock is 220 MHz. With a total spread of 200 kHz at 20 MHz, the spread at the 11th harmonic would be 2.20 MHz which greatly reduces the peak energy content. It is typical to see as much as 12 to 18 dB. reduction at the higher harmonics, due to a modulated clock.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2 - 3 dB. reduction at the fundamental and as much as 8 - 10 dB. reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

Application Notes and Schematic

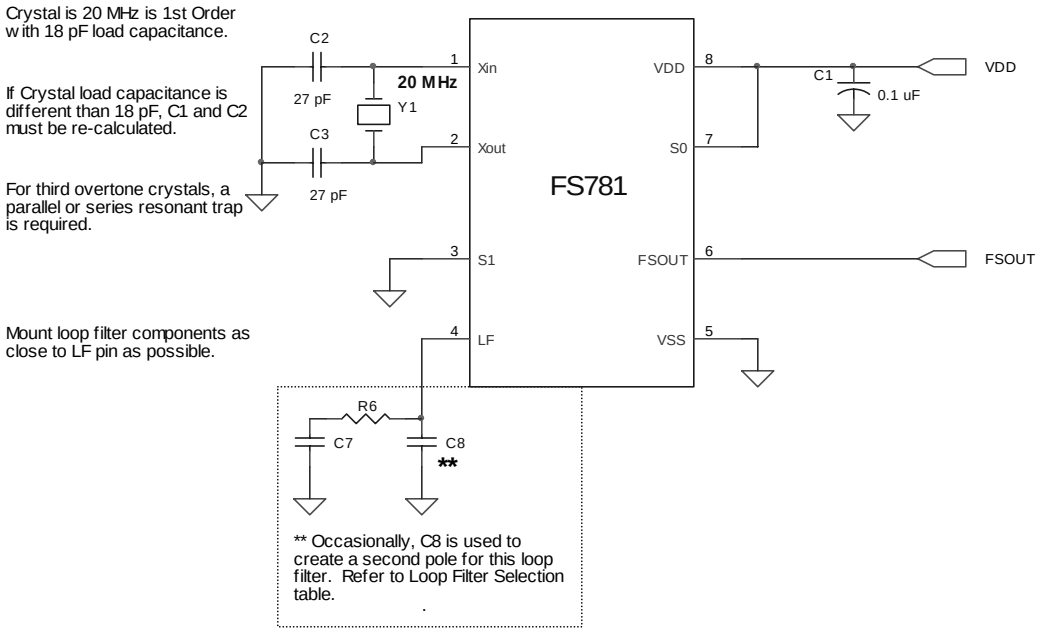
The schematic at the right is configured for the following parameters;

Package selected = FS781

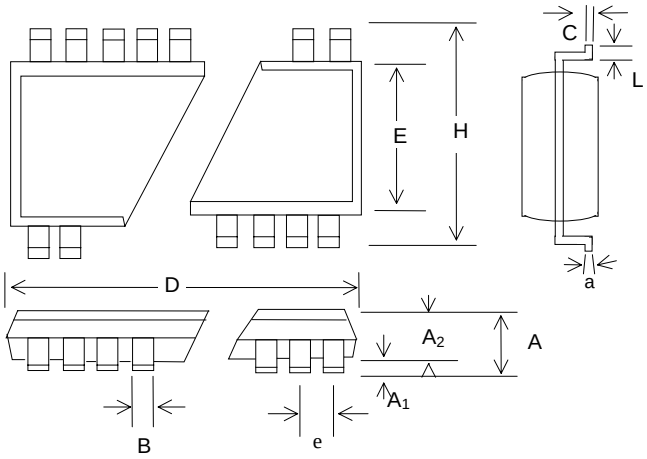
Xin = 20 MHz Crystal

FSOUT = 20 MHz (S0=1 and S1=0)

Bandwidth of the FSOUT clock is determined by the values of the loop filter connected to pin 4.



Package Drawing and Dimensions



8 Pin SOIC Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	-	0.069	1.35	-	1.75
A_1	0.004	-	0.010	0.10	-	0.25
A2	0.047	-	0.059	1.20	-	1.50
B	0.013	-	0.020	0.33	-	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.189	-	0.197	4.80	-	5.00
E	0.150	-	0.157	3.80	-	4.00
e	0.050 BSC			1.27 BSC		
H	0.228	-	0.244	5.80	-	6.20
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

8 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

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**	106957	06/11/01	IKA	Convert from IMI to Cypress