19-2812; Rev 0; 2/08

EVALUATION KIT AVAILABLE

4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

General Description

The MAX17079 is a 7-channel logic-level input to high-voltage output level shifter. Each channel has two inputs plus a shared enable input. Each channel has two outputs, which can be set to five output levels. Two outputs are complementary to each other. The five output levels are set by five supply rails that are common to all 14 outputs.

The five supply rails include a typical TFT VCOM rail. Two upper rails are always greater than VCOM, with VH1 always greater than VH2. The two lower rails are always less than VCOM, with VL1 always less than VL2. Other supply rails are VLS (the typical TFT AVDD supply) and VCC (the logic supply). The MAX17079 can also be configured as a two-level voltage shifter.

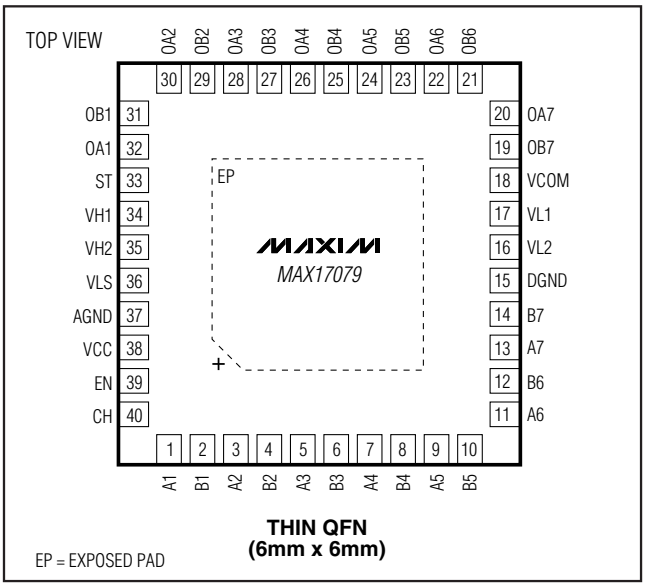
When EN is low, all 14 outputs connect to VCOM, and when EN is high, the outputs are determined by their inputs. The logic inputs are driven by the timing controller. The output switches are typically 3Ω with low propagation delays and fast rise times. The MAX17079 has a minimum dead time to prevent shoot-through currents between supplies. The MAX17079 has thermal shutdown to protect against overheating, VCC undervoltage lockout (UVLO), and VLS UVLO.

The MAX17079 is in a 40-pin, 6mm x 6mm, thin QFN package, with exposed pad and a maximum height of 0.8mm.

Applications

TFT LCD TV Panels

Pin Configuration



Features

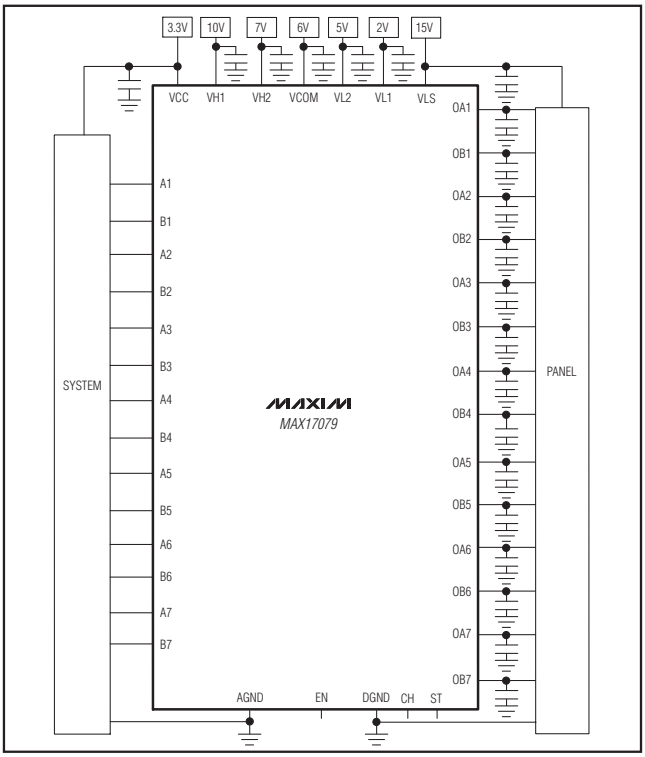
- ♦ 7-Channel Logic-Level Input to High-Voltage Output Level Shifter
- ♦ Complementary Outputs in Each Channel
- ♦ VLS Input Range from 10V to 18V
- ♦ VCC Input Range from 2.3V to 3.6V
- ♦ 2-Level or 4-Level Operation
- ♦ Sequential or Combinational Logic
- ♦ 3Ω Output Switches
- ♦ 5-Level Output
- ♦ Short Propagation Delay (80ns typ)
- ♦ Fast Rise Time (30ns typ)
- ♦ Built-In Dead Time to Prevent Shoot-Through
- ♦ Thermal Shutdown
- ♦ VLS and VCC Undervoltage Lockout

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX17079GTL+	-40°C to +105°C	40 TQFN-EP* (6mm x 6mm)	T4066+5

*EP = Exposed paddle.

Simplified Operating Circuit



4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

ABSOLUTE MAXIMUM RATINGS

VCC to AGND .....-0.3V to +7V
Ax, Bx, CH, ST, EN to AGND .....-0.3V to +7V
DGND to AGND .....-0.3V to +0.3V
VLS to DGND .....-0.3V to +20V
VH1, VH2, VL1, VL2, VCOM to DGND .....-0.3V to (V_{LS} + 0.3V)
OAx, OBx to DGND .....(V_{L1} - 0.3V) to (V_{H1} + 0.3V)
OBx, OAx RMS Current 50mA
VH1, VH2, VL1, VL2 RMS Current 300mA
VH1, VL2, VCOM, to DGND .....(VL1 - 0.3V) to (VH1 + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
40-Pin, 6mm x 6mm TQFN
(derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{VCC} = 3.3V, V_{VLS} = 15V, V_{VH1} = 10V, V_{VH2} = 7V, V_{VCOM} = 6V, V_{VL2} = 5V, V_{VL1} = 2V, T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
VCC Input Voltage Range		2.3		3.6	V
VCC Input Undervoltage Lockout	Rising edge, 200mV typical hysteresis	1.8	2.0	2.2	V
VLS Input Voltage Range		10		18	V
VLS Input Undervoltage Lockout	Rising edge, 500mV typical hysteresis	8.0	8.5	9.0	V
VH1 Input Voltage Range		4		V_{VLS}	V
VH2 Input Voltage Range		0		V_{VLS} - 4	V
VL2 Input Voltage Range		0		V_{VLS} - 4	V
VL1 Input Voltage Range		0		V_{VLS} - 4	V
VCOM Input Voltage Range		4		V_{VLS} - 4	V
VCC Quiescent Current			50		µA
VLS Quiescent Current	All channels in STATE 2		300		µA
VH1 Quiescent Current	All channels in STATE 1 or STATE 3		150		µA
VH2 Quiescent Current	All channels in STATE 2 or STATE 4		-125		µA
VL1 Quiescent Current	All channels in STATE 1 or STATE 3		-90		µA
VL2 Quiescent Current	All channels in STATE 2 or STATE 4		-130		µA
INPUTS AND OUTPUTS					
Logic-Input Low Voltage	EN, CH, ST, Ax, Bx			0.3 x V_{VCC}	V
Logic-Input High Voltage	EN, CH, ST, Ax, Bx	0.7 x V_{VCC}			V
Logic-Low Input Current	EN, CH, ST, Ax, Bx to AGND	-1		+1	µA
Logic-High Input Current	VCC to EN, CH, ST, Ax, Bx	10.0	16.5	30.0	µA
VH1 - OAx, VH1 - OBx On-Resistance	V_{VLS} = 10V, V_{VH1} = 5V, $I_{(OAx, OBx)}$ = 20mA		3		Ω
VH2 - OAx, VH2 - OBx On-Resistance	V_{VLS} = 10V, V_{VH2} = 5V, $I_{(OAx, OBx)}$ = 20mA		3		Ω

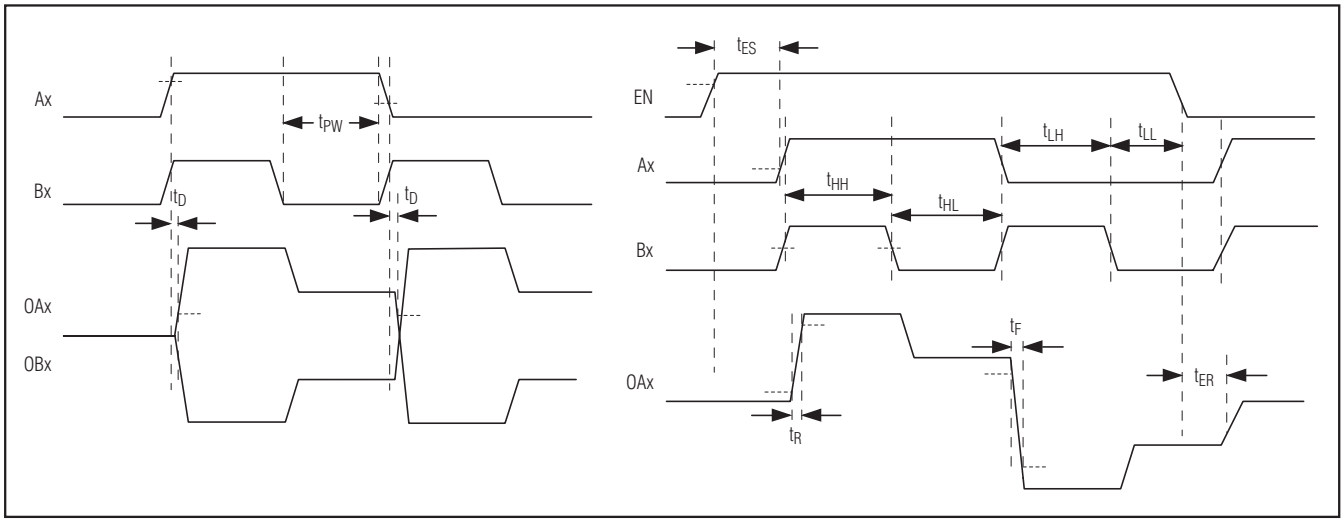
ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VCC} = 3.3V, V_{VLS} = 15V, V_{VH1} = 10V, V_{VH2} = 7V, V_{VCOM} = 6V, V_{VL2} = 5V, V_{VL1} = 2V, T_A = -40°C to +105°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VL1 - OAx, VL1 - OBx On-Resistance	V_{VLS} = 10V, V_{VL1} = 5V, $I_{(OAx, OBx)}$ = 20mA		3		Ω
VL2 - OAx, VL2 - OBx On-Resistance	V_{VLS} = 10V, V_{VL2} = 5V, $I_{(OAx, OBx)}$ = 20mA		3		Ω
On-Resistance Difference	V_{VLS} = 10V, V_{VH2} = 6V, V_{VL2} = 4V, $I_{(OAx, OBx)}$ = 20mA (VH2 to OAx) - (VL2 to OAx), (VH2 to OBx) - (VL2 to OBx)	-0.5	0	+0.5	Ω
	V_{VLS} = 10V, V_{VH1} = 6V, V_{VL1} = 4V, $I_{(OAx, OBx)}$ = 20mA (VH1 to OAx) - (VL1 to OAx), (VH1 to OBx) - (VL1 to OBx)	-1.5	0	+1.5	
VCOM - OAx, VCOM - OBx On-Resistance	V_{VLS} = 10V, V_{VCOM} = 5V, $I_{(OAx, OBx)}$ = 20mA		15		Ω
TIMING					
Input Pulse Width	t_{HH}, t_{HL}, t_{LH}, t_{LL}, refers to the minimum duration of input for a given state	500			ns
EN Setup Time	t_{ES}	-50		+100	ns
EN Falling Delay	t_{ER}		70	200	ns
Output Delay Time	t_D, no load, input to 10% output		80	200	ns
Output Rise Time	t_R, no load, rails of 0V and 18V, measured from 2V to 16V		30	100	ns
Output Fall Time	t_F, no load, rails of 0V and 18V, measured from 16V to 2V		30	100	ns
Input Pulse Width	t_{PW}, no load, refers to the minimum high or low time of Ax or Bx	500			ns

Note 1: T_A = -40°C specifications are guaranteed by design, not production tested. Production test is done at T_A = +25°C and T_A = +85°C.

Timing Diagram

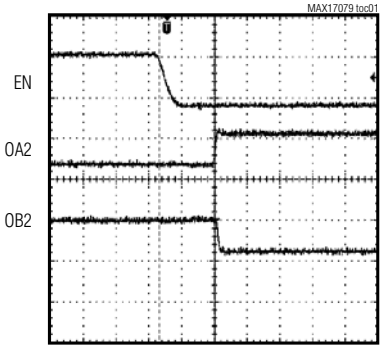


4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Typical Operating Characteristics

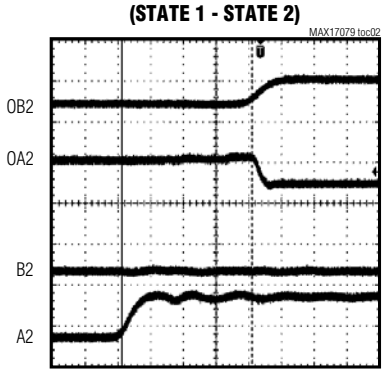
(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

ENABLE PROPAGATION DELAY



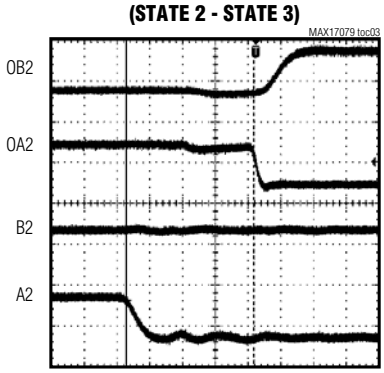
EN: 2V/div
OA2: 5V/div
OB2: 5V/div

PROPAGATION DELAY (STATE 1 - STATE 2)



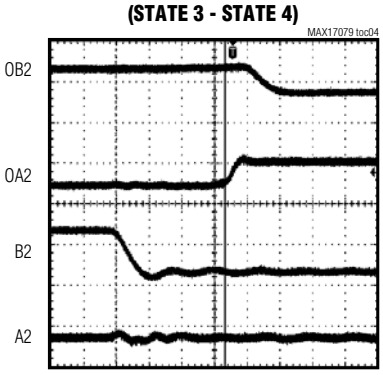
OB2: 5V/div
OA2: 5V/div
B2: 5V/div
A2: 5V/div

PROPAGATION DELAY (STATE 2 - STATE 3)



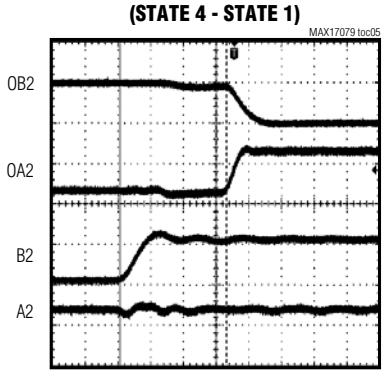
OB2: 5V/div
OA2: 5V/div
B2: 5V/div
A2: 5V/div

PROPAGATION DELAY (STATE 3 - STATE 4)



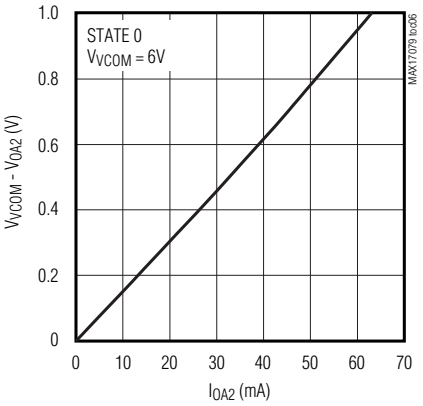
OB2: 5V/div
OA2: 5V/div
B2: 5V/div
A2: 5V/div

PROPAGATION DELAY (STATE 4 - STATE 1)

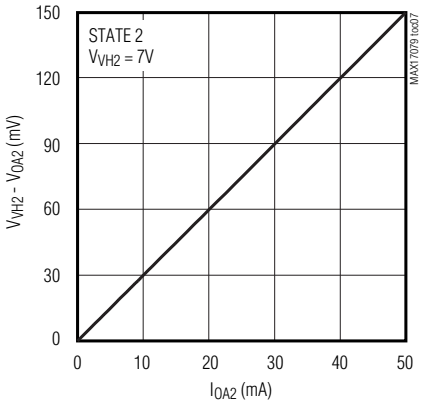


OB2: 5V/div
OA2: 5V/div
B2: 5V/div
A2: 5V/div

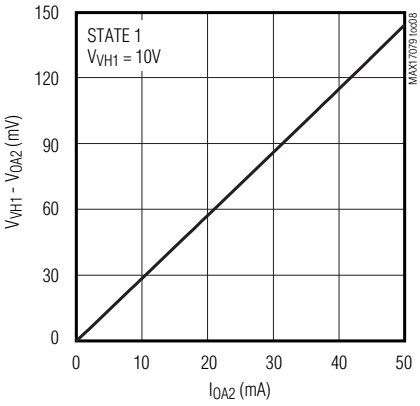
VCOM SWITCH OUTPUT RESISTANCE



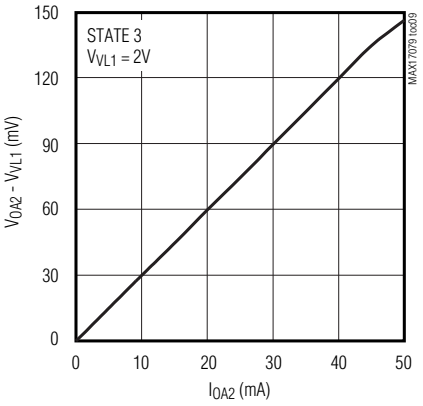
VH2 SWITCH OUTPUT RESISTANCE



VH1 SWITCH OUTPUT RESISTANCE



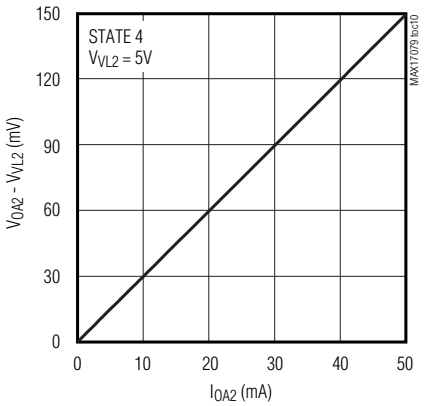
VL1 SWITCH OUTPUT RESISTANCE



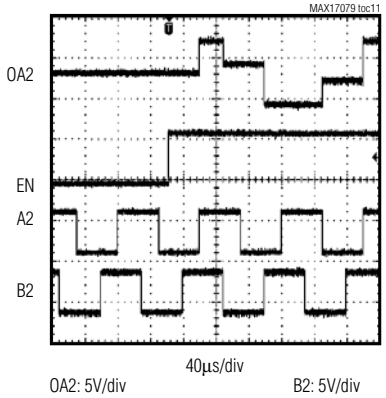
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

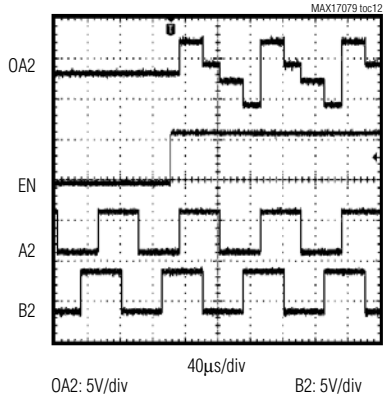
VL2 SWITCH OUTPUT RESISTANCE



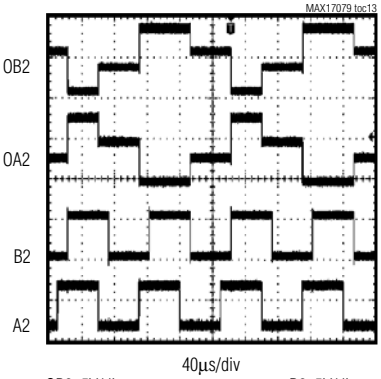
4-LEVEL SEQUENTIAL STARTUP



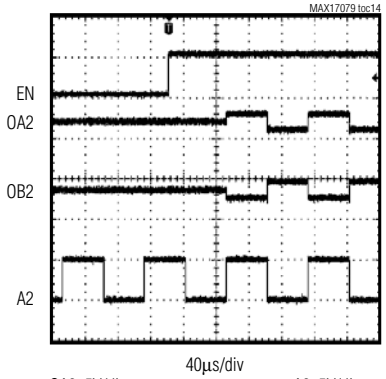
4-LEVEL COMBINATIONAL STARTUP



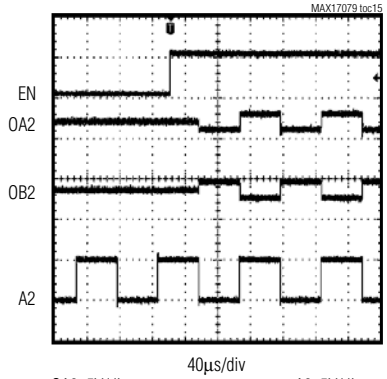
4-LEVEL SEQUENTIAL OPERATION



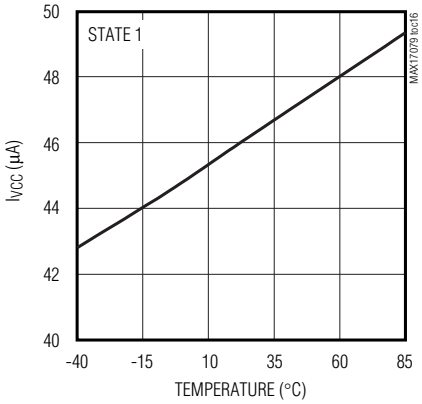
2-LEVEL SEQUENTIAL STARTUP



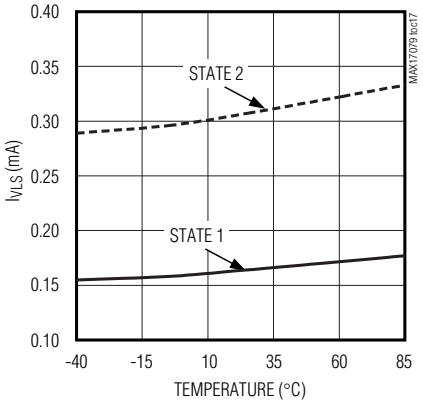
2-LEVEL COMBINATIONAL STARTUP



VCC QUIESCENT CURRENT vs. TEMPERATURE



VLS QUIESCENT CURRENT vs. TEMPERATURE



4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Pin Description

PIN	NAME	FUNCTION
1	A1	Level Shifter Logic Input
2	B1	Level Shifter Logic Input
3	A2	Level Shifter Logic Input
4	B2	Level Shifter Logic Input
5	A3	Level Shifter Logic Input
6	B3	Level Shifter Logic Input
7	A4	Level Shifter Logic Input
8	B4	Level Shifter Logic Input
9	A5	Level Shifter Logic Input
10	B5	Level Shifter Logic Input
11	A6	Level Shifter Logic Input
12	B6	Level Shifter Logic Input
13	A7	Level Shifter Logic Input
14	B7	Level Shifter Logic Input
15	DGND	Output Supply Ground Connection
16	VL2	Output Supply Rail. Bypass VL2 to DGND with a 0.1µF capacitor.
17	VL1	Output Supply Rail. Bypass VL1 to DGND with a 0.1µF capacitor.
18	VCOM	Output Supply Rail. Bypass VCOM to DGND with a 0.1µF capacitor.
19	OB7	Level Shifter Output
20	OA7	Level Shifter Output
21	OB6	Level Shifter Output
22	OA6	Level Shifter Output
23	OB5	Level Shifter Output
24	OA5	Level Shifter Output
25	OB4	Level Shifter Output
26	OA4	Level Shifter Output
27	OB3	Level Shifter Output
28	OA3	Level Shifter Output
29	OB2	Level Shifter Output
30	OA2	Level Shifter Output
31	OB1	Level Shifter Output
32	OA1	Level Shifter Output
33	ST	State/Combinational Logic Select. Connect ST to VCC for state logic and to DGND for combinational logic operation.
34	VH1	Output Supply Rail. Bypass VH1 to DGND with a 0.1µF capacitor.
35	VH2	Output Supply Rail. Bypass VH2 to DGND with a 0.1µF capacitor.
36	VLS	Upper Supply Rail. Bypass VLS to DGND with a 0.1µF capacitor.
37	AGND	Input Logic Ground Connection
38	VCC	Input Logic Supply Connection. Bypass to AGND with a minimum 0.1µF capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
39	EN	Enable Input. All outputs connect to VCOM when EN is low.
40	CH	Select Input for Two Level/Four Level. Connect CH to VCC for two-level operation and tie CH to DGND or let it float for four-level operation. For two-level operation, power VH2 and VL2 and control the outputs with Ax inputs. Bx inputs can be left floating or be connected to AGND.
—	EP	Exposed Pad. Connect the exposed backside pad to AGND and DGND.

Detailed Description

The MAX17079 is a 7-channel level shifter that converts a 2-bit logic-level input to a five-level high-voltage output. The outputs are connected to the four output rails (VH1, VH2, VL1, VL2) through 3Ω switches and to the fifth rail (VCOM) through a 15Ω switch. The output rails lie between DGND and the upper supply rail (VLS).

The MAX17079 has two modes of operation. When ST = VCC, it operates in sequential mode and when ST = AGND, it operates in combinational mode. The MAX17079 can operate in either two-level output or four-level output configuration. In four-level output mode, the output can connect to VH1, VH2, VL2, or VL1, and in two-level output mode, the output can connect to VH2 or VL2. Connect CH to AGND for four-level operation and connect CH to VCC for two-level operation.

The output supply rail voltages should satisfy the following condition at all times:

$$VLS \geq VH1 \geq (VH2, VL2, VCOM) \geq VL1$$

The MAX17079 has built-in dead time to avoid shoot-through current. The propagation delay between input and output is 80ns and the rise time is 30ns.

Figure 1 is the MAX17079 typical operating circuit and Figure 2 shows the functional diagram.

Four-Level Combinational Logic

Connect CH and ST to AGND for four-level combinational operation. If EN is LOW or VCC is less than UVLO or VLS is less than its UVLO, the outputs are in STANDBY and the outputs connect to VCOM. After EN is HIGH or VCC is greater than UVLO and VLS is greater than its UVLO, the outputs are ready to respond to logic inputs at Ax, Bx. If EN goes HIGH after a rising or falling edge of Ax or Bx, the device remains in STANDBY state until the next edge comes. All state transitions can be level triggered. The output is determined by the following truth table (Table 1).

Table 1. Truth Table Four-Level Combinational Operation

	HIGH (Ax)	LOW (Ax)
HIGH (Bx)	OAx = VH1 OBx = VL1	OAx = VL1 OBx = VH1
LOW (Bx)	OAx = VH2 OBx = VL2	OAx = VL2 OBx = VH2

4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

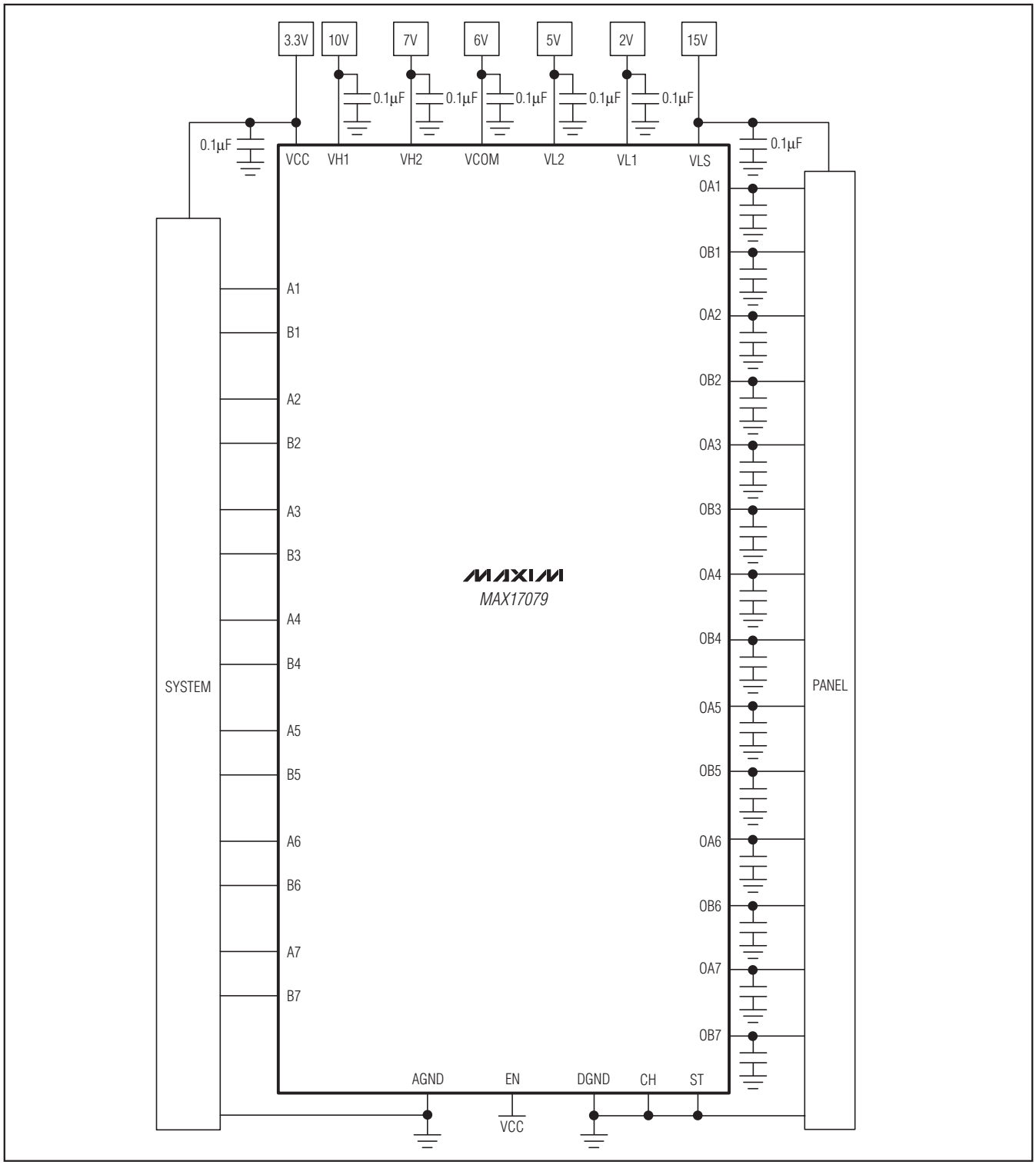


Figure 1. Typical Operating Circuit

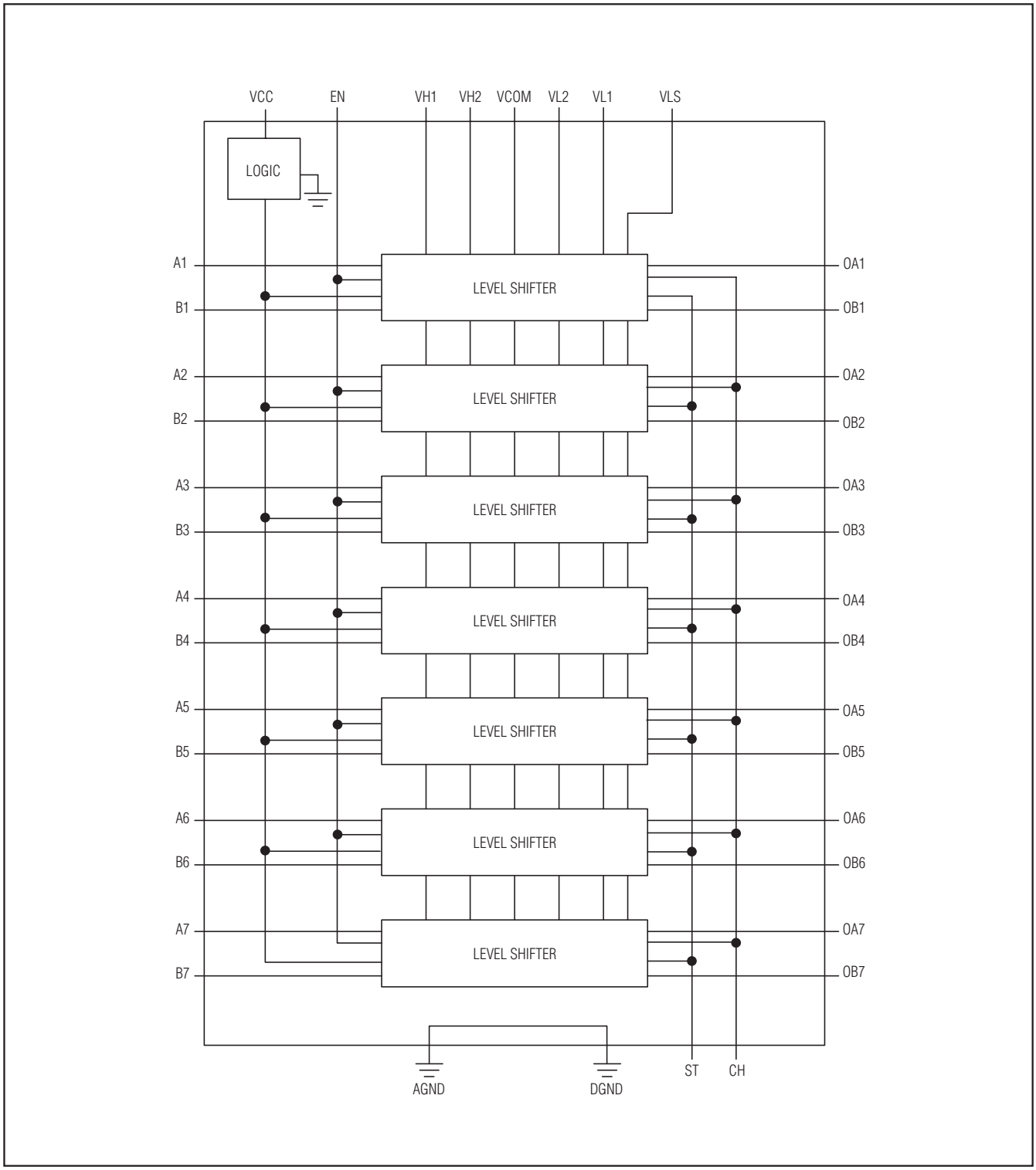


Figure 2. Functional Diagram

4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Sequential Operation

Connect CH to AGND and ST to VCC for four-level sequential operation. If EN is LOW or VCC is less than its UVLO or V_{VLS} is less than its UVLO, the outputs are in STANDBY and the outputs connect to VCOM. After EN is HIGH, VCC exceeds its UVLO and VLS exceeds its UVLO, the outputs are ready to respond to logic inputs at Ax and Bx. In sequential operation, the logic inputs and corresponding output states sequence only in a predefined order. In four-level operation, it is only possible to progress from STATE 1 to STATE 2 or to STANDBY. The same applies to the other transitions, including from STATE 4 to STATE 1. Table 2 shows the logic states of the level shifter in a sequential mode of operation.

Figure 3 shows the sequence of operation. Outputs OAx and OBx always change in the same sequence.

Table 2. Truth Table Four-Level Sequential Mode of Operation

STATE	Ax	Bx	OAx	OBx
STATE 1	H	H	VH1	VL1
STATE 2	H	L	VH2	VL2
STATE 3	L	H	VL1	VH1
STATE 4	L	L	VL2	VH2

x = Don't care.

Two-Level Operation

The MAX17079 also has a two-level output voltage operation. Connect CH to VCC for two-level operation. In two-level operation, the device transitions between two states and the outputs can be connected only to VH2 or VL2 or VCOM in STANDBY. Other than the start-up condition, there is no way to distinguish between sequential operation and combinational operation. If EN is LOW or VCC is less than its UVLO or VLS is less than its UVLO, the outputs are in STANDBY and the outputs connect to VCOM. After EN is HIGH, VCC is greater than its UVLO and VLS is greater than its UVLO, the outputs are ready to respond to logic inputs at Ax. Connect Bx to AGND, as the outputs respond only to the rising and falling edge of Ax. The outputs transition from VCOM to the specific output only on the rising edge of Ax in sequential mode. In combinational mode, the outputs transition from VCOM to the specific output on either rising or falling edge of Ax. The following truth table (Table 3) shows the output states.

Table 3. Truth Table Two-Level Operation

HIGH (Ax)	OAx = VH2, OBx = VL2
LOW (Ax)	OAx = VL2, OBx = VH2

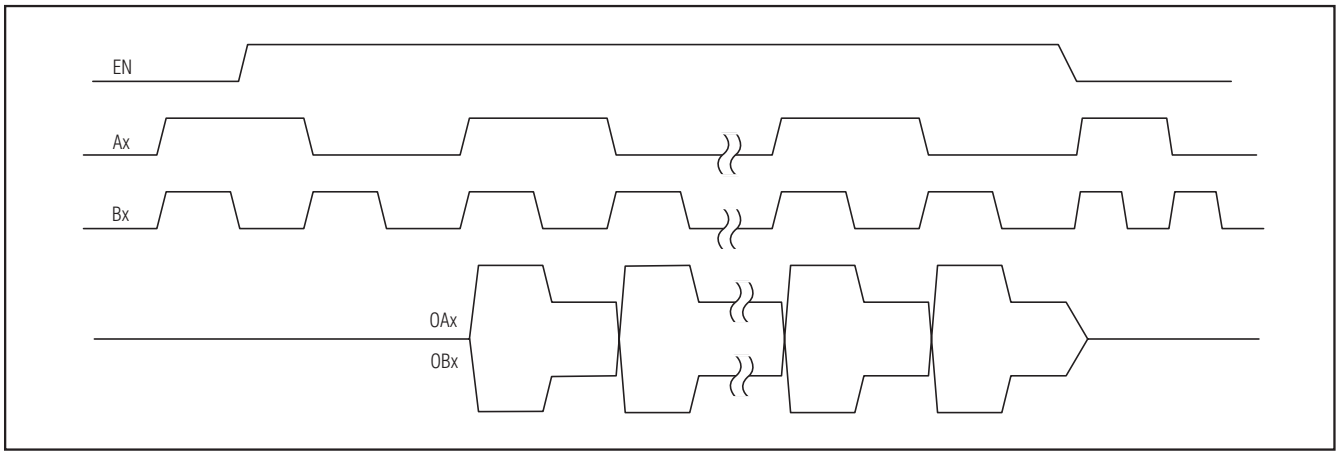


Figure 3. Sequential Mode Operation

4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Startup

The MAX17079 supply rail voltages should satisfy the startup sequence shown in Figure 4. The supply rail voltages should also satisfy the following conditions:

$$VLS \geq VH1 \geq (VH2, VL2, VCOM) \geq VL1$$

For proper operation, EN should be HIGH only after all the supply rails are ON.

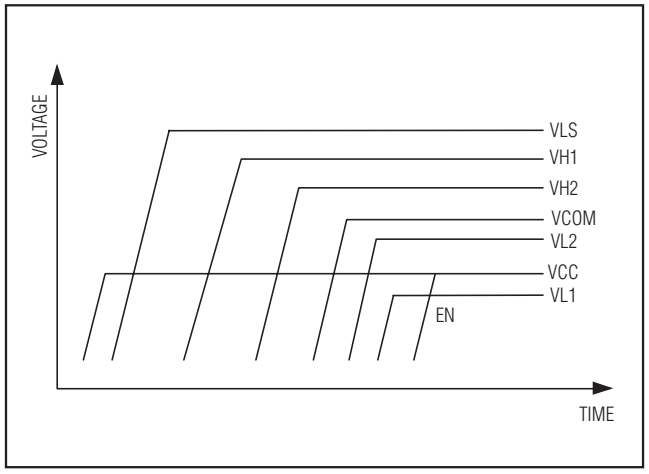


Figure 4. Startup Sequence

Load Characteristics

The load has a typical characteristic of large TFT LCD panels. During state transitions, a built-in dead time prevents shoot-through current. During dead time as the output is not connected, the output can be affected by the panel load. To avoid voltage spikes during the deadline, 1nF to 4.7nF capacitors can be added at each output.

PCB Layout Guidelines

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- The MAX17079 has a backside pad to dissipate heat. Do not route any trace around or under the backside pad.
- Ensure good decoupling of supply rails and put the bypass capacitor for each power supply very close to the pin.
- Create an analog ground island (AGND) that includes the AGND pin and the VCC bypass capacitor to ground. Connect AGND to the backside pad directly under the IC. Create a power ground plane (DGND) that includes the DGND pin, the remaining supply rails bypass capacitor grounds, and output bypass capacitors, if used in the system. Connect DGND to the backside pad directly under the IC. Other than the backside connection, avoid connecting AGND and DGND.

Chip Information

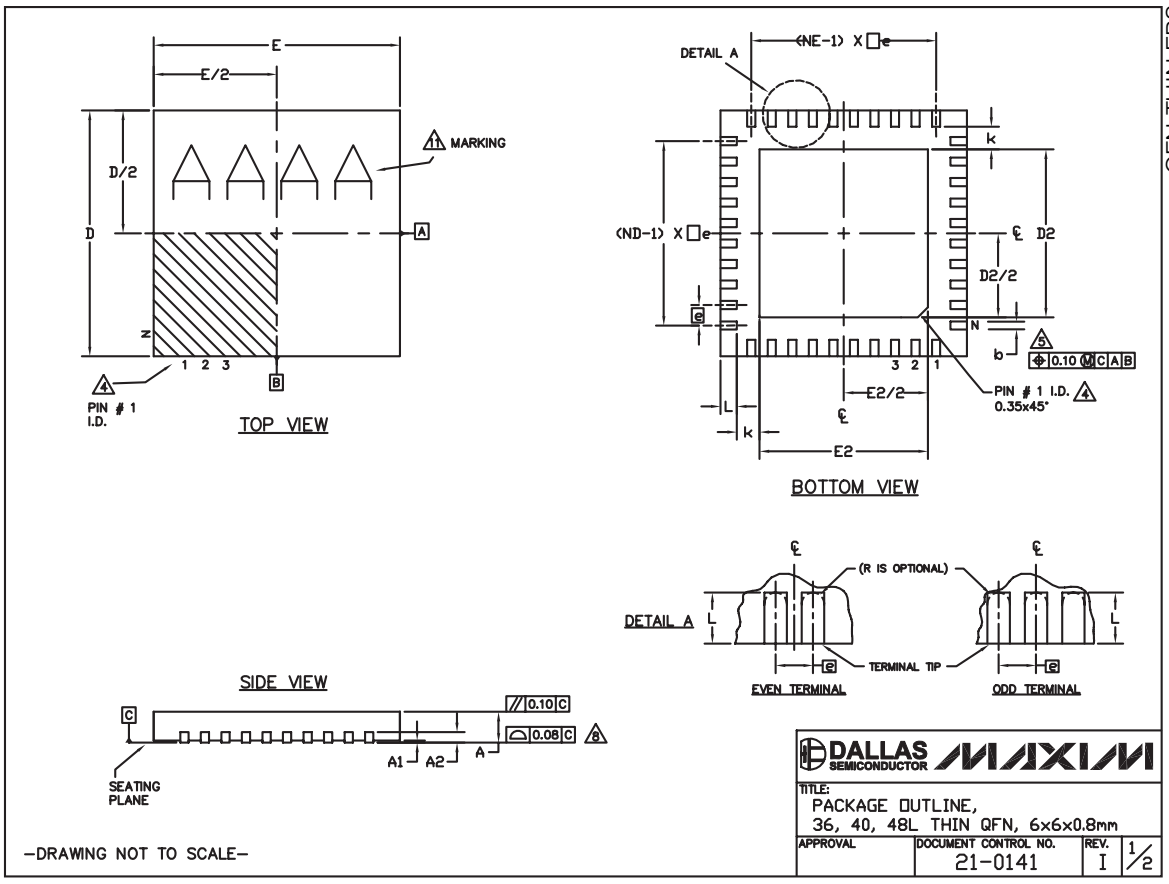
TRANSISTOR COUNT: 7580

PROCESS: BiCMOS

4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



4-Level or 2-Level Logic to High-Voltage Level Shifter for TFT LCD TV Display

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2		0.20 REF.			0.20 REF.			0.20 REF.	
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e		0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N		36			40			48	
ND		9			10			12	
NE		9			10			12	
JEDEC		WJJD-1			WJJD-2			–	

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	I	2/2