

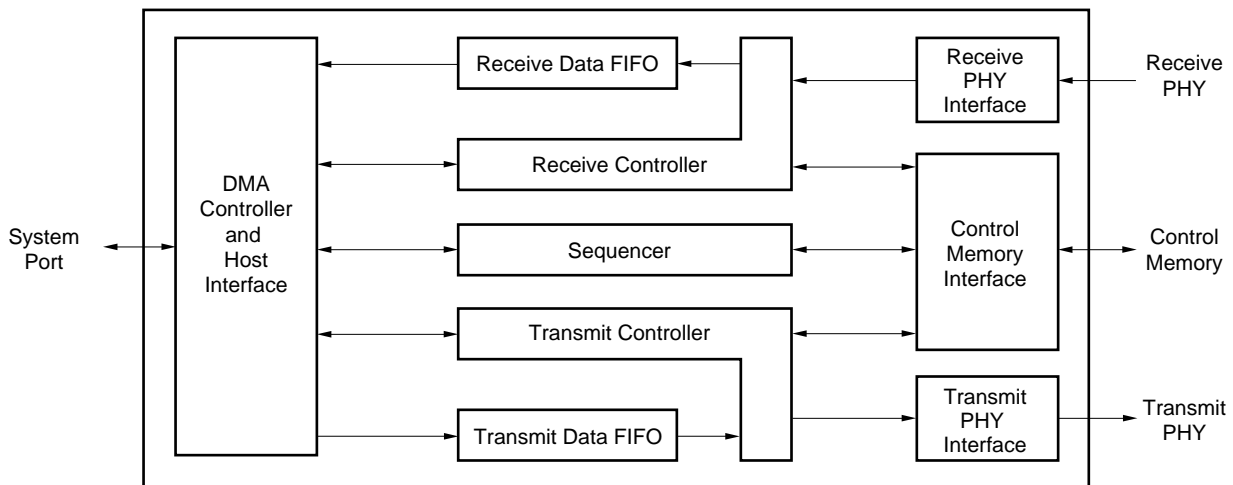
μ PD98401A

LOCAL ATM SAR CHIP (NEASCOT-S15™)

Features

- Conforms to the ATM-Forum recommendations
- Implements AAL-5 SAR sublayer and ATM layer functions
- Fully supports AAL-5 (non AAL-5 types can be supported in software)
- Supports up to 32 K active virtual channels for high-end server applications
- Features 16 traffic shapers using dual leaky bucket scheduling algorithm; handles traffic based on specified priority level, specified average, and peak traffic rates
- Adopts a generic 32-bit bus interface for simple connection to most popular I/O buses
- Features an extremely flexible buffer management scheme
- Operates at speeds up to 33 MHz
- Adopts the widely accepted UTOPIA interface with physical layer
- CMOS, +5 V power supply, 208-pin plastic QFP(fine pitch)

Block Diagram



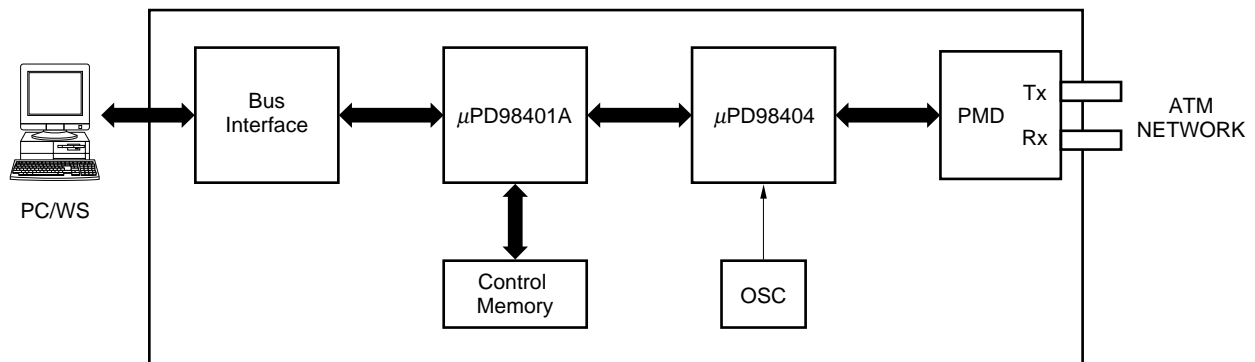
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Improvements from μ PD98401

The μ PD98401A has improved in function and performance as follows keeping compatibility with current μ PD98401.

- Supports 12 words DMA burst data transmission in addition to 2, 4, 8, 16 words
- Supports byte data arrangement of the receiving data in addition to the transmitting data
- Supports UTOPIA interface standard cell level handshake mode
- Adopts bus monitoring terminals
- Adopts an enlarged receive data FIFO from 10 cells size to 23 cells size
- Features user data part byte size indication in the packet size field of the receive indication
- Features idle cell transmission in addition to unassigned cell for the cell speed adjustment
- Features transmitting cell scheduling function in per VC mode including in per shaper mode

Sample Configuration of ATM Adapter Card



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