1 DIGITAL Semiconductor 21340-AB Overview

The DIGITAL Semiconductor 21340-AB 10/100-Mb/s Buffered Port Switch (also called the 21340-AB) is an intelligent, multisegment, four-port buffered repeater building block. The 21340-AB can be used to build a variety of advanced Ethernet port switching architectures in both managed and nonmanaged configurations.

1.1 General Description

The 21340-AB device is targeted for port switch applications, 10/100-Mb/s buffered repeater applications, and as a Fast Ethernet topology limitation solution.

When used in port switch applications, the 21340-AB device enables dynamic allocation of ports between four separate segments, supporting VLAN implementations. It offloads traffic from the forwarding switch engine by implementing an address filtering scheme between ports sharing the same segment. Intersegment packets are filtered out and are not presented to the switching engine.

The 21340-AB device enlarges the available bandwidth by enabling the filtering of fragment packets and preventing collisions from being propagated to other ports. The 21340-AB enables the use of a low-cost switch engine with a relatively small buffer size. In addition, it enables the setting of different priority schemes to different ports for bandwidth-hungry or time-bounded applications.

The 21340-AB allows a simple and low-cost migration path from a 10-Mb/s data rate network to a 100-Mb/s data rate network. Upgrading single or multiple end-stations from 10 Mb/s to 100 Mb/s does not require any hardware changes in a 21340-AB-based hub. The current hardware's value is maintained.

The 21340-AB allows the building of a Fast Ethernet network topology of unlimited length. Although the Fast Ethernet protocol scales the timing parameters along all network components, it creates some severe topological restrictions. Class II Fast Ethernet repeaters allow cascading of only two level of repeaters, reaching a maximum network length of 205 m. The 21340-AB-based port switch eliminates this network length restriction by transforming each of the connected ports into a distinct collision domain handled on the port switch side by a fully featured MAC with full-packet buffering capability.

1.2 Conventions and Terminology

This document uses the following subscript notation terminology:

Subscript Notation	Description
[i]	Generic reference to one segment of the 21340-AB parallel bus. For example, **cntl[i]** refers to the control lines for one segment (out of 4) of the parallel bus.
{j}	Generic reference to signals of a single 21340-AB port. For example, **gnt{j}** refers to the grant line of a 21340-AB port.
<>	Numbers inside the angle brackets indicate specific bits of a register. For example, **sts{j}<5>** is a generic reference to bit 5 in the STR register in any of the four 21340-AB ports. Bit 0 is always the LSB.

1.3 Features

The 21340-AB has the following features:

- Offers four distinct standard MII/SYM interface ports, each connected to a separate collision domain.
- Supports CAT3 unshielded twisted-pair (UTP), CAT5 UTP, shielded twisted-pair (STP), or fiber cables. Multiple media types can be connected to a single 21340-AB simultaneously. With external PHY devices, each individual port can support multiple media connections.
- Contains Physical Coding Sublayer (PCS) functions per port to significantly reduce the cost of 100BASE-TX solutions.
- Offers unique inverse MII functionality[1] enabling direct connection to any MII PHY or MII MAC device without the need of a glue logic.
- Supports MII management functions.
- Supports 10-Mb/s or 100-Mb/s network ports.
- Receives and transmits at full wire speed.
- Implements partition, receive jabber, and carrier integrity isolation functions.
- Offers expansion ports that enable cascading up to 36 ports on one board.
- Supports up to 256 ports in a stackable configuration.
- Provides onchip round-robin and bursty round-robin with a priority arbitration scheme with no additional logic.
- Supports a wide range of external arbitration schemes.

- Provides dynamic allocation of ports to the four parallel bus segments supporting virtual LAN (VLAN) implementation.
- Supports half-duplex or full-duplex flow control between two 21340-AB ports.
- Provides filtering capability for one MAC address per port.
- Supports External Address Lookup Table logic unit.
- Ensures zero packet loss.
- Provides fragment packet filtering mode.
- Provides full RMON statistic group counters implementation.
- Provides full repeater MIB statistic counters implementation.
- Provides Ethernet-like MIB statistic counters implementation.
- Provides 21340-AB private MIB statistic counters implementation.
- Implements an interrupt pin for error notifications, isolation events, and statistic counter wrap-around notifications.
- Provides external and internal loopback capabilities.
- Supports JTAG boundary scan.

[1] DIGITAL Semiconductor patent pending.

1.4 Microarchitecture

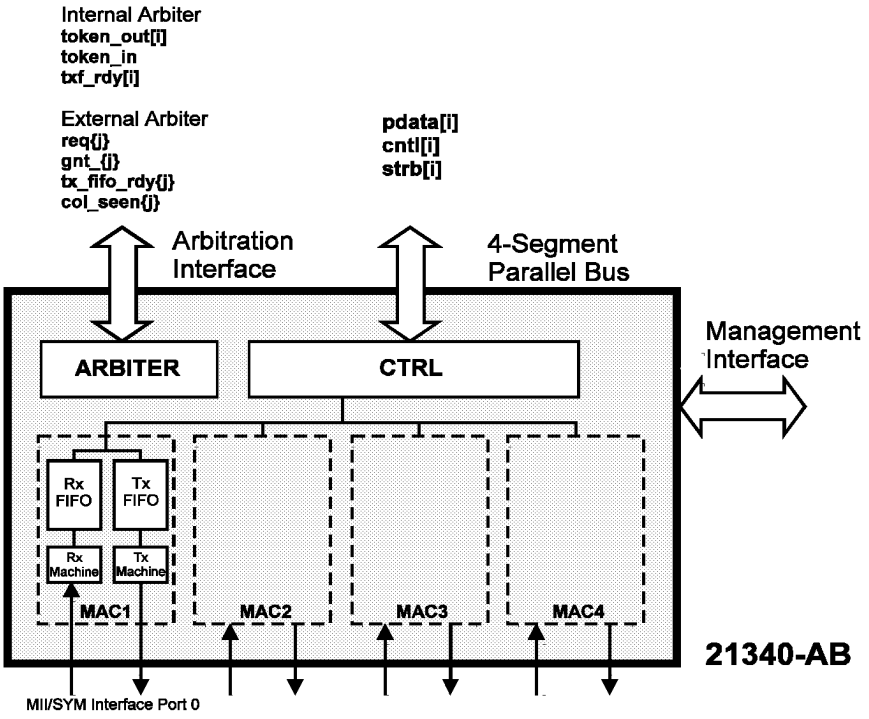
The 21340-AB is an enhanced version of the 21340 device. It is fully backward-compatible to the 21340. To benefit from its advanced features and enhancements, connect the **emop** pin to **Vdd**. Connecting the **emop** pin to **Vss** will mask out all the 21340-AB features and the device will maintain the basic 21340 functionality.

Figure 1 is a block diagram of the 21340-AB chip. The 21340-AB includes four independent ports. Each of the ports can be connected dynamically to any of the four segments of the 21340-AB parallel bus. Each segment of the parallel bus can be brought out as an expansion port to external devices such as additional 21340-AB units.

The 21340-AB contains four independent MAC-layer interfaces. These interfaces can connect directly to either an MII PHY device, an MII MAC device, or a SYM PHY device, allowing for 100BASE-TX cost optimization in the system solution.

The MAC interfaces contain smart FIFO buffers that eliminate packet loss and enhance throughput. The buffer size (4KB receive FIFO and 2KB transmit FIFO) eliminates the need for additional onboard memory.

Figure 1 DIGITAL Semiconductor 21340-AB Block Diagram



1.5 21340-AB Functional Description

This section describes the major functions of the 21340-AB and the data flow from one receiving port to all other transmitting ports.

1.5.1 Data Flow

A 21340-AB port can receive data packets when there is enough space in its receive FIFO (Rx_FIFO). Each 21340-AB port uses various methods to ensure zero packet loss in case of Rx_FIFO congestion. The method selected depends on the remote node's capabilities. When a 21340-AB port identifies its remote node as another 21340 node*, the 21340 – 21340 credit-based flow-control (FCTL) method is

activated. When a 21340-AB port identifies its remote node as a non-21340 node*, it uses a backpressure (BP) mechanism whenever the 21340-AB port's Rx_FIFO is congested, holding off the remote node until the 21340-AB port is ready to receive a full packet.

* This node can be either a 21340 or a 21340-AB remote node.

1.5.1.1 Backpressure Mechanisms

The 21340-AB port uses two programmable backpressure mechanisms (BPM control bit in OPM{j}) to deliberately generate a carrier on the physical media to block the remote node's transmission. One mechanism causes the 21340-AB port to continuously send a special BP packet to the remote node. This makes the remote node suspend its attempt to transmit until the port is ready to receive a full packet. The other mechanism causes the 21340-AB port to collide with each carrier activity from the remote node by transmitting 96-bit JAM patterns. No additional packets are generated and spread throughout the network. In both mechanisms, other 21340-AB ports are not affected by the backpressure operation.

1.5.1.2 Arbitration and Data Forwarding Functions

When a received packet starts loading into the Rx_FIFO, the port asserts its request to ask the arbiter for permission to broadcast the packet on the parallel bus. The arbiter logic verifies that all target ports are ready to load the broadcast packet before granting the requesting port permission to broadcast.

The 21340-AB provides two internal onchip arbitration schemes that can be selected on a per-port basis:

- Round robin
- Bursty round robin

The internal onchip arbitration scheme, based on token passing, is expandable to support stackable configuration.

The 21340-AB can also support an external arbiter. The external arbiter uses the same 21340-AB pins as the internal arbitration scheme. See Sections 1.5.15 and 1.5.16 for a detailed description of the onchip internal and external arbitration schemes.

The granted port starts broadcasting the packet over the parallel bus segment [i]. First it drives a preamble octet, followed by a Start Frame Delimiter (SFD), on the **pdata[i]** lines while driving a *start frame* op-code on the **cntl[i]** lines. Next, the port transfers the received packet from its Rx_FIFO to the **pdata[i]** lines while driving a

data valid op-code on **cntl[i]**. After the last data byte is transferred the granted port drives the chip_id, port_id, and received_packet_status bytes on **pdata[i]** while driving an *end frame* op-code on **cntl[i]**.

The broadcast packet is buffered in the target ports' transmit FIFOs (Tx_FIFOs) while it is transmitted to the respective remote nodes through MII or SYM PHY devices, according to the IEEE 802.3 standard.

1.5.2 Port Assignment to Segment and Data Rate Selection

Each 21340-AB port can be assigned dynamically to any of the four parallel bus segments. Each 21340-AB port can operate independently at either 10 Mb/s or 100 Mb/s, depending on the local PHY configuration. All ports allocated to the same parallel bus segment must be configured to the same data transfer rate.

Reassigning a port from one parallel bus segment to another, or changing the data rate, is software controlled. This can only be done when there is no packet being broadcast on the parallel bus and the arbiter is disabled.

1.5.3 Remote Node Flow-Control Autodetection Process

The purpose of the flow-control autodetection process is to check if the remote node is capable of running the 21340 credit-based flow-control scheme. The 21340-AB ports use the following two autodetection methods, based on the port's local and remote PHY device capabilities: Nway or Non-Nway.

1.5.3.1 Nway-Supported Autodetection

If the local PHY is an MII PHY device, the management entity uses an Auto-Negotiation process to check the remote node capabilities.

If the remote node is not capable of running Auto-Negotiation, the management entity performs the non-Nway autodetection identification process as described in Section 1.5.3.2. If the remote node supports Auto-Negotiation and the flow-control operation, the management entity:

Sets...	To...
Enable_nway_link in OPM{j} register	Configure the 21340-AB port{j} to perform the Nway autodetection process.

Based on the results of the Nway autodetection process, the port either:

Asserts...	To...
FCTL_on in STR{j} register	Notify the management entity that the link supports credit-based flow control. The port then operates according to the 21340 flow-control regime.
— or —	
FCTL_id_Failed in STR{j} register	Notify the management entity that the link does not support the 21340 flow-control regime. The link should be initialized to work in half-duplex 21340-client mode.

1.5.3.2 Non-Nway FCTL Autodetection

If the local PHY device has a SYM interface, or if the remote node does not support Auto-Negotiation, the management entity:

Sets...	To...
Enable_non_nway_link_id in OPM{j} register	Configure the 21340-AB port{j} to perform the non-Nway autodetection process

Based on the results of the non-Nway autodetection process, the port:

Asserts...	To...
FCTL_on bit in STR{j} register	Notify the management entity that the link supports credit-based flow control

The management entity, in turn, initializes the port to operate in the 21340 credit-based flow-control scheme.

If 21340 credit-based flow control has not been identified after a predefined period, the management entity initializes the port to operate in half-duplex 21340-client mode.

The user has the ability to manually set the link to a credit-based flow-control link, using the Force-FCTL control bit in the OPM{j} register. If the local and remote nodes do not use the same flow-control algorithm, the 21340-AB port's behavior will be UNPREDICTABLE and may lead to a system failure. See Section 1.7 for a description of the PHY hardware requirements needed to avoid false identifications.

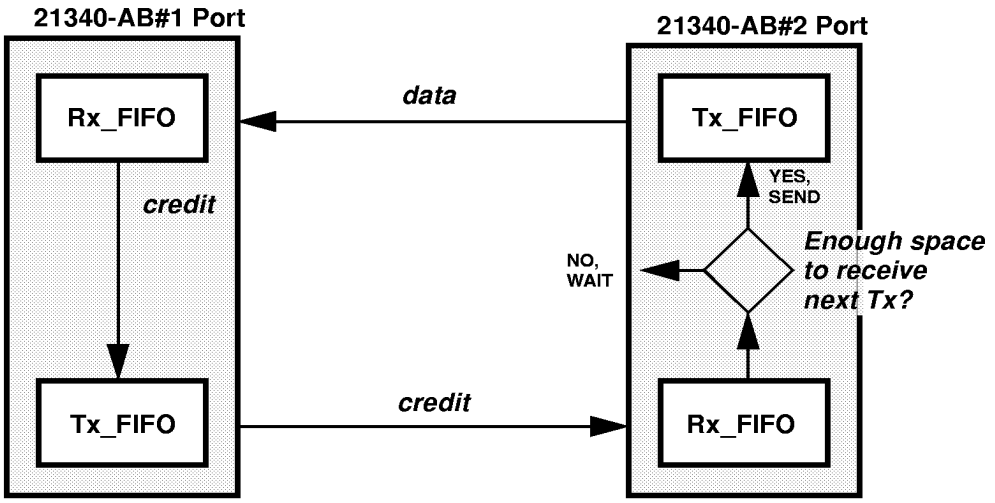
1.5.4 Flow-Control Mechanism

Network performance enhancement is achieved by a unique credit-based flow-control (FCTL) mechanism optimized for the 21340-AB's Tx and Rx buffers. The mechanism is utilized whenever autodetection determines that a port's remote node is able to use the same FCTL mechanism.

Each port supports credit-based FCTL in both directions. As a receiver, each port sends credits — the amount of free space that is available in its Rx_FIFO — to its remote node. As a sender, each port traces the amount of free space in the remote node's Rx_FIFO, using the credit value that has been transmitted by the remote node. The sender only transmits data packets to the remote node when it has enough credit. The received credit-based FCTL packets are filtered after the credit value is extracted from them.

Figure 2 illustrates the 21340-AB credit-based FCTL mechanism. In Figure 2, the 21340-AB#2 port is transmitting data to 21340-AB#1. The 21340-AB#1 port sends the amount of free space in its Rx_FIFO (credit) to its remote node. The 21340-AB#2 port then decides, according to the credit value, whether or not it can send a packet.

Figure 2 Credit-Based FCTL Mechanism



1.5.5 Address Filtering Scheme

To improve overall network performance, a 21340-AB port can filter out packets that are addressed to another port's remote node. The filtering level can be adjusted by the management entity.

When the internal address filtering mode is enabled, each 21340-AB port stores the last source address (SA) received from its remote node. This address is valid until the aging timer (T1) expires. The aging timer is set upon each packet reception.

During T1, the valid bit (V_bit) is set, and the port compares the broadcasted packet's destination address (DA) field with the stored address. If they match, the port asserts the **pkt_abort_l[i]** signal (active low), signaling other ports on the same parallel bus segment to filter out the packet.

On reception of a packet with a new SA, the port sets the T2 timer and the flood bit (F_bit). Until T2 expires, the port transmits all broadcasted packets, unless the **pkt_abort_l[i]** signal was deasserted by another 21340-AB port. When T2 expires, and V_bit is valid, the F_bit is cleared and the port filters out all broadcasted packets with destination addresses (DAs) that do not match the stored address.

1.5.5.1 Filtering Levels

The following three filtering levels can be applied using the F_bit and V_bit:

- **Most aggressive level**
  When the 21340-AB port determines that only one remote node is connected to it; F_bit is cleared and V_bit is set. The port filters out all packets that are not destined to its remote node. The port notifies other ports to filter out packets destined to its remote node.
- **Less aggressive level**
  When the port identifies at least one remote node, but is not certain about the existence of additional remote nodes; both the F_bit and V_bit are set. In this mode, the port filters out only packets that were identified as destined uniquely to one of the other ports. The port notifies other ports to filter out packets destined to its identified remote node. (The **pkt_abort_l[i]** signal was asserted for these packets.)

- **Least aggressive level**
  When no specific remote node has been identified by the port; F_bit is set and V_bit is cleared. In *flooding mode,* the 21340-AB port filters out only packets that are identified as uniquely destined to one of the other ports' remote nodes. This mode does not affect any other port's filtering operation.

  Note: The state of having both F_bit and V_bit cleared is not allowed.

Multicast packets (addressed to a specific group of ports) are always transmitted to the remote node unless **pkt_abort_l[i]** assertion by an external device is detected. The **pkt_abort_l[i]** signal is shared among all ports connected to the same parallel bus segment [i].

The F_BIT and C_VBIT control bits in OPM{j} enable limiting the 21340-AB port address filtering level.

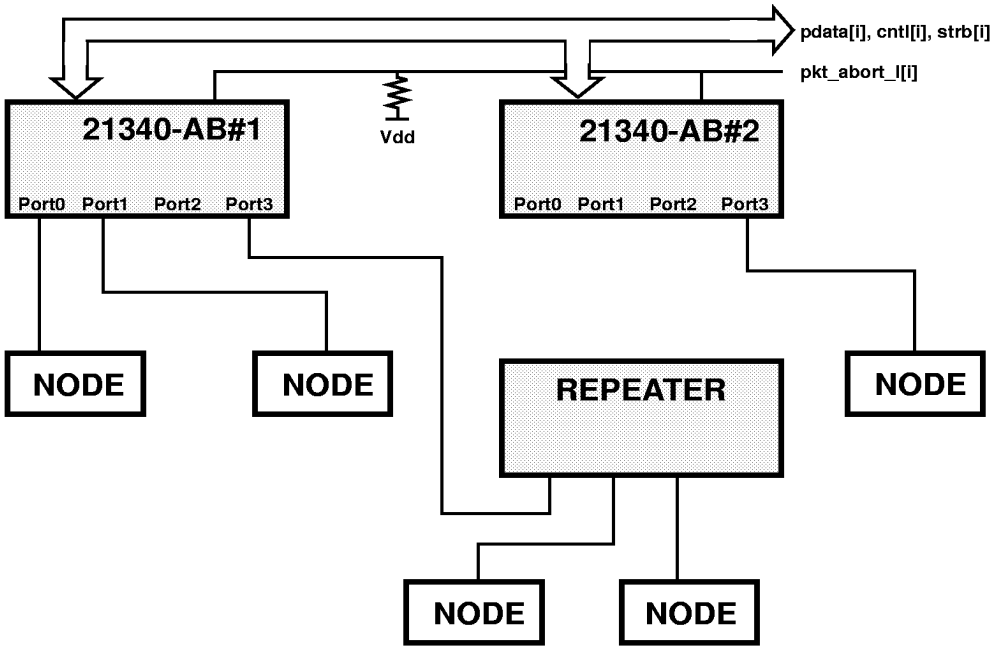
Table 1 summarizes the filtering levels available in a 21340-AB port.

Table 1 Port Filtering Levels

Aggression Level	F_bit	V_bit	Filtering Operation	Notify Other Ports (Asserts pkt_abort_l[i])
High	0	1	Pass only packets destined to the remote node.	Yes
Medium	1	1	Filter out only packets for which **pkt_abort_l[i]** is asserted.	Yes
Low	1	0	Filter out only packets for which **pkt_abort_l[i]** is asserted.	No

Figure 3 illustrates a network configuration in which one of the 21340-AB ports on a segment is connected to multiple nodes.

Figure 3 Internal Address Filtering with Multiple Nodes



Port0 and Port1 of device 21340-AB#1 are connected to single remote nodes, respectively. Port3 of device 21340-AB#1 is connected to multiple remote nodes.

1.5.6 External Address Lookup Table

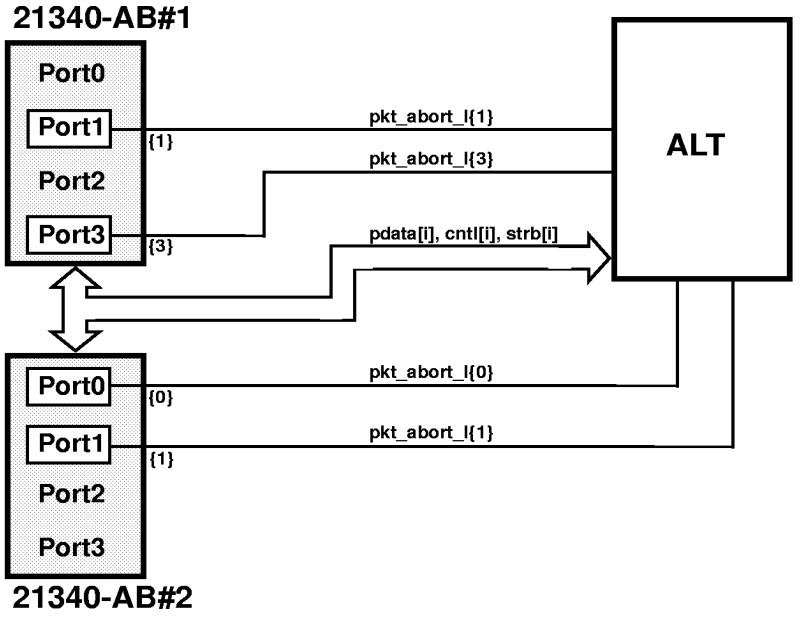
The 21340-AB allows the user to add an external Address Lookup Table (ALT) logic unit in order to further enhance system performance. When operating with an external ALT, the internal address filtering mechanism should be disabled (clear_v_bit control bit in the OPM{j} register is set), and the external ALT mode bit enabled (External_ALT_Enabled control bit in the MTC register is set).

In this mode, the ports' **pkt_abort_l{j}** signals are utilized as outputs from the ALT unit to all 21340-AB ports. The ALT decodes the destination address of the broadcast packet and compares it to the content of the address table it maintains. If a match occurs, the ALT asserts the **pkt_abort_l{j}** signal within the first loaded 16 bytes to ports that the broadcast packet is not addressed to.

If the **pkt_abort_l{j}** signal assertion is detected after the first 16-byte time, the port ignores it and transmits the loaded packet.

Figure 4 shows a segment with an external ALT. The ALT recognizes the destination address and compares it to the remote nodes' addresses, which it maintains in its local lookup table. It then asserts the **pkt_abort_l{j}** signals of the ports that are not connected to the destination remote node.

Figure 4 Address Filtering Using an External ALT



1.5.7 MII Port Interface

Each of the 21340-AB ports implements a fully compliant IEEE 802.3u media-independent interface (MII), providing a direct connection to a PHY device located on the same board, or on a daughtercard, or to a cable (similar to an AUI connection).

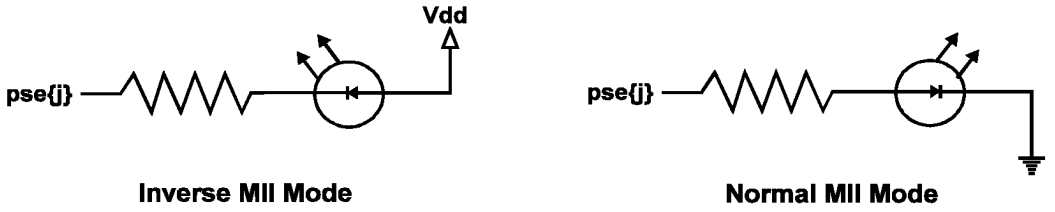
In addition, each of the 21340-AB ports implements an inverse MII interface that enables a direct glueless connection to any 802.3u MII MAC device. When initialized to work in the inverse mode of operation, the 21340-AB device can be

used as a simple, low-cost, off-the-shelf component for directly connecting commercial MAC devices or switching cores to the 21340-AB parallel bus segments via a standard MII interface without requiring any glue logic or PHY device. See Figure 9.

The 21340-AB port is set to the normal or inverse mode upon hardware reset, according to the configuration of the components connected to the **pse{j}** pins. When a resistor and an optional LED are connected between the **pse{j}** and **Vdd**, port{j} is initialized to work in the inverse MII mode of operation. When a register and an optional LED are connected between **pse{j}** and **Vss**, port{j} is initialized to work in the standard MII mode of operation.

A special internal circuit senses the polarity of **pse{j}** during hardware reset and adjusts the **pse{j}** LED driver accordingly. Figure 5 shows the **pse{j}** configurations for selecting normal and inverse MII modes.

Figure 5 pse{j} Normal and Inverse MII Mode



While operating in the normal or Iinverse MII mode of operation, each of the 21340-AB ports can operate in either a 10-Mb/s or 100-Mb/s data transfer rate.

- 100-Mb/s Operation

  The port's MII operates in nibble mode with a clock rate of 25 MHz.

- 10-Mb/s Operation

  The port's MII operates in nibble mode with a clock rate of 2.5 MHz.

The port should be connected to a segment configured to operate at the same data transfer rate. Connecting a port to a segment operating in another data transfer rate may lead to UNPREDICTABLE behavior and data corruption.

1.5.8 100BASE-TX SYM Interface Mode of Operation

The 100BASE-TX SYM interface is an alternative to the standard MII interface between the MAC and the PHY device. It provides a lower-level interface and therefore enables the use of lower cost SYM PHY devices. The SYM interface

provides a direct unframed 5-bit interface to the physical medium attachment (PMA) layer. Data is exchanged between the MAC and the PHY device at a 25-MHz clock rate. Since only one of the interfaces, SYM or MII, is active at a certain time, their pins are multiplexed.

The 100BASE-TX SYM interface is selected by setting the PCS control bit in JBR{j} register, and by setting the port to work at 100-Mb/s data transfer rate (setting the appropriate bits in MTC<31:28> register). The port should be connected to a segment operating at the same 100-Mb/s data transfer rate. Table 2 lists the mapping of the pins.

Table 2 MII and SYM Interface Pin Mapping

MII Interface	SYM Interface
mii_cs_tclk	**sym_tclk**
mii_cs_txen	**sym_txd<4>**
mii_cs_txd<3:0>	**sym_txd<3:0>**
mii_cs_rclk	**sym_rclk**
mii_cs_rxd<3:0>	**sym_rxd<3:0>**
mii_clsn	**sym_rxd<4>**
mii_dv	Status indicator LED
mii_cs_errr	Has no meaning in this mode
mii_crs	**sd**

1.5.9 Serial Management Interface

The serial management interface is used for control, status, and statistic registers access. It is also used for management access to an MII PHY device if one is connected to the port. The serial management interface is composed of the following four pins:

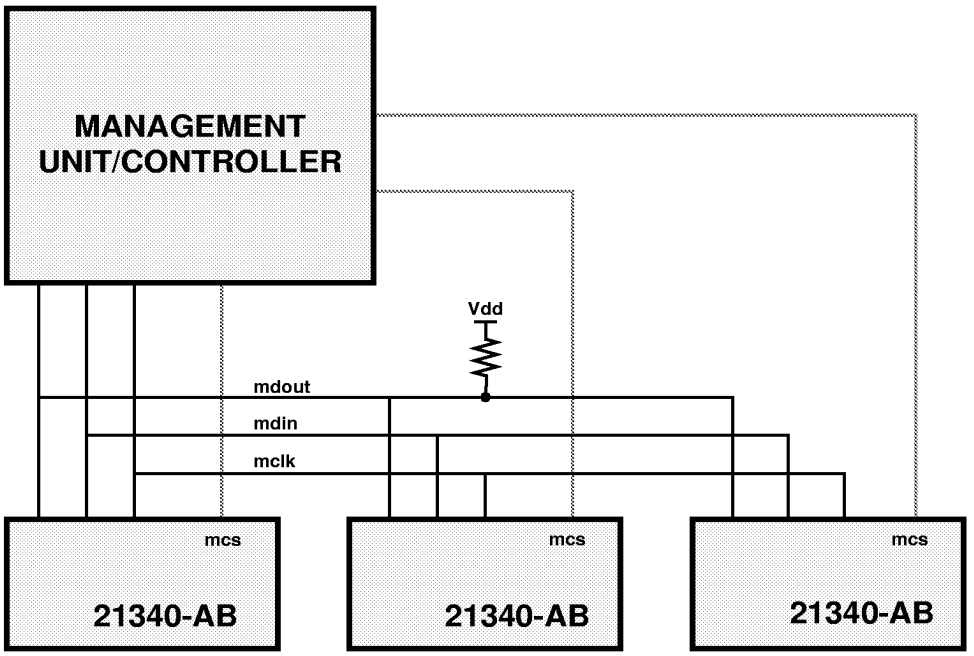
- **mclk**
  Used as a clock. All other management interface pins are synchronized to this pin. The **mclk** pin should be active during CSR access.
- **mcs**
  A unique chip-select line for each 21340-AB in an application. It is used to choose which 21340-AB device is currently accessed.

- **mdin**
  Data-in. The management entity drives the CSR's address and data on this pin.
- **mdout**
  Data-out. When reading a CSR, the 21340-AB drives the read data on this pin.

The **mclk**, **mdin**, and **mdout** signals can be shared by all 21340-AB devices. All 21340-AB devices in the system have these pins connected together in parallel, except the **mcs** signal. The **mcs** signal is unique for each 21340-AB device.

Figure 6 shows a typical configuration of the serial management interface signals.

Figure 6 Serial Management Interface Configuration



1.5.9.1 Read and Write Operations

When the management entity wants to access a register in one of the 21340-AB devices, it activates **mclk**. After two clock cycles, the management entity asserts the **mcs** line and drives the following bits on **mdin**:

op_code — First bit driven. "0" indicates that the management entity is writing; "1" indicates that the management entity is reading.

port_id — The number of the port that the accessed register is related to. Access to a register that is implemented only once in the 21340-AB should be done with port_id set to 0.

Next, the management entity drives 8 bits of address, according to the accessed register's internal address, and then drives 32 bits of data. For a read operation, the management entity waits for a start bit 0 to be driven on the **mdout** line for one full **mclk** cycle. In the next cycle the 21340-AB will drive the data, read from the register, on **mdout**. For a write operation, the management entity drives 32 bits of data following the register offset field.

After the last bit is driven, the management deasserts **mcs** line and drives another two cycles of **mclk** before it may deactivate the clock. If the **mcs** line is deasserted in the middle of an access, the access is aborted. See Sections 3.5.3 to 3.5.5.

1.5.9.2 MII PHY Device Access

Management of the local PHY device is done through the **mdc** and **mdio** pins per port. The 21340-AB provides the management entity with two methods for accessing the MII PHY registers: an indirect access method and a direct access method.

The indirect access method of driving these pins is done through the MTC register. The management entity may access all four MII PHY devices connected to the same 21340-AB at the same time. The values of the appropriate bits of the MTC register are reflected over the MII management pins.

Table 3 describes the 4 bits per each MII PHY device in the MTC register.

Table 3 MTC Register Functions

MTC Register	Description
Clock	Directly connected to **mdc** pin.
I/O Direction	Determines **mdio** pin direction: 0 – output 1 – input
Data-In	Samples **mdio** pin every **clk** cycle when **mdio** is set for input.
Data-Out	Drives data on the **mdio** pin every **clk** cycle when **mdio** is set for output.

The direct access mode shortens the time required for accessing the MII PHY device registers. The **mdc** and **mdio** pins are connected directly to the **mclk**, **mdin**, and **mdout** pins. Setting this mode is done by setting the DAE control bit in the MTC register.

When direct access mode is enabled, the management entity performs the following tasks:

- Writes the DAD and DAP control bits in the MTC register with the direct access direction and the accessed port number
- Asserts the **mcs** pin while keeping the **mclk** pin at a 0 level for at least 40 ns
- Toggles the **mclk** pin and either drives data on **mdin**, or samples **mdout** according to the access direction

To complete accessing the MII PHY device registers, the management entity:

- Drives **mclk** to 0 for at least 60 ns
- Deasserts the **mcs** pin
- Holds **mclk** at 0 for at least 60 ns after deassertion of **mcs**

Deasserting the **mcs** pin will reset the DAE bit in the MTC register.

1.5.10 Isolation Functions

The 21340-AB supports three defined repeater isolation functions of link unstable, partitioning, and receive jabber. When the 21340-AB port is in isolation, it ceases to receive and load packets. It resets the transmit path to flush the loaded packets and continues to monitor the line until the isolation is over. Each isolation function can be disabled by setting the appropriate control bits in the OPM{j}, JBR{j}, and CCC{j} registers.

Table 4 describes the 21340-AB isolation functions.

Table 4 21340-AB Isolation Functions

Isolation Function	Description
Link Unstable	Occurs when the carrier-integrity-isolation is enabled and one of the following conditions occur: - Two consecutive false-carrier events - A false-carrier event longer than 450–500 bit-times - A link-failed event - Hardware (HW) or software (SW) reset The port does not receive or transmit any packets during the isolation. The isolation is over when the link is stable and the 21340-AB port detects either no activity of 33,000 bit-times or a valid carrier of at least 450 bit-times, preceded by an idle time of 64–84 bit-times.
Partitioning	Occurs when the port attempts to transmit and the number of consecutive collisions, without any successful activity in between, exceeds the predefined limit. The isolation is over on a successful transmission or reception of more than 64 bytes.
Receive Jabber	Defined as a too long receive carrier (more than 40,960–45,056 bit-times). During isolation the port does not receive or transmit any packets. The isolation is over after the carrier drops.

1.5.11 Management Support

The 21340-AB device presents network statistics, error and abnormal events directly, by using the 21340-AB onchip event flags and statistic counters, and indirectly, by appending the received packet's status information to the packet broadcasted on the parallel bus segment.

Each 21340-AB port has its own set of snapshot and event flags: flags that provide a snapshot of the 21340-AB current operation state and flags that provide an indication that an event has occurred.

Table 5 lists the 21340-AB port snapshot and event flags with their functions.

Table 5 21340-AB Port Event Flags

Flags	Description
	Snapshot Flags
Auto partitioning	Indicates whether a port is currently partitioned.
Jabber	Indicates whether a port is in jabber state.
Link unstable	Indicates whether a port is in link unstable isolation state.
Backpressure	Indicates whether a port is in backpressure state.
Administration	Indicates whether a port is in a stopped state.
Flow control	Indicates whether a credit-based flow-control link has been identified.
Scrambler lock	Indicates that the descrambler is locked to the input data signal while the port is configured to work in SYM interface mode.
Link failed	Indicates that a link failed event is detected.
No grant	Indicates that a grant was not issued to the port at least 0.33 seconds after the port's request for parallel bus segment ownership.
	Event Flags
Auto partitioning	Indicates that a port has been partitioned.
Jabber isolation	Indicates that a port has been in jabber state.
Link unstable isolation	Indicates that a port has been in link unstable isolation.
Late collision	Indicates that a transmit late collision event has been detected. Late collision causes a packet abort (no retransmission attempts).
Short carrier	Indicates that a short carrier event has been detected.
Transmit underflow	Indicates that an error in 21340-AB transmit operation has occurred. The Tx_FIFO has been emptied during transmission.
Receive underflow	Indicates that an internal error has occurred in the 21340-AB port's receive operation. The Rx_FIFO has been full.
Link failed flag	Indicates that a link-failed event has been detected.

Each port implements a complete set of the RMON Ethernet statistic group MIB, Repeater statistic MIB, and Ethernet-like MIB.

Table 6 lists the 21340-AB port statistic counters and their function.

Table 6 21340-AB Statistic Counters *(Sheet 1 of 2)*

Register Description	Mnemonic
Statistic Counters[1]	
Overflow counter	ROVF[i]
Total octet counter low	ROCTL[i]
Total octet counter high	ROCTH[i]
Broadcast packet counter	RBCT[i]
Multicast packet counter	RMCT[i]
Undersized packet counter	RUSZ[i]
Oversized packet counter	ROSZ[i]
Fragment counter	RFRG[i]
Too long packets with CRC errors	RJBR[i]
Collision counter	RCOL[i]
64 octets packet counter	R64[i]
65 – 127 octets packet counter	R65TO127[i]
128 – 255 octets packet counter	R128TO255[i]
256 – 511 octets packet counter	R256TO511[i]
512 – 1023 octets packet counter	R512TO1023[i]
1024 – 1518 octets packet counter	R1024TO1518[i]
Alignment error packet counter	MALI[i]
CRC error packet counter	MCRC[i]
Single collision counter	MSCOL[i]
Multicollision counter	MMCOL[i]
Deferred transmission counter	MDEF[i]
Late collision counter	MLCOL[i]
Partition isolation counter	MPAR[i]
Carrier integrity isolation counter	MISO[i]

Table 6 21340-AB Statistic Counters *(Sheet 2 of 2)*

Register Description	Mnemonic
Symbol error counter	MSYE[i]
Source address changed counter	MSAC[i]
Last source address low	UAR1[i]
Last source address high	UAR2[i]
Short event counter	MSHE[i]
Good octets counter low	MOCTL[i]
Good octets counter high	MOCTH[i]
Receive jabber counter	MVLE[i]
Control packet counter	MCPKT[i]
Total transmitted octets – low	MTOCTL[i]
Total transmitted octets – high	MTOCTH[i]
Total transmitted packets	MTPKT[i]
Total transmitted control packets	MTCPKT[i]
Total filtered packets in transmit	MTFTR[i]

[1] Each statistic register has two addresses:

- Read-only address. Reading the register address does not affect the register's content.
- Clear-by-read address. Reading the register address clears the register's content.

Table 7 summarizes the 21340-AB counters, grouped according to function.

Table 7 21340-AB Counters Summary *(Sheet 1 of 4)*

Name	21340-AB Registers
RMON MIB Counters	
etherStatsDropEvents	ROVF
etherStatsOctets	ROCTH × 100000000h + ROCTL
etherStatsPkts	RUSZ + RFGR + R64 + R65TO127 + R128TO255 + R256TO511 + R512TO1023 + R1024TO1518 + RJBR + ROSZ
etherStatsBroadcastPkts	RBCT
etherStatsMulticastPkt	RMCT
etherStatsCRCAlignErrors	MALI + MCRC
etherStatsUndersizePkts	RUSZ
etherStatsOversizePkts	ROSZ
etherStatsFragments	RFRG
etherStatsJabbers	RJBR
etherStatsCollisions	RCOL + MLCOL
etherStatsPkts64Octets	R64
etherStatsPkts65to127Octets	R65TO127
etherStatsPkts128to255Octets	R128TO255
etherStatsPkts256to511Octets	R256TO511
etherStatsPkts512to1023Octets	R512TO1023
etherStatsPkts1024to1518Octets	R1024TO1518
Repeater MIB Counters (RFC1516)	
rptrMonitorPortReadableFrames	R64 + R65TO127 + R128TO255 + R256TO511 + R512TO1023 + R1024TO1518 - MALI - MCRC
rptrMonitorPortReadableOctets	MOCTH × 100000000h + MOCTL
rptrMonitorPortFCSErrors	MCRC
rptrMonitorPortAlignmentErrors	MALI
rptrMonitorPortFrameTooLongs	MJBR + MOSZ
rptrMonitorPortShortEvents	MSHE

Table 7 21340-AB Counters Summary *(Sheet 2 of 4)*

Name	21340-AB Registers
rptrMonitorPortRunts	MFRG + RUSZ
rptrMonitorPortCollisions	RCOL + MLCOL
rptrMonitorPortLateEvents	MLCOL
rptrMonitorPortVeryLongEvents	MVLE
rptrMonitorPortDataRateMismatches	Not applicable
rptrMonitorPortAutoPartitions	MPAR
rptrMonitorPortTotalErrors	MCRC + MALI + ROSZ + RJBR + MSHE + MLCOL + MVLE
rptrAddrTrackNewLastSrsAddress	UAR1, UAR2
rptrAddrTrackSourceAddrChanges	MSAC
Ethernet-Like MIB Counters (RFC1643)	
dot3StatsAlignmentErrors	MALI
dot3StatsFCSErrors	MCRC
dot3StatsSingleCollisionFrames	MSCOL
dot3StatsMultipleCollisionFrames	MMCOL
dot3StatsSQETestErrors	Not applicable
dot3StatsDeferredTransmissions	MDEF
dot3StatsLateCollisions	MLCOL
dot3StatsExcessiveCollisions	Not applicable
dot3StatsInternalMACTransmitErrors	Not applicable
dot3StatsCarrierSenseErrors	Not applicable
dot3StatsFrameTooLongs	RJBR+ROSZ
dot3StatsInternalMACReceiveErrors	Not applicable
MAC Entity Managed Object Class (IEEE Std 802.3)	
aFrameTransmittedOK	MTPKT
aSingleCollisionFrames	MSCOL
aMultipleCollisionFrames	MMCOL

Table 7 21340-AB Counters Summary *(Sheet 3 of 4)*

Name	21340-AB Registers
aFrameReceivedOK	R64 + R65TO127 + R128TO255 + R256TO511 + R512TO1023 + R1024TO1518 - MALI - MCRC
aFrameCheckSequenceErrors	MCRC
aAlignmentErrors	MALI
aOctetsTransmittedOK	MTOCTH × 100000000h + MTOCTL
aFramesWithDeferredXmissions	MDEF
aLateCollisions	MLCOL
aFrameAbortedDueToXSColls	Not applicable
aFrameLostDueToIntMACXmitError	Not applicable
aCarrierSenseError	Not applicable
aOctetsReceivedOK	MOCTH × 100000000h + TOCTL
aFrameLostDueToIntMACRcvError	Not applicable
aMulticastFrameXmittedOK	Not implemented
aBroadcastFramesXmittedOK	Not implemented
aFrameWithExcessiveDeferral	Not applicable
aMulticastFrameReceivedOK	RMCT
aBroadcastFrameReceivedOK	RBCT
alnRangeLengthErrors	Not implemented
aOutOfRangeLengthField	Not implemented
aFrameTooLongErrors	RJBR+BOSZ
Repeater Managed Object Class (IEEE Std 802.3)	
aReadableFrames	R64 + R65TO127 + R128TO255 + R256TO511 + R512TO1023 + R1024TO1518 - MALI - MCRC
aReadableOctets	MOCTH × 100000000h + MOCTL
aFrameCheckSequenceErrors	MCRC
aAlignmentErrors	MALI
aFrameTooLong	ROSZ + RJBR

Table 7 21340-AB Counters Summary *(Sheet 4 of 4)*

Name	21340-AB Registers
aShortEvents	MSHE
aRunts	RUSZ + RFRG
aCollisions	RCOL + MLCOL
aLateEvents	MLCOL
aVeryLongEvents	MVLE
aDataRateMismatches	Not applicable
aAutoPartitions	MPAR
aIsolates	MISO
aSymbolErrorDuringPacket	MSYE
aLastSourceAddress	UAR1, UAR2
aSourceAddressChanges	MSAC

The statistical information of each received packet is appended to it, following broadcast of the packet's data onto the parallel bus segment.

The statistical information is 5 bytes long and contains the following information about the packet:

- The receiving port identification number
- The receiving 21340-AB chip identification number
- The packet's length in bytes
- Indications of:
  - CRC error
  - Alignment error
  - MII or a SYM error
  - Packet longer than the legal Ethernet packet
  - Packet longer than 1600 bytes
  - 802.3 or Ethernet packet
  - Multicast or unicast packet
  - Runt packet (shorter than the minimum valid packet)

1.5.11.1 Interrupt Mechanism

The 21340-AB is capable of informing the management entity about various events occurring during run time, using its interrupt mechanism.

The 21340-AB's interrupt is asserted whenever one or more unmasked interrupt events are asserted. It is deasserted when all unmasked interrupt events are deasserted.

Interrupt events are divided into three event groups based on their functionality:

- The error group includes the following events:
  - Rx_FIFO overflow condition
  - Tx_FIFO underflow condition
  - Short carrier event
  - Late collision event
  - No grant issue to port
  - Link change direction
- The informative group includes notification events:
  - Carrier integrity isolation
  - Receive jabber isolation
  - Partitioning isolation
  - Flow-control identification, process failed notification
  - Flow-control identification, process succeeded
- The service group includes all statistic counters' overflow interrupt events

The 21340-AB device provides the management entity with a dedicated status register that enables quick identification of the interrupt source port and its nature. Following identification, the management entity can easily identify and handle the cause of the interrupt.

1.5.12 LED Status Indicators

The 21340-AB device supports three status LEDs. Table 8 describes the LEDs and their pin connections.

Table 8 21340-AB LED Support

LED	Pin Number	Description
Activity LED	120, 97 143, 166	Turns on when either transmit or receive activity is detected. This signal is stretched to ensure that a signal activity event will be seen. If the activity is continuous, the LED will appear permanently on.
Link Integrity LED	108, 83 150, 127	Turns on when link integrity status is OK.
Isolation Indication LED	175, 176 177, 178	Turns on when the 21340-AB isolates the network port. Port isolation occurs when the port either enters into partition state, detects link unstable or receive jabber condition, performs remote node autodetection, or is in a stopped state.

Note: The 21340-AB port MII interface mode provides only the isolation indication LED. Status indications for link integrity and link activity are provided by the MII PHY device.

1.5.13 Reset Commands

The following commands are available to reset the 21340-AB:

- **Hardware reset**
  Asserts the **rst** line for a minimum duration of 0.64 µs (16 **clk** cycles) to initialize the hardware. After the reset command, the 21340-AB should be allowed to stabilize for at least 50 **clk** cycles before the first transaction.
- **Software reset**
  Sets the SWR{j} register through the 21340-AB management interface port to initiate a software reset. After a software reset, the management entity should poll the STR{j} register's STOP_RX and STOP_TX status bits before initiating a new write operation to that port.

For either reset command, the **clk** and **mii_cs_clk/sym_tclk{j}** clocks should be operating normally. At the end of the reset sequence, both receive and transmit paths of the 21340-AB are halted. It is possible to issue successive reset commands.

1.5.14 Joint Test Action Group Test Logic

This section describes the joint test action group (JTAG) test logic and associated registers (instruction, bypass, and boundary scan) as implemented in the 21340-AB.

Note: To understand the description of the 21340-AB JTAG test logic in this section, the reader should be familiar with the IEEE 1149.1 standard.

1.5.14.1 Test Access Port Controller

The test access port (TAP) controller interprets IEEE 1149.1 protocols received on the 21340-AB's four test pins. The following table lists the 21340-AB test pins and their functions.

Pin Name	Description
tms	Test mode select
tclk	Test clock
tdi	Test data and instruction in
tdo	Test data out

All inputs and output data are synchronous to the test clock (**tclk**). The input signals (**tdi**, **tms**) are clocked into the test logic at the rising edge of **tclk** while the output signal (**tdo**) is clocked on the **tclk** falling edge.

The TAP controller interprets IEEE 1149.1 protocols received on the **tms**, **tclk** and **tdi** pins. It generates clocks and control signals to control the operation on the test logic. The control signals switch **tdi** and **tdo** between the instruction and test data registers.

1.5.14.2 JTAG Test Registers

In the JTAG test logic, three registers are implemented through the 21340-AB's pads:

- Instruction register
- Bypass register
- Boundary-scan register

Table 9 describes the types of test instructions that are interpreted by the 21340-AB's JTAG test logic.

Table 9 21340-AB JTAG Test Instructions

Instruction	Operation Code	Description
Bypass Instruction	111	Used to provide a minimum length serial path between the **tdi** and **tdo** pins of the 21340-AB when the test logic in the 21340-AB is bypassed. When power is applied, JTAG test logic resets to bypass mode.
Extest Instruction	000	Allows testing of the 21340-AB board-level interconnections. Test data is shifted into the boundary-scan register on the 21340-AB and then transferred in parallel to the output pins.
Sample/Preload Instruction	001	Allows scanning of the boundary-scan register without causing interference to the normal operation of the onchip system logic.
Continuity Instruction	110	Allows checking of the connectivity of the 21340-AB pins on the board. This instruction causes all output pins of the 21340-AB to drive the value 0.
Tristate Instruction	101	Causes all output pins of the 21340-AB to be tristated.

1.5.15 Internal Arbitration Scheme Support

When the internal onchip arbiter function is enabled, a token is circulated between all ports sharing the same segment. When a 21340-AB port receives a token, it has the permission to broadcast its received packet(s) onto the parallel segment. If the port has stored packets in its Rx_FIFO and it receives a token, it captures the token and broadcasts its stored packets until one of the following conditions occurs:

- The port broadcasted a full burst of packets, as defined by the its burst-size control bits.
- The port has no more packets stored in its Rx_FIFO.
- The destination ports cannot load a new packet.

When a port completes its broadcast operation, or does not have any stored packets in its Rx_FIFO, it passes the token on to the next inline port sharing the same segment [i].

Because the burst size can be defined separately for each of the 21340-AB ports, the user can initialize some of the 21340-AB ports with higher priority by programming them to have a larger allowed burst size.

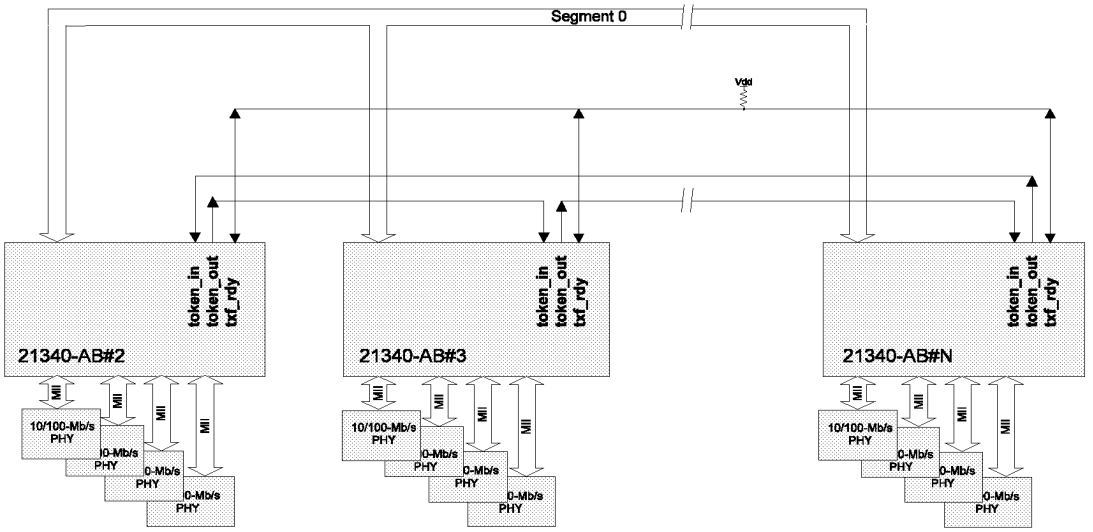
Table 10 lists the interface provided for the internal arbitration scheme.

Table 10 Internal Arbiter Interface

Pin Name	Description
token_out[i]	Together with the **token_in[i]** pin, creates a ring connectivity between all ports sharing segment[i]. Grants the following 21340-AB port connected to segment[i] to broadcast a burst of its received packets in its turn.
token_in[i]	Together with the **token_out** pin, creates a ring connectivity between all ports sharing segment[i]. Grants the current 21340-AB port connected to segment[i] to broadcast a burst of its received packets in its turn. The port captures and holds the token while broadcasting. When the port completes its broadcast operation, it passes the token on to the next port connected to segment[i], through the **token_out[i]** pin.
txf_rdy[i]	Shared among all ports connected to segment[i]. Asserted by the 21340-AB port to inform the broadcasted port that it does not have enough space to load a new packet from the parallel packet to its Tx_FIFO. When the broadcasting port detects the **txf_rdy[i]** signal assertion, it completes the current packet's broadcast operation, and then passes the token on to the next inline port sharing the same segment.
ext_arb	Should be connected to **Vss**.

Figure 7 shows the internal arbitration scheme connectivity for one segment.

Figure 7 Internal Arbitration Scheme Connectivity



1.5.16 External Arbitration Scheme Support

When the external arbiter mode of operation is enabled, the arbitration scheme is performed by an external arbiter. It determines which of the ports on a parallel bus segment is granted the next opportunity to broadcast its received packet.

The arbitration scheme should avoid deadlocks. Table 11 lists the interface provided for the arbiter.

Table 11 External Arbiter Interface

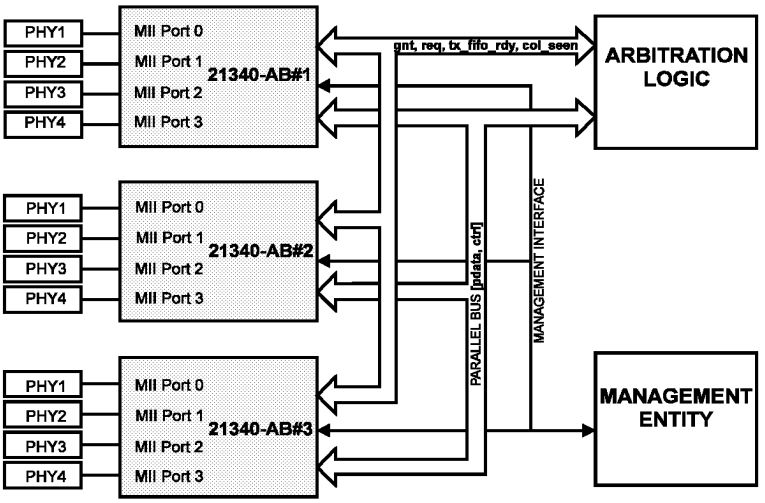
Pin Name	Description
tx_fifo_rdy{j}	Indicates that the 21340-AB port is able to load a new packet for transmission.
req{j}	Indicates the 21340-AB port's request to broadcast a received packet.
col_seen{j}	When set, indicates that the port has experienced a collision during transmission when the **req{j}** line was not asserted. (Optional for advanced arbitration algorithms.)
gnt{j}	When asserted, notifies the 21340-AB port that it owns the **pdata[i]**, **cntl[i]**, and **strb[i]** lines, and may broadcast its received packet.
ext_arb	Should be connected to **Vdd**.

In addition to the hooks listed in Table 11, other factors must be considered:

- The arbiter should not grant a port unless all target ports' **tx_fifo_rdy** signals are asserted.
- The **gnt** signal should be set for at least 10 **clk** cycles during broadcast and deasserted no later than one **clk** cycle after termination of broadcast. (See Figure 28.)

In a segmented network, each network segment should have its own arbitration logic. Each arbiter should be notified of the ports grouped in its segment and update the ports dynamically. Figure 8 shows the external arbitration connectivity.

Figure 8 External Arbitration Connectivity



1.6 Network Applications

This section describes the use of the 21340-AB in various network applications.

1.6.1 21340-AB in Port Switch Applications

A port switch is a cost-optimized approach for addressing the need of additional network bandwidth while maintaining the flexibility of adding, removing or moving users between segments.

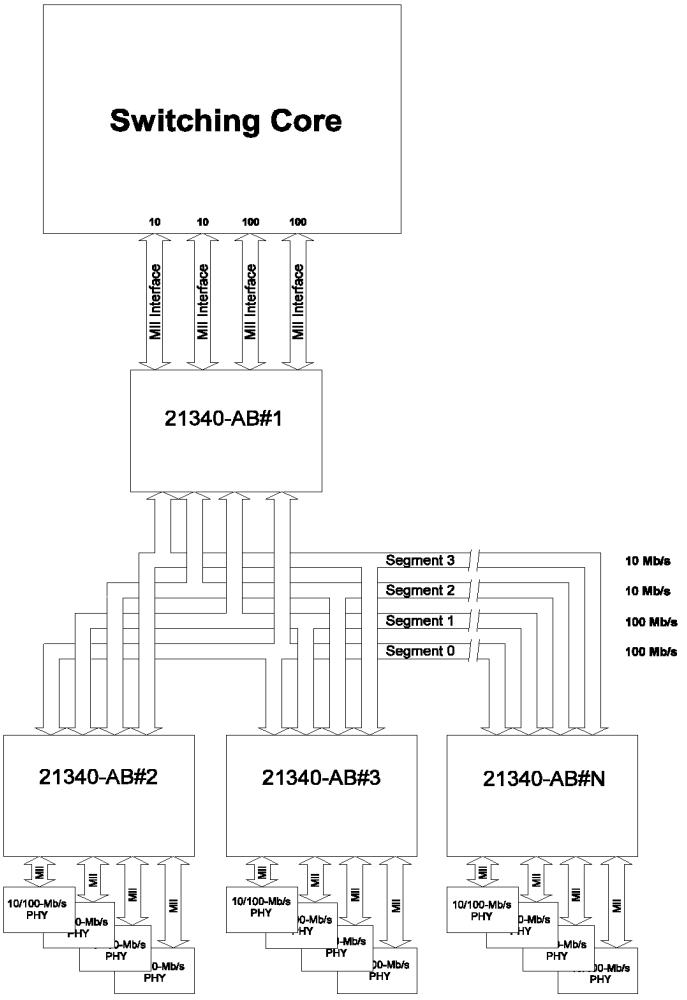
A port switch can balance a network by assigning the bandwidth-hungry users to a less utilized or even separate segment while assigning other users, with lower bandwidth requirements, to share a different segment. As network conditions change, users can be moved from one segment to another, thus balancing the network. A port switch also provides excellent support for workgroup security and VLAN-based applications. Users can share applications, data, and server without being interfered by users on other segments.

A 10/100-Mb/s dual-rate port enables the assignment of ports to segments, based on their data transfer rate and bandwidth allocation requirements. When a port is ready to migrate to 100 Mb/s, it is reallocated by a software command to a 100-Mb/s segment. No other modification in the wiring closet is required.

Features unique to the 21340-AB enable it to improve the performance of port switch applications, lower the solution cost, and reduce development time-to-market while maintaining the powerful features of the switching core.

Figure 9 shows how the 21340-AB building block can be configured in a port switch application. The switch engine in Figure 9 has four ports, each connected to the 21340-AB system's four independent segments using the 21340-AB#1 device. The 21340-AB#1, which is configured to work in the inverse mode of operation, provides a simple, low-cost, glueless connection between the switch MII interface and the 21340-AB parallel bus segments.

Figure 9 21340-AB in a 10/100-Mb/s Switch Application



The 21340-AB improves network throughput compared to a standard multisegment repeater. Collisions experienced on any of its ports do not propagate to other ports sharing the same segments and switching core. In addition, the 21340-AB filters out fragment packets, preventing them from being propagated in the network. The 21340-AB address filtering mechanism filters out intrasegment packets that otherwise would have been presented to the switching engine by a standard multisegment repeater.

The 21340 port's flow-control mechanism (backpressure or credit-based) ensures no packet loss. When the switch engine is congested, backpressure is applied only against the aggressive node. Other remote nodes in the network segment are not affected by the backpressure built-in operation.

The unique features of the 21340-AB (dual MII mode of operation, expandable and flexible internal arbitration scheme, and backpressure scheme) reduce port switch system cost and development time. In addition, the 21340-AB ports can be allocated to segments by a simple software command. This ability to move, add, or remove users from a segment, provides an excellent support for VLAN applications. Because ports can have different priorities by programming them to a larger packet's burst size while granted, there is greater flexibility in designing port switch-based applications.

1.6.2 21340-AB in 10/100 Dual-Rate Enhanced Repeater Applications

Figure 10 shows how 21340-AB building blocks can be configured in a non-SNMP-managed 10/100-Mb/s dual-rate enhanced repeater system. The management entity detects the local and remote PHY capabilities, initializes the 21340-AB ports' modes of operation appropriately, and then enables the ports.

Figure 10 21340-AB in Enhanced Repeater Application

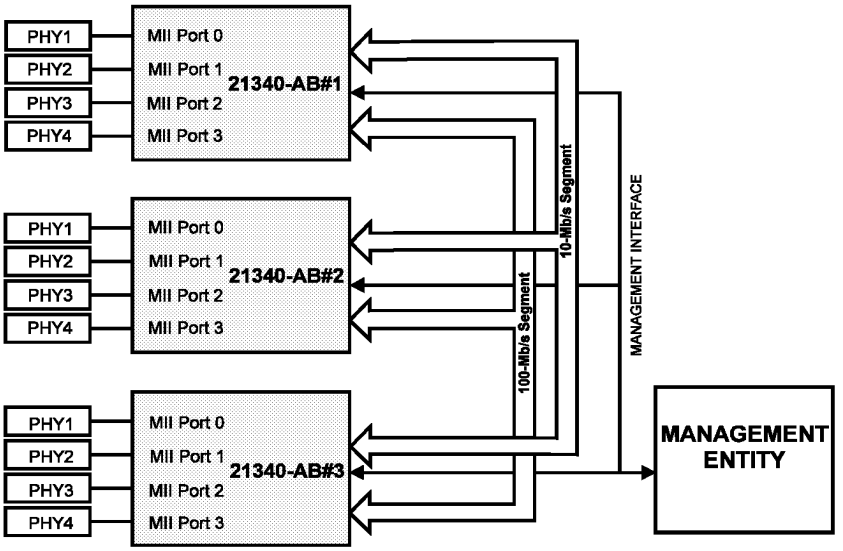
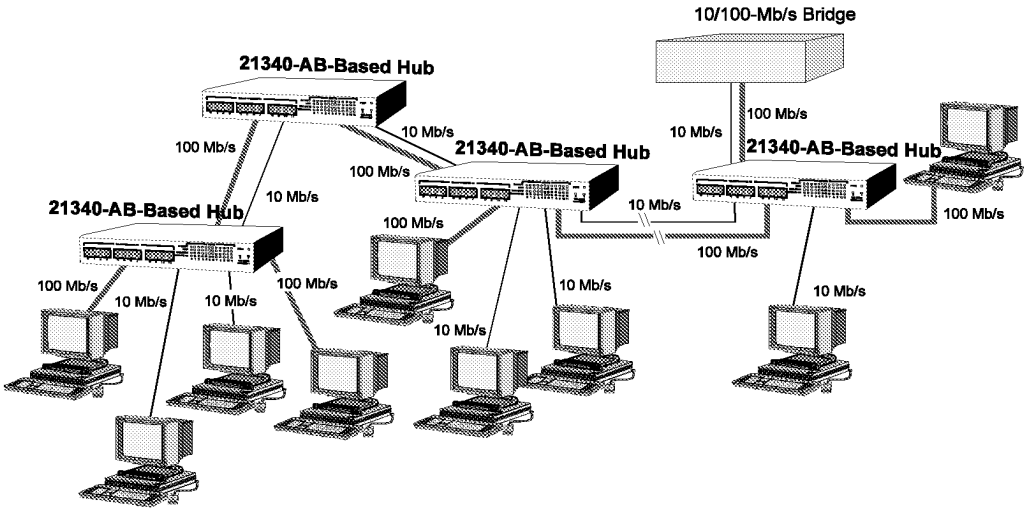


Figure 11 shows a network of 10/100-Mb/s dual-rate enhanced repeater systems that use 21340-AB building blocks. The network includes two segments: one operates at 10 Mb/s and the other operates at 100 Mb/s. A 10/100-Mb/s bridge device is used in order to connect between the 10-Mb/s and the 100-Mb/s segments.

When a remote node is changed from 10 Mb/s to 100 Mb/s, the management entity identifies the change through Auto-Negotiation. Based on this information, the management entity reassigns the port to the segment with the matching data transfer rate of 100 Mb/s. Upgrading remote nodes can occur gradually without changing the hardware.

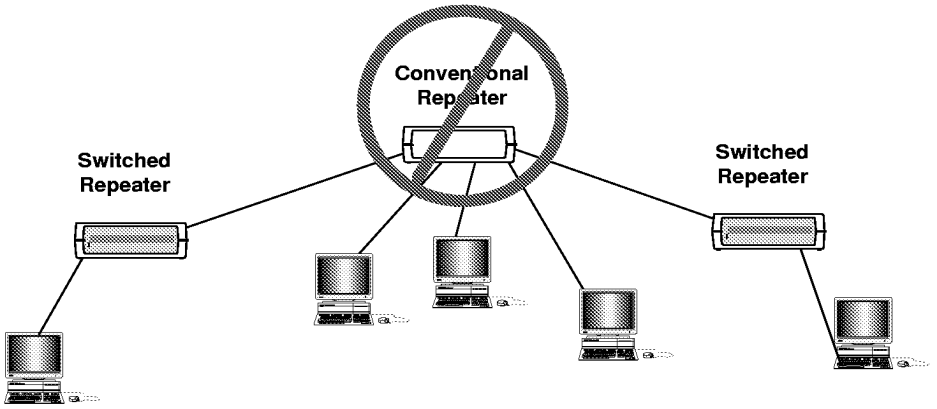
Figure 11 Low-Cost Migration from 10 Mb/s to 100 Mb/s



1.7 Limitations

It is not recommended to create a topology with conventional repeaters interleaved between 21340-AB-based repeaters because this may lead to degradation in performance. Figure 12 shows an example of the unrecommended topology.

Figure 12 Unrecommended Network Topology



1.8 Recommended PHY Devices

The 21340-AB implements a remote node autodetection scheme that detects if the remote node connected to a 21340-AB port is capable of using the 21340-AB flow-control scheme. Table 12 lists the capability requirements for the PHY devices.

Table 12 PHY Device Capability Requirements

Protocol	Interface	Capability
10BASE-T or 100BASE-TX	MII	Full-duplex support with Auto-Negotiation
100BASE-TX	SYM PHY	Full-duplex with **txen** pin
10BASE-T or 100BASE-T4	MII	Auto-Negotiation

Other PHY devices may require manual programming to establish 21340-AB-21340-AB flow-control connections.

1.9 Related Documents

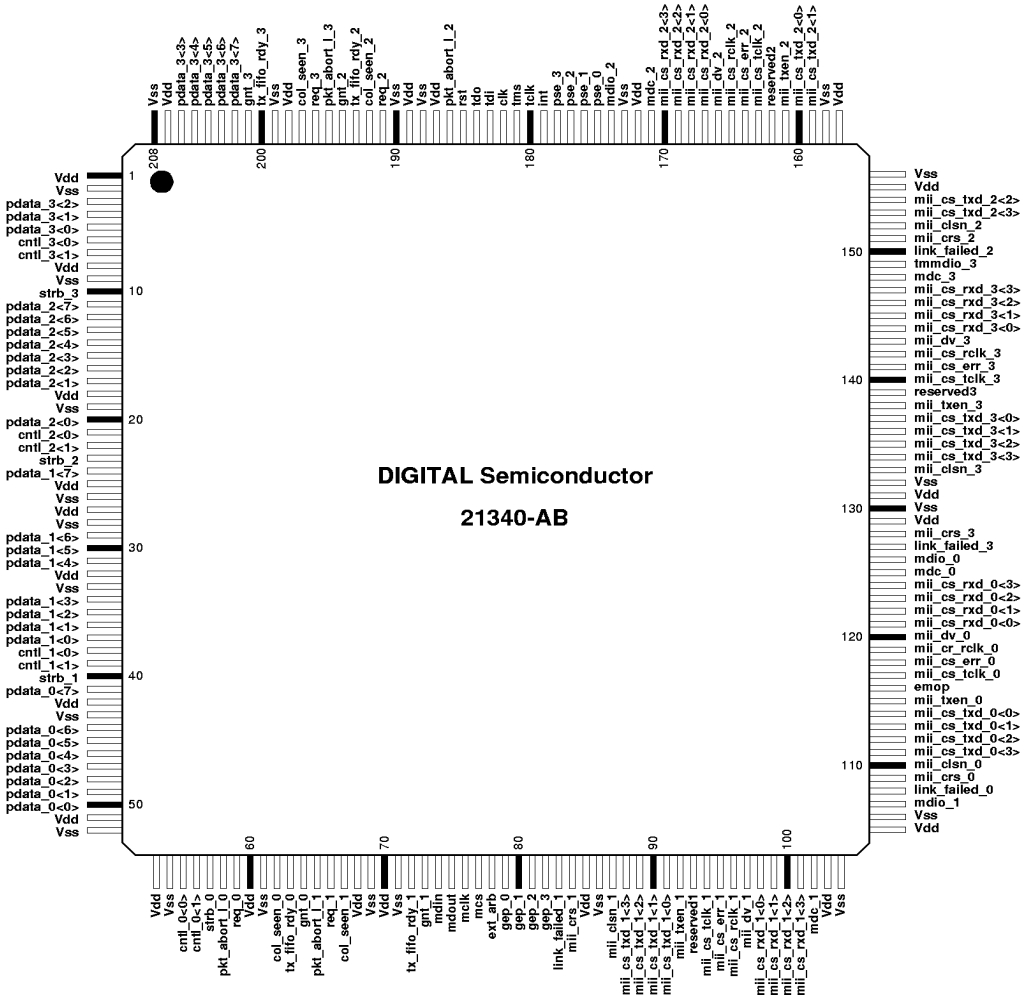
The 21340-AB design criteria meets the following specifications:

- *IEEE Standard 802.3u–1995 Supplement to ISO/IEC 8802-3:1993*
- *IETF Remote Network Monitoring (RMON) MIB (RFC 1757)*
- *IETF Repeater Device MIB (RFC 1516)*
- *IETF Ethernet-Like MIB (RFC 1643)*
- *IEEE Standard 1149.1 Test Access Port and Boundary Scan Architecture*

2 Pinout

The 21340-AB is packaged in a 208-pin plastic quad flat pack (PQFP). Figure 13 shows the 21340-AB pinout.

Figure 13 DIGITAL Semiconductor 21340-AB Pinout Diagram (Top View)



2.1 Signal List

Table 13 lists the 21340-AB's external signals and their associated pins.

Table 13 Pin/Signal List *(Sheet 1 of 3)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
ext_arb	78	**link_failed_1**	83	**mii_cs_err_0**	118
clk	182	**link_failed_2**	150	**mii_cs_err_1**	95
cntl_0<0>	55	**link_failed_3**	127	**mii_cs_err_2**	164
cntl_0<1>	56	**mclk**	76	**mii_cs_err_3**	141
cntl_1<0>	38	**mcs**	77	**mii_cs_rclk_0**	119
cntl_1<1>	39	**mdc_0**	125	**mii_cs_rclk_1**	96
cntl_2<0>	21	**mdc_1**	102	**mii_cs_rclk_2**	165
cntl_2<1>	22	**mdc_2**	171	**mii_cs_rclk_3**	142
cntl_3<0>	6	**mdc_3**	148	**mii_cs_rxd_0<0>**	121
cntl_3<1>	7	**mdin**	74	**mii_cs_rxd_0<1>**	122
col_seen_0	62	**mdio_0**	126	**mii_cs_rxd_0<2>**	123
col_seen_1	67	**mdio_1**	107	**mii_cs_rxd_0<3>**	124
col_seen_2	192	**mdio_2**	174	**mii_cs_rxd_1<0>**	98
col_seen_3	197	**mdio_3**	149	**mii_cs_rxd_1<1>**	99
gep_0	79	**mdout**	75	**mii_cs_rxd_1<2>**	100
gep_1	80	**mii_clsn_0**	110	**mii_cs_rxd_1<3>**	101
gep_2	81	**mii_clsn_1**	87	**mii_cs_rxd_2<0>**	167
gep_3	82	**mii_clsn_2**	152	**mii_cs_rxd_2<1>**	168
gnt_0	64	**mii_clsn_3**	133	**mii_cs_rxd_2<2>**	169
gnt_1	73	**mii_crs_0**	109	**mii_cs_rxd_2<3>**	170
gnt_2	194	**mii_crs_1**	84	**mii_cs_rxd_3<0>**	144
gnt_3	201	**mii_crs_2**	151	**mii_cs_rxd_3<1>**	145
link_failed_0	108	**mii_crs_3**	128	**mii_cs_rxd_3<2>**	146
mii_cs_rxd_3<3>	147	**mii_txen_3**	138	**pdata_3<3>**	206

Table 13 Pin/Signal List *(Sheet 2 of 3)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
mii_cs_tclk_0	117	**pdata_0<0>**	50	**pdata_3<4>**	205
mii_cs_tclk_1	94	**pdata_0<1>**	49	**pdata_3<5>**	204
mii_cs_tclk_2	163	**pdata_0<2>**	48	**pdata_3<6>**	203
mii_cs_tclk_3	140	**pdata_0<3>**	47	**pdata_3<7>**	202
mii_cs_txd_0<0>	114	**pdata_0<4>**	46	**pkt_abort_l_0**	58
mii_cs_txd_0<1>	113	**pdata_0<5>**	45	**pkt_abort_l_1**	65
mii_cs_txd_0<2>	112	**pdata_0<6>**	44	**pkt_abort_l_2**	186
mii_cs_txd_0<3>	111	**pdata_0<7>**	41	**pkt_abort_l_3**	195
mii_cs_txd_1<0>	91	**pdata_1<0>**	37	**int**	179
mii_cs_txd_1<1>	90	**pdata_1<1>**	36	**pse_0**	175
mii_cs_txd_1<2>	89	**pdata_1<2>**	35	**pse_1**	176
mii_cs_txd_1<3>	88	**pdata_1<3>**	34	**pse_2**	177
mii_cs_txd_2<0>	160	**pdata_1<4>**	31	**pse_3**	178
mii_cs_txd_2<1>	159	**pdata_1<5>**	30	**req_0**	59
mii_cs_txd_2<2>	154	**pdata_1<6>**	29	**req_1**	66
mii_cs_txd_2<3>	153	**pdata_1<7>**	24	**req_3**	196
mii_cs_txd_3<0>	137	**pdata_2<0>**	20	**emop**	116
mii_cs_txd_3<1>	136	**pdata_2<1>**	17	**reserved1**	93
mii_cs_txd_3<2>	135	**pdata_2<2>**	16	**reserved2**	162
mii_cs_txd_3<3>	134	**pdata_2<3>**	15	**reserved3**	139
mii_dv_0	120	**pdata_2<4>**	14	**rst**	185
mii_dv_1	97	**pdata_2<5>**	13	**strb_0**	57
mii_dv_2	166	**pdata_2<6>**	12	**strb_1**	40
mii_dv_3	143	**pdata_2<7>**	11	**strb_2**	23
mii_txen_0	115	**pdata_3<0>**	5	**strb_3**	10
mii_txen_1	92	**pdata_3<1>**	4	**tclk**	180
mii_txen_2	161	**pdata_3<2>**	3	**tdi**	183
tdo	184	**Vdd**	85	**Vss**	43

Table 13 Pin/Signal List *(Sheet 3 of 3)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
tms	181	**Vdd**	103	**Vss**	52
tx_fifo_rdy_0	63	**Vdd**	105	**Vss**	54
tx_fifo_rdy_1	72	**Vdd**	129	**Vss**	61
tx_fifo_rdy_2	193	**Vdd**	131	**Vss**	69
tx_fifo_rdy_3	200	**Vdd**	155	**Vss**	71
Vdd	1	**Vdd**	157	**Vss**	86
Vdd	8	**Vdd**	172	**Vss**	104
Vdd	18	**Vdd**	187	**Vss**	106
Vdd	25	**Vdd**	189	**Vss**	130
Vdd	27	**Vdd**	198	**Vss**	132
Vdd	32	**Vdd**	207	**Vss**	156
Vdd	42	**Vss**	2	**Vss**	158
Vdd	51	**Vss**	9	**Vss**	173
Vdd	53	**Vss**	19	**Vss**	188
Vdd	60	**Vss**	26	**Vss**	190
Vdd	68	**Vss**	28	**Vss**	199
Vdd	70	**Vss**	33	**Vss**	208

2.2 Signal Descriptions

Table 14 provides a functional description of each of the 21340-AB signals. These signals are listed alphabetically.

The following terms describe the 21340-AB pinout:

- **MII/SYM** Indicates dual function pins that are multiplexed to provide different functions depending on the connection of a given 21340-AB port to either an MII PHY or SYM PHY device.
- **[i]** Indicates the division of the 21340-AB parallel bus into four identical segments.
- **{j}** Indicates a signal of a single 21340-AB port.

The following abbreviations are used in Table 14:

I = Input

O = Output

OD = Open Drain

I/O = Input/Output

P = Power

Table 14 Signal Descriptions *(Sheet 1 of 9)*

Signal	Type	Description	Number of Pins
clk	I	25-MHz external clock. All 21340-ABs and external arbiter logic use this clock.	1
cntl[3:0]<1:0>	I/O	Control lines. These signals determine the cycle and meaning of the data that appears on **pdata[i]** according to the following encoding:	8
		cntl<1:0> pdata<7:0>	
		11b Idle mode. A preamble pattern is forced on the data lines as default. Achieved by pull-up and pull-down resistors.	
		01b Starting delimiter. In parallel, the granted port broadcasts preamble and SFD patterns onto **pdata[i]**.	
		00b Data valid. The data packet is broadcast on the data bus by the granted 21340-AB port.	
		10b Ending delimiter. When the data packet transfer is completed, the granted port broadcasts the following data on **pdata[i]**: chip_id, port_id, and receive_status.	
		Note: The **cntl** lines are common to all the connected 21340-ABs and the external arbiter. When not driven, the **cntl** lines are externally pulled up to 11b (Idle).	
col_seen{j}	O	Significant only in the external arbiter mode. Asserted by a 21340-AB port when a collision is detected during its attempt to transmit on the physical media while the port's **req{j}** line is not asserted. This signal is deasserted when the 21340-AB port asserts its **req{j}** signal.	4

Table 14 Signal Descriptions *(Sheet 2 of 9)*

Signal	Type	Description	Number of Pins
emop	I	Enhanced mode of operation. When connected to **Vss**, all the 21340-AB added features and functions relative to the 21340 device are masked. When connected to **Vdd**, all 21340-AB added features are enabled.	1
ext_arb	I	When **emop** is connected to **Vdd**, the **ext_arb** selects the internal or the external arbitration schemes to be used between the 21340-AB ports. • When **ext_arb** is connected to **Vss**, the 21340-AB uses its internal onchip arbitration scheme. • When **ext_arb** is connected to **Vdd**, the 21340-AB uses an external arbitration scheme. When **emop** is connected to **Vss**, **ext_arb** should be connected to **Vdd**.	1
gep{j}	I/O	General-purpose pins. These pins can be configured by software (MTC register) to be either input or output pins.	4
gnt{j}/token_in[i]	I	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Input from an external arbiter. Grants a 21340-AB port ownership of the parallel bus segment[i] to broadcast a received packet. **Onchip arbiter mode**. Together with the **token_out[i]**, creates a loop connectivity between all ports connected to the same segment [i]. Grants the 21340-AB port connected to segment [i] to broadcast in its turn a burst of its received packets, based on the permitted port's burst size. The port holds the token while broadcasting. When the port completes its broadcast operation, it passes the token to the next port connected to segment [i] through the **token_out[i]** pin.	4

Table 14 Signal Descriptions *(Sheet 3 of 9)*

Signal	Type	Description	Number of Pins
int	OD	Interrupt pin activated when **emop** is connected to **Vdd**. Asserted whenever one or more unmasked interrupt events are asserted. Deasserted when all unmasked interrupt events are cleared. Can be shared by all 21340-AB devices on the same system. An external pull-up resistor is required.	1
link_failed{j}/ link_ok{j}	I/O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Performs input function. Asserted by the PHY device when a link-failed condition occurs. If this pin is not supported by the PHY device, it should be connected to **Vss**. PCS mode: Performs output function. Provides a LED control that indicates signal detection activity and that the port's scrambler has been locked.	4
mclk	I	Serial management clock. The clock range is from 0 to 12.5 MHz.	1
mcs	I	Serial management chip select. Asserted by the management unit to select a 21340-AB for CSR access.	1
mdc{j}	O	MII management data clock. Used as timing reference for MII management information transfer on the **mdio** line between each MII port and its connected PHY device.	4
mdin	I	Serial management data in. Serial input for management command/data. The **mdin** signal is common for all connected 21340-ABs.	1
mdio{j}	I/O	MII management data input/output. Used to transfer serial control and status information between each MII port and its connected PHY device.	4
mdout	O	Serial management data out. Serial output for management data output. The **mdout** signal should be common for all 21340-ABs connected together in a system. When not driven, it should be pulled up to 1 by an external device.	1

Table 14 Signal Descriptions *(Sheet 4 of 9)*

Signal	Type	Description	Number of Pins
mii_clsn{j}/ sym_rxd{j}<4>	I	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Collision detected. Asserted by the PHY device upon detection of collision on the media. PCS mode: Receive data. Together with **mii_cs_rxd{j}<3:0>/sym_rxd{j}<3:0>,** provides five parallel lines of data in symbol form. This data should be synchronized to the **mii/sym_rclk**.	4
mii_crs{j}/sd{j}	I	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Functions as the carrier sense indicator and is asserted by the PHY device when the media is active. PCS mode: Functions as the signal detect indicator. It is controlled by an external physical medium dependent (PMD) device.	4
mii_cs_err{j}	I	Receive error. Significant only when the 21340-AB is connected to the MII PHY device. MII mode: Driven by the PHY device, indicating that a coding error or other error has been detected by that PHY device. **Note:** When initialized to the PCS mode, this pin should be connected to Vss.	4
mii_cs_rclk{j}/ sym_rclk{j}	I	Receive clock. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Provides the timing reference for the transfer of **mii_dv{j}, mii_cs_rxd{j}**, and **mii_cs_err{j}** signals. Supports either 2.5 MHz for 10-Mb/s data transfer rate, or 25 MHz for 100-Mb/s data transfer rate. PCS mode: Provides the timing reference for the transfer of **sym_rxd<4:0>**.	4

Table 14 Signal Descriptions *(Sheet 5 of 9)*

Signal	Type	Description	Number of Pins
mii_cs_rxd{j}<3:0>/ sym_rxd{j}<3:0>	I	Receive data. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Driven by the PHY device. MII mode: Synchronous with **mii_cs_rclk{j}**. While **mii_dv** is deasserted, the **mii_cs_rxd** has no meaning. PCS mode: Receive data's four least significant bits. Together with **mii/clsn{j}/sym_rxd{j}<4>,** provides five parallel lines of data in SYM form.	16
mii_cs_tclk{j}/ sym_tclk{j}	I	Transmit clock. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Supports either 25-MHz or 2.5-MHz clock supplied by the PHY device. This clock must always be active. MII mode: Provides the timing reference for the **mii_txen{j}** and **mii_cs_txd{j}** signals. PCS mode: Provides the timing reference for the transfer of **sym_txd<4:0>**.	4
mii_cs_txd{j}<3:0>/ sym_txd{j}<3:0>	O	Transmit data. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Driven by the 21340-AB port. MII mode: Synchronous with **mii_cs_tclk{j}**. PCS mode: Receive data's four least significant bits. Together with **mii_txen{j}/sym_txd{j}<4>**, these signals provide the five parallel lines of data in SYM form. This data is synchronized to the **mii/sym_tclk** signal.	16
mii_dv{j}/ link_activity{j}	I/O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Receive data valid. Driven by the PHY when receive data is present on the **mii_cs_rxd{j}** lines. The **mii_dv{j}** pin is deasserted at the end of the packet. PCS mode: Serves as a status pin indicating either receive or transmit activity. Can be used to drive a status LED.	4

Table 14 Signal Descriptions *(Sheet 6 of 9)*

Signal	Type	Description	Number of Pins
RESERVED<3:1>	—	RESERVED. It is recommended to connect these pins to **gnd** through a resistor.	4
mii_txen{j}/ sym_txd{j}<4>	O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII Mode: Functions as transmit enable. The signal indicates that a transmission is active on the MII port to an external PHY device. PCS mode: Functions as the transmit data high-order bit. Together with the other four data transmit lines, **sym_txd{j}<3:0>**, provides the five parallel data lines for SYM-form data. The data is synchronized to the rising edge of the **sym_tclk** signal.	4
pdata[i]<7:0>	I/O	Data bus. Data is transferred on the parallel bus at 100 Mb/s or 10 Mb/s, depending on the data rate selected for the port (12.5 MHz or 1.25 MHz). The parallel bus comprises four identical segments, each having an 8-bit **pdata** datapath. The **pdata[i]** lines are used for packet broadcasts, including starting/ending packet delimiter information among 21340-AB ports connected to the same segment. When it is not driven, the pattern forced on the **pdata[i]** lines by external pull-up and pull-down devices is 01010101b.	32
pkt_abort_l{j}	I/OD	Packet abort bit. Determines if the current loaded packet of the port should be aborted before transmission. Its functionality is controlled by the OPM{j} register. Internal address filtering mode: Shared among all ports connected to the same segment. When not driven, it is pulled up by an external pull-up device. External address filtering mode: Per-port inputs driven by the external ALT.	4

Table 14 Signal Descriptions *(Sheet 7 of 9)*

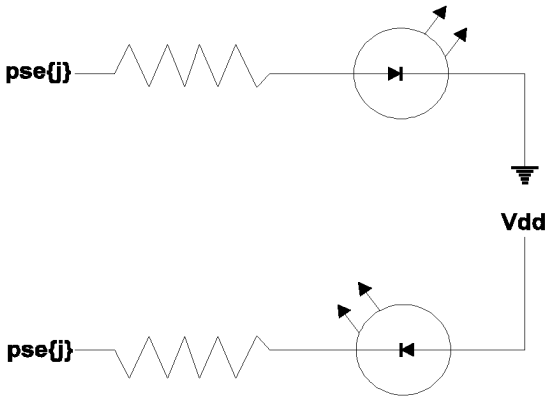
Signal	Type	Description	Number of Pins
pse{j}	I/O	Status pins that provide a LED output to indicate when port [j] is isolated; activated when **emop** is connected to **Vss**. LED and resistor are connected between the **pse{j}** pin and the ground or **Vdd**. If LEDs are not needed for the application, a resistor should be connected. A 1 kΩ resistor is recommended. Upon power-up reset, the **pse{j}** pin is used to set port [j]'s MII interface mode of operation either to the normal mode where it is connected to an MII PHY device, or to the inverse mode of operation, connecting it to the MII MAC device. Following power-up reset, the pins become LED status indicators. The **pse{j}** actual value for setting the port [j]'s MII mode of operation depends on the configuration of the LED and resistor components. When the LED and resistor are connected between the **pse{j}** pin and **Vdd**, port [j] is initialized to an inverse MII mode of operation. When the LED and resistor are connected between the **pse{j}** and ground, the port [j] is initialized to the normal MII mode of operation. A special circuit senses the polarity and adjusts the **pse{j}** driver logic to turn the LED on or off.  	4

Table 14 Signal Descriptions *(Sheet 8 of 9)*

Signal	Type	Description	Number of Pins
req{j}/token_out[i]	O	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Asserted by a 21340-AB port to indicate that a packet has been received from the media. **Onchip arbiter mode**. Together with the **token_in[i]**, creates a loop connectivity between all ports connected to the same segment [i]. Grants the following 21340-AB port connected to segment [i] to broadcast in its turn a burst of its received packets, based on the permitted port's burst size.	4
rst	I	21340-AB reset. Resets the 21340-AB to its initial state. This signal must be asserted for at least 16 **clk** cycles. When asserted, all **pdata[i]**, **cntl[i]**, and **strb[i]** signals are put into tristate.	1
strb[i]	I/O	Either 12.5-MHz or 1.25-MHz clock sourced by the granted port. It is synchronized to the **pdata** bus. All other 21340-AB devices sharing the same segment use this signal to sample the **pdata** and **cntl** buses. Shared among all 21340-AB devices and management logic that share the same segment. When the **pdata** bus is in Idle state, the **strb** signal is pulled down to 0 by an external pull-down device.	4
tclk	I	JTAG clock shifts state information and test data into and out of the 21340-AB during JTAG test operations. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 0.	1
tdi	I	JTAG data in is used to serially shift test data and instructions into the 21340-AB during JTAG test operations. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 1.	1
tdo	O	JTAG data out is used to serially shift test data and instructions out of the 21340-AB during JTAG test operations.	1

Table 14 Signal Descriptions *(Sheet 9 of 9)*

Signal	Type	Description	Number of Pins
tms	I	JTAG test mode select. Controls operation of JTAG testing in the 21340-AB. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 1.	1
tx_fifo_rdy{j}/ txf_rdy[i]	O/OD	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Asserted by the 21340-AB port when it is able to load a full, new packet from the parallel bus to its Tx_FIFO. **Onchip arbiter mode**. Shared among all ports. Asserted (pulled down) by the 21340-AB port to notify the broadcasted port that it does not have enough space to load a new packet from the parallel bus to its Tx_FIFO. When not driven, it is pulled up to 1 by external pull-up device.	4

2.3 Signals Grouped by Function

The following sections list the various signals of the 21340-AB grouped together in their respective functional interfaces.

2.3.1 Parallel Interface

Table 15 and Table 16 provide functional descriptions of the data path and arbiter signals in the 21340-AB parallel interface. These signals are listed alphabetically.

The following terms describe the 21340-AB pinout:

MII/SYM Indicates dual-function pins that are multiplexed to provide different functions depending on the connection of a given 21340-AB port to either an MII PHY or SYM PHY device.

[i] Indicates the division of the 21340-AB parallel bus into four identical segments.

{j} Indicates a signal of a single 21340-AB port.

The following abbreviations are used in Table 15 and Table 16:

I = Input

O = Output

OD = Open Drain

I/O = Input/Output

P = Power

Table 15 Parallel Interface – Data Path Signals *(Sheet 1 of 2)*

Signal	Type	Description	Number of Pins
clk	I	25-MHz external clock. All 21340-ABs and arbiter logic use this clock.	1
cntl[i]<1:0>	I/O	Control lines. These signals determine the cycle and meaning of the data appearing on **pdata[i]** according to the following encoding: **cntl<1:0>** — **pdata<7:0>** 11b — Idle mode. A preamble pattern is forced on the data lines as default. Achieved by pull-up and pull-down resistors. 01b — Starting delimiter. In parallel, the granted port broadcasts preamble and SFD patterns onto **pdata[i]**. 00b — Data valid. The data packet is broadcast on the data bus by the granted 21340-AB port. 10b — Ending delimiter. When the data packet transfer is completed, the granted port broadcasts the following data on **pdata[i]**: chip_id, port_id, and receive_status. **Note**: The **cntl** lines are common to all the connected 21340-ABs and the arbiter. When not driven, the **cntl** lines are externally pulled up to 11b (Idle).	8
pdata[i]<7:0>	I/O	Data bus. Data is transferred on the parallel bus at 100 Mb/s or 10 Mb/s, depending on the data rate selected for the port (12.5 MHz or 1.25 MHz). The parallel bus comprises four identical segments, each having an 8-bit **pdata** data path. The **pdata[i]** lines are used for packet broadcasts, including starting/ending packet delimiter information among 21340-AB ports connected to the same segment. When it is not driven, the pattern forced on the **pdata[i]** lines by external pull-up and pull-down devices is 01010101b.	32

Table 15 Parallel Interface – Data Path Signals *(Sheet 2 of 2)*

Signal	Type	Description	Number of Pins
pkt_abort_l{j}	I/OD	Packet abort bit. Determines if the current loaded packet of the port should be aborted before transmission. Its functionality is controlled by the OPM{j} register. Internal address filtering mode: Shared among all ports connected to the same segment. When not driven, it is pulled up by an external pull-up device. External address filtering mode: Per-port inputs driven by the external ALT.	4
strb[i]	I/O	Either 12.5-MHz or 1.25-MHz clock sourced by the granted port. It is synchronized to the **pdata** bus. All other 21340-AB devices sharing the same segment use this signal to sample the **pdata** and **cntl** buses. Shared among all 21340-AB devices and management logic that share the same segment. When the **pdata** bus is in Idle state, the **strb** signal is pulled down to 0 by an external pull-down device.	4

Table 16 lists the signals used for arbitration control in the parallel interface.

Table 16 Parallel Interface – Arbiter Signals *(Sheet 1 of 2)*

Signal	Type	Function	Number of Pins
ext_arb	I	When **emop** is connected to **Vdd**, the **ext_arb** selects the internal or the external arbitration schemes to be used between the 21340-AB ports. • When **ext_arb** is connected to **Vss**, the 21340-AB uses its internal onchip arbitration scheme. • When ext_arb is connected to **Vdd**, the 21340-AB uses an external arbitration scheme. When **emop** is connected to **Vss**, **ext_arb** should be connected to **Vdd**.	1
col_seen{j}	O	Significant only in the external arbiter mode. Asserted by a 21340-AB port when a collision is detected during its attempt to transmit on the physical media while the port's **req{j}** line is not asserted. This signal is deasserted when the 21340-AB port asserts its **req{j}** signal.	4
gnt{j}/ token_in[i]	I	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Input from an external arbiter. Grants a 21340-AB port ownership of the parallel bus segment[i] to broadcast a received packet. **Onchip arbiter mode**. Together with the **token_out[i]**, creates a loop connectivity between all ports connected to the same segment [i]. Grants the 21340-AB port connected to segment [i] to broadcast in its turn a burst of its received packets, based on the permitted port's burst size. The port holds the token while broadcasting. When the port completes its broadcast operation, it passes the token to the next port connected to segment [i] through the **token_out[i]** pin.	4

Table 16 Parallel Interface – Arbiter Signals *(Sheet 2 of 2)*

Signal	Type	Function	Number of Pins
req{j}/ token_out[i]	O	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Asserted by a 21340-AB port to indicate that a packet has been received from the media. **Onchip arbiter mode**. Together with the **token_in[i]**, creates a loop connectivity between all ports connected to the same segment [i]. Grants the following 21340-AB port connected to segment [i] to broadcast in its turn a burst of its received packets, based on the permitted port's burst size.	4
tx_fifo_rdy{j}/ txf_rdy[i]	O/OD	Dual function pin, set by initializing the 21340-AB device to operate in either the external arbitration scheme or the onchip internal arbitration scheme. **External arbiter mode**. Asserted by the 21340-AB port when it is able to load a full, new packet from the parallel bus to its Tx_FIFO. **Onchip arbiter mode**. Shared among all ports. Asserted (pulled down) by the 21340-AB port to notify the broadcasted port that it does not have enough space to load a new packet from the parallel bus to its Tx_FIFO. When not driven, it is pulled up to "1" by external pull-up device.	4

2.3.2 Management Interface

Table 17 provides functional descriptions of the 21340-AB management interface signals. These signals are listed alphabetically.

The following abbreviations are used in Table 17:

I = Input

O = Output

OD = Open Drain

Table 17 Serial Management Interface Signals

Signal	Type	Function	Number of Pins
int	OD	Interrupt pin, activated when **emop** is connected to **Vdd**. Asserted whenever one or more unmasked interrupt events are asserted. Deasserted when all unmasked interrupt events are cleared. Can be shared by all 21340-AB devices on the same system. An external pull-up resistor is required.	1
mclk	I	Serial management clock. The clock range is from 0 to 12.5 MHz.	1
mcs	I	Serial management chip select. Asserted by the management unit to select a 21340-AB for CSR access.	1
mdin	I	Serial management data in. Serial input for management command/data. The **mdin** signal is common for all connected 21340-ABs.	1
mdout	O	Serial management data out. Serial output for management data output. The **mdout** signal should be common for all 21340-ABs connected together in a system. When not driven, it should be pulled up to 1 by an external device.	1

2.3.3 PHY Interface

Table 18 provides functional descriptions of the 21340-AB PHY interface signals. These signals are listed alphabetically.

The following terms describe the 21340-AB pinout:

MII/SYM Indicates dual-function pins that are multiplexed to provide different functions depending on the connection of a given 21340-AB port to either an MII PHY or SYM PHY device.

[i] Indicates the division of the 21340-AB parallel bus into four identical segments.

{j} Indicates a signal of a single 21340-AB port.

The following abbreviations are used in Table 18:

I = Input

O = Output

I/O = Input/Output

Table 18 PHY Interface Signals *(Sheet 1 of 4)*

Signal	Type	Function	Number of Pins
link_failed{j}/ link_ok{j}	I/O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Performs input function. Asserted by the PHY device when a link-failed condition occurs. If this pin is not supported by the PHY device, it should be connected to **Vss**. PCS mode: Performs output function. Provides a LED control that indicates signal detection activity and that the port's scrambler has been locked.	4
mdc{j}	O	MII management data clock. Used as timing reference for MII management information transfer on the **mdio** line between each MII port and its connected PHY device.	4
mdio{j}	I/O	MII management data input/output. Used to transfer serial control and status information between each MII port and its connected PHY device.	4

Table 18 PHY Interface Signals *(Sheet 2 of 4)*

Signal	Type	Function	Number of Pins
mii_clsn{j}/ sym_rxd{j}<4>	I	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Collision detected. Asserted by the PHY device upon detection of collision on the media. PCS mode: Receive data. Together with **mii_cs_rxd{j}<3:0>/sym_rxd{j}<3:0>,** provides five parallel lines of data in SYM form. This data should be synchronized to the **mii/sym_rclk**.	4
mii_crs{j}/sd{j}	I	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Functions as the carrier sense indicator and is asserted by the PHY device when the media is active. PCS mode: Functions as the signal detect indicator. It is controlled by an external physical medium dependent (PMD) device.	4
mii_cs_err{j}	I	Receive error. Significant only when the 21340-AB is connected to the MII PHY device. MII mode: Driven by the PHY device to indicate that a coding error or other error has been detected by that PHY device. **Note:** When initialized to the PCS mode, this pin should be connected to Vss.	4
mii_cs_rclk{j}/ sym_rclk{j}	I	Receive clock. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Provides the timing reference for the transfer of **mii_dv{j}, mii_cs_rxd{j}**, and **mii_cs_err{j}** signals. Supports either 2.5-MHz for 10-Mb/s data transfer rate, or 25-MHz for 100-Mb/s data transfer rate. PCS mode: Provides the timing reference for the transfer of **sym_rxd<4:0>**.	4

Table 18 PHY Interface Signals *(Sheet 3 of 4)*

Signal	Type	Function	Number of Pins
mii_cs_rxd{j}<3:0>/ sym_rxd{j}<3:0>	I	Receive data. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Driven by the PHY device. MII mode: Synchronous with **mii_cs_rclk{j}**. While **mii_dv** is deasserted, the **mii_cs_rxd** has no meaning. PCS mode: Receive data's four least significant bits. Together with **mii/clsn{j}/sym_rxd{j}<4>,** provides five parallel lines of data in SYM form.	16
mii_cs_tclk{j}/ sym_tclk{j}	I	Transmit clock. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Supports either 25-MHz or 2.5-MHz clock supplied by the PHY device. This clock must always be active. MII mode: Provides the timing reference for the **mii_txen{j}** and **mii_cs_txd{j}** signals. PCS mode: Provides the timing reference for the transfer of **sym_txd<4:0>**.	4
mii_cs_txd{j}<3:0>/ sym_txd{j}<3:0>	O	Transmit data. Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. Driven by the 21340-AB port. MII mode: Synchronous with **mii_cs_tclk{j}**. PCS mode: Receive data's four least significant bits. Together with **mii_txen{j}/sym_txd{j}<4>**, these signals provide the 5 parallel lines of data in SYM form. This data is synchronized to the **mii/sym_tclk** signal.	16

Table 18 PHY Interface Signals *(Sheet 4 of 4)*

Signal	Type	Function	Number of Pins
mii_dv{j}/ link_activity{j}	I/O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII mode: Receive data valid. Driven by the port's PHY when receive data is present on the **mii_cs_rxd{j}** lines. The **mii_dv{j}** pin is deasserted at the end of the packet. PCS mode: Serves as a status pin indicating either receive or transmit activity. Can be used to drive a status LED.	4
mii_txen{j}/ sym_txd{j}<4>	O	Dual-function pin depending on the connection of a 21340-AB port to either an MII PHY or a SYM PHY device. MII Mode: Functions as transmit enable. The signal indicates that a transmission is active on the MII port to an external PHY device. PCS mode: Functions as the transmit data high-order bit. Together with the other four data transmit lines, **sym_txd{j}<3:0>** provides the five parallel data lines for SYM-form data. The data is synchronized to the rising edge of the **sym_tclk** signal.	4

2.3.4 Miscellaneous Interface Signals

Table 19 describes several miscellaneous 21340-AB signals:

- Test access port signals (**tclk**, **tdi**, **tdo**, **tms**)
- General-purpose ports and LEDs (**gep**, **pse**)
- System signals (**rst**)

The following term describes the 21340-AB pinout:

{j} Indicates a signal of a single 21340-AB port.

The signals are listed in alphabetical order. The following abbreviations are used in Table 19:

I = Input

O = Output

I/O = Input/Output

Table 19 Miscellaneous Interface Signals *(Sheet 1 of 2)*

Signal	Type	Function	Number of Pins
gep{j}	I/O	General-purpose pins. These pins can be configured by software (MTC register) to be either input or output pins.	4
pse{j}	I/O	Status pins that provide a LED output to indicate when port [j] is isolated; activated when **emop** is connected to **Vss**. LED and resistor are connected between the **pse{j}** pin and the ground or **Vdd**. If LEDs are not needed for the application, a resistor should be connected. A 1 kΩ resistor is recommended. Upon power-up reset, the **pse{j}** pin is used to set port [j]'s MII interface mode of operation either to the normal mode where it is connected to an MII PHY device, or to the inverse mode of operation, connecting it to the MII MAC device. Following power-up reset, the pins become LED status indicators. The **pse{j}** actual value for setting the port [j]'s MII mode of operation depends on the configuration of the LED and resistor components. When the LED and resistor are connected between the **pse{j}** pin and **Vdd**, port [j] is initialized to an inverse MII mode of operation. When the LED and resistor are connected between the **pse{j}** and ground, the port [j] is initialized to the normal MII mode of operation. A special circuit senses the polarity and adjusts the **pse{j}** driver logic to turn the LED on or off.	4
rst	I	21340-AB reset. Resets the 21340-AB to its initial state. This signal must be asserted for at least 16 **clk** cycles. When asserted, all **pdata[i]**, **cntl[i]**, and **strb[i]** signals are put into tristate.	1

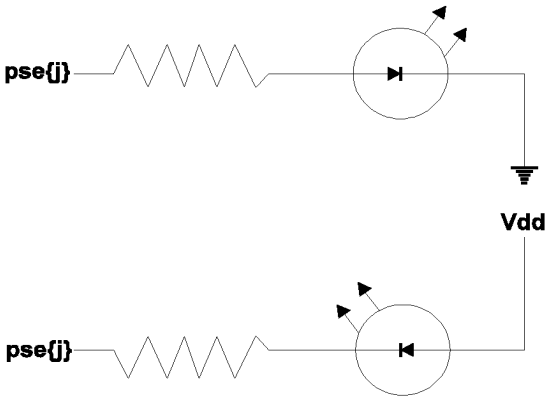


Table 19 Miscellaneous Interface Signals *(Sheet 2 of 2)*

tclk	I	JTAG clock shifts state information and test data into and out of the 21340-AB during JTAG test operations. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 0.	1
tdi	I	JTAG data in is used to serially shift test data and instructions into the 21340-AB during JTAG test operations. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 1.	1
tdo	O	JTAG data out is used to serially shift test data and instructions out of the 21340-AB during JTAG test operations.	1
tms	I	JTAG test mode select. Controls operation of JTAG testing in the 21340-AB. This pin should not be left unconnected. When the JTAG mechanism is not activated, this bit should be driven to 1.	1

3 Electrical Specifications

This section contains the electrical specifications for the 21340-AB.

3.1 Absolute Maximum Ratings

Table 20 lists the absolute maximum ratings.

Caution: Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21340-AB. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21340-AB.

Table 20 Absolute Maximum Ratings

Parameter	Minimum	Maximum
Storage temperature range	–55°C	125°C
Supply voltage **Vdd**	3.0 V	3.6 V
DC voltage on any pin	–0.5 V	5.5 V
EDS protection voltage	—	2000 V

3.2 Normal Operating Conditions

Table 21 lists the normal operating conditions.

Table 21 Normal Operating Conditions

Parameter	Minimum	Maximum
Operating temperature	0°C	70°C
Ambient temperature	0°C	70°C
Supply voltage **Vdd**	3.0 V	3.6 V

3.3 Supply Current and Power Dissipation

The supply current and power dissipation are estimates based on a network data rate of 100 Mb/s for MII.

Table 22 Supply Current and Power Dissipation

	Typical[1]		Maximum[2]	
Symbol	**Idd (mA)**	**Power (mW)**	**Idd (mA)**	**Power (mW)**
Normal Operation[3]	373	1230	469	1689

[1] **Vdd** = 3.3 V, Ta = 25°C
[2] **Vdd** = 3.6 V, Ta = 0°C
[3] Measured with a capacitive load of 30 pF on all output and I/O pins

3.4 AC and DC Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the 21340-AB.

The ac specifications are defined for a capacitive load of 30 pF.

3.4.1 Parallel and Arbiter Interface Operating Specifications

This section describes the timing characteristics of the signals in the parallel and external arbiter interfaces.

Table 23 lists the functional operating dc parameters for the 21340-AB under normal operating conditions. The normal operating conditions are specified in Table 21.

Note: In Table 23, currents into the chip (current-sinking) are positive and currents from the chip (current-sourcing) are negative (–).

Table 23 DC Specifications

Symbol	Definition	Minimum	Maximum	Unit	Notes
V_{il}	Low-level input voltage	-0.5	0.8	V	—
V_{ih}	High-level input voltage	2.0	5.5	V	—
V_{ol}	Low-level output voltage	—	0.55	V	1
V_{oh}	High-level output voltage	2.4	—	V	—
I_{oz}	Tristate leakage current	—	±70	µA	2
C_{in}	Input capacitance	—	—	pF	—
C_o	I/O or output-only pin capacitance	5	8	pF	3

[1] Iol =6.0 mA
[2] 0.5 V < Vin < 2.7 V
[3] Parameter design guarantee

3.4.1.1 clk-to-strb Delay

Figure 14 shows the timing characteristics and required measurements for the delay between **clk** leading edge and **strb** float-to-active events.

Figure 14 clk-to-strb Delay Timing Diagram

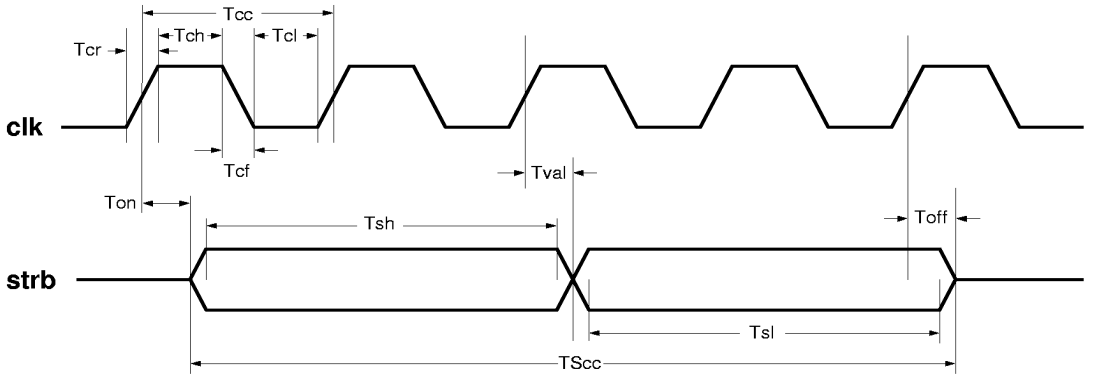


Table 24 lists specifications for the **clk**-to-**strb** delay.

Table 24 clk-to-strb Delay Specifications

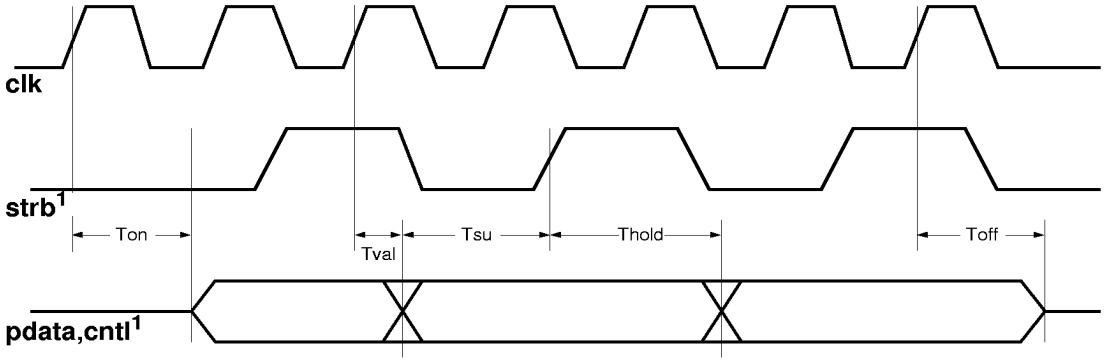
Symbol	Definition	Minimum	Maximum	Typical	Unit
Tcc	**clk** cycle time	39.996	40.004	40	ns
Tch	**clk** high time	16	—	—	ns
Tcl	**clk** low time	16	—	—	ns
Tcr	**clk** rise time	—	4	4	ns
Tcf	**clk** fall time	—	4	4	ns
Tval	**clk**-to-**strb** valid time	7	26	—	ns
Ton	Float-to-active delay from **clk**	7	35	—	ns
Toff	Active-to-float delay from **clk**		35	—	ns
TScc	**strb**[1] cycle time	79.992t[2]	80.008t	80t	ns
TScr	**strb** rise time	—	4	4	ns
TScf	**strb** fall time	—	4	4	ns
Tsh	**strb** high time	33	—	—	ns
Tsl	**strb** low time	33	—	—	ns

[1] When not driven, the **strb** pin is pulled down to 0 by an external pull-down device.
[2] t = 1 for 100-Mb/s operation; t = 10 for 10-Mb/s operation.

3.4.1.2 clk-to-pdata, cntl Delay

Figure 15 shows the timing characteristics and required measurements for the delay between **clk** leading edge and **pdata** or **cntl** float-to-active/active-to-float events (output).

Figure 15 clk-to-pdata, cntl Delay Timing Diagram



[1] Segment output.

Table 25 defines the specifications for the **clk**-to-**pdata, cntl** delay.

Table 25 clk-to-pdata, cntl Delay Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tval	**clk** to signal valid delay	2	26	ns
Ton	Float-to-active delay from **clk**	2	35	ns
Toff	Active-to-float delay from **clk**	—	35	ns
Tsu	**pdata**[1] and **cntl**[2] output signals stable before **strb** assertion (calculated)	20	—	ns
Thold	**pdata** and **cntl** output signals stable after **strb** assertion (calculated)	15	—	ns

[1] When not driven, the **pdata** lines are pulled to 01010101b by external pull-up and pull-down devices.
[2] When not driven, the **cntl** lines are pulled up to 11b by external pull-up devices.

3.4.1.3 strb-to-pdata, cntl Synchronization

Figure 16 shows the timing characteristics and required measurements for the synchronization between **strb** leading edge and **pdata** or **cntl** float-to-active/ active-to-float events (input).

Figure 16 strb-to-pdata, cntl Synchronization Timing Diagram

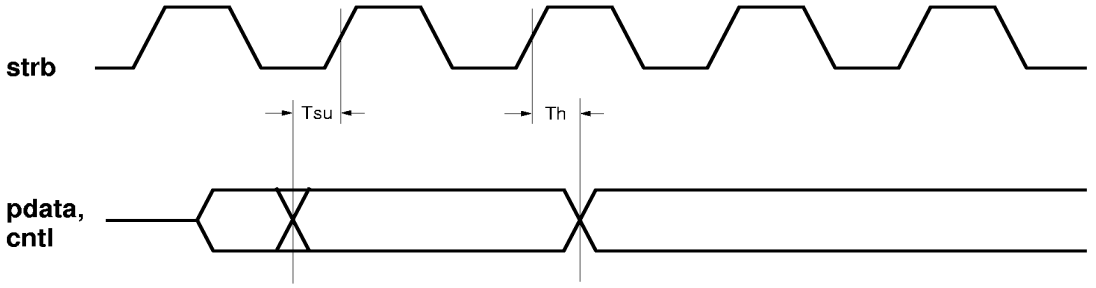


Table 26 lists the specifications for the **strb**-to-**pdata**, **cntl** synchronization.

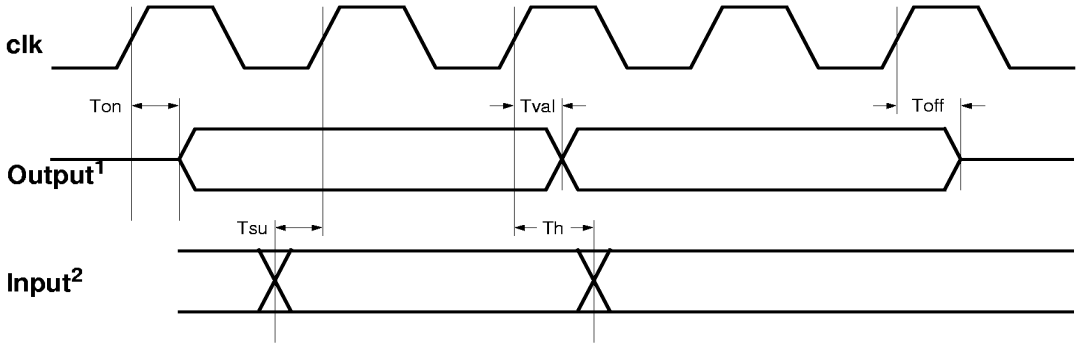
Table 26 strb-to-pdata, cntl Synchronization Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tsu	Input signal valid setup time before **strb**	5	—	ns
Th	Input signal hold time from **strb**	5	—	ns

3.4.1.4 clk to External Arbiter Signals Synchronization

Figure 17 shows the timing characteristics and required measurements for the synchronization between **clk** leading edge and the envelope for the external arbiter output signals: **tx_fifo_rdy[0:3]**, **req[0:3]**, and **col_seen[0:3]**. It also shows the parameter measurements for synchronization between **clk** and the envelope for external arbiter input signals **gnt[0:3]**.

Figure 17 clk to non-pdata Signals Characteristics



[1] External arbiter output signals: **tx_fifo_rdy[0:3]**, **req[0:3]**, **col_seen[0:3]**
[2] External arbiter input signals: **gnt[0:3]**

Table 27 lists the specifications for the **clk** to external arbiter signals synchronization.

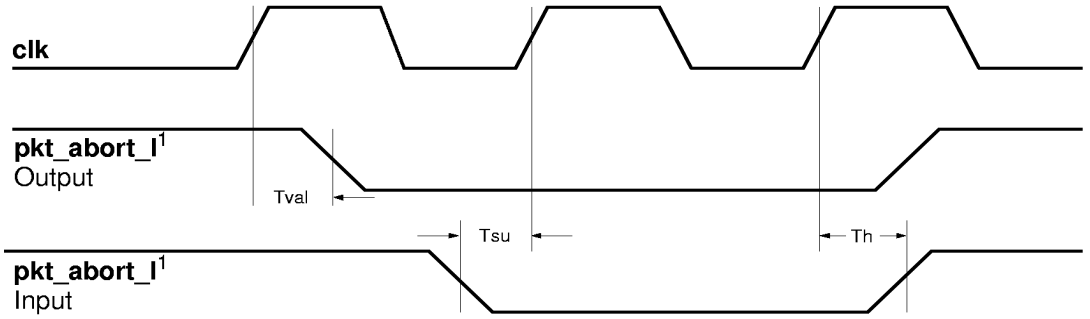
Table 27 clk to non-pdata Signals Synchronization Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tval	**clk** to signal valid delay	2	25	ns
Tsu	Input signal valid setup time before **clk**	8	—	ns
Th	Input signal hold time from **clk**	1	—	ns
Ton	Float-to-active delay from **clk**	2	—	ns
Toff	Active-to-float delay from **clk**	—	25	ns

3.4.1.5 clk-to-pkt_abort_l Synchronization

Figure 18 shows the timing characteristics and required measurements for the synchronization between **clk** leading edge and **pkt_abort_l** events.

Figure 18 clk-to-pkt_abort_l Synchronization Timing Diagram



[1] When not driven, **pkt_abort_l** line is pulled up to 1 by an external pull-up device.

Table 28 lists the specifications for the **clk**-to-**pkt_abort_l** synchronization.

Table 28 clk-to-pkt_abort_l Synchronization Specifications

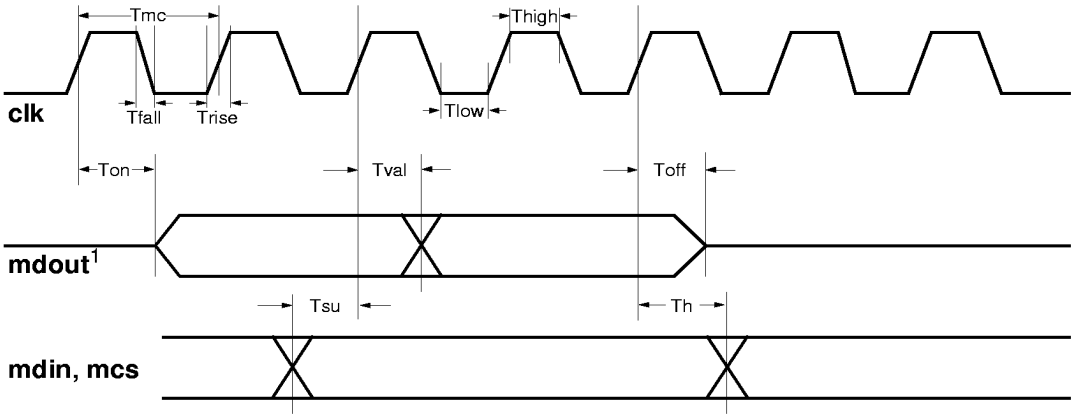
Symbol	Definition	Minimum	Maximum	Unit
Tval	**clk** to signal valid delay (output)	2	25	ns
Tsu	Input signal valid setup time before **clk**	7	—	ns
Th	Input signal hold time from **clk**	1	—	ns

3.4.2 Serial Management Interface Timing Specifications

This section describes the timing characteristics and relationships between signals in the serial management interface.

Figure 19 shows the timing characteristics and required measurements for the synchronization between **mclk** leading edge and the serial management interface serial I/O signals.

Figure 19 mclk to Serial Management I/O Synchronization Timing Diagrams



[1] When not driven, **mdout** line is pulled up to 1 by an external pull-up device.

Table 29 lists specifications for the **mclk** to serial management I/O signals synchronization.

Table 29 mclk to Serial Management I/O Synchronization Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tval	**mclk** to signal valid delay	2	35	ns
Ton	Float-to-active delay from **mclk**	2	—	ns
Toff	Active-to-float delay from **mclk**	—	35	ns
Tsu	Input signal valid setup time before **mclk**	7	—	ns
Th	Input signal hold time from **mclk**	1	—	ns
Tmc	Management clock cycle time	80	—	ns
Trise	Management clock rise time	—	4	ns
Tfall	Management clock fall time	—	4	ns
Thigh	Management clock high time	36	—	ns
Tlow	Management clock low time	36	—	ns

3.4.2.1 Access Modes

Managing an MII interface PHY device is done through a 21340-AB port's **mdio** and **mdc** pins. The 21340-AB port provides two modes for an external controller to drive the **mdc** and **mdio** pins:

- **Serial Access Mode**
  Each external controller serial write access to the 21340-AB's MTC register can toggle the **mdc** and **mdio** pins. Each read access reads the content of the **mdio** pin. This method of accessing the PHY device can be very slow.
- **MII Direct Access Mode**
  While operating in this mode, the **mii_mdc[i]** and **mii_mdio[i]** pins are directly driven by the external controller (through the **mclk**, **mcs**, **mdin**, and **mdout** pins) for the duration of the read or write operation. When the operation has completed, the management serial lines return to their primary functionality. This method of operation shortens the time required to access the MII PHY registers for read and write operations.

3.4.2.2 Timing Measurement Conditions

Figure 20 shows the timing characteristics and relationships between **mclk** and the management interface signals when a 21340-AB port drives the **mdio** pin in MII direct access mode.

Figure 20 Management Interface Timing – Input

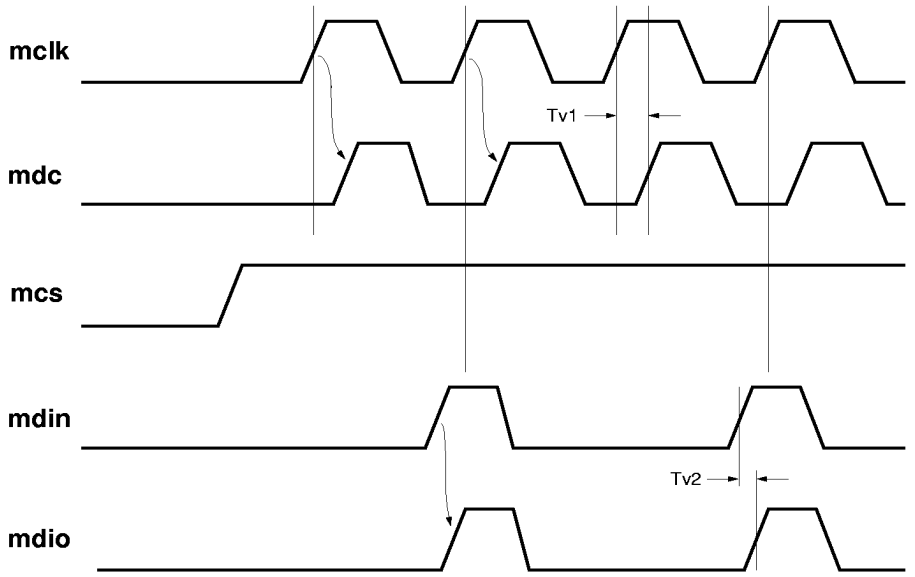


Figure 21 shows the timing characteristics and relationships between **mclk** and the management interface signals when a 21340-AB port drives the **mdio** pin management data output in MII direct access mode.

Figure 21 Management Interface Timing – Output

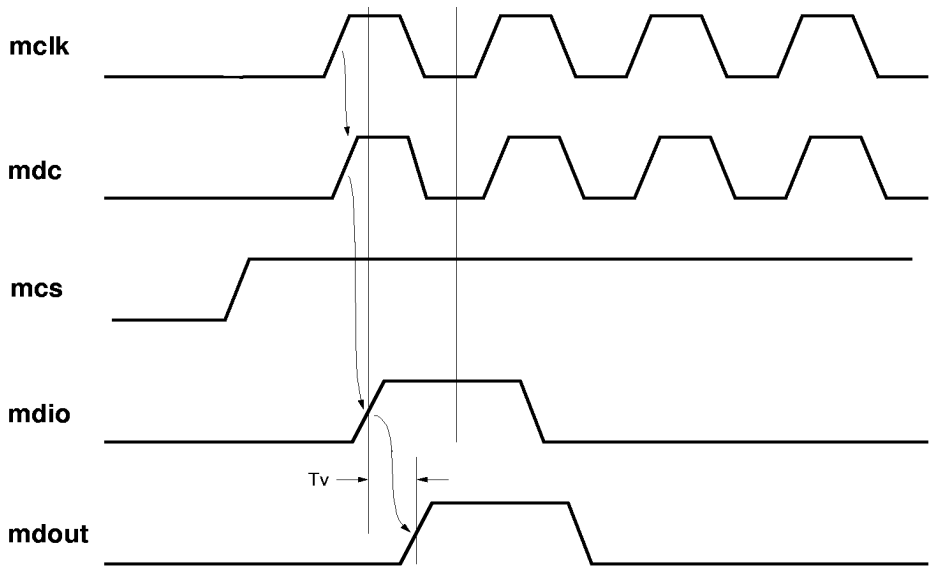


Table 30 lists the timing parameters for **mdio**, **mdc**, and **mdout** in MII direct access mode.

Table 30 MII Direct Access Mode Timing Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tv1	**mclk**-to-**mdc** valid signal time	2	25	ns
Tv2	**mdin**-to-**mdio** valid signal time	2	25	ns
Tv	**mdio**-to-**mout** valid signal time	2	25	ns

3.4.3 MII Interface Operating Specifications

This section describes the timing characteristics of the signals in the MII/SYM interface.

Table 31 lists the functional operating specifications for the MII interface.

Table 31 MII Interface Specifications

Symbol	Definition	Minimum	Maximum	Unit	Notes
V_{oh}	Output high voltage	2.4	—	V	1
V_{ol}	Output low voltage	—	0.4	V	2
V_{ih}	Input high voltage	2.0	—	V	—
V_{il}	Input low voltage	—	0.8	V	—
I_{in}	Input current	–10.0	10.0	µA	3
I_{oz}	Maximum tristate output leakage current	–10.0	10.0	µA	3

[1] I_{oh} = -4 mA
[2] I_{ol} = 4 mA
[3] V_{in} = **Vcc** or **Vss**

3.4.3.1 MII/SYM 10/100-Mb/s and 10-Mb/s Timing – Transmit

Figure 22 shows the MII/SYM port transmit timing characteristics.

Figure 22 MII/SYM Port Timing Diagram – Transmit

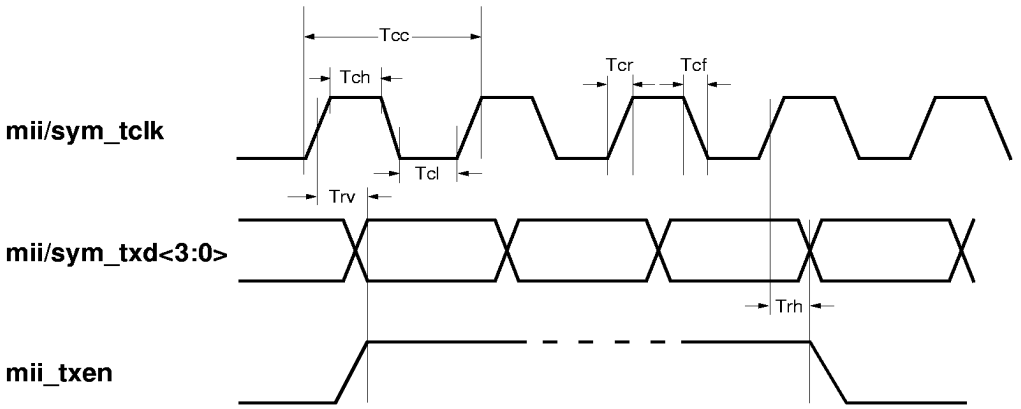


Table 32 lists the MII/SYM port transmit timing specifications.

Table 32 MII/SYM Port Timing Specifications – Transmit

Symbol	Definition	Minimum	Maximum	Typical	Unit
Tcc[1]	**mii/sym_tclk** cycle time	—	40t[2]	—	ns
Tch	**mii/sym_tclk** high time	14t[2]	26t[2]	—	ns
Tcl	**mii/sym_tclk** low time	14t[2]	26t[2]	—	ns
Tcr	**mii/sym_tclk** rise time	—	—	8	ns
Tcf	**mii/sym_tclk** fall time	—	—	8	ns
Trv[3]	**mii_tclk** rise to **mii_txen** valid time or **mii/sym_tclk** rise to **mii/sym_txd** valid time	5	20	—	ns

[1] ± 50 parts per million.
[2] t = 1 for 100-Mb/s operation and t = 10 for 10-Mb/s operation.
[3] The transmit data (**mii/sym_txd**) and transmit enable (**mii_txen**) output pins are driven internally from the rising edge of **mii/sym_tclk**.

3.4.3.2 MII/SYM 10/100-Mb/s and 10-Mb/s Timing – Receive

Figure 23 shows the MII/SYM port receive timing characteristics.

Figure 23 MII/SYM Port Timing Diagram – Receive

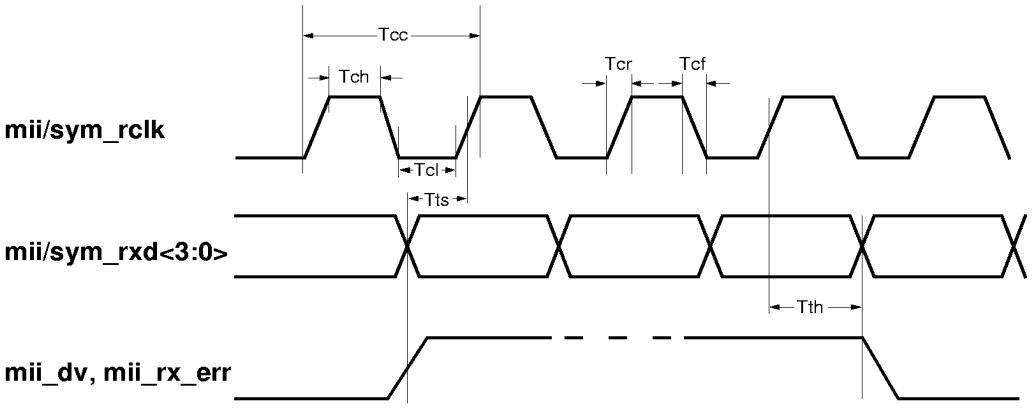


Table 33 lists the MII/SYM port receive timing specifications.

Table 33 MII/SYM Port Timing Specifications – Receive

Symbol	Definition	Minimum	Maximum	Typical	Unit
Tcc[1]	**mii/sym_tclk** cycle time	—	—	$40t^2$	ns
Tch	**mii/sym_tclk** high time	$14t^2$	$26t^2$	—	ns
Tcl	**mii/sym_tclk** low time	$14t^2$	$26t^2$	—	ns
Tcr	**mii/sym_tclk** rise time	—	—	8	ns
Tcf	**mii/sym_tclk** fall time	—	—	8	ns
Tts[3]	**mii/sym_rxd** setup to **mii/sym_rclk** rise time or **mii_dv**, **mii_rx_err** setup after **mii_rclk** rise time	10	—	—	ns
Tth	**mii/sym_rxd** hold after **mii/sym_rclk** rise time or **mii_dv**, **mii_rx_err** hold after **mii_rclk** rise time	10	—	—	ns

[1] ± 50 parts per million.
[2] t = 1 for 100-Mb/s operation and t = 10 for 10-Mb/s operation.
[3] The receive data (**mii/sym_rxd**) and data valid (**mii_dv**) input pins are latched internally on the rising edge of **mii/sym_rclk**.

3.4.3.3 SYM 100-Mb/s Timing – Signal Detect

Figure 24 shows the SYM port signal detect timing characteristics.

Figure 24 SYM Port Timing Diagram – Signal Detect

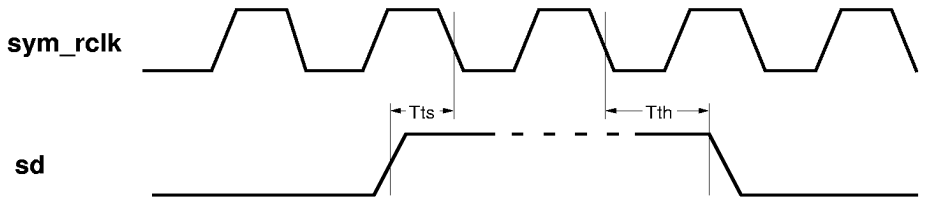


Table 34 lists the SYM port signal detect timing limits.

Table 34 SYM Port Timing Specifications – Signal Detect

Symbol	Definition	Minimum	Maximum	Unit
Tts[1]	**sd** setup (both rise and fall transactions) to **sym_rclk** fall time	10	—	ns
Tth[1]	**sd** hold (both rise and fall transactions) after **sym_rclk** fall time	12	—	ns

[1] Input signal detect (**sd**) is latched internally on the falling edge of **sym_rclk**.

3.4.3.4 MII 10/100-Mb/s Timing – Carrier Sense and Collision

Figure 25 shows the MII port carrier sense and collision timing characteristics.

Figure 25 MII Port Timing Diagram – Carrier Sense and Collision

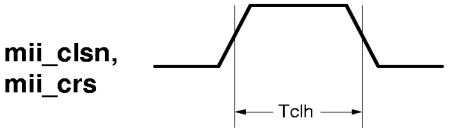


Table 35 lists the MII port carrier sense and collision timing specifications.

Table 35 MII Port Timing Specifications – Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Unit
Tclh	**mii_crs**, **mii_clsn** high time	20t[1]	—	ns

[1] t = 1 for 100-Mb/s operation and t = 10 for 10-Mb/s operation.

3.4.4 Joint Test Action Group – Test Access Port

This section describes the joint test action group (JTAG) test access port specifications.

Table 36 lists the dc specifications for the JTAG pins.

Table 36 JTAG DC Specifications

Symbol	Definition	Minimum	Maximum	Unit	Notes
V_{oh}	Output high voltage	2.4	—	V	1
V_{ol}	Output low voltage	—	0.4	V	2
V_{ih}	Input high voltage	2.0	—	V	—
V_{il}	Input low voltage	—	0.8	V	—
I_{ip}	Input leakage current on pins with internal pull-ups (**tck**, **tdi**, and **tms**)	—	+20/-1000[1]	µA	3,4
I_{oz}	Tristate output leakage current (**tdo**)	—	±20	µA	3

[1] I_{oh} = -4 mA.
[2] I_{oh} = 4 mA.
[3] 0.0 < V_{in} < **Vdd**.
[4] For **tck**, **tdi**, and **tms** pins that have internal pull-ups, the leakage current can get to 1.0 mA when V_{in} = 0 V

3.4.4.1 JTAG Boundary-Scan Timing

Figure 26 shows the JTAG boundary-scan timing.

Figure 26 JTAG Boundary-Scan Timing Diagram

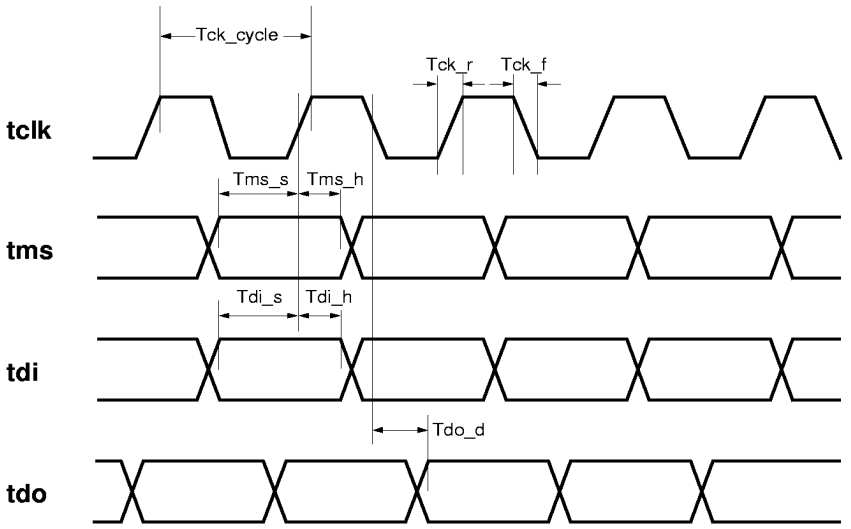


Table 37 lists the JTAG interface signal timing specifications.

Table 37 JTAG Interface Signal Timing Specifications

Symbol	Definition	Minimum	Maximum	Unit
Tms_s	**tms** setup time	20	—	ns
Tms_h	**tms** hold time	5	—	ns
Tdi_s	**tdi** setup time	20	—	ns
Tdi_h	**tdi** hold time	5	—	ns
Tdo_d	**tdo** delay time	—	20	ns
Tck_r[1]	**tck** rise time	—	3	ns
Tck_f[1]	**tck** fall time	—	3	ns
Tck_cycle	**tck** cycle time	40	—	ns

[1] Parameter design guarantee

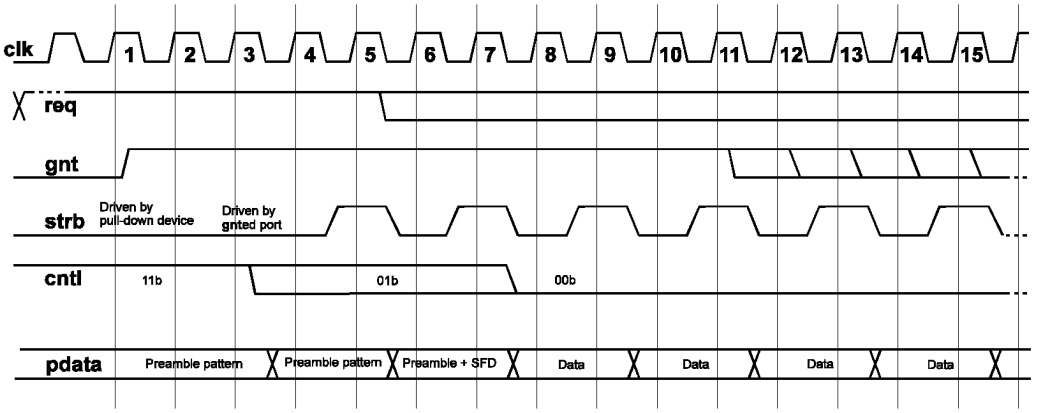
3.5 21340-AB Operation Timing Diagrams

This section describes the cause-and-effect relationships among key signals during typical 21340-AB parallel bus operations and management access operations.

3.5.1 Parallel Bus – Start Broadcasting Packet

Figure 27 shows how a packet broadcast is initiated on the 21340-AB parallel bus.

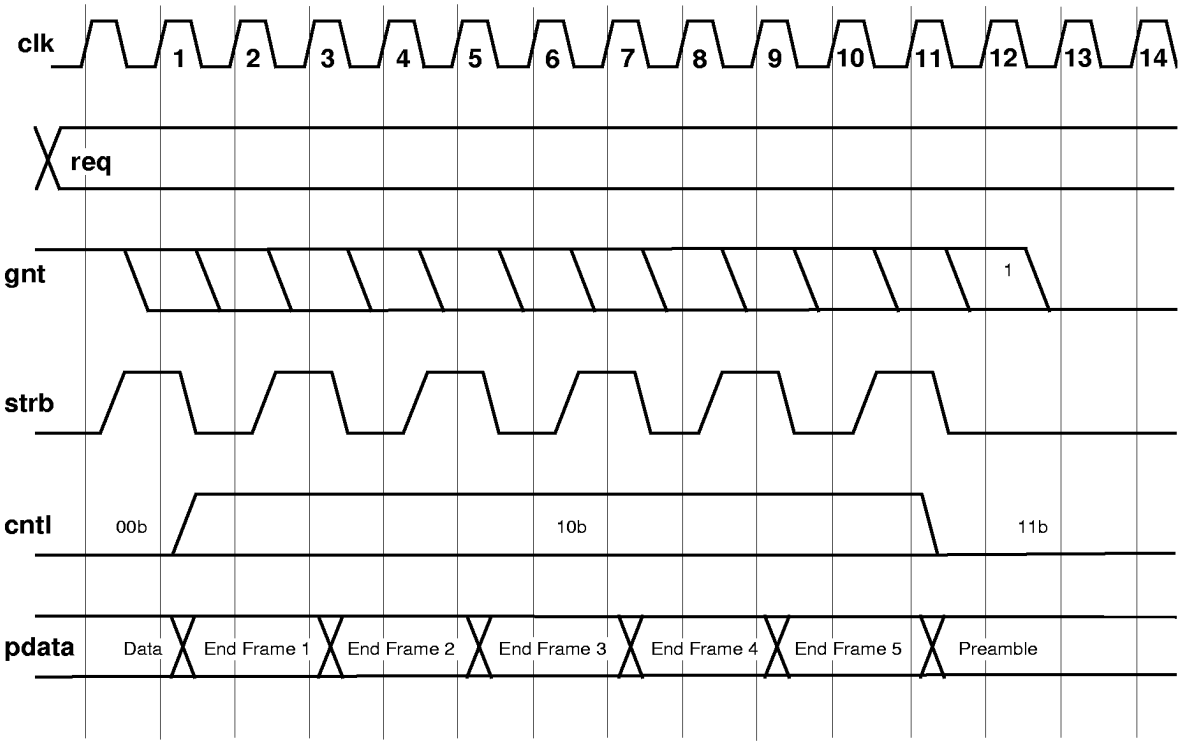
Figure 27 Parallel Bus Operation – Start Broadcasting Packet



3.5.2 Parallel Bus – End Broadcasting Packet

Figure 28 shows how a packet broadcast is completed on the 21340-AB parallel bus.

Figure 28 Parallel Bus Operation – End Broadcasting Packet



[1] The **gnt** signal should be set for at least 10 **clk** cycles during broadcast and deasserted no later than one **clk** cycle after termination of broadcast.

Figure 29 expands the 5 bytes of the end frame packet broadcasting.

Figure 29 End Frame Format

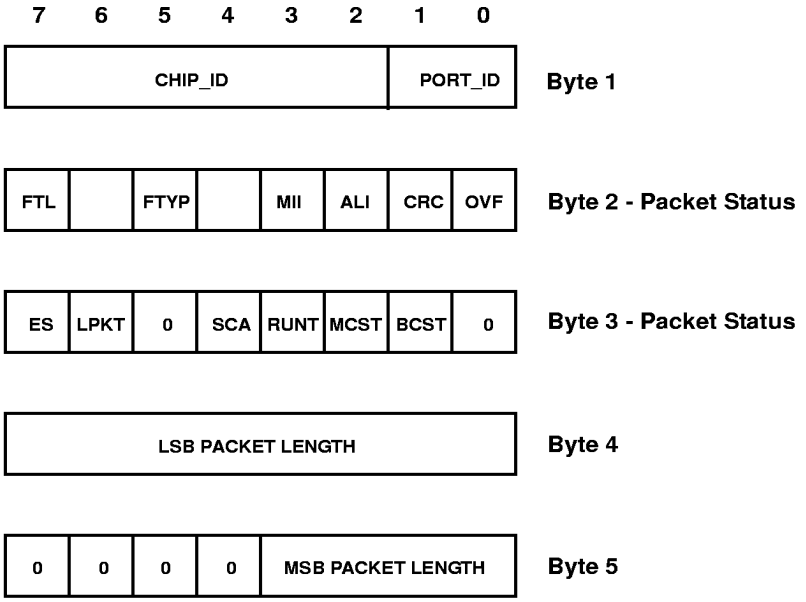


Table 38 and Table 39 describe the bit fields of the packet status bytes in the end frame.

Table 38 Packet Status – Byte 2 *(Sheet 1 of 2)*

Bit	Field	Description
7	**FTL**	Frame-too-long indication. Asserted when frame data length is greater than 1518 bytes.
6	—	RESERVED.
5	**FTYP**	Frame type: 1 = Ethernet 0 = IEEE
4	—	RESERVED.
3	**MII**	MII error was detected during packet reception.

Table 38 Packet Status – Byte 2 *(Sheet 2 of 2)*

Bit	Field	Description
2	ALI	Alignment error was detected during packet reception.
1	CRC	CRC error was detected during packet reception.
0	OVF	Overflow error condition was detected during operation.

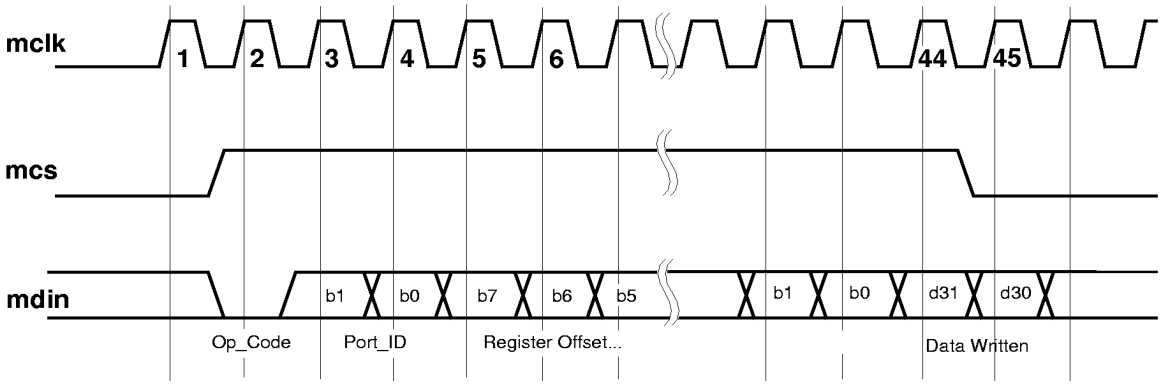
Table 39 Packet Status – Byte 3

Bit	Field	Description
7	ES	Error summary. Asserted when bits 0, 1, 2, 3, or 7 were asserted in packet status byte 2, or bit 4 in byte 3.
6	LPKT	Packet equal to or longer than 1600 bytes was detected and stripped after 1600 bytes.
5	0	—
4	SCA	Short carrier event was detected.
3	RUNT	Runt packet was detected.
2	MCST	Multicast frame was detected.
1	BCST	Broadcast frame was detected.
0	0	—

3.5.3 Serial Management – Write Operation

Figure 30 shows how data is written to the management registers.

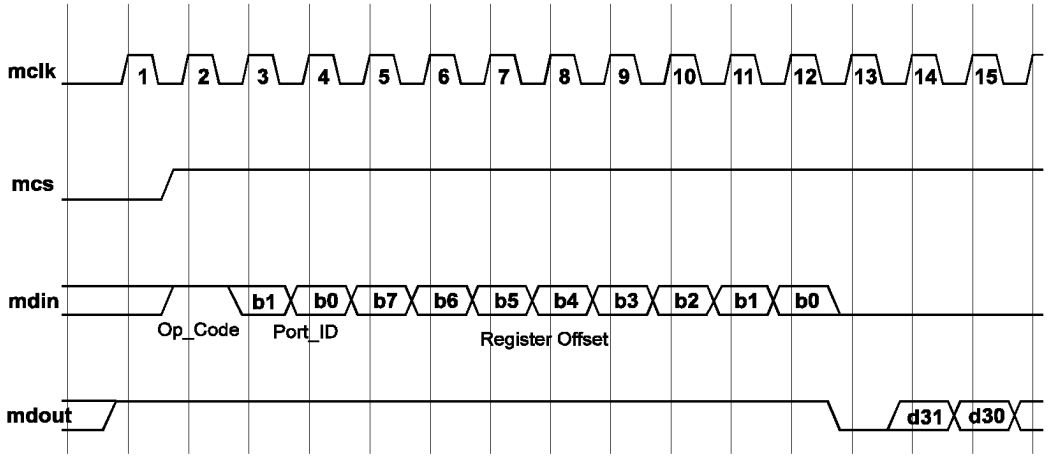
Figure 30 Serial Management – Write Operation



3.5.4 Serial Management – Read Operation

Figure 31 shows how data is read from the management registers.

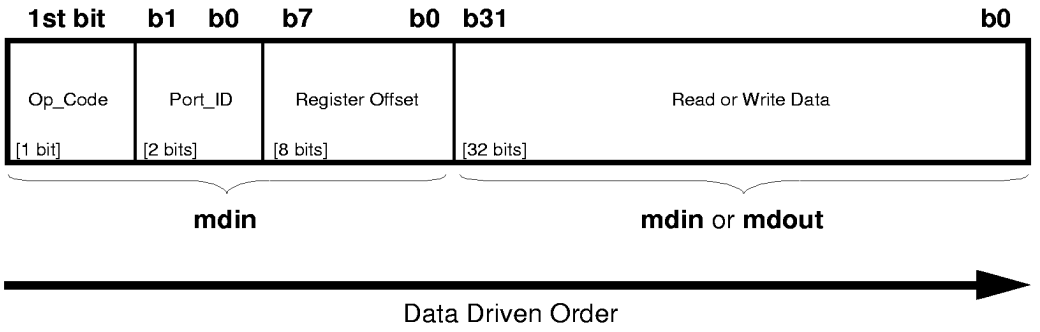
Figure 31 Serial Management – Read Operation



3.5.5 Serial Bit Order

Figure 32 shows the serial bit order for accessing the management interface using the **mdin** or **mdout** pins.

Figure 32 mdin/mdout – Serial Bit Order



4 Mechanical Specifications

The 21340-AB is contained in a 208-pin plastic quad flat pack (PQFP). Figure 33 shows the chip labeling.

Figure 33 Part Marking

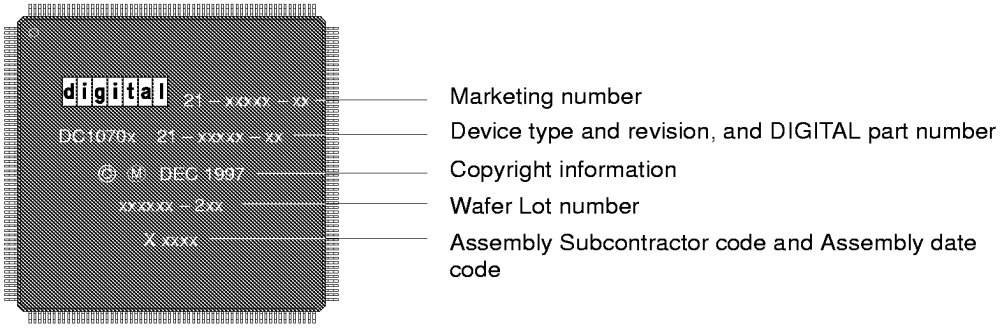


Figure 34 shows the mechanical layout of the 21340-AB, and Table 40 lists the mechanical specifications.

Figure 34 208-Pin PQFP Package

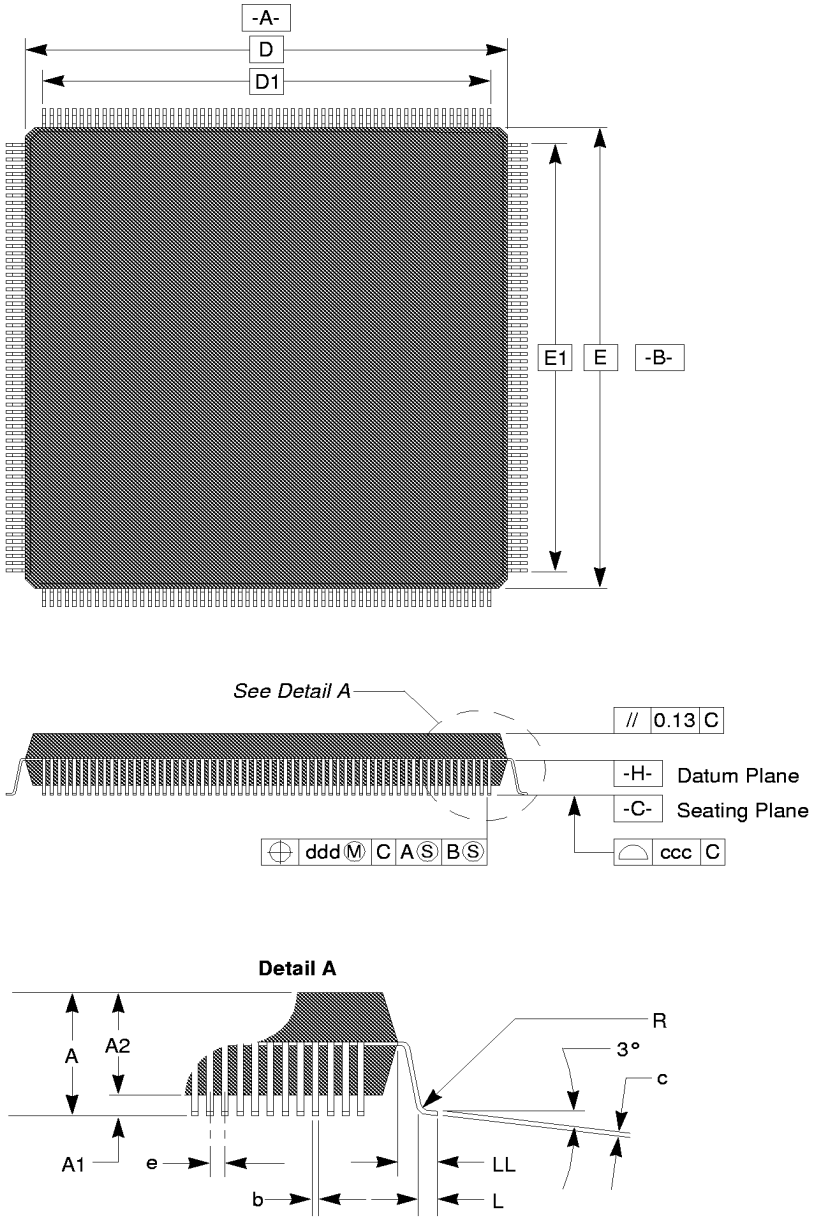


Table 40 208-Pin PQFP Mechanical Specifications

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	—	—	4.07
A1	0.25	—	—
A2	3.20	—	3.60
b	0.17	—	0.27
c	0.15	—	—
D	—	28.00 BSC[2]	—
D1	—	25.50 BSC	—
ddd	—	0.08	—
E	—	28.00 BSC	—
E1	—	25.50 BSC	—
e	—	0.50 BSC	—
L	0.50	—	0.75
LL	—	1.30 reference	—
R	0.20	—	0.35

1 All dimensions are in millimeters.

2 ANSI Y14.5M-1982 American National Standard Dimensioning and Tolerancing, Section 1.3.2, defines Basic Dimension (BSC) as: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. It is the basis from which permissible variations are established by tolerances on other dimensions, in notes, or in feature control frames.

5 Register Descriptions

This section describes the 21340-AB registers. Registers are divided into two classes:

- Control and status registers (CSRs)
- Management statistics counters

5.1 General Register Conventions

Registers that are implemented in each of the four ports of a 21340-AB chip are described once, with the {j} subscript indicating that there are four duplicate registers of that type on the chip. The same convention is used for bit fields that are duplicated across the four ports within these registers.

In the register description tables throughout this chapter, the following abbreviations are used to indicate register access modes and fields:

R	=	Read.
W	=	Write.
W1C	=	Cleared by Write 1. When set, the bit in a given register is cleared.
MBZ	=	Must be zero. This bit is always 0.
MBO	=	Must be one. This bit is always 1.

Notes: 1. Reserved bits are set to 0 for reading.

2. Violating MBZ or MBO control bits value may result in UNPREDICTABLE behavior.

5.2 21340-AB Register Mapping

Table 41 lists each 21340-AB register name, mnemonic, offset, access, and the section that describes the register.

Table 41 21340-AB Register Mapping *(Sheet 1 of 5)*

Register Description	Mnemonic	I/O Address Offset	Access	Section
Control and Status Registers				5.3
Source address field, register 1	SA1{j}	00H	r/w	5.3.1
Source address field, register 2	SA2{j}	01H	r/w	5.3.2
Destination address field, register 1	DA1{j}	07H	r/w	5.3.3
Destination address field, register 2	DA2{j}	08H	r/w	5.3.4
Flow control type register	FCT{j}	02H	r/w	5.3.5
Collision count and control register	CCC{j}	03H	r/w	5.3.6
Software reset register	SWR	04H	r/w	5.3.7
Status register	STR{j}	05H	r/wlc	5.3.8
Operating mode register	OPM{j}	06H	r/w	5.3.9
Management control register	MTC	09H	r/w	5.3.10
Chip identification register	CID	0AH	r	5.3.11
Vendor identification register	VID	0BH	r	5.3.12
Port timers register	PTR{j}	0CH	r/w	5.3.13
Port segmentation control register	PSC	0DH	r/w	5.3.14
Jabber register	JBR{j}	0FH	r/w	5.3.15
Operating mode 2 register	OPM{2}	40H	r/w	5.3.16
Device interrupt status register	ISR	41H	r	5.3.17
Global operation register	GOR	42H	r/w	5.3.18
Interrupt mask register 1	MIMSK1{j}	43H	r/w	5.3.19
Interrupt mask register 2	MIMSK2{j}	44H	r/w	5.3.20
Interrupt status register 1	MINT1{j}	45H	r/wlc	5.3.21

Table 41 21340-AB Register Mapping *(Sheet 2 of 5)*

Register Description	Mnemonic	I/O Address Offset	Access	Section
FCTL source address low	FSA1{j}	46H	r	5.3.22
FCTL source address high	FSA2{j}	47H	r	5.3.23
Backwards Compatible 21340 Statistics Counters				5.4
Transmit collision counter register	TCC{j}	10H	r	5.4.1
Runt packet counter register	RPC{j}	11H	r	5.4.2
21340-AB Statistic Registers				5.5
Overflow counter	ROVF{j}	50H	r/w	5.5.1
Total octet counter low	ROCTL{j}	51H	r/w	5.5.2
Total octet counter high	ROCTH{j}	52H	r/w	5.5.3
Broadcast packet counter	RBCT{j}	53H	r/w	5.5.4
Multicast packet counter	RMCT{j}	54H	r/w	5.5.5
Undersized packet counter	RUSZ{j}	55H	r/w	5.5.6
Oversized packet counter	ROSZ{j}	56H	r/w	5.5.7
Fragment counter	RFRG{j}	57H	r/w	5.5.8
Too long packets with CRC errors	RJBR{j}	58H	r/w	5.5.9
Collision counter	RCOL{j}	59H	r/w	5.5.10
64 octets packet counter	R64{j}	5AH	r/w	5.5.11
65 – 127 octets packet counter	R65TO127{j}	5BH	r/w	5.5.12
128 – 255 octets packet counter	R128TO255{j}	5CH	r/w	5.5.13
256 – 511 octets packet counter	R256TO511{j}	5DH	r/w	5.5.14
512 – 1023 octets packet counter	R512TO1023{j}	5EH	r/w	5.5.15
1024 – 1518 octets packet counter	R1024TO1518{j}	5FH	r/w	5.5.16
Alignment error packet counter	MALI{j}	60H	r/w	5.5.17
CRC error packet counter	MCRC{j}	61H	r/w	5.5.18
Single collision counter	MSCOL{j}	62H	r/w	5.5.19
Multicollision counter	MMCOL{j}	63H	r/w	5.5.20

Table 41 21340-AB Register Mapping *(Sheet 3 of 5)*

Register Description	Mnemonic	I/O Address Offset	Access	Section
Deffered transmission counter	MDEF{j}	64H	r/w	5.5.21
Late collision counter	MLCOL{j}	65H	r/w	5.5.22
Partition isolation counter	MPAR{j}	66H	r/w	5.5.23
Carrier integrity isolation counter	MISO{j}	67H	r/w	5.5.24
Symbol error counter	MSYE{j}	68H	r/w	5.5.25
Source address changed counter	MSAC{j}	69H	r/w	5.5.26
Last source address low	UAR1{j}	6AH	r/w	5.5.27
Last source address high	UAR2{j}	6BH	r/w	5.5.28
Short event counter	MSHE{j}	6CH	r/w	5.5.29
Good octets counter low	MOCTL{j}	6DH	r/w	5.5.30
Good octets counter high	MOCTH{j}	6EH	r/w	5.5.31
Receive jabber counter	MVLE{j}	6FH	r/w	5.5.32
Control packet counter	MCPKT{j}	71H	r/w	5.5.33
Total transmitted octets low	MTOCTL{j}	72H	r/w	5.5.34
Total transmitted octets high	MTOCTH{j}	73H	r/w	5.5.35
Total transmitted packets	MTPKT{j}	74H	r/w	5.5.36
Total transmitted control packets	MTCPKT{j}	75H	r/w	5.5.37
Total filtered packets in transmit	MTFTR{j}	76H	r/w	5.5.38
21340-AB Statistic Registers – Clear-by-Read Addresses				5.5
Overflow counter	ROVF{j}	D0H	r/w	5.5.1
Total octet counter low	ROCTL{j}	D1H	r/w	5.5.2
Total octet counter high	ROCTH{j}	D2H	r/w	5.5.3
Broadcast packet counter	RBCT{j}	D3H	r/w	5.5.4
Multicast packet counter	RMCT{j}	D4H	r/w	5.5.5
Undersized packet counter	RUSZ{j}	D5H	r/w	5.5.6
Oversized packet counter	ROSZ{j}	D6H	r/w	5.5.7

Table 41 21340-AB Register Mapping *(Sheet 4 of 5)*

Register Description	Mnemonic	I/O Address Offset	Access	Section
Fragment counter	RFRG{j}	D7H	r/w	5.5.8
Too long packets with CRC errors	RJBR{j}	D8H	r/w	5.5.9
Collision counter	RCOL{j}	D9H	r/w	5.5.10
64 octets packet counter	R64{j}	DAH	r/w	5.5.11
65 – 127 octets packet counter	R65TO127{j}	DBH	r/w	5.5.12
128 – 255 octets packet counter	R128TO255{j}	DCH	r/w	5.5.13
256 – 511 octets packet counter	R256TO511{j}	DDH	r/w	5.5.14
512 – 1023 octets packet counter	R512TO1023{j}	DEH	r/w	5.5.15
1024 – 1518 octets packet counter	R1024TO1518{j}	DFH	r/w	5.5.16
Alignment error packet counter	MALI{j}	E0H	r/w	5.5.17
CRC error packet counter	MCRC{j}	E1H	r/w	5.5.18
Single collision counter	MSCOL{j}	E2H	r/w	5.5.19
Multicollision counter	MMCOL{j}	E3H	r/w	5.5.20
Deferred transmission counter	MDEF{j}	E4H	r/w	5.5.21
Late collision counter	MLCOL{j}	E5H	r/w	5.5.22
Partition isolation counter	MPAR{j}	E6H	r/w	5.5.23
Carrier integrity isolation counter	MISO{j}	E7H	r/w	5.5.24
Symbol error counter	MSYE{j}	E8H	r/w	5.5.25
Source address changed counter	MSAC{j}	E9H	r/w	5.5.26
Last source address low	UAR1{j}	EAH	r/w	5.5.27
Last source address high	UAR2{j}	EBH	r/w	5.5.28
Short event counter	MSHE{j}	ECH	r/w	5.5.29
Good octets counter low	MOCTL{j}	EDH	r/w	5.5.30
Good octets counter high	MOCTH{j}	EEH	r/w	5.5.31
Receive jabber counter	MVLE{j}	EFH	r/w	5.5.32
Control packet counter	MCPKT{j}	F1H	r/w	5.5.33

Table 41 21340-AB Register Mapping *(Sheet 5 of 5)*

Register Description	Mnemonic	I/O Address Offset	Access	Section
Total transmitted octets low	MTOCTL{j}	F2H	r/w	5.5.34
Total transmitted octets high	MTOCTH{j}	F3H	r/w	5.5.35
Total transmitted packets	MTPKT{j}	F4H	r/w	5.5.36
Total transmitted control packets	MTCPKT{j}	F5H	r/w	5.5.37
Total filtered packets in transmit	MTFTR{j}	F6H	r/w	5.5.38

5.3 Control and Status Registers (CSRs)

The following sections describe the individual CSR registers.

5.3.1 Source Address Header, Register 1

Mnemonic: SA1{j}

Offset: 00H

This register contains the lower 4 bytes of the IEEE SA of the 21340-AB port used for FCTL and BP packets. There is one SA1 register per each of the four 21340-AB ports.

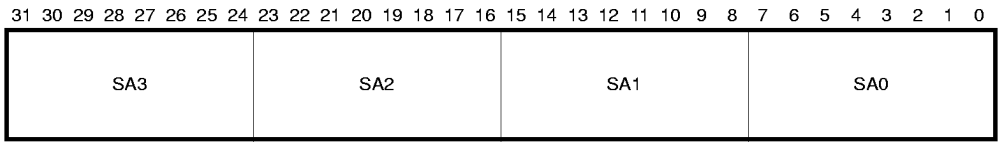


Table 42 defines the bit fields of the SA1.

Table 42 SA1 Bit Fields

Bits	Field	Access	Description
<31:24>	**SA3**	R/W	Fourth IEEE address byte
<23:16>	**SA2**	R/W	Third IEEE address byte
<15:08>	**SA1**	R/W	Second IEEE address byte
<07:00>	**SA0**	R/W	First IEEE address byte

Table 43 defines the access rules of the SA1 register.

Table 43 SA1 Access Rules

Category	Description
Register access	R/W
Register address offset	00H
Value after reset	00000000H
Read access rules	None
Write access rules	Must be written only during initialization

5.3.2 Source Address Header, Register 2

Mnemonic: SA2{j}

Offset: 01H

This register contains the higher 2 bytes of the IEEE SA of the 21340-AB port used for flow-control (FCTL) and backpressure (BP) packets, as well as the type field used for BP packets. There is one SA2 register per each of the four 21340-AB ports.

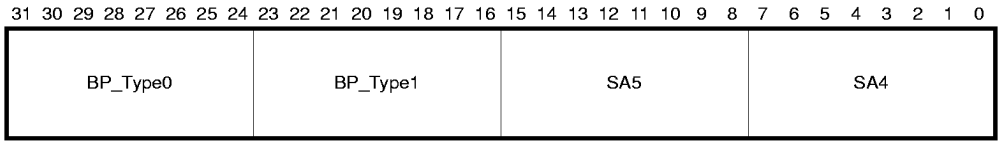


Table 44 defines the bit fields of the SA2 register.

Table 44 SA2 Bit Fields

Bits	Field	Access	Description
<31:24>	**BP_Type0**	R/W	Low byte of BP packet type field
<23:16>	**BP_Type1**	R/W	High byte of BP packet type field
<15:08>	**SA5**	R/W	Sixth IEEE address byte
<07:00>	**SA4**	R/W	Fifth IEEE address byte

Table 45 defines the access rules of the SA2 register.

Table 45 SA2 Access Rules

Category	Description
Register access	R/W
Register address offset	01H
Value after reset	00000000H
Read access rules	None
Write access rules	Must be written only during initialization

5.3.3 DA Field, Register 1

Mnemonic: DA1{j}

Offset: 07H

This register contains the lower 4 bytes of the IEEE DA used for BP and FCTL packets. There is one DA1 register per each of the four 21340-AB ports.

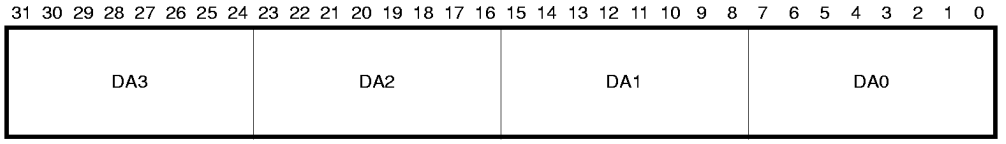


Table 46 defines the bit fields of the DA1 register.

Table 46 DA1 Bit Fields

Bits	Field	Access	Description
<31:24>	**DA3**	R/W	Fourth IEEE address byte
<23:16>	**DA2**	R/W	Third IEEE address byte
<15:08>	**DA1**	R/W	Second IEEE address byte
<07:00>	**DA0**	R/W	First IEEE address byte

Table 47 defines the access rules of the DA1 register.

Table 47 DA1 Access Rules

Category	Description
Register access	R/W
Register address offset	07H
Value after reset	00000000H
Read access rules	None
Write access rules	Must be written only during initialization

5.3.4 DA Field, Register 2

Mnemonic: DA2{j}

Offset: 08H

This register contains the higher 2 bytes of the IEEE address used for BP and FCTL packets. There is one DA2 register per each of the four 21340-AB ports.

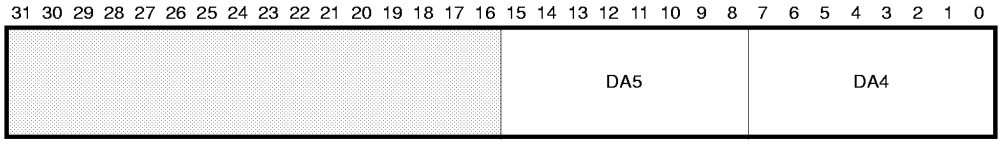


Table 48 defines the bit fields of the DA2 register.

Table 48 DA2 Bit Fields

Bits	Field	Access	Description
<31:16>	—	—	RESERVED
<15:08>	**DA5**	R/W	Sixth IEEE address byte
<07:00>	**DA4**	R/W	Fifth IEEE address byte

Table 49 defines the access rules of the DA2 register.

Table 49 DA2 Access Rules

Category	Description
Register access	R/W
Register address offset	08H
Value after reset	00000000H
Read access rules	None
Write access rules	Must be written only during initialization

5.3.5 Flow Control Packet Type Register

Mnemonic: FCT{j}

Offset: 02H

This register contains the packet type and OpCode fields used for flow-control packets. There is one FCT register per each of the four 21340-AB ports.

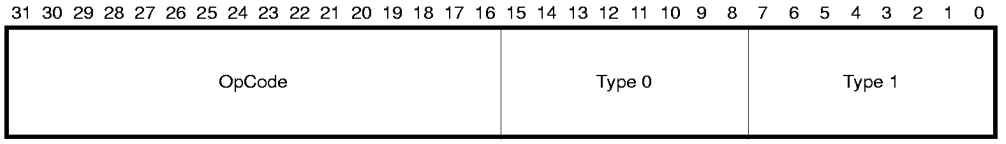


Table 50 defines the bit fields of the FCT register.

Table 50 FCT Bit Fields

Bits	Field	Access	Description
<31:16>	**OpCode**	R/W	Flow-control packet OpCode field
<15:08>	**Type 0**	R/W	Low byte of flow-control packet type field
<07:00>	**Type 1**	R/W	High byte of flow-control packet type field

Table 51 explains the access rules of the FCT register.

Table 51 FCT Access Rules

Category	Description
Register access	R/W
Register address offset	02H
Value after reset	00000000H
Read access rules	None
Write access rules	Must be written only during initialization

5.3.6 Collision Count and Control Register

Mnemonic: CCC{j}

Offset: 03H

This register defines the maximum backoff limit when multiple collisions occur while trying to transmit and the 21340-AB is not in backpressure mode. It also defines the collision count limit (CCL) in order to activate the partition function. There is one CCC register per each of the four 21340-AB ports.

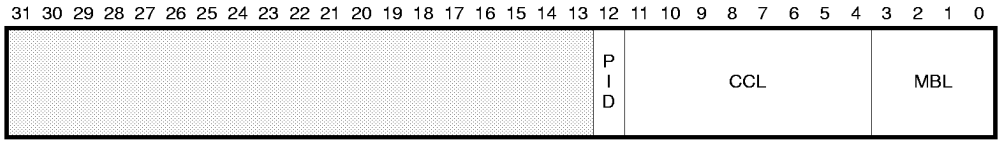


Table 52 defines the bit fields of the CCC register.

Table 52 CCC Bit Fields

Bits	Field	Access	Description
<31:13>	—	—	RESERVED.
<12>	**PID**	R/W	**Partition isolation disable**. When *set*, disables the partition function. When *cleared*, enables the partition function.
<11:04>	**CCL**	R/W	**Collision count limit**. Defines the maximum number of consecutive collisions with a node before partitioning. The CCL value multiplied by 30 results in the absolute number of allowed collisions. The CCL field should be greater than 0. Writing 0 to the CCL field may yield UNPREDICTABLE behavior.
<3:0>	**MBL**	R/W	**Maximum backoff limit**. The actual maximum backoff limit is the number defined in this field + 1.

Table 53 defines the access rules of the CCC register.

Table 53 CCC Access Rules

Category	Description
Register access	R/W.
Register address offset	03H.
Value after reset	00000029H.
Read access rules	None.
Write access rules	Writing the register's field values is allowed only when the port's receive and transmit paths are stopped (STRI{j}<5> and STR{j}<6> are set).

5.3.7 Software Reset Register

Mnemonic: SWR

Offset: 04H

This register controls the 21340-AB software reset. It provides separate reset lines to each receive and transmit path in the 21340-AB. For full chip software reset, all SWR bits must be set. In order to reset only one port, the appropriate Tx path and Rx path reset should be set. Software reset to a port sets all its registers to their default values. It does not reset the MTC, CID, VID, and PSC registers.

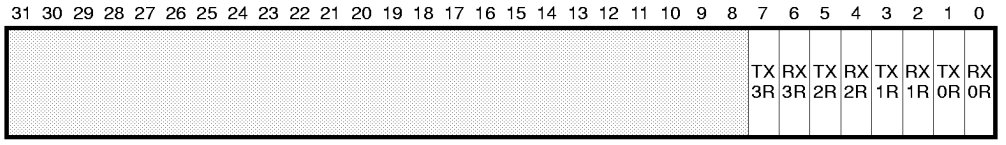


Table 54 defines the bit fields of the SWR register.

Table 54 SWR Bit Fields *(Sheet 1 of 2)*

Bits	Field	Access	Description
<31:08>	—	—	RESERVED
<07>	**Tx3R**	W	**Port[3] Tx path reset.** When *set*, resets the port[3] transmit path. The reset operation then clears this bit.
<06>	**Rx3R**	W	**Port[3] Rx path reset.** When *set*, resets the port[3] receive path. The reset operation then clears this bit.
<05>	**Tx2R**	W	**Port[2] Tx path reset.** When *set*, resets the port[2] transmit path. The reset operation then clears this bit.
<04>	**Rx2R**	W	**Port[2] Rx path reset.** When *set*, resets the port[2] receive path. The reset operation then clears this bit.
<03>	**Tx1R**	W	**Port[1] Tx path reset.** When *set*, resets the port[1] transmit path. The reset operation then clears this bit.

Table 54 SWR Bit Fields *(Sheet 2 of 2)*

Bits	Field	Access	Description
<02>	**Rx1R**	W	**Port[1] Rx path reset**. When *set*, resets the port[1] receive path. The reset operation then clears this bit.
<01>	**Tx0R**	W	**Port[0] Tx path reset**. When *set*, resets the port[0] transmit path. The reset operation then clears this bit.
<00>	**Rx0R**	W	**Port[0] Rx path reset**. When *set*, resets the port[0] receive path. The reset operation then clears this bit.

Table 55 defines the access rules of the SWR register.

Table 55 SWR Access Rules

Category	Description
Register access	Write-only register
Register address offset	04H
Value after reset	00000000H
Read access rules	Write-only register
Write access rules	—

Note: When resetting a port, always reset both its Rx and Tx paths. Resetting only the port's Tx path may affect the receive path; resetting only the port's Rx path may affect the transmit path. This may lead to UNPREDICTABLE behavior.

The port performs the software reset operation only when it is not broadcasting data onto the parallel interface (the **gnt** pin is deasserted). If the port is broadcasting data and the management unit issues a software reset, the reset operation is delayed until the parallel interface enters the Idle state.

5.3.8 Status Register

Mnemonic: STR{j}

Offset: 05H

This register contains the status bits that each 21340-AB port reports to the management agent. There is one STR register per each of the four 21340-AB ports.

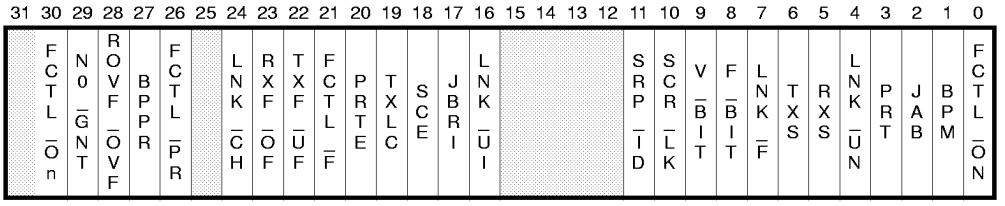


Table 56 defines the bit fields of the STR register.

Table 56 STR Bit Fields *(Sheet 1 of 4)*

Bits	Field	Access	Description
<31>	—	—	RESERVED
<30>	**FCTL_ON**	R/W1C	**Flow control identification succeeded.** When *set*, indicates that the port was able to detect its remote node as capable of using the 21340 credit-based flow-control scheme.
<29>	**NO_GNT**	R/W1C	**No grant.** When *set*, indicates that no grant has been issued to the port for at least 0.33 seconds since the port's **req** pin was asserted.
<28>	**ROVF_OVF**	R/W1C	**ROVF overflow.** When set, indicates that an ROVF statistic counter wraparound event has been detected.
<27>	**BPPR**	R/W1C	**Backpressure packet received**. When *set*, indicates that a special backpressure packet has been received. The identification of backpressure packet is done based on the packet's header TYPE field.

Table 56 STR Bit Fields *(Sheet 2 of 4)*

Bits	Field	Access	Description
<26>	**FCTL_PR**	R/W1C	**FCTL packet received**. When *set*, indicates that an FCTL packet preceded by the legal preamble SFD pattern has been received. The identification of FCTL packet is done based on the packet's TYPE and OPCODE fields.
<25>	—	—	RESERVED
<24>	**LNK_CH**	R/W1C	**Link change event**. When *set*, indicates that a change in the port link status has occurred from link OK to link failed or vice versa.
<23>	**RXF_OF**	R/W1C	**RxF overflow**. When *set*, indicates that the 21340-AB port encountered an Rx_FIFO full condition. Assertion of this flag indicates a wrong port setting or system problem.
<22>	**TXF_UF**	R/W1C	**TxF underflow**. When *set*, indicates that an internal error in 21340-AB operation occurred. An underflow error indicates that the 21340-AB port encountered an empty Tx_FIFO during transmission.
<21>	**FCTL_F**	R/W1C	**FCTL_id_Failed**. When *set*, indicates that the 21340-AB can not use its credit-based flow control with the remote node. The 21340-AB port is isolated and aborts received and broadcast packets. The management entity should reinitialize the port's FCTL mode of operation.
<20>	**PRTE**	R/W1C	**Partition event.** When *set*, indicates that the port has been isolated due to partitioning.
<19>	**TXLC**	R/W1C	**Transmit Llate collision.** When *set*, indicates that a transmit late collision event has occurred.

Table 56 STR Bit Fields *(Sheet 3 of 4)*

Bits	Field	Access	Description
<18>	**SCE**	R/W1C	**Short event.** When *set*, indicates that a short event has occurred. A short event is defined as a carrier with duration less then 84 bit-times.
<17>	**JBRI**	R/W1C	**Jabber isolation**. When *set*, indicates that the port has been isolated due to jabber detection.
<16>	**LNK_UI**	R/W1C	**Link unstable isolation.** When *set*, indicates that the port has been isolated due to Llink unstable condition.
<15:12>	—	—	RESERVED
<11>	**SRP_ID**	R	**On_SREP_id.** When *set*, indicates that the 21340-AB port performs remote node identification in order to determine if it can work in either credit-based FCTL or 21340-AB client mode of operation. The 21340-AB port does not store received packets, nor does it load packets seen on the parallel interface.
<10>	**SCR_LK**	R	**Scrambler locked.** When *set*, indicates that the descrambler is locked to the input data signal. Meaningful only when the PHY device connected to the 21340-AB port is SYM PHY.
<9>	**V_BIT**	R	**V_bit.** The status of the port's address filtering valid_bit. When V_bit is *set*, the address stored in the port is valid and the port may pull down the **pkt_abort_l** signal in case the broadcast packet's DA field matched the value it stores. When V_bit is *cleared*, the address stored in the port is not valid.

Table 56 STR Bit Fields *(Sheet 4 of 4)*

Bits	Field	Access	Description
<8>	**F_BIT**	R	**F_bit.** The status of the port's address filtering Flood_bit. When *cleared*, indicates that the 21340-AB port uses its most aggressive level of filtering. When *set,* indicates that the 21340-AB port uses its less or least level of filtering, depending on the setting of V_bit.
<7>	**LNK_F**	R	**Link_Failed.** When *set*, indicates that a link failed event is detected.
<6>	**TXS**	R	**Transmit path is stopped.** When *set*, indicates that the transmit path is stopped.
<5>	**RXS**	R	**Receive path is stopped.** When *set*, indicates that the receive path is stopped.
<4>	**LNK_UN**	R	**Link unstable.** When *set*, indicates that the port is isolated due to link unstable condition.
<3>	**PRT**	R	**Partitioning.** When *set*, indicates that the port is isolated due to partitioning.
<2>	**JAB**	R	**Jabber.** When *set*, indicates that the port is isolated due to jabber detection.
<1>	**BPM**	R	**Backpressure state.** When *set*, indicates that the 21340-AB port, while working in 21340-AB client mode of operation, does not have enough space to receive a new packet – it is in BP mode.
<0>	**FCTL_ON**	R	**FCTL_On.** When *set*, indicates either a 21340-AB-21340-AB connection or the 21340-AB port is using flow control to communicate with its remote node.

Table 57 defines the access rules of the STR register.

Table 57 STR Access Rules

Category	Description
Register access	Read-only register.
Memory address	05H.
Value after reset	00010170H.
Read access rules	—
Write access rules	Bits 11:0 are read only. Bits 30:16 are cleared by write 1.

Note: During initialization, the management unit should set bits <30:16> to 1 to clear them.

5.3.9 Operating Mode Register

Mnemonic: OPM{j}

Offset: 06H

This register establishes the receive and transmit operating modes and commands. It should be the last register to be written in the initialization process. There is one OPM register per each of the four 21340-AB ports.

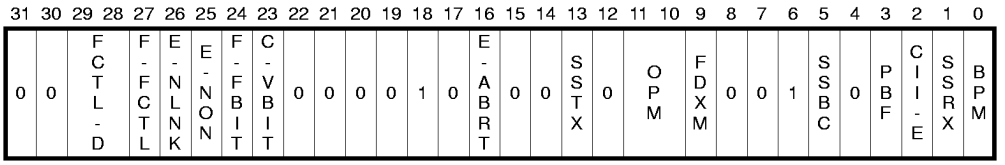


Table 58 defines the bit fields of the OPM register.

Table 58 OPM Bit Fields *(Sheet 1 of 4)*

Bits	Field	Access	Description
<31:30>	MBZ	R/W	**Must Be Zero.**
<29:28>	FCTL_D	R/W	**FCTL_Delay.** Meaningful only when using credit-based flow control. Determines the relationship between free space in the Rx_FIFO and the value sent as credit to the remote node. The FCTL_Delay value takes into account the following delays: • Round-trip delay • FCTL packet transmission delay (packet length) • Sender and remote receiver processing time • Internal margins taken due to Rx-FIFO operation The FCTL_Delay values are: 00 192-byte time delay 01 224-byte time delay 10 256-byte time delay 11 Reserved
<27>	F_FCTL	R/W	**Force_FCTL.** When *set*, the 21340-AB port acts as if linked to a remote node that is capable of running the 21340-AB's flow-control scheme.

Table 58 OPM Bit Fields *(Sheet 2 of 4)*

Bits	Field	Access	Description
<26>	E_NLNK	R/W	**Enable_Nway_link_id.** When *set*, the Nway flow-control identification process state machine is enabled. This bit should be written only during the initialization process.
<25>	E_NON	R/W	**Enable_non_Nway _link_id.** When *set*, the non-Nway flow-control identification process state machine is enabled. This mode should be enabled when either the local port's PHY device has a SYM interface, or the port's remote node is without Auto-Negotiation. This bit should be written only during the initialization process.
<24>	F_FBIT	R/W	**Force_F_bit.** When *set*, the address filtering F-bit is forced to 1. The 21340-AB port may filter only loaded packets when **pkt_abort_l** has been detected low within the first 16-byte time since the start of a packet broadcast. When *cleared*, the F-bit value is determined according to the address filtering function.
<23>	C_VBIT	R/W	**Clear_V_bit.** When *set*, the address filtering V-bit is forced to 0. The remote node address stored in the port is invalid. The port does not notify other peer ports about its address match conditions. When *cleared*, V_bit value is determined according to the address filtering function. When working with external ALT, this bit should be set.
<22:19>	MBZ	—	**Must Be Zero.**
<18>	MBO	—	**Must Be One.**
<17>	MBZ	—	**Must Be Zero.**

Table 58 OPM Bit Fields *(Sheet 3 of 4)*

Bits	Field	Access	Description
<16>	E_ABRT	R/W	**Enable_packet_abort.** When *set*, if **pkt_abort_l** assertion is detected within the first 16-byte time since the start of a packet broadcast, the port aborts the loaded packet until end-of-packet notification is detected. When *cleared*, any packet broadcasted on the parallel interface will be transmitted to the remote node.
<15:14>	MBZ	—	**Must Be Zero.**
<13>	SSTX	R/W	**Start/stop transmit.** When *set*, the transmit path is enabled. When cleared, the transmit path is stopped after completing the transmission of the current frame.
<12>	MBZ	—	**Must Be Zero.**
<11:10>	OPM	R/W	**Operating mode.** 00 Normal. 01 Internal loopback performed on the SYM/MII port. The **mii_txen** signal is disabled. 10 External loopback. 11 Reserved.
<09>	FDXM	R/W	**Full-duplex mode.** When *set*, the 21340-AB port operates in full-duplex mode and can transmit and receive simultaneously. Setting the 21340-AB port to operate in full duplex is allowed only if the remote node is capable of performing the 21340-AB's flow-control scheme and the port FCTL scheme is enabled. This bit should be written during the initialization process.
<08>	MBZ	—	**Must Be Zero.**
<07>	MBZ	—	**Must Be Zero.**
<06>	MBO	—	**Must Be One.**

Table 58 OPM Bit Fields *(Sheet 4 of 4)*

Bits	Field	Access	Description
<05>	SSBC	R/W	**Start/stop_backoff_counter.** When *set*, indicates that the internal backoff counter stops counting when any carrier activity is detected. The backoff counter resumes when the carrier drops. When *reset*, the internal backoff counter is not affected by the carrier activity.
<04>	MBZ	—	**Must Be Zero.**
<03>	PBF	R/W	**Pass_bad_frames.** When *set*, the 21340-AB port broadcasts all incoming frames including runt packets. When *cleared*, runt packets are filtered. The 21340-AB port receives only packets with length greater than or equal to 64 bytes.
<02>	CII_E	R/W	**Carrier_integrity_isolation_enable.** When *set*, the Carrier Integrity Checking and Isolation mechanism is enabled. The media is checked for link unstable events. When *cleared*, the false Carrier Integrity Checking and Isolation mechanism is disabled.
<01>	SSRX	R/W	**Start/stop_receive.** When *set*, the receive path is enabled. When *cleared*, the receive path enters the stopped state after completing the reception of the current frame.
<00>	BPM	R/W	**BP_mode_selection.** Only affected when the 21340-AB port is initialized to work in 21340-AB client mode of operation. This bit determines the backpressure method that the port uses. When *set*, the 21340-AB port collides every received packet with 96-bit JAM pattern. When *cleared*, the 21340-AB port uses a special BP packet scheme for backpressuring the physical link. This bit should be written during the initialization process.

Table 59 defines the 21340-AB flow-control modes that can be achieved with various settings of the OPM bits.

Table 59 OPM Settings/21340-AB Flow-Control Modes

OPM[i]<9>/OPM[i]<27:25>	Description
0/000	Flow-control identification and operation are disabled. The 21340-AB port uses BP algorithm as determined in OPM[i]<0> for data transfer.
0/001	Non-Nway identification process is enabled. This mode is used when the remote PHY device does not have Auto-Negotiation, or the local PHY has a SYM interface. The first stage of the detection process is performed in HDX link. The transition to FDX is done by the management unit after it detects that the FCTL_On flag is set.
0/010	Nway half-duplex identification process is enabled. (Used for MII 100BASE-T4 PHY device.)
X/011	ILLEGAL COMBINATION.
0/1XX	Forced half-duplex flow-control connection.
1/000	ILLEGAL COMBINATION.
1/001	This mode is set when the non-Nway identification process has detected the remote node as 21340-AB FCTL 100BASE-TX-capable.
1/010	Full-duplex Nway identification process is enabled. This mode should be used when the local PHY device is an MII FDX device and the remote PHY node is an FDX PHY device with Auto-Negotiation capabilities.
1/1XX	Forced full-duplex flow-control connection.

Table 60 defines the access rules of the OPM register.

Table 60 OPM Access Rules

Category	Description
Register access	Read/Write
Register address offset	06H
Value after reset	000C004CH
Read access rules	—
Write access rules	—

Note: To work in the FDX mode of operation:

- Disable the false_carrier_isolation function while initializing the port.
- Disable the jabber isolation function.

Clear the CII_E bit while internal loopback mode is activated.

5.3.10 Management Control Register

Mnemonic: MTC

Offset: 09H

This register provides an interface to the MII management entity and the general-purpose ports.

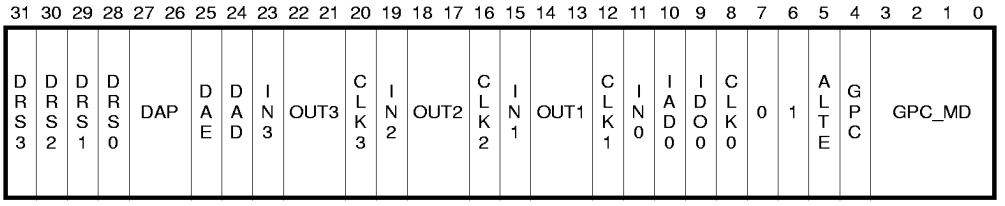


Table 61 defines the bit fields of the MTC register.

Table 61 MTC Bit Fields *(Sheet 1 of 4)*

Bits	Field	Access	Description
<31>	**DRS3**	R/W	**Port 3 10/100 data rate selection.** Selects the port 3 MII/SYM data rate of 100 Mb/s or 10 Mb/s. When *set*, the data rate is selected to be 10 Mb/s. The MII/SYM should be set to MII mode (JBR[3]<9> = 0). When *cleared*, the data rate is selected to be 100 Mb/s. The MII/SYM mode is selected by JBR[3]<9>.
<30>	**DRS2**	R/W	**Port 2 10/100 data rate selection.** Selects the port 2 MII/SYM data rate of 100 Mb/s or 10 Mb/s. When *set*, the data rate is selected to be 10 Mb/s. The MII/SYM should be set to MII mode (JBR[2]<9> = 0). When *cleared*, the data rate is selected to be 100 Mb/s. The MII/SYM mode is selected by JBR[2]<9>.
<29>	**DRS1**	R/W	**Port 1 10/100 data rate selection.** Selects the port 1 MII/SYM data rate of 100 Mb/s or 10Mb/s. When *set*, the data rate is selected to be 10 Mb/s. The MII/SYM should be set to MII mode (JBR[1]<9> = 0). When *cleared*, the data rate is selected to be 100 Mb/s. The MII/SYM mode is selected by JBR[1]<9>.

Table 61 MTC Bit Fields *(Sheet 2 of 4)*

Bits	Field	Access	Description
<28>	DRS0	R/W	**Port 0 10/100 data rate selection**. Selects the port 0 MII/SYM data rate of 100 Mb/s or 10 Mb/s. When *set*, the data rate is selected to be 10 Mb/s. The MII/SYM should be set to MII mode (JBR[0]<9> = 0). When *cleared*, the data rate is selected to be 100 Mb/s. The MII/SYM mode is selected by JBR[0]<9>.
<27:26>	DAP	R/W	**MII direct access port number.** Determines the port number where the MII direct access operation is performed. **MII_Direct_Access_Port_Number Port** 00 0 01 1 10 2 11 3
<25>	DAE	W	**MII direct access mode enable.** Controls the MII direct mode operation when the next management access is a direct access to the MII PHY device registers. This bit is reset upon deassertion of **mcs**.
<24>	DAD	R/W	**MII direct access mode direction.** Determines the MII direct mode operation: 0 — Read operation 1 — Write operation
<23>	IN3	R	**MII management data_in bit, port 3.**
<22:21>	OUT3	R/W	**MII management mode/data_out bit, port 3.**
<20>	CLK3	R/W	**MII management clock bit, port 3.**
<19>	IN2	R	**MII management data_in bit, port 2.**
<18:17>	OUT2	R/W	**MII management mode/data_out bit, port 2.**
<16>	CLK2	R/W	**MII management clock bit, port 2.**
<15>	IN1	R	**MII management data_in bit, port 1.**
<14:13>	OUT1	R/W	**MII management mode/data_out bit, port 1.**
<12>	CLK1	R/W	**MII management clock bit, port 1.**

Table 61 MTC Bit Fields *(Sheet 3 of 4)*

Bits	Field	Access	Description
<11>	IN0	R	**MII management data_in bit, port 0.** Used by the 21340-AB to read data from the PHY connected to port 0.
<10>	IAD0	R/W	**Indirect access direction, MII port 0.** Defines the direction of the MII indirect access for the MII PHY device registers. 0 — Write 1 — Read
<9>	IDO0	W	**Indirect access data_out bit, port 0**. Sets the value that will be driven on the **mdio** pin for a write access.
<08>	CLK0	R/W	**MII management clock_bit, port 0.** Controls the **mii_mdc_0** signal to the PHY connected to port 0. It is used as a timing reference.
<07>	MBZ		**Must Be Zero.**
<06>	MBO	R/W	**Must Be One.**
<05>	ALTE	R/W	**External ALT enable.** When *set*, the 21340-AB **pkt_abort_l** signals are interpreted as per-port connections. External ALT logic can be used in order to abort storing of packets not targeted to the port. When *set*, Clear_V_bit should be set as well (OPM[i]<23>). When *cleared*, the 21340-AB **pkt_abort_l** signals are interpreted as per-segment. In this mode, external ALT can not be used.
<04>	GPC	R/W	**General-purpose control.**

Table 61 MTC Bit Fields *(Sheet 4 of 4)*

Bits	Field	Access	Description
<03:00>	**GPC_MD**	R/W	**General-purpose mode and data.** When MTC<4> is set, the value written to MTC<3:0> sets the direction of each **gep** pin to be either input or output. For example, if MTC<3> is 1, then **gep<3>** is defined as an output pin. If MTC<3> is 0, then **gep<3>** is defined as input. When MTC<4> is cleared, writing a value to MTC<3:0> sets values on the pins configured as output pins. Reading MTC<3:0> reflects the input values of the pins configured as input pins. When a hardware reset is initiated, all **gep** pins become input pins.

Table 62 defines the access rules of the MTC register.

Table 62 MTC Access Rules

Category	Description
Register access	Read/Write
Register address offset	09H
Value after reset	00XXXX4XH
Read access rules	—
Write access rules	—

Note: When accessing the MII management pins, the management unit can use either direct accessing mode or the serial accessing mode using the port's management_data_in, management_data_out/mode, and management_clock control pins.

The management unit should not change the accessing mode during MII register operation.

After hardware reset, MTC bits <23>, <19>, <15>, <11>, and <3:0> get their values from the corresponding input pins.

5.3.11 Chip Identification Register

Mnemonic: CID

Offset: 0AH

This register identifies the 21340-AB as an electrical component and as a part in a group of several 21340-AB chips connected in the same repeater box.

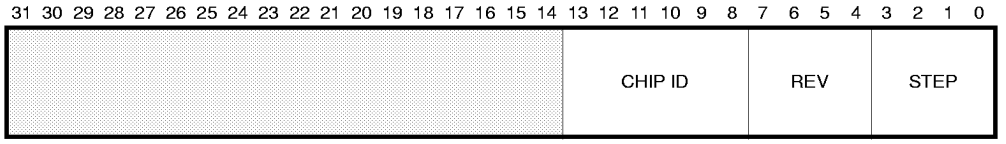


Table 63 defines the bit fields of the CID register.

Table 63 CID Bit Fields

Bits	Field	Access	Description
<31:14>	—	—	RESERVED
<13:08>	**CHIP ID**	R/W	Chip identification number. This field is part of the statistical information appended to each packet as it is broadcasted onto the parallel bus segment. It is used to identify the packet's source.
<07:04>	**REV**	R	**Revision number.** Indicates the 21340-AB revision number. It is equal to 2H.
<03:00>	**STEP**	R	**Step number.** Indicates the 21340-AB step number. It is equal to 1H.

Table 64 defines the access rules of the CID register.

Table 64 CID Access Rules

Category	Description
Register access	R/W.
Register address offset	0AH.
Value after reset	00000021H.
Read access rules	None.
Write access rules	Bits <7:0> are read-only. Bits <13:08> are read/write. This register should be written only during the initialization process.

5.3.12 Vendor Identification Register

Mnemonic: VID

Offset: 0BH

This register identifies the 21340-AB as an electrical component.

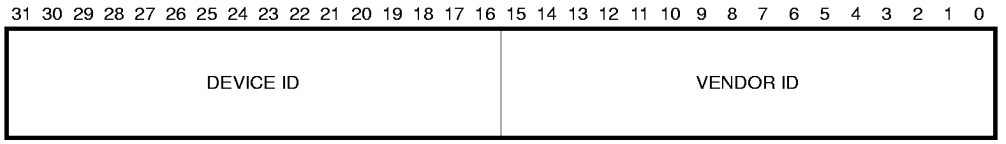


Table 65 defines the bit fields of the VID register.

Table 65 VID Bit Fields

Bits	Field	Access	Description
<31:16>	**DEVICE ID**	R	**Device ID.** Provides the unique 21340-AB ID number (1050H).
<15:00>	**VENDOR ID**	R	**Vendor ID.** Specifies the manufacturer of the 21340-AB (1011H).

Table 66 defines the access rules of the VID register.

Table 66 VID Access Rules

Category	Description
Register access	Read-only register
Register address offset	0BH
Value after reset	10501011H
Read access rules	None
Write access rules	Read-only register

5.3.13 Port Timers Register

Mnemonic: PTR{j}

Offset: 0CH

This register is used for defining the expiration values for the 21340-AB timers. It defines the T1 and T2 timers, which are used for the 21340-AB port address filtering algorithm.

The T1 timer is set on every received packet and indicates that its SA address, stored in the port, is the valid remote node address. The T1 timer expiration event clears the V_bit. T2 is set on receiving a packet with a new SA. When the T2 timer expires, F-bit is cleared.

This register has no meaning if the internal address filtering feature is disabled (OPM<23> is set). There is one PTR register per each of the 21340-AB ports.

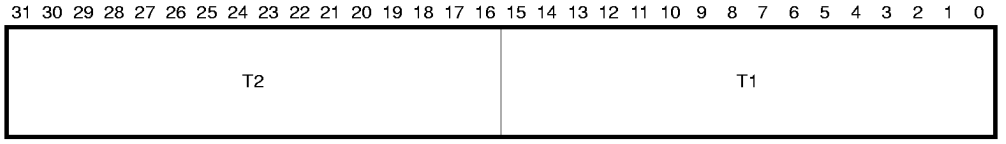


Table 67 defines the bit fields of the PTR register.

Table 67 PTR Bit Fields

Bits	Field	Access	Description
<31:16>	**T2**	R/W	**T2 timer limit**. Defines the expiration limit of the T2 counter used to detect if a port is connected to single or multiple end-stations. The T2 timer value +1 multiplied by 0.335 seconds results in the absolute time of expiration.
<15:00>	**T1**	R/W	**T1 timer limit**. Defines the expiration limit of the T1 counter used to detect if a port is connected to a valid end-node. The T1 timer value + 1 multiplied by 0.335 seconds results in the absolute time of expiration.

Table 68 defines the access rules of the PTR register.

Table 68 PTR Access Rules

Category	Description
Register access	Read/Write
Register address offset	0CH
Value after reset	00C00020H
Read access rules	None
Write access rules	None

5.3.14 Port Segmentation Control Register

Mnemonic: PSC

Offset: 0DH

This register is used for defining the 21340-AB segmentation configuration. It defines to which parallel segment each 21340-AB port is connected.

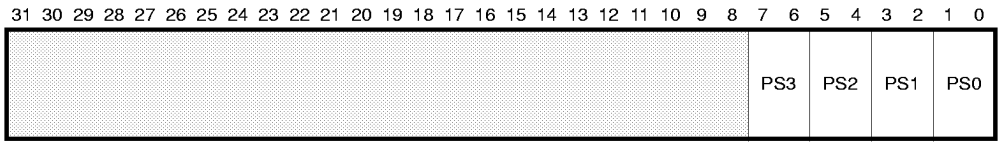


Table 69 defines the bit fields of the PSC register.

Table 69 PSC Bit Fields

Bits	Field	Access	Description
<31:08>	—	—	RESERVED
<07:06>	**PS3**	R/W	**Port 3 segment.** Defines the parallel segment to which 21340-AB port 3 is connected.
<05:04>	**PS2**	R/W	**Port 2 segment.** Defines the parallel segment to which 21340-AB port 2 is connected.
<03:02>	**PS1**	R/W	**Port 1 segment.** Defines the parallel segment to which 21340-AB port 1 is connected.
<01:00>	**PS0**	R/W	**Port 0 segment**. Defines the parallel segment to which 21340-AB port 0 is connected.

Table 70 defines the access rules of the PSC register.

Table 70 PSC Access Rules

Category	Description
Register access	Read/Write.
Register address offset	0DH.
Value after reset	00000000H.
Read access rules	None.
Write access rules	The management entity should not modify this register during the packet broadcasting phase. This may cause UNPREDICTABLE port behavior.

Note: The writing should be done only after verifying that the relevant segments are in Idle state. See Section 5.3.18.1.

5.3.15 Jabber Register

Mnemonic: JBR{j}

Offset: 0FH

This register is used to control the jabber detection function. There is one JBR register per each of the four 21340-AB ports.

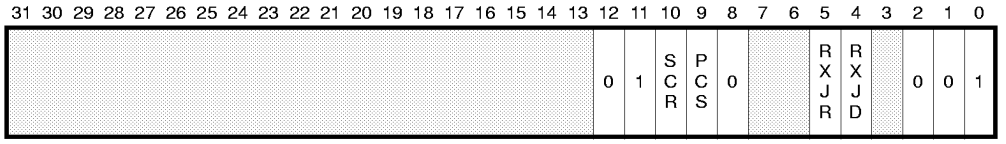


Table 71 defines the bit fields of the JBR register.

Table 71 JBR Bit Fields *(Sheet 1 of 2)*

Bits	Field	Access	Description
<31:13>	—	—	RESERVED
<12>	**MBZ**	R/W	**Must Be Zero.**
<11>	**MBO**	R/W	**Must Be One.**
<10>	**SCR**	—	**SCR.** Scrambler Mode. When *set*, the scrambler function is active and the MII/SYM port transmits and receives scrambled symbols.
<09>	**PCS**	—	**PCS.** When *set*, the MII/SYM port operates in SYM mode. When *cleared*, the MII/SYM port operates in MII mode. All MII/SYM port control signals are generated internally.
<08>	**MBZ**	R/W	**Must Be Zero.**
<07:06>	—	—	RESERVED

Table 71 JBR Bit Fields *(Sheet 2 of 2)*

Bits	Field	Access	Description
<05>	RXJR	—	**Receive jabber release**. Defines the time interval *from* the moment the jabber condition terminated *to* the receive packet operation. When *set*, the receive path is reenabled 40–48 bit-times from the last carrier deassertion. When *reset*, the receive path is re-enabled 16–24 bit-times from the last carrier deassertion.
<04>	RXJD	—	**Receive jabber disable.** When *set*, the receive jabber counter is disabled. When *reset*, receive carriers longer than 40,561 bit-times cause the jabber counter to time out and to isolate the node due to jabber detection. Receive carriers shorter than 140,960 bit-times do not activate the jabber isolation mechanism.
<03>	—	—	RESERVED
<02:01>	MBZ	R/W	**Must Be Zero**.
<00>	MBO	R/W	**Must Be One**.

Table 72 defines the access rules of the JBR register.

Table 72 JBR Access Rules

Category	Description
Register access	Read/Write.
Register address offset	0FH.
Value after reset	00000801H.
Read access rules	None.
Write access rules	Writing is allowed only when the port's receive and transmit paths are stopped (STR{j}<6:5> are set).

5.3.16 Operation Mode 2 Register

Mnemonic: OPM2{j}

Offset: 40H

This register establishes the new operating modes and features added to 21340-AB.

There is one OPM2 register for each of the four 21340-AB ports.

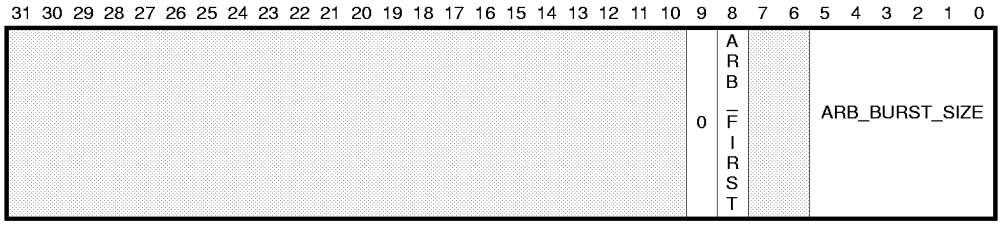


Table 73 defines the bit fields of the OPM2 register.

Table 73 OPM2 Bit Fields

Bits	Field	Access	Description
<31:10>	—	—	RESERVED
<9>	**MBZ**	—	**Must be zero.**
<08>	**ARB_FIRST**	R/W	**Arbiter first.** When *set*, the port issues the first token to the next port inline sharing the same segment, after initialization is completed. The management needs to set this bit to only one port per segment. Setting it to more than one port per segment may lead to IMPROPER behavior. Meaningful only when the internal arbitration scheme is enabled.
<07:06>	**MBZ**	—	**Must be zero.**
<05:00>	**ARB_BURST_SIZE**	R/W	**Arbiter burst size.** Defines the size of the allowed burst of packets a port is allowed to broadcast over the parallel interface segment before it needs to pass the token to the next port inline. Meaningful only when the internal arbitration scheme is enabled.

Table 74 defines the access rules of the OPM2 register.

Table 74 OPM2 Access Rules

Category	Description
Register access	Read/Write.
Register address offset	40H.
Value after reset	00000001H.
Read access rules	None.
Write access rules	Meaningful only when the internal arbitration scheme is enabled. Should be written after device ports are assigned to the proper segment by writing to the 21340-AB's PSC register, and after the segment's chain is connected by writing the 21340-AB's GOR register.

Note: See Section 5.3.18.1 for the initialization sequence.

5.3.17 Device Interrupt Status Register

Mnemonic: ISR

Offset: 41H

This register contains interrupt status indications describing the nature and source of the interrupt.

The management entity can identify the source port of the interrupt and its nature when reading this register. It can then read the specific port's status register to identify and handle the interrupt cause.

This register reduces the number of status register read operations the management performs to identify and treat the source of the interrupt.

Interrupts are divided into three groups per 21340-AB port:

- **Error event interrupts**
  This group includes the following interrupt events: NO_GNT, RXF_OF, TXF_UF, LNK_FE, TXLC, and SCE.
- **Informative event interrupt**
  This group includes the following event: FCTL_F, FCTL_ON, PRTE, JBRI, and LNK_UI.
- **Service event interrupts**
  This group includes all statistic counters' overflow interrupt events.

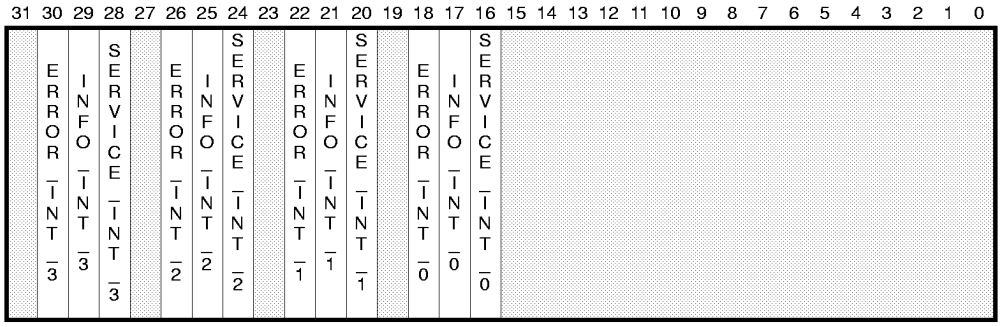


Table 75 defines the bit fields of the ISR register.

Table 75 ISR Bit Fields *(Sheet 1 of 2)*

Bits	Field	Access	Description
<31>	—	—	RESERVED
<30>	**ERROR_INT_3**	R	**Port 3 error event asserted.** When *set*, indicates that one of the unmasked error events of port 3 is asserted. This field is cleared only when all unmasked error events in port 3 are cleared.
<29>	**INFO_INT_3**	R	**Port 3 info event asserted.** When *set*, indicates that one of the unmasked info events of port 3 is asserted. This field is cleared only when all unmasked info events in port 3 are cleared.
<28>	**SERVICE_INT_3**	R	**Port 3 service event asserted.** When *set*, indicates that one of the unmasked service events of port 3 is asserted. This field is cleared only when all unmasked service events in port 3 are cleared.
<27>	—	—	RESERVED
<26>	**ERROR_INT_2**	R	**Port 2 error event asserted.** When *set*, indicates that one of the unmasked error events of port 2 is asserted. This field is cleared only when all unmasked error events in port 2 are cleared.
<25>	**INFO_INT_2**	R	**Port 2 info event asserted.** When *set*, indicates that one of the unmasked info events of port 2 is asserted. This field is cleared only when all unmasked info events in port 2 are cleared.
<24>	**SERVICE_INT_2**	R	**Port 2 service event asserted.** When *set*, indicates that one of the unmasked service events of port 2 is asserted. This field is cleared only when all unmasked service events in port 2 are cleared.
<23>	—	—	RESERVED

Table 75 ISR Bit Fields *(Sheet 2 of 2)*

Bits	Field	Access	Description
<22>	**ERROR_INT_1**	R	**Port 1 error event asserted.** When *set*, indicates that one of the unmasked error events of port 1 is asserted. This field is cleared only when all unmasked error events in port 1 are cleared.
<21>	**INFO_INT_1**	R	**Port 1 info event asserted.** When *set*, indicates that one of the unmasked info events of port 1 is asserted. This field is cleared only when all unmasked info events in port 1 are cleared.
<20>	**SERVICE_INT_1**	R	**Port 1 service event asserted.** When *set*, indicates that one of the unmasked service events of port 1 is asserted. This field is cleared only when all unmasked service events in port 1 are cleared.
<19>	—	—	RESERVED
<18>	**ERROR_INT_0**	R	**Port 0 error event asserted.** When *set*, indicates that one of the unmasked error events of port 0 is asserted. This field is cleared only when all unmasked error events in port 0 are cleared.
<17>	**INFO_INT_0**	R	**Port 0 info event asserted.** When *set*, indicates that one of the unmasked info events of port 0 is asserted. This field is cleared only when all unmasked info events in port 0 are cleared.
<16>	**SERVICE_INT_0**		**Port 0 service event asserted.** When *set*, indicates that one of the unmasked service events of port 0 is asserted. This field is cleared only when all unmasked service events in port 0 are cleared.
<15:0>	—	—	RESERVED

Table 76 defines the access rules of the ISR register.

Table 76 ISR Access Rules

Category	Description
Register access	Read-only register
Register address offset	41H
Value after reset	00000000H
Read access rules	None
Write access rules	Read-only register

5.3.18 Global Operation Register

Mnemonic: GOR

Offset: 42H

This register controls the operating modes and features added to 21340-AB, that are controlled per device.

There is one GOR register per 21340-AB device.

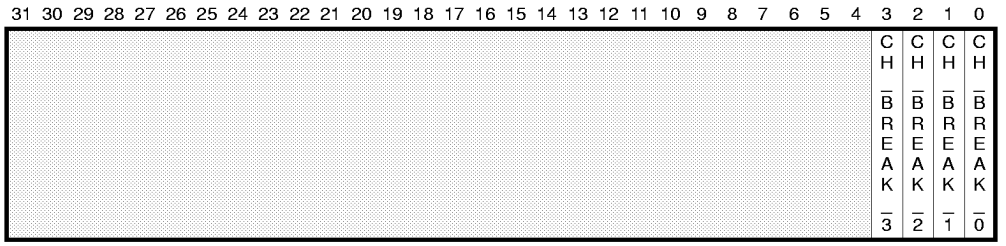


Table 77 defines the bit fields of the GOR register.

Table 77 GOR Bit Fields *(Sheet 1 of 2)*

Bits	Field	Access	Description
<31:04>	—	—	RESERVED
<03>	**CH_BREAK_3**	R/W	**Segment 3 chain break.** When *set*, the segment 3 token passing chain is torn. As a result, the port holding the arbitration token will not pass it to the next port inline. The management entity can therefore modify the port's segmentation assignment. Meaningful only when the internal arbitration scheme is activated.
<02>	**CH_BREAK_2**	R/W	**Segment 2 chain break.** When *set*, the segment 2 token passing chain is torn. As a result, the port holding the arbitration token will not pass it to the next port inline. The management entity can therefore modify the port's segmentation assignment. Meaningful only when the internal arbitration scheme is activated.

Table 77 GOR Bit Fields *(Sheet 2 of 2)*

Bits	Field	Access	Description
<01>	**CH_BREAK_1**	R/W	**Segment 1 chain break.** When *set*, the segment 1 token passing chain is torn. As a result, the port holding the arbitration token will not pass it to the next port inline. The management entity can therefore modify the port's segmentation assignment. Meaningful only when the internal arbitration scheme is activated.
<00>	**CH_BREAK_0**	R/W	**Segment 0 chain break.** When *set*, the segment 0 token passing chain is torn. As a result, the port holding the arbitration token will not pass it to the next port inline. The management entity can therefore modify the port's segmentation assignment. Meaningful only when the internal arbitration scheme is activated.

Table 78 defines the access rules of the GOR register.

Table 78 GOR Access Rules

Category	Description
Register access	Read/Write.
Register address offset	42H.
Value after reset	0000000FH.
Read access rules	None.
Write access rules	Needs to be written before initialization is complete. Should be written after device ports are assigned to the proper segment by writing the 21340-AB PSC register.

Note: See Figure 35 for GOR enable initialization and requirements.

5.3.18.1 Port Assignment Initialization Sequence

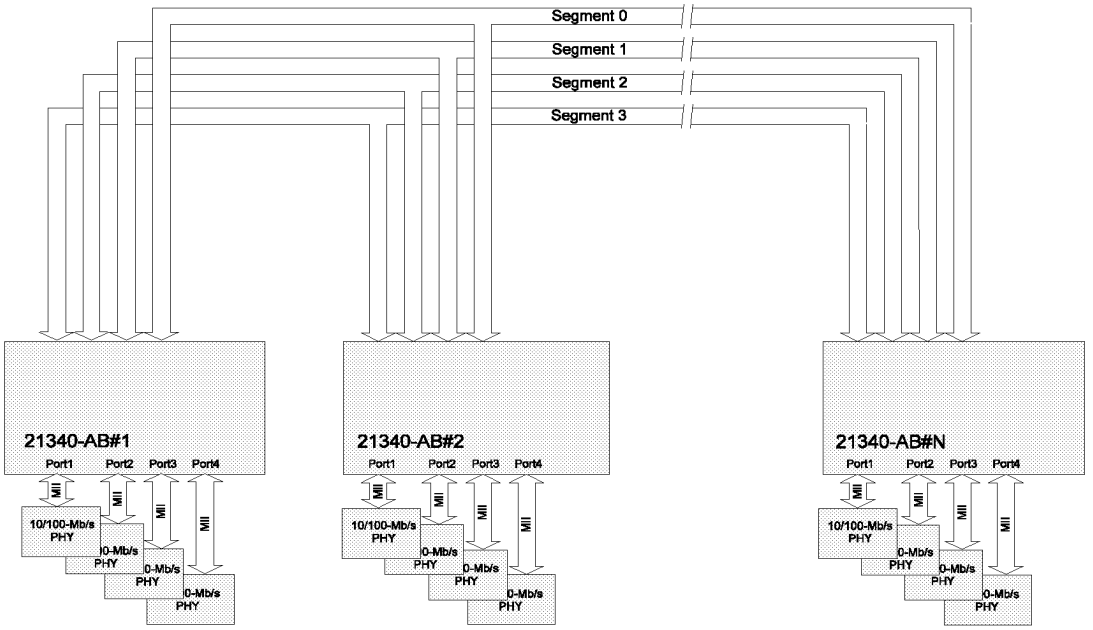
The GOR PSC and OPM2 control the assignment and reassignment of ports to segments.

For every change in the assignment of ports to segments, the following scheme should be applied for each segment:

1. Break the token ring in the relevant segment by asserting the corresponding bit of the GOR register in the device that initiated the token in that segment (the device with its OPM{j}<ARB_FIRST> set).
   This operation tears the token ring and clears the OPM{j}<ARB_FIRST> control bit.
2. Verify that the segments, of which token rings were torn, are in the Idle state. This can be done by activating the watchdog timer that expires when there are no more packets broadcasted over the segment.
3. Reassign ports to segments by modifying the appropriate 21340-AB device's PSC registers.
4. Reconnect the segment's token ring by deasserting the corresponding bits of the GOR register in all devices assigned to the relevant segment.
5. Initiate the token by writing the OPM2{j}<ARB_FIRST> control bit in only one port sharing this segment.

Figure 35 shows an example of an initialization scheme in a four-segment system.

Figure 35 Four-Segment System



Port#1 in 21340-AB#1 needs to be assigned to segment#0;
Port#2 in 21340-AB#1 needs to be assigned to segment#0;
Port#3 in 21340-AB#1 needs to be assigned to segment#1;
Port#4 in 21340-AB#1 needs to be assigned to segment#3;

Port#1 in 21340-AB#2 needs to be assigned to segment#0;
Port#2 in 21340-AB#2 needs to be assigned to segment#1;
Port#3 in 21340-AB#2 needs to be assigned to segment#2;
Port#4 in 21340-AB#2 needs to be assigned to segment#2;

Port#1 in 21340-AB#N needs to be assigned to segment#1;
Port#2 in 21340-AB#N needs to be assigned to segment#1;
Port#3 in 21340-AB#N needs to be assigned to segment#3;
Port#4 in 21340-AB#N needs to be assigned to segment#3;

To initialize a four-segment system, apply the following scheme to each segment:

1. Break the four segment token rings by setting the 21340-AB#1, 21340-AB#2, and 21340-AB#N GORs to be oxOF.
   This operation will clear the appropriate OPM{j}<ARB_FIRST> control bits.
2. Initialize the PSC register as follows:
   - Set 21340-AB#1 PSC to 0xD0.
   - Set 21340-AB#2 PSC to 0xA4.
   - Set 21340-AB#N PSC to 0xF5.
3. Reconnect the segment's token rings by setting the 21340-AB#1, 21340-AB#2, and 21340-AB#N GORs to be ox00.
4. Initiate the tokens of the segments by choosing *only one* port per segment to initiate the token. For example:
   - Set 21340-AB#1 OPM2{of port#1} ARB_FIRST control bit to initiate the segment#0 token.
   - Set 21340-AB#1 OPM2{of port#3} ARB_FIRST control bit to initiate the segment#1 token.
   - Set 21340-AB#1 OPM2{of port#4} ARB_FIRST control bit to initiate the segment#3 token.
   - Set 21340-AB#2 OPM2{of port#4} ARB_FIRST control bit to initiate the segment#2 token.

5.3.19 Management Interrupt Mask Register 1

Mnemonic: MIMSK1{j}

Offset: 43H

This register enables masking the statistic counters overflow interrupt conditions.

There is one MIMSK1 register per 21340-AB device.

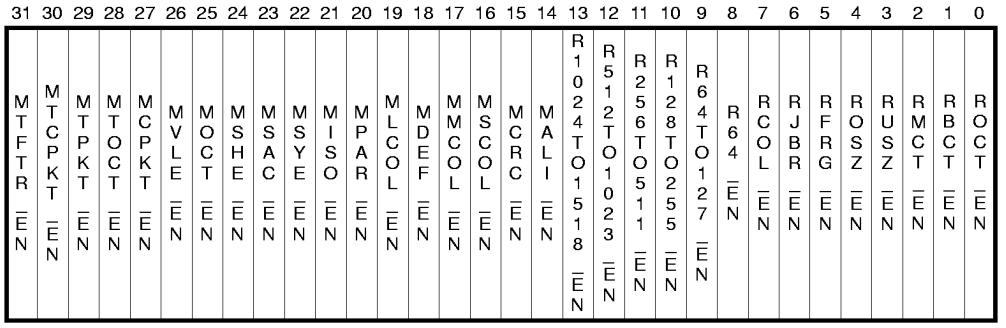


Table 79 defines the bit fields of the MIMSK1 register.

Table 79 MIMSK1 Bit Fields *(Sheet 1 of 6)*

Bits	Field	Access	Description
<31>	**MTFTR_EN**	R/W	**MTFTR interrupt event enable.** When *set*, enables an interrupt in case the MTFTR counter wraps around. When *cleared*, disables the interrupt line in case the MTFTR counter wraps around.
<30>	**MTCPKT_EN**	R/W	**MTCPKT interrupt event enable.** When *set*, enables an interrupt in case the MTCPKT counter wraps around. When *cleared*, disables the interrupt line in case the MTCPKT counter wraps around.
<29>	**MTPKT_EN**	R/W	**MTPKT interrupt event enable.** When *set*, enables an interrupt in case the MTPKT counter wraps around. When *cleared*, disables the interrupt line in case the MTPKT counter wraps around.

Table 79 MIMSK1 Bit Fields *(Sheet 2 of 6)*

Bits	Field	Access	Description
<28>	MTOCT_EN	R/W	**MTOCT interrupt event enable.** When *set*, enables an interrupt in case the MTOCT counter wraps around. When *cleared*, disables the interrupt line in case the MTOCT counter wraps around.
<27>	MCPKT_EN	R/W	**MCPKT interrupt event enable.** When *set*, enables an interrupt in case the MCPKT counter wraps around. When *cleared*, disables the interrupt line in case the MCPKT counter wraps around.
<26>	MVLE_EN	R/W	**MVLE interrupt event enable.** When *set*, enables an interrupt in case the MVLE counter wraps around. When *cleared*, disables the interrupt line in case the MVLE counter wraps around.
<25>	MOCT_EN	R/W	**MOCT interrupt event enable.** When *set*, enables an interrupt in case the MOCT counter wraps around. When *cleared*, disables the interrupt line in case the MOCT counter wraps around.
<24>	MSHE_EN	R/W	**MSHE interrupt event enable.** When *set*, enables an interrupt in case the MSHE counter wraps around. When *cleared*, disables the interrupt line in case the MSHE counter wraps around.
<23>	MSAC_EN	R/W	**MSAC interrupt event enable.** When *set*, enables an interrupt in case the MSAC counter wraps around. When *cleared*, disables the interrupt line in case the MSAC counter wraps around.
<22>	MSYE_EN	R/W	**MSYE interrupt event enable.** When *set*, enables an interrupt in case the MSYE counter wraps around. When *cleared*, disables the interrupt line in case the MSYE counter wraps around.

Table 79 MIMSK1 Bit Fields *(Sheet 3 of 6)*

Bits	Field	Access	Description
<21>	MISO_EN	R/W	**MISO interrupt event enable.** When *set*, enables an interrupt in case the MISO counter wraps around. When *cleared*, disables the interrupt line in case the MISO counter wraps around.
<20>	MPAR_EN	R/W	**MPAR interrupt event enable.** When *set*, enables an interrupt in case the MPAR counter wraps around. When *cleared*, disables the interrupt line in case the MPAR counter wraps around.
<19>	MLCOL_EN	R/W	**MLCOL interrupt event enable.** When *set*, enables an interrupt in case the MLCOL counter wraps around. When *cleared*, disables the interrupt line in case the MLCOL counter wraps around.
<18>	MDEF_EN	R/W	**MDEF interrupt event enable.** When *set*, enables an interrupt in case the MDEF counter wraps around. When *cleared*, disables the interrupt line in case the MDEF counter wraps around.
<17>	MMCOL_EN	R/W	**MMCOL interrupt event enable.** When *set*, enables an interrupt in case the MMCOL counter wraps around. When *cleared*, disables the interrupt line in case the MMCOL counter wraps around.
<16>	MSCOL_EN	R/W	**MSCOL interrupt event enable.** When *set*, enables an interrupt in case the MSCOL counter wraps around. When *cleared*, disables the interrupt line in case the MSCOL counter wraps around.
<15>	MCRC_EN	R/W	**MCRC interrupt event enable.** When *set*, enables an interrupt in case the MCRC counter wraps around. When *cleared*, disables the interrupt line in case the MCRC counter wraps around.

Table 79 MIMSK1 Bit Fields *(Sheet 4 of 6)*

Bits	Field	Access	Description
<14>	MALI_EN	R/W	**MALI interrupt event enable.** When *set*, enables an interrupt in case the MALI counter wraps around. When *cleared*, disables the interrupt line in case the MALI counter wraps around.
<13>	R1024TO1518_EN	R/W	**R1024TO1518 interrupt event enable.** When *set*, enables an interrupt in case the R1024TO1518 counter wraps around. When *cleared*, disables the interrupt line in case the R1024TO1518 counter wraps around.
<12>	R512TO1023_EN	R/W	**R512TO1023 interrupt event enable.** When *set*, enables an interrupt in case the R512TO1023 counter wraps around. When *cleared*, disables the interrupt line in case the R512TO1023 counter wraps around.
<11>	R256TO511_EN	R/W	**R256TO511 interrupt event enable.** When *set*, enables an interrupt in case the R256TO511 counter wraps around. When *cleared*, disables the interrupt line in case the R256TO511 counter wraps around.
<10>	R128TO255_EN	R/W	**R128TO255 interrupt event enable.** When *set*, enables an interrupt in case the R128TO255 counter wraps around. When *cleared*, disables the interrupt line in case the R128TO255 counter wraps around.
<09>	R65TO127_EN	R/W	**R65TO127 interrupt event enable.** When *set*, enables an interrupt in case the R65TO127 counter wraps around. When *cleared*, disables the interrupt line in case the R65TO127 counter wraps around.
<08>	R64_EN	R/W	**R64 interrupt event enable.** When *set*, enables an interrupt in case the R64 counter wraps around. When *cleared*, disables the interrupt line in case the R64 counter wraps around.

Table 79 MIMSK1 Bit Fields *(Sheet 5 of 6)*

Bits	Field	Access	Description
<07>	RCOL_EN	R/W	**RCOL interrupt event enable.** When *set*, enables an interrupt in case the RCOL counter wraps around. When *cleared*, disables the interrupt line in case the RCOL counter wraps around.
<06>	RJBR_EN	R/W	**RJBR interrupt event enable.** When *set*, enables an interrupt in case the RJBR counter wraps around. When *cleared*, disables the interrupt line in case the RJBR counter wraps around.
<05>	RFGR_EN	R/W	**RFGR interrupt event enable.** When *set*, enables an interrupt in case the RFGR counter wraps around. When *cleared*, disables the interrupt line in case the RFGR counter wraps around.
<04>	ROSZ_EN	R/W	**ROSZ interrupt event enable.** When *set*, enables an interrupt in case the ROSZ counter wraps around. When *cleared*, disables the interrupt line in case the ROSZ counter wraps around.
<03>	RUSZ_EN	R/W	**RUSZ interrupt event enable.** When *set*, enables an interrupt in case the RUSZ counter wraps around. When *cleared*, disables the interrupt line in case the RUSZ counter wraps around.

Table 79 MIMSK1 Bit Fields *(Sheet 6 of 6)*

Bits	Field	Access	Description
<02>	**RMCT_EN**	R/W	**RMCT interrupt event enable.** When *set*, enables an interrupt in case the RMCT counter wraps around. When *cleared*, disables the interrupt line in case the RMCT counter wraps around.
<01>	**RBCT_EN**	R/W	**RBCT interrupt event enable.** When *set*, enables an interrupt in case the RBCT counter wraps around. When *cleared*, disables the interrupt line in case the RBCT counter wraps around.
<00>	**ROCT_EN**	R/W	**ROCT interrupt event enable.** When *set*, enables an interrupt in case the ROCT counter wraps around. When *cleared*, disables the interrupt line in case the ROCT counter wraps around.

Table 80 defines the access rules of the MIMSK1 register.

Table 80 MIMSK1 Access Rules

Category	Description
Register access	Read/Write
Register address offset	43H
Value after reset	00000000H
Read access rules	None
Write access rules	None

5.3.20 Management Interrupt Mask Register 2

Mnemonic: MIMSK2{j}

Offset: 44H

This register enables masking of error and informative event interrupts.

There is one MIMSK2 register per 21340-AB port.

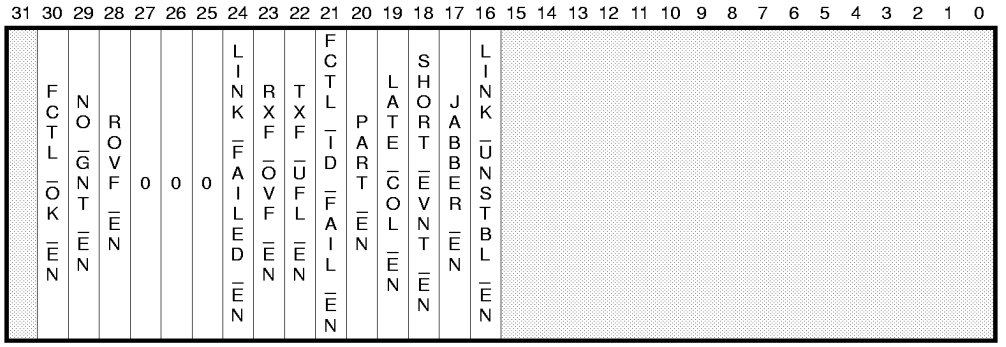


Table 81 defines the bit fields of the MIMSK2 register.

Table 81 MIMSK2 Bit Fields *(Sheet 1 of 3)*

Bits	Field	Access	Description
<31>	—	—	RESERVED
<30>	**FCTL_OK_EN**	R/W	**Flow-control OK event enable.** When *set*, enables an interrupt when the 21340-AB credit-based auto-configuration process had succeeded and the remote node identified as 21340-AB flow-control capable.
<29>	**NO_GNT_EN**	R/W	**No grant interrupt event enable.** When *set*, enables an interrupt if no grant has been issued to the port for at least 0.33 seconds after assertion of the port's **req** pin. When the internal arbitration is enabled, the interrupt is asserted.

Table 81 MIMSK2 Bit Fields *(Sheet 2 of 3)*

Bits	Field	Access	Description
<28>	ROVF_EN	R/W	**ROVF interrupt enable.** When *set*, enables an interrupt in case an ROVF counter wraparound event is detected.
<27:25>	MBZ	—	**Must be zero.**
<24>	LINK_FAILED_EN	R/W	**Link failed interrupt event enable.** When *set*, enables an interrupt when a link-failed event has been detected.
<23>	RXF_OVF_EN	R/W	**Receive FIFO overflow interrupt event enable.** When *set*, enables an interrupt when a receive FIFO overflow condition has been detected.
<22>	TXF_UFL_EN	R/W	**Transmit FIFO underflow interrupt event enable.** When *set*, enables an interrupt when a transmit FIFO underflow condition has been detected.
<21>	FCTL_ID_FAIL_EN	R/W	**Flow control ID interrupt event enable.** When *set*, enables an interrupt when the port has failed to detect its remote node as 21340-AB credit-based flow-control capable.
<20>	PART_EN	R/W	**Partition isolation interrupt event enable.** When *set*, enables an interrupt when a partition isolation event has been detected.
<19>	LATE_COL_EN	R/W	**Late collision interrupt event enable.** When *set*, enables an interrupt when a late collision event has been detected.
<18>	SHORT_EVNT_EN	R/W	**Short event interrupt event enable.** When *set*, enables an interrupt when a short event has been detected by the port.

Table 81 MIMSK2 Bit Fields *(Sheet 3 of 3)*

Bits	Field	Access	Description
<17>	**JABBER_EN**	R/W	**Receive jabber isolation interrupt event enable.** When *set*, enables an interrupt when a receive jabber isolation event has been detected.
<16>	**LINK_UNSTBL_EN**	R/W	**Carrier integrity isolation interrupt event enable.** When *set*, enables an interrupt when a carrier integrity isolation event has been detected.
<15:00>	—	—	RESERVED

Table 82 defines the access rules of the MIMSK2 register.

Table 82 MIMSK2 Access Rules

Category	Description
Register access	Read/Write
Register address offset	44H
Value after reset	00000000H
Read access rules	None
Write access rules	None

5.3.21 Management Interrupt Status Register

Mnemonic: MINT1{j}

Offset: 45H

This register contains the RMON and statistic counters overflow indication statuses. An asserted status bit indicates that the associated counter has an overflow condition. If the appropriate counter's interrupt mask bit is enabled, the **int** pin is asserted.

All MINT1 bits are cleared by a write one operation to them, or by a hardware or software reset.

There is one MINT1 register per 21340-AB port.

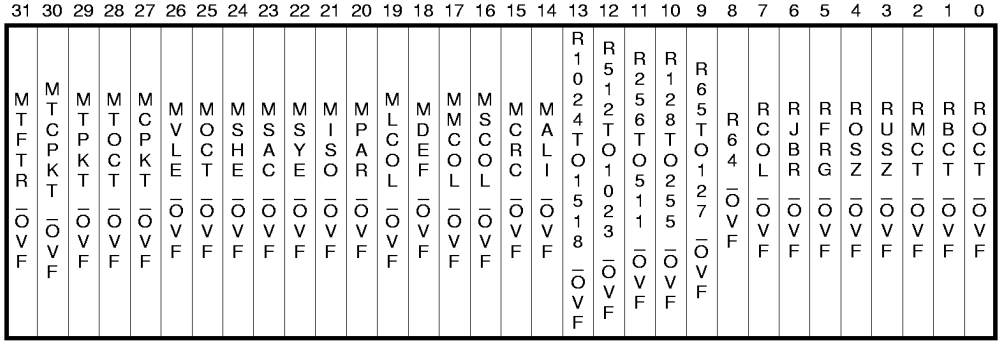


Table 83 defines the bit fields of the MINT1 register.

Table 83 MINT1 Bit Fields *(Sheet 1 of 4)*

Bits	Field	Access	Description
<31>	**MTFTR_OVF**	R/W1C	**MTFTR overflow.** When *set*, indicates that an MTFTR counter wraparound event has occurred.
<30>	**MTCPKT_OVF**	R/W1C	**MTCPKT overflow.** When *set*, indicates that an MTCPKT counter wraparound event has occurred.
<29>	**MTPKT_OVF**	R/W1C	**MTPKT overflow.** When *set*, indicates that an MTPKT counter wraparound event has occurred.

Table 83 MINT1 Bit Fields *(Sheet 2 of 4)*

Bits	Field	Access	Description
<28>	MTOCT_OVF	R/W1C	**MTOCT overflow.** When *set*, indicates that an MTOCT counter wraparound event has occurred.
<27>	MCPKT_OVF	R/W1C	**MCPKT overflow.** When *set*, indicates that an MCPKT counter wraparound event has occurred.
<26>	MVLE_OVF	R/W1C	**MVLE overflow.** When *set*, indicates that an MVLE counter wraparound event has occurred.
<25>	MOCT_OVF	R/W1C	**MOCT overflow.** When *set*, indicates that an MOCT counter wraparound event has occurred.
<24>	MSHE_OVF	R/W1C	**MSHE overflow.** When *set*, indicates that an MSHE counter wraparound event has occurred.
<23>	MSAC_OVF	R/W1C	**MSAC overflow.** When *set*, indicates that an MSAC counter wraparound event has occurred.
<22>	MSYE_OVF	R/W1C	**MSYE overflow.** When *set*, indicates that an MSYE counter wraparound event has occurred.
<21>	MISO_OVF	R/W1C	**MISO overflow.** When *set*, indicates that an MISO counter wraparound event has occurred.
<20>	MPAR_OVF	R/W1C	**MPAR overflow.** When *set*, indicates that an MPAR counter wraparound event has occurred.
<19>	MLCOL_OVF	R/W1C	**MLCOL overflow.** When *set*, indicates that an MLCOL counter wraparound event has occurred.
<18>	MDEF_OVF	R/W1C	**MDEF overflow.** When *set*, indicates that an MDEF counter wraparound event has occurred.

Table 83 MINT1 Bit Fields *(Sheet 3 of 4)*

Bits	Field	Access	Description
<17>	**MMCOL_OVF**	R/W1C	**MMCOL overflow.** When *set*, indicates that an MMCOL counter wraparound event has occurred.
<16>	**MSCOL_OVF**	R/W1C	**MSCOL overflow.** When *set*, indicates that an MSCOL counter wraparound event has occurred.
<15>	**MCRC_OVF**	R/W1C	**MCRC overflow.** When *set*, indicates that an MCRC counter wraparound event has occurred.
<14>	**MALI_OVF**	R/W1C	**MALI overflow.** When *set*, indicates that an MALI counter wraparound event has occurred.
<13>	**R1024TO1518_OVF**	R/W1C	**R1024TO1518 overflow.** When *set*, indicates that an R1024TO1518 counter wraparound event has occurred.
<12>	**R512TO1023_OVF**	R/W1C	**R512TO1023 overflow.** When *set*, indicates that an R512TO1023 counter wraparound event has occurred.
<11>	**R256TO511_OVF**	R/W1C	**R256TO511 overflow.** When *set*, indicates that an R256TO511 counter wraparound event has occurred.
<10>	**R128TO255_OVF**	R/W1C	**R128TO255 overflow.** When *set*, indicates that an R128TO255 counter wraparound event has occurred.
<09>	**R65TO127_OVF**	R/W1C	**R65TO127 overflow.** When *set*, indicates that an R65TO127 counter wraparound event has occurred.
<08>	**R64_OVF**	R/W1C	**R64 overflow.** When *set*, indicates that an R64 counter wraparound event has occurred.
<07>	**RCOL_OVF**	R/W1C	**RCOL overflow.** When *set*, indicates that an RCOL counter wraparound event has occurred.
<06>	**RJBR_OVF**	R/W1C	**RJBR overflow.** When *set*, indicates that an RJBR counter wraparound event has occurred.

Table 83 MINT1 Bit Fields *(Sheet 4 of 4)*

Bits	Field	Access	Description
<05>	**RFRG_OVF**	R/W1C	**RFRG overflow.** When *set*, indicates that an RFRG counter wraparound event has occurred.
<04>	**ROSZ_OVF**	R/W1C	**ROSZ overflow.** When *set*, indicates that an ROSZ counter wraparound event has occurred.
<03>	**RUSZ_OVF**	R/W1C	**RUSZ overflow.** When *set*, indicates that an RUSZ counter wraparound event has occurred.
<02>	**RMCT_OVF**	R/W1C	**RMCT overflow.** When *set*, indicates that an RMCT counter wraparound event has occurred.
<01>	**RBCT_OVF**	R/W1C	**RBCT overflow.** When *set*, indicates that an RBCT counter wraparound event has occurred.
<00>	**ROCT_OVF**	R/W1C	**ROCT overflow.** When *set*, indicates that an ROCT counter wraparound event has occurred.

Table 84 defines the access rules of the MINT1 register.

Table 84 MINT1 Access Rules

Category	Description
Register access	Read/Clear by write 1 register
Register address offset	45H
Value after reset	00000000H
Read access rules	None
Write access rules	Cleared by write 1 register

5.3.22 Flow-Control Source Address Low Register

Mnemonic: FSA1{1}

Offset: 46H

This register holds the low 32 bits of the remote node source address, in case the remote node is capable of running the 21340-AB credit-based flow-control scheme.

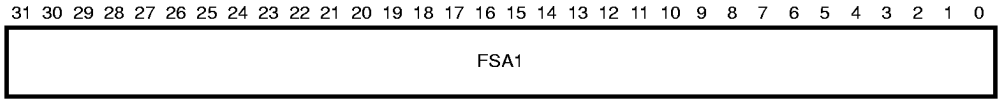


Table 85 defines the bit fields of the FSA1 register.

Table 85 FSA1 Bit Fields

Bits	Field	Access	Description
<31:00>	**FSA1**	R	**Flow-control source address high.** The low 32 bits of the remote node source address, in case the remote node is capable of running the 21340-AB credit-based flow-control scheme.

Table 86 defines the access rules of the FSA1 register.

Table 86 FSA1 Access Rules

Category	Description
Register access	Read only
Register address offset	46H
Value after reset	00000000H
Read access rules	None
Write access rules	Read-only register

5.3.23 Flow-Control Source Address High Register

Mnemonic: FSA2{j}

Offset: 47H

This register holds the high 16 bits of the remote node source address, in case the remote node is capable of running the 21340-AB credit-based flow-control scheme.

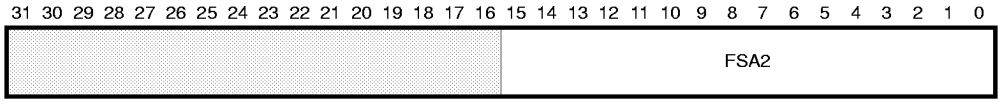


Table 87 defines the bit fields of the FSA2 register.

Table 87 FSA2 Bit Fields

Bits	Field	Access	Description
<31:00>	—	—	RESERVED
<15:00>	**FSA2**	R	High 16 bits of the remote node source address, in case the remote node is capable of running the 21340-AB credit-based flow-control scheme.

Table 88 defines the access rules of the FSA2 register.

Table 88 FSA2 Access Rules

Category	Description
Register access	Read/Write
Register address offset	47H
Value after reset	00000000H
Read access rules	None
Write access rules	Read-only register

5.4 16-Bit Statistic Counters

The 16-bit statistic counters of the 21340-AB are wraparound. They are cleared by a read operation and are maintained for 21340 device backward-compatibility.

5.4.1 16-Bit Transmit Collision Counter Register

Mnemonic: TCC{j}

Offset: 10H

This register counts the total number of collisions within the collision window encountered in a port during transmit attempts. There is one16-bit TCC counter per each of the four 21340-AB ports.

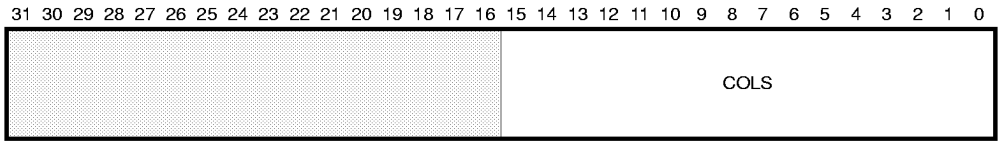


Table 89 defines the bit fields of the TCC counter.

Table 89 TCC Bit Fields

Bits	Field	Access	Description
<31:16>	—	—	RESERVED
<15:00>	**COLS**	R	**Collisions** Count of collisions

Table 90 defines the access rules of the TCC counter.

Table 90 TCC Access Rules

Category	Description
Register access	Read
Register address offset	10H
Value after reset	00000000H
Read access rules	Cleared by read-counter
Write access rules	Read-only register

Note: This register is maintained for 21340 device backward-compatibility.

5.4.2 16-Bit Runt Packet Counter Register

Mnemonic: RPC{j}

Offset: 11H

This register counts the number of runt packets received by a port. A runt packet is defined as a packet with a length that is greater than a short packet event (84 bits) and less than the minimum valid packet length (64 bytes). There is one16-bit RPC counter per each of the four 21340-AB ports.

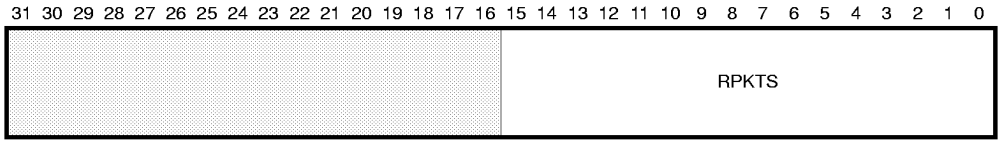


Table 91 defines the bit fields of the RPC counter.

Table 91 RPC Bit Fields

Bits	Field	Access	Description
<31:16>	—	—	RESERVED
<15:00>	**RPKTS**	R	**Runt packets** The count of runt packets

Table 92 defines the access rules of the RPC register.

Table 92 RPC Access Rules

Category	Description
Register access	Read-only register
Register address offset	11H
Value after reset	00000000H
Read access rules	Cleared by read-counter
Write access rules	Read-only register

Note: This register is maintained for 21340 device backward-compatibility.

5.5 Statistic Registers

All the statistic counters are cleared either by hardware reset, or when reading them using the clear-by-read offset.

All statistic counters appear once on each of the four 21340-AB ports.

5.5.1 RMON Overflow Counter

Mnemonic: ROVF{j}

Offset: 50H

Clear-by-read offset: D0H

This counter counts the total number of times an overflow condition (lack of Rx_FIFO available space during packet reception) has been detected.

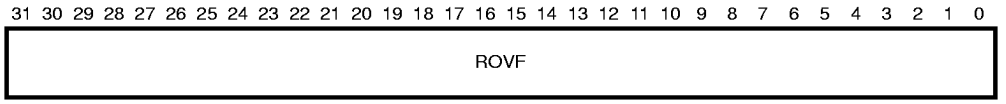


Table 93 defines the bit fields of the ROVF counter.

Table 93 ROVF Bit Fields

Bits	Field	Access	Description
<31:00>	**ROVF**	R/W	**Overflow event counter** The total number of times an overflow condition event has occurred

Table 94 defines the access rules of the ROVF counter.

Table 94 ROVF Access Rules

Category	Description
Register access	Read/Write
Register address offset	50H, D0H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D0H
Write access rules	None

5.5.2 RMON Octets Counter Low

Mnemonic: ROCTL{j}

Offset: 51H

Clear-by-read offset: D1H

This counter holds the lower 32 bits (of 40 bits) of the total number of data octets, including those in bad packets, received by a port.

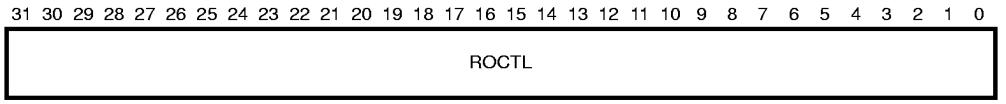


Table 95 defines the bit fields of the ROCTL counter.

Table 95 ROCTL Bit Fields

Bits	Field	Access	Description
<31:00>	**ROCTL**	R/W	**Received octets low** The lower 32 bits (of 40 bits) of the total number of octets received by a port

Table 96 defines the access rules of the ROCTL counter.

Table 96 ROCTL Access Rules

Category	Description
Register access	Read/Write
Register address offset	51H, D1H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D1H
Write access rules	None

5.5.3 RMON Octets Counter High

Mnemonic: ROCTH{j}

Offset: 52H

Clear-by-read offset: D2H

This counter holds the upper 8 bits (of 40 bits) of the total number of data octets, including those in bad packets, received by a port.

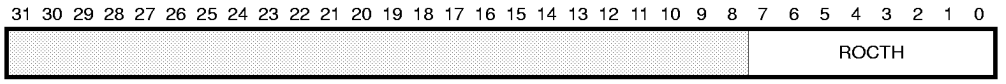


Table 97 defines the bit fields of the ROCTH counter.

Table 97 ROCTH Bit Fields

Bits	Field	Access	Description
<31:08>	—	—	RESERVED
<07:00>	**ROCTH**	R/W	**RMON octets high** The upper 8 bits (of 40 bits) of the total number of octets received by a port

Table 98 defines the access rules of the ROCTH counter.

Table 98 ROCTH Access Rules

Category	Description
Register access	Read/Write
Register address offset	52H, D2H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D2H
Write access rules	None

5.5.4 RMON Broadcast Packet Counter

Mnemonic: RBCT{j}

Offset: 53H

Clear-by-read offset: D3H

This counter holds the total number of good packets received by a port, directed to broadcast address (DA=FF-FF-FF-FF-FF-FFH).

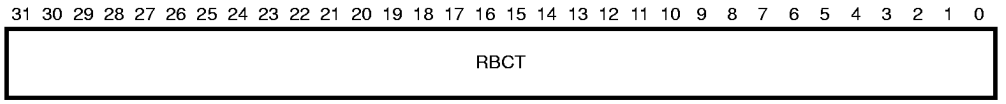


Table 99 defines the bit fields of the RBCT counter.

Table 99 RBCT Bit Fields

Bits	Field	Access	Description
<31:00>	**RBCT**	R/W	**RMON broadcast address** The total number of good broadcast packets received by a port

Table 100 defines the access rules of the RBCT counter.

Table 100 RBCT Access Rules

Category	Description
Register access	Read/Write
Register address offset	53H, D3H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D3H
Write access rules	None

5.5.5 RMON Multicast Packet Counter

Mnemonic: RMCT{j}

Offset: 54H

Clear-by-read offset: D4H

This counter holds the total number of good packets received by a port, directed to a multicast address (the destination address I/G bit is set to "1"). This number does not include packets directed to the broadcast address

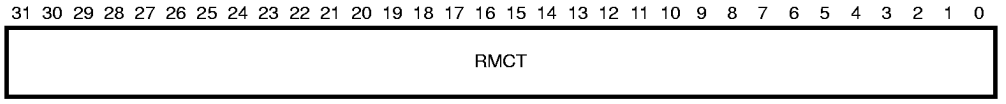


Table 101 defines the bit fields of the RMCT counter.

Table 101 RMCT Bit Fields

Bits	Field	Access	Description
<31:00>	**RMCT**	R/W	**RMON multicast packets** The total number of good multicast packets received by a port

Table 102 defines the access rules of the RMCT counter.

Table 102 RMCT Access Rules

Category	Description
Register access	Read/Write
Register address offset	54H, D4H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D4H
Write access rules	None

5.5.6 RMON Undersized Packets Counter

Mnemonic: RUSZ{j}

Offset: 55H

Clear-by-read offset: D5H

This counter holds the total number of packets shorter than 64 bytes in length and well formed, received by a port.

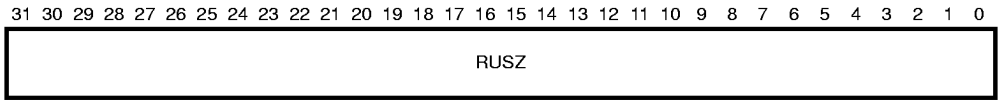


Table 103 defines the bit fields of the RUSZ counter.

Table 103 RUSZ Bit Fields

Bits	Field	Access	Description
<31:00>	**RUSZ**	R/W	**RMON undersized frames** The total number of well formed frames received with less than 64 bytes in length

Table 104 defines the access rules of the RUSZ counter.

Table 104 RUSZ Access Rules

Category	Description
Register access	Read/Write
Register address offset	55H, D5H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D5H
Write access rules	None

5.5.7 RMON Oversized Packets Counter

Mnemonic: ROSZ{j}

Offset: 56H

Clear-by-read offset: D6H

This counter holds the total number of packets longer than 1518 bytes and well formed, received by a port.

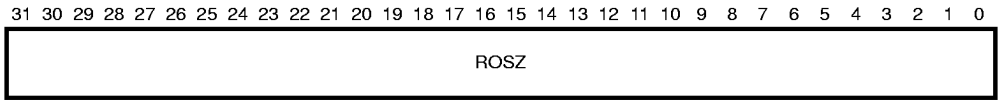


Table 105 defines the bit fields of the ROSZ counter.

Table 105 ROSZ Bit Fields

Bits	Field	Access	Description
<31:00>	**ROSZ**	R/W	**RMON oversized frames** The total number of well formed frames longer than 1518 bytes

Table 106 defines the access rules of the ROSZ counter.

Table 106 ROSZ Access Rules

Category	Description
Register access	Read/Write
Register address offset	56H, D6H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D6H
Write access rules	None

5.5.8 RMON Fragments Counter

Mnemonic: RFRG{j}

Offset: 57H

Clear-by-read offset: D7H

This counter holds the total number of packets shorter than 64 bytes in length with a CRC error (with or without an alignment error), received by a port.

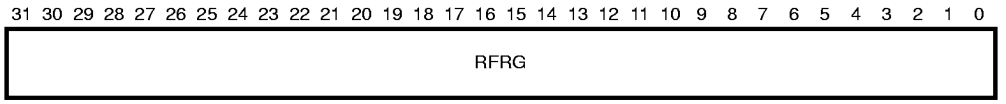


Table 107 defines the bit fields of the RFRG counter.

Table 107 RFRG Bit Fields

Bits	Field	Access	Description
<31:00>	**RFRG**	R/W	The total number of packets shorter than 64 bytes with a CRC error

Table 108 defines the access rules of the RFRG counter.

Table 108 RFRG Access Rules

Category	Description
Register access	Read/Write
Register address offset	57H, D7H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D7H
Write access rules	None

5.5.9 RMON Jabbers Counter

Mnemonic: RJBR{j}

Offset: 58H

Clear-by-read offset: D8H

This counter holds the total number of packets longer than 1518 bytes in length with a CRC error (with or without an alignment error), received by a port.

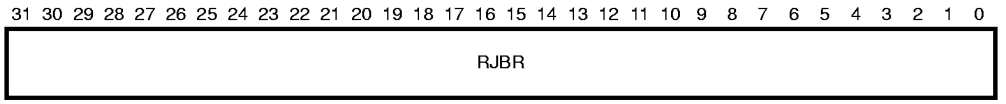


Table 109 defines the bit fields of the RJBR counter.

Table 109 RJBR Bit Fields

Bits	Field	Access	Description
<31:00>	**RJBR**	R/W	**RMON Jabber frames** The total number of frames that are longer than 1518 bytes and have a CRC error

Table 110 defines the access rules of the RJBR counter.

Table 110 RJBR Access Rules

Category	Description
Register access	Read/Write
Register address offset	58H, D8H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D8H
Write access rules	None

5.5.10 RMON Collisions Counter

Mnemonic: RCOL{j}

Offset: 59H

Clear-by-read offset: D9H

This counter holds the total number of collisions that are not late collisions experienced by a port.

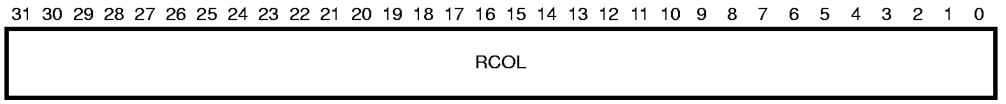


Table 111 defines the bit fields of the RCOL counter.

Table 111 RCOL Bit Fields

Bits	Field	Access	Description
<31:00>	**RCOL**	R/W	**RMON collision** The total number of collisions that are not late collisions experienced by a port

Table 112 defines the access rules of the RCOL counter.

Table 112 RCOL Access Rules

Category	Description
Register access	Read/Write
Register address offset	59H, D9H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset D9H
Write access rules	None

5.5.11 RMON 64 Octet Packets Counter

Mnemonic: R64{j}

Offset: 5AH

Clear-by-read offset: DAH

This counter holds the total number of packets 64 bytes in length, including bad packets, received by a port.

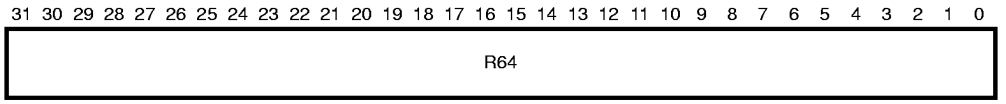


Table 113 defines the bit fields of the R64 counter.

Table 113 R64 Bit Fields

Bits	Field	Access	Description
<31:00>	**R64**	R/W	**Received 64-byte packets** The total number of packets 64 bytes in length, received by a port

Table 114 defines the access rules of the R64 counter.

Table 114 R64 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5AH, DAH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DAH
Write access rules	None

5.5.12 RMON 65 to 127 Octet Packets Counter

Mnemonic: R65TO127{j}

Offset: 5BH

Clear-by-read offset: DBH

This counter holds the total number of packets between 65 and 127 bytes in length, including bad packets, received by a port.

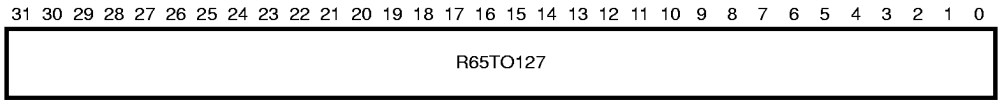


Table 115 defines the bit fields of the R65TO127 counter.

Table 115 R65TO127 Bit Fields

Bits	Field	Access	Description
<31:00>	**R65TO127**	R/W	**Received 65 to 127-byte packets** The total number of frames with length between 65 and 127 bytes, received by a port

Table 116 defines the access rules of the R65TO127 counter.

Table 116 R65TO127 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5BH, DBH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DBH
Write access rules	None

5.5.13 RMON 128 to 255 Octet Packets Counter

Mnemonic: R128TO255{j}

Offset: 5CH

Clear-by-read offset: DCH

This counter holds the total number of packets between 128 and 255 bytes in length, including bad packets, received by a port.

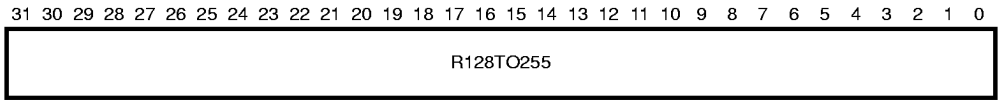


Table 117 defines the bit fields of the R128TO255 counter.

Table 117 R128TO255 Bit Fields

Bits	Field	Access	Description
<31:00>	**R128TO255**	R/W	**Received 128 to 255-byte packets** The total number of frames between 128 and 255 bytes in length received on a port

Table 118 defines the access rules of the R128TO255 register.

Table 118 R128TO255 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5CH, DCH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DCH
Write access rules	None

5.5.14 RMON 256 to 511 Octet Packets Counter

Mnemonic: R256TO511{j}

Offset: 5DH

Clear-by-read offset: DDH

This counter holds the total number of packets between 256 and 511 bytes in length, including bad packets, received by a port.

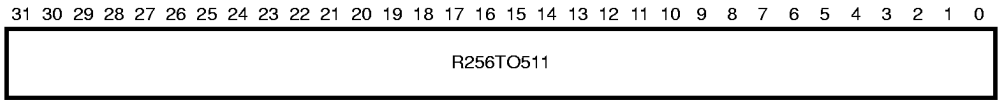


Table 119 defines the bit fields of the R256TO511 counter.

Table 119 R256TO511 Bit Fields

Bits	Field	Access	Description
<31:00>	**R256TO511**	R/W	**Received 256 to 511-byte packets** The total number of frames between 256 and 511 received by a port

Table 120 defines the access rules of the R256TO511 counter.

Table 120 R256TO511 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5DH, DDH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DDH
Write access rules	None

5.5.15 RMON 512 to 1023 Octet Packets Counter

Mnemonic: R512TO1023{j}

Offset: 5EH

Clear-by-read offset: DEH

This counter holds the total number of packets between 512 and 1023 bytes in length, including bad packets, received by a port.

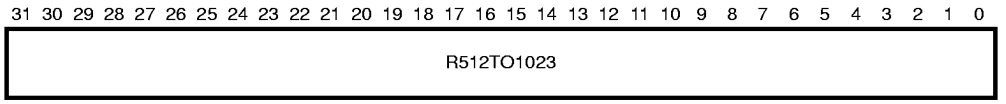


Table 121 defines the bit fields of the R512TO1023 counter.

Table 121 R512TO1023 Bit Fields

Bits	Field	Access	Description
<31:00>	**R512TO1023**	R/W	**Received 512 to 1023-byte packets** The total number of frames between 512 and 1023 received by a port

Table 122 defines the access rules of the R512TO1023 counter.

Table 122 R512TO1023 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5EH, DEH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DEH
Write access rules	None

5.5.16 RMON 1024 to 1518 Octet Packets Counter

Mnemonic: R1024TO1518{j}

Offset: 5FH

Clear-by-read offset: DFH

This counter holds the total number of packets between 1024 and 1518 bytes in length, including bad packets, received by a port.

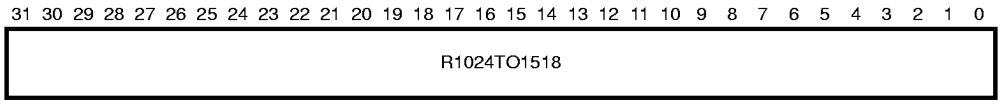


Table 123 defines the bit fields of the R1024TO1518 counter.

Table 123 R1024TO1518 Bit Fields

Bits	Field	Access	Description
<31:00>	**R1024TO1518**	R/W	**Received 1024 to 1518-byte packets** The total number of frames between 1024 and 1518 received by a port

Table 124 defines the access rules of the R1024TO1518 counter.

Table 124 R1024TO1518 Access Rules

Category	Description
Register access	Read/Write
Register address offset	5FH, DFH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset DFH
Write access rules	None

5.5.17 Management Alignment Errors Counter

Mnemonic: MALI{j}

Offset: 60H

Clear-by-read offset: E0H

This counter holds the total number of times that packets, equal or greater than 64 bytes and shorter or equal to 1518 bytes, did not have an integral number of octets in length and had a CRC error (alignment error), received by a port.

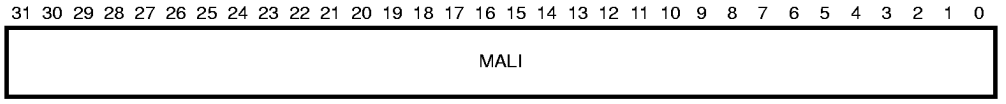


Table 125 defines the bit fields of the MALI counter.

Table 125 MALI Bit Fields

Bits	Field	Access	Description
<31:00>	**MALI**	R/W	**Management alignment error** The total number of frames with an alignment error and bad CRC received by a port

Table 126 defines the access rules of the MALI counter.

Table 126 MALI Access Rules

Category	Description
Register access	Read/Write
Register address offset	60H, E0H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E0H
Write access rules	None

5.5.18 Management CRC Errors Counter

Mnemonic: MCRC{j}

Offset: 61H

Clear-by-read offset: E1H

This counter holds the total number of times that packets, equal or greater than 64 bytes and shorter or equal to 1518 bytes, with an integral number of octets in length and with a CRC error, received by a port.

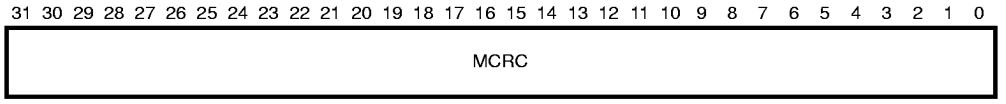


Table 127 defines the bit fields of the MCRC counter.

Table 127 MCRC Bit Fields

Bits	Field	Access	Description
<31:00>	**MCRC**	R/W	**Management CRC error** The total number of frames without an alignment error and with bad CRC received by a port

Table 128 defines the access rules of the MCRC counter.

Table 128 MCRC Access Rules

Category	Description
Register access	Read/Write
Register address offset	61H, E1H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E1H
Write access rules	None

5.5.19 Management Single Collision Counter

Mnemonic: MSCOL{j}

Offset: 62H

Clear-by-read offset: E2H

This counter holds the total number of times that packets experiencing exactly one collision, successfully transmitted by a port.

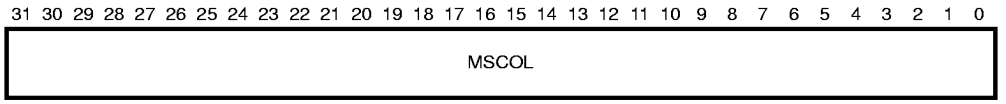


Table 129 defines the bit fields of the MSCOL counter.

Table 129 MSCOL Bit Fields

Bits	Field	Access	Description
<31:00>	**MSCOL**	R/W	**Management single collision** The total number of frames experiencing exactly one collision, successfully transmitted by a port

Table 130 defines the access rules of the MSCOL counter.

Table 130 MSCOL Access Rules

Category	Description
Register access	Read/Write
Register address offset	62H, E2H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E2H
Write access rules	None

5.5.20 Management Alignment Errors Counter

Mnemonic: MMCOL{j}

Offset: 63H

Clear-by-read offset: E3H

This counter holds the total number of times that packets experiencing more than one collision, successfully transmitted by a port.

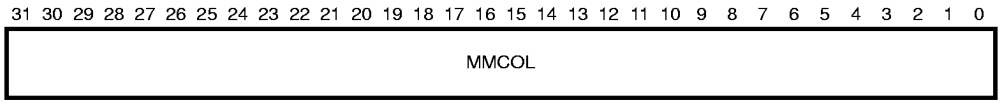


Table 131 defines the bit fields of the MMCOL counter.

Table 131 MMCOL Bit Fields

Bits	Field	Access	Description
<31:00>	**MMCOL**	R/W	**Management multi-collisions** The total number of frames experiencing more than one collision, successfully transmitted by the port

Table 132 defines the access rules of the MMCOL counter.

Table 132 MMCOL Access Rules

Category	Description
Register access	Read/Write
Register address offset	63H, E3H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E3H
Write access rules	None

5.5.21 Management Deferred Transmissions Counter

Mnemonic: MDEF{j}

Offset: 64H

Clear-by-read offset: E4H

This counter holds the total number of times the first packet's transmission attempt is delayed because the medium is busy.

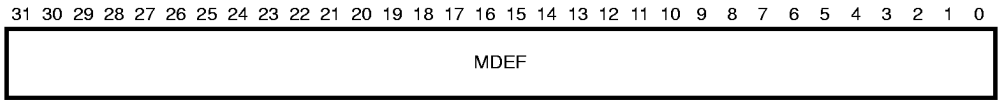


Table 133 defines the bit fields of the MDEF counter.

Table 133 MDEF Bit Fields

Bits	Field	Access	Description
<31:00>	**MDEF**	R/W	**Management deferred transmissions** The total number of times the first packet's transmission attempt is delayed because the medium is busy

Table 134 defines the access rules of the MDEF counter.

Table 134 MDEF Access Rules

Category	Description
Register access	Read/Write
Register address offset	64H, E4H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E4H
Write access rules	None

5.5.22 Management Late Collision Counter

Mnemonic: MLCOL{j}

Offset: 65H

Clear-by-read offset: E5H

This counter holds the total number of times that a collision was detected on the port, 512 bit-times into the transmission of the packet and on.

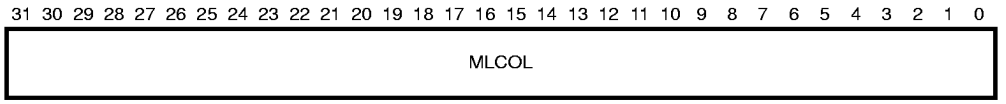


Table 135 defines the bit fields of the MLCOL counter.

Table 135 MLCOL Bit Fields

Bits	Field	Access	Description
<31:00>	**MLCOL**	R/W	**Management late collision detection** The total number of times a collision was detected on the port, 512 bit-times into the transmission of the packet and on

Table 136 defines the access rules of the MLCOL counter.

Table 136 MLCOL Access Rules

Category	Description
Register access	Read/Write
Register address offset	65H, E5H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E5H
Write access rules	None

5.5.23 Management Partitioning Counter

Mnemonic: MPAR{j}

Offset: 66H

Clear-by-read offset: E6H

This counter counts the number of times a port was partitioned by the auto-partition mechanism.

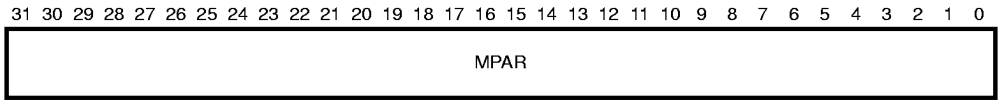


Table 137 defines the bit fields of the MPAR counter.

Table 137 MPAR Bit Fields

Bits	Field	Access	Description
<31:00>	**MPAR**	R/W	**Management partitioning** The total number of times a port was partitioned by the auto-partition mechanism

Table 138 defines the access rules of the MPAR counter.

Table 138 MPAR Access Rules

Category	Description
Register access	Read/Write
Register address offset	66H, E6H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E6H
Write access rules	None

5.5.24 Management Carrier Isolation Counter

Mnemonic: MISO{j}

Offset: 67H

Clear-by-read offset: E7H

This counter holds the total number of times that a port has been isolated due to false carrier events or link-failed scenarios.

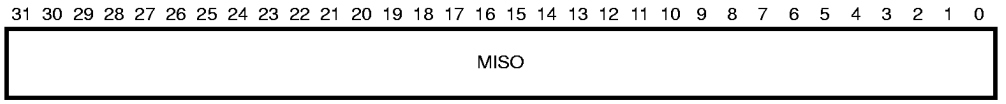


Table 139 defines the bit fields of the MISO counter.

Table 139 MISO Bit Fields

Bits	Field	Access	Description
<31:00>	**MISO**	R/W	**Management isolation** The total number of times a port has been isolated due to false carrier events, or link-failed scenarios

Table 140 defines the access rules of the MISO counter.

Table 140 MISO Access Rules

Category	Description
Register access	Read/Write
Register address offset	67H, E7H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E7H
Write access rules	None

5.5.25 Management Symbol Error Counter

Mnemonic: MSYE{j}

Offset: 68H

Clear-by-read offset: E8H

This counter holds the total number of times that a packet with valid length was received by a port with at least one occurrence of an invalid data symbol. A collision occurrence will not increment this counter.

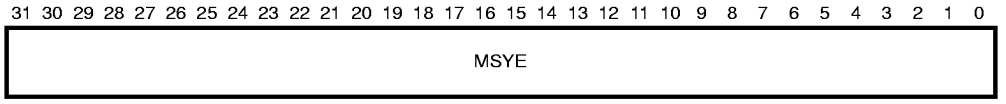


Table 141 defines the bit fields of the MSYE counter.

Table 141 MSYE Bit Fields

Bits	Field	Access	Description
<31:00>	**MSYE**	R/W	**Management symbol error** The number of times a packet with a valid length was received by a port with at least one occurrence of an invalid data symbol

Table 142 defines the access rules of the MSYE counter.

Table 142 MSYE Access Rules

Category	Description
Register access	Read/Write
Register address offset	68H, E8H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E8H
Write access rules	None

5.5.26 Management Source Address Changes Counter

Mnemonic: MSAC{j}

Offset: 69H

Clear-by-read offset: E9H

This counter holds the total number of times that the port's remote node last source address has been changed. This may indicate whether a link is connected to a single DTE or a multi-user segment.

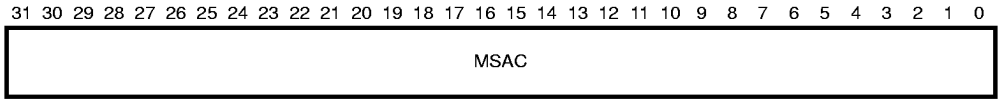


Table 143 defines the bit fields of the MSAC counter.

Table 143 MSAC Bit Fields

Bits	Field	Access	Description
<31:00>	**MSAC**	R/W	**Management source address changes** The number of times the port's remote node source address has been changed

Table 144 defines the access rules of the MSAC counter.

Table 144 MSAC Access Rules

Category	Description
Register access	Read/Write
Register address offset	69H, E9H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset E9H
Write access rules	None

5.5.27 Management Last Source Address Low

Mnemonic: UAR1{j}

Offset: 6AH

This register holds the lower 32 bits (of 48 bits) of the source address of the last valid frame received by this port.

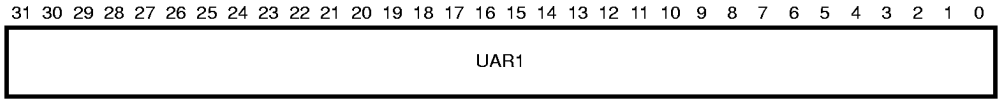


Table 145 defines the bit fields of the UAR1 register.

Table 145 UAR1 Bit Fields

Bits	Field	Access	Description
<31:00>	**UAR1**	R	**Remote node source address low** The lower 32 bits of the source address of the last valid frame received by this port

Table 146 defines the access rules of the UAR1 register.

Table 146 UAR1 Access Rules

Category	Description
Register access	Read only
Register address offset	6AH
Value after hardware reset	00000000H
Read access rules	None
Write access rules	Read-only register

5.5.28 Management Last Source Address High

Mnemonic: UAR2{j}

Offset: 6BH

This register holds the upper 16 bits (of 48 bits) of the source address of the last valid frame received by this port.

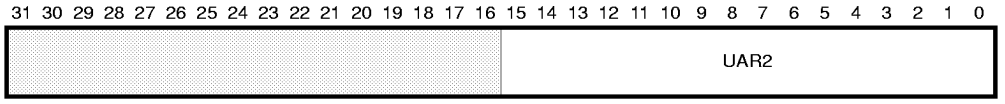


Table 147 defines the bit fields of the UAR2 register.

Table 147 UAR2 Bit Fields

Bits	Field	Access	Description
<31:16>	—	—	RESERVED
<15:00>	**UAR2**	R	**Remote source address high** The upper 16 bits of the source address of the last valid frame received by this port

Table 148 defines the access rules of the UAR2 register.

Table 148 UAR2 Access Rules

Category	Description
Register access	Read only
Register address offset	6BH
Value after hardware reset	00000000H
Read access rules	None
Write access rules	Read-only register

5.5.29 Management Short Events Counter

Mnemonic: MSHE{j}

Offset: 6CH

Clear-by-read offset: ECH

This counter holds the number of times a short carrier event has been detected by a port. For 10 Mb/s, a short event is defined as carrier activity greater than 74 bit-times and lower than 82 bit-times. For 100 Mb/s, a short event is defined as a carrier activity shorter than 84 bit-times.

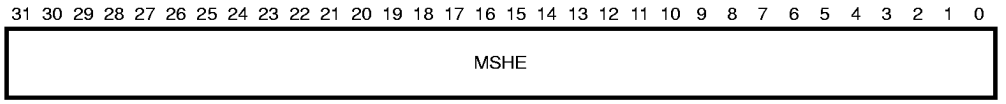


Table 149 defines the bit fields of the MSHE counter.

Table 149 MSHE Bit Fields

Bits	Field	Access	Description
<31:00>	**MSHE**	R/W	**Management short events** The number of times a short carrier event has been detected by a port

Table 150 defines the access rules of the MSHE counter.

Table 150 MSHE Access Rules

Category	Description
Register access	Read/Write
Register address offset	6CH, ECH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset EC
Write access rules	None

5.5.30 Management Octets Counter Low

Mnemonic: MOCTL{j}

Offset: 6DH

Clear-by-read offset: EDH

This register holds the lower 32 bits (of 40 bits) of the total number of data octets of packets between 64 and 1518 bytes long with no CRC or alignment errors, received by a port.

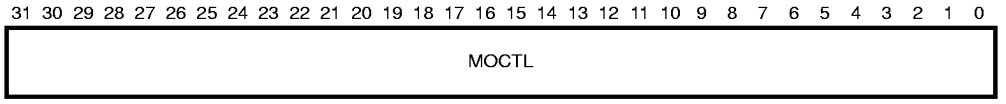


Table 151 defines the bit fields of the MOCTL register.

Table 151 MOCTL Bit Fields

Bits	Field	Access	Description
<31:00>	**MOCTL**	R/W	**Management octets counter low** The lower 32 bits (of 40 bits) of the total number of data octets of packets 64 to 1518 bytes long with no CRC or alignment errors, received by a port

Table 152 defines the access rules of the MOCTL register.

Table 152 MOCTL Access Rules

Category	Description
Register access	Read/Write
Register address offset	6DH, EDH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset EDH
Write access rules	None

5.5.31 Management Octets Counter High

Mnemonic: MOCTH{j}

Offset: 6EH

Clear-by-read offset: EEH

This register holds the upper 8 bits (of 40) of the total number of data octets of the packets 64 to 1518 bytes long with no CRC or alignment errors, received by a port.

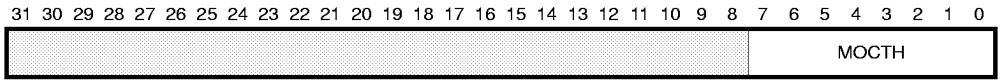


Table 153 defines the bit fields of the MOCTH register.

Table 153 MOCTH Bit Fields

Bits	Field	Access	Description
<31:08>	—	—	RESERVED
<07:00>	**MOCTH**	R/W	**Management octets counter high** The upper bits of the total number of data octets of packets 64 to 1518 bytes long with no CRC or alignment errors, received by a port

Table 154 defines the access rules of the MOCTH register.

Table 154 MOCTH Access Rules

Category	Description
Register access	Read/Write
Register address offset	6EH, EEH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset EEH
Write access rules	None

5.5.32 Management Very Long Event Counter

Mnemonic: MVLE{j}

Offset: 6FH

Clear-by-read offset: EFH

This counter holds the total number of times a receive jabber event has been detected by a port.

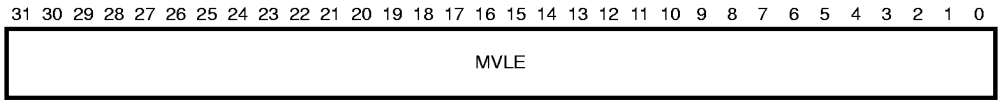


Table 155 defines the bit fields of the MVLE counter.

Table 155 MVLE Bit Fields

Bits	Field	Access	Description
<31:00>	**MVLE**	R/W	**Management very long event** The number of times a receive jabber event has been detected by a port

Table 156 defines the access rules of the MVLE counter.

Table 156 MVLE Access Rules

Category	Description
Register access	Read/Write
Register address offset	6FH, EFH
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset EFH
Write access rules	None

5.5.33 Management Control Packet Counter

Mnemonic: MCPKT{j}

Offset: 71H

Clear-by-read offset: F1H

This register holds the total number of times that a valid 21340-AB control packet 64 to 1518 bytes long has been received by the port.

A valid 21340-AB control packet is either a backpressure packet 64 to 1518 bytes long, or a 21340-AB credit-based flow-control packet with legal CRC.

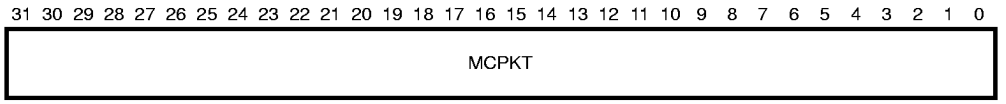


Table 157 defines the bit fields of the MCPKT register.

Table 157 MCPKT Bit Fields

Bits	Field	Access	Description
<31:00>	**MCPKT**	R/W	**Management control packet.** The total number of times that a valid 21340-AB control packet has been received by a port. A valid control packet is defined as either a legal backpressure packet, or a legal credit-based flow-control packet.

Table 158 defines the access rules of the MCPKT register.

Table 158 MCPKT Access Rules

Category	Description
Register access	Read/Write
Register address offset	71H, F1H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F1H
Write access rules	None

5.5.34 Transmitted Octets Counter Low

Mnemonic: MTOCTL{j}

Offset: 72H

Clear-by-read offset: F2H

This register holds the lower 32 bits (of 40 bits) of the total number of data octets, including those in bad packets and collided packets, that are transmitted by a port.

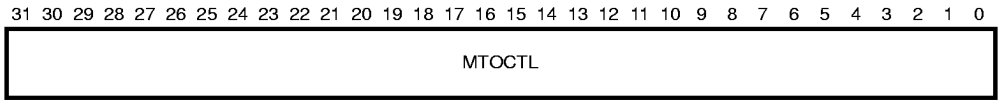


Table 159 defines the bit fields of the MTOCTL register.

Table 159 MTOCTL Bit Fields

Bits	Field	Access	Description
<31:00>	**MTOCTL**	R/W	**Management transmit octets low** The lower 32 bits (of 40 bits) of the total number of octets transmitted by a port

Table 160 defines the access rules of the MTOCTL register.

Table 160 MTOCTL Access Rules

Category	Description
Register access	Read/Write
Register address offset	72H, F2H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F2H
Write access rules	None

5.5.35 Transmitted Octets Counter High

Mnemonic: MTOCTH{j}

Offset: 73H

Clear-by-read offset: F3H

This register holds the upper 8 bits (of 40 bits) of the total number of data octets, including those in bad packets, transmitted by a port.

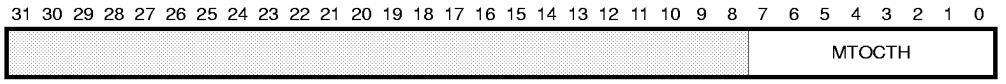


Table 161 defines the bit fields of the MTOCTH register.

Table 161 MTOCTH Bit Fields

Bits	Field	Access	Description
<31:08>	—	—	RESERVED
<07:00>	**MTOCTH**	R/W	**Management transmit octets high** The upper 8 bits (of 40 bits) of the total number of octets transmitted by a port

Table 162 defines the access rules of the MTOCTH register.

Table 162 MTOCTH Access Rules

Category	Description
Register access	Read/Write
Register address offset	73H, F3H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F3H
Write access rules	None

5.5.36 Management Transmit Packet Counter

Mnemonic: MTPKT{j}

Offset: 74H

Clear-by-read offset: F4H

This register holds the total number of packets transmitted by a port, including bad packets and control packets.

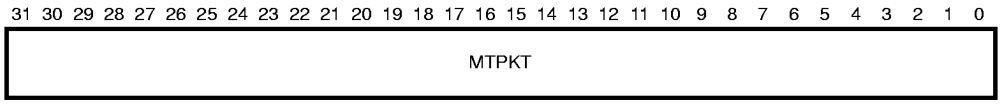


Table 163 defines the bit fields of the MTPKT register.

Table 163 MTPKT Bit Fields

Bits	Field	Access	Description
<31:00>	**MTPKT**	R/W	**Management transmit packet** Holds the total number of packets transmitted by a port

Table 164 defines the access rules of the MTPKT register.

Table 164 MTPKT Access Rules

Category	Description
Register access	Read/Write
Register address offset	74H, F4H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F4H
Write access rules	None

5.5.37 Management Transmit Control Packet Counter

Mnemonic: MTCPKT{j}

Offset: 75H

Clear-by-read offset: F5H

This counter holds the total number of control packets (flow-control and backpressure packets) transmitted by a port.

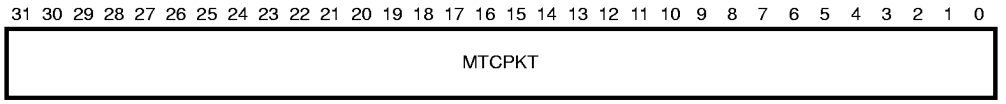


Table 165 defines the bit fields of the MTCPKT counter.

Table 165 MTCPKT Bit Fields

Bits	Field	Access	Description
<31:00>	**MTCPKT**	R/W	**Management transmit control packet.** Holds the total number control packet transmitted by a port. A control packet is either a backpressure packet, or a credit-based flow-control packet.

Table 166 defines the access rules of the MTCPKT counter.

Table 166 MTCPKT Access Rules

Category	Description
Register access	Read/Write
Register address offset	75H, F5H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F5H
Write access rules	None

5.5.38 Management Transmit Filtered Packet Counter

Mnemonic: MTFTR{j}

Offset: 76H

Clear-by-read offset: F6H

This counter holds the total number of packets filtered by the destination port (either by the internal or the external address filtering function).

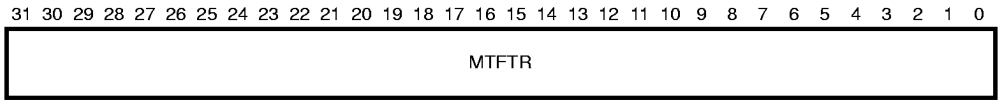


Table 167 defines the bit fields of the MTFTR counter.

Table 167 MTFTR Bit Fields

Bits	Field	Access	Description
<31:00>	**MTFTR**	R/W	**Management transmit filter packet** Holds the total number of packets filtered by a port (either by the internal address filtering function, or by the external address filtering function)

Table 168 defines the access rules of the MTFTR counter.

Table 168 MTFTR Access Rules

Category	Description
Register access	Read/Write
Register address offset	76H, F6H
Value after hardware reset	00000000H
Read access rules	Cleared when read from the register offset F6H
Write access rules	None

A List of Terms and Acronyms

The following terms are used in this document:

Table 169 21340-AB Terms and Descriptions *(Sheet 1 of 2)*

Term	Description
BP	Backpressure. When a 21340-AB port becomes congested, a backpressure mechanism is activated against the remote node.
Broadcasts	Indicates the 21340-AB port transferring a received packet toward other ports through their parallel bus segment.
DA	Destination address.
FCTL	Flow control.
FDX	Full-duplex operation mode.
HDX	Half-duplex operation mode.
Load	Indicates the other ports transferring a broadcast packet from the parallel bus segment into their respective Tx_FIFOs.
MII	Media-independent interface.
Parallel Bus	The group of data and control signals that are shared by all 21340-AB devices connected together in an application design. Internal to each 21340-AB device, the four 21340-AB ports can be assigned variously to any of four subsections of the external parallel bus, called segments.
PHY	Physical layer device.
PMD	Physical layer medium dependent.
Preamble	A pattern of seven octets of 10101010b, preceding the SFD.
Receive	Indicates that a packet is received from the physical side into one of the 21340-AB ports.
Rx_FIFO	Receive FIFO.
SA	Source address.
Segment	A group of 21340-AB ports operating at the same data rate that are able to broadcast and load packets across a shared subset of the control and data lines in the 21340-AB parallel bus.
SFD	Start frame delimiter. The byte 10101011b indicates the start of a frame.

Table 169 21340-AB Terms and Descriptions *(Sheet 2 of 2)*

Term	Description
SNMP	Simple Network Management Protocol.
Transmit	Indicates that a packet is received from the physical side into one of the 21340-AB ports.
Tx_FIFO	Transmit FIFO.
100BASE-TX	IEEE 802.3 Physical Layer specification for a 100-Mb/s CSMA/CD LAN over two pairs of CAT5 unshielded twisted-pair (UTP) or shielded twisted-pair (STP) cables.
100BASE-T4	IEEE 802.3 Physical Layer specification for a 100-Mb/s CSMA/CD LAN over four pairs of CAT3, CAT4, or CAT5 UTP cables.

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Note: The following products and order numbers might have been revised. For the latest versions, contact your local distributor.

Chips	Order Number
DIGITAL Semiconductor 21340 10/100-Mb/s Managed Buffered Port Switch	21340–AB

DIGITAL Semiconductor Documentation

The following table lists some of the available DIGITAL Semiconductor documentation.

Title	Order Number
DIGITAL Semiconductor 21340 10/100-Mb/s Managed Buffered Port Switch Product Brief	EC–R07NB–TE