LAMBDA ADVANCED ANALOG INC.

ATW2800D Series

Dual Output, Hybrid - High Reliability
DC/DC Converter

DESCRIPTION

The ATW2800D Series of DC/DC converters feature high power density and an extended temperature range for use in military and industrial applications. Designed to MIL-STD-704 input requirements, these devices have nominal 28VDC inputs with ±12V and ±15V dual outputs to satisfy a wide range of requirements. The circuit design incorporates a pulse width modulated push-pull topology operating in the feed-forward mode at a nominal switching frequency of 270KHz. Input to output isolation is achieved through the use of transformers in the forward and feedback circuits.

The advanced feedback design provides fast loop response for superior line and load transient characteristics and offers greater reliability and radiation tolerance than devices incorporating optical feedback circuits.

Three standard temperature grades are offered. Refer to Part Number section for more severe enviroments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are available in four screening grades to satisfy a wide range of requirements. The CH grade is fully compliant to the requirements of MIL-PRF-38534 for class H. The HB grade is processed and screened to the class H requirement, but may not necessarily meet all of the other MIL-PRF-38534 requirements, e.g., element evaluation and Periodic Inspection (P.I.) not required. Both grades are tested to meet the complete group "A" test specification over the full military temperature range without output power deration. Two grades with more limited screening are also available for use in less demanding applications. Variations in electrical, mechanical and screening can be accommodated. Contact Lambda Advanced Analog for special requirements.

FEATURES

- **18 To 40 Volt Input Range (28VDC Nominal)**
- **± 12 and ± 15 Volt Outputs Available**
- **Indefinite Short Circuit and Overload Protection**
- **22.8 W/in^3 Power Density**
- **30 Watts Output Power**
- **Fast Loop Response For Superior Transient Characteristics**
- **Operating Temperature Range From -55°C to +125°C Available**
- **Popular Industry Standard Pin-Out**
- **Resistance Seam Welded Case For Superior Long Term Hermeticity**
- **Efficiencies Up to 85%**
- **Shutdown From External Signal**
- **Full Military Screening**
- **200,000 Hour MTBF at 85°C**
- **MIL-PRF-38534 Compliant Versions Available**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.5V to 180V
Soldering Temperature	300°C for 10 seconds
Case Temperature	Operating-55°C to +125°C Storage -65°C to +135°C

TABLE I. Electrical Performance Characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output voltage	V_{OUT}	I_{OUT} = 0	1	All	±11.88	±12.12	V
			2,3		±11.76	±12.24	
Output current 1/ 2/	I_{OUT}	V_{IN} = 18, 28, and 40 V dc, each output	1,2,3	All	250	2250	mA
Output ripple voltage 3/	V_{RIP}	V_{IN} = 18, 28, and 40 V dc, B.W. = 20 Hz to 2 MHz	1,2,3	All		85	mV p-p
Line regulation 4/	VR_{LINE}	V_{IN} = 18, 28, and 40 V dc, I_{OUT} = 0, 1250, and 2500 mA	1	All		30	mV
			2,3			60	
Load regulation 4/	VR_{LOAD}	V_{IN} = 18, 28, and 40 V dc, I_{OUT} = 0, 1250, and 2500 mA	1,2,3	All		120	mV
Cross regulation 5/	VR_{CROS}	10 percent to 90 percent load change	1,2,3	All		3.5	%
Input current	I_{IN}	I_{OUT} = 0, inhibit (pin 8) tied to input return (pin 10)	1,2,3	All		18	mA
		I_{OUT} = 0, inhibit (pin 8) = open				50	
Input ripple current 3/ 4/	I_{RIP}	I_{OUT} = 2500 mA, B.W. = 20 Hz to 2 MHz	1,2,3	All		50	mA p-p
Efficiency 4/	E_{FF}	I_{OUT} = 2500 mA, T_C = +25°C	1	All	80		%
Isolation	ISO	Input to output or any pin to case (except pin 7) at 500 V dc, T_C = +25°C	1	All	100		MΩ
Capacitive load 6/ 7/	C_L	No effect on dc performance, T_C = +25°C, total for both outputs	4	All		200	µF
Power dissipation load fault	P_D	Overload, T_C = +25°C 8/	1	All		12	W
		Short circuit, T_C = +25°C				9	

See footnotes at end of table.

TABLE I. Electrical Performance Characteristics - Continued

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{IN} = 28 V dc ±5%, C_L = 0 unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
Switching frequency 4/	F_S	I_{OUT} = 2500 mA	4,5,6	01	250	300	KHz
				02	250	270	
				03	275	300	
Output response to step transient load changes 4/ 9/	VO_{TLOAD}	1250 mA to/from 2500 mA	4,5,6	All	-400	+400	mV pk
		0 mA to/from 2500 mA	4,5,6	All	-800	+800	
Recovery time, step transient load changes 4/ 9/ 10/	TT_{LOAD}	1250 mA to/from 2500 mA	4,5,6	All		70	µs
		0 mA to/from 1250 mA	4,5,6	All		500	
		1250 mA to/from 0 mA	4,5,6	All		5	ms
Output response transient step line changes 4/ 7/ 11/	VO_{TLINE}	Input step from/to 18 to 40 V dc, I_{OUT} = 2500 mA	4,5,6	All	-800	+800	mV pk
Recovery time transient step line changes 4/ 7/ 10/ 11/	TT_{LINE}	Input step from/to 18 to 40 V dc, I_{OUT} = 2500 mA	4,5,6	All		4000	µs
Turn on overshoot 4/	$VTon_{OS}$	I_{OUT} = 0 and 2500 mA	4,5,6	All		750	mV pk
Turn on delay 4/ 12/	Ton_D	I_{OUT} = 0 and 2500 mA	4,5,6	All		14	ms
Load fault recovery 7/	Tr_{LF}		4,5,6	All		14	ms
Weight		Flange				75	grams

Notes:

1/ Parameter guaranteed by line load, and cross regulation tests.
2/ Up to 90 percent of full power is available from either output provided the total output does not exceed 30 W.
3/ Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
4/ Load current split equally between $+V_{OUT}$ and $-V_{OUT}$.
5/ Three-watt load on output under test, 3 watt to 27 watt load change on other output.
6/ Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.
7/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter, parameters shall be guaranteed to the limits specified in Table I.
8/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
9/ Load step transition time between 2 and 10 microseconds.
10/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1 percent of V_{OUT} at 50 percent load.
11/ Input step transition time between 2 and 10 microseconds.
12/ Turn-on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 8) while power is applied to the input.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.5V to 180V
Soldering Temperature	300°C for 10 seconds
Case Temperature	Operating-55°C to +125°C Storage -65°C to +135°C

TABLE II - Electrical Performance Characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{IN} = 28VDC ±5%, C_L = 0 Unless Otherwise Specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Output Voltage	V_{OUT}	VIN = 18, 28, 40 VDC I_{OUT} = 0	1	ALL	±14.85	±15.15	VDC
			2, 3	ALL	±14.70	±15.30	VDC
Output Current 11/ 13/	I_{OUT}	V_{IN} = 18, 28, 40 VDC	1, 2, 3	ALL	0.200	2000	mADC
Output Ripple Voltage 8/	V_{RIP}	VIN = 18, 28 40 VDC B.W. = DC TO 1 MHz	1, 2, 3	ALL		85	mVp-p
Output Power 4/ 11/	P_{OUT}	V_{IN} = 18, 28, 40 VDC	1, 2, 3	ALL	30		W
Line Regulation 9/ 10/	VR_{LINE}	V_{IN} = 18, 28, 40 VDC I_{OUT} = 0, 1000, 2000 mA	1	ALL		35	mV
			2, 3	ALL		75	mV
Load Regulation 9/ 10/	VR_{LOAD}	V_{IN} = 18, 28, 40 VDC I_{OUT} = 0, 1000, 2000 mA	1, 2, 3	ALL		150	mV
Input Current	I_{IN}	I_{OUT}=0, inhibit (pin 8) = 0	1, 2, 3	ALL		12	mADC
		I_{OUT}=0, inhibit (pin 8) Open	1, 2, 3	ALL		30	mADC
Input Ripple Current	I_{RIP}	I_{OUT} = 2000mA	1, 2, 3	ALL		60	mAp-p
Efficiency	EFF	I_{OUT} = 2000mA T_C = 25°C	1	ALL	80		%
Isolation	ISO	Input to output or any pin to case (except pin 8) at 500 VDC, T_C = 25°C	1	ALL	100		Mohms
Capacitive Load 6/ 12/	C_L	No effect on DC performance T_C = 25°C	4	ALL		500	ufd
Power dissipation load fault	P_D	Overload, T_C = 25°C 3/	1	ALL		9	W
		Short Circuit, T_C = 25°C	1	ALL		9	W
Switching frequency	F_S	I_{OUT} = 2000 mA	1, 2, 3	01	237	263	KHz
			1, 2, 3	02	230	245	KHz
			1, 2, 3	03	250	265	KHz

See footnotes at end of table.

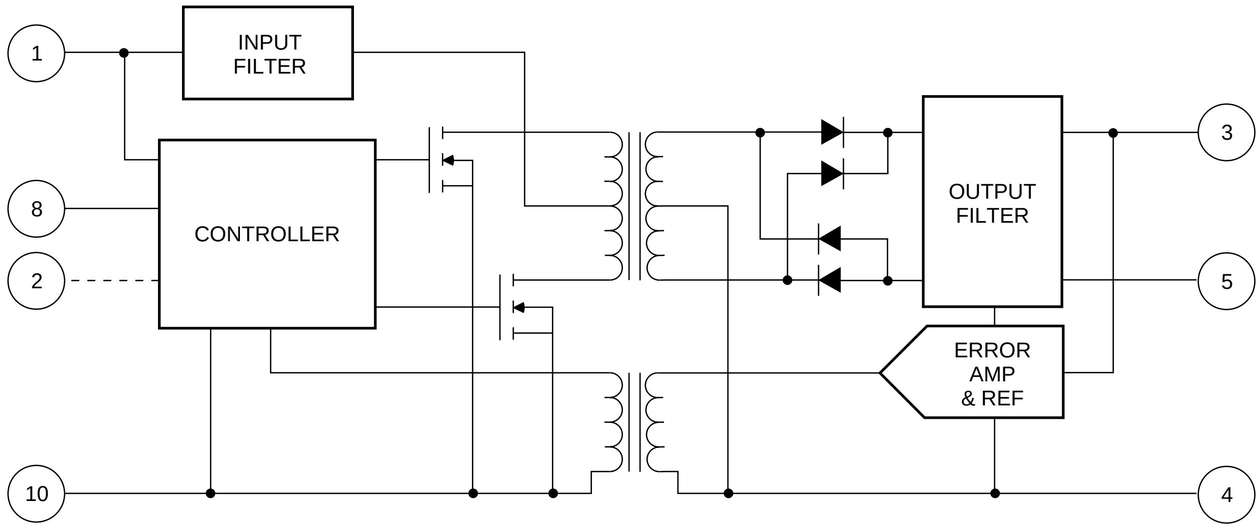
TABLE II - Electrical Performance Characteristics (continued)

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{IN} = 28VDC ±5%, C_L = 0 UNLESS OTHERWISE SPECIFIED	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Output response to step transient load changes 7/ 9/ 10/	VO_{TLOAD}	50% load to/from 100% load	4, 5, 6	All	-300	+300	mV pk
		No load to 100% load	4, 5, 6	All	-800	-800	mV pk
		100% load to no load	4, 5, 6	All	+800	+800	
Recovery time, step transient load changes 1/ 7/	TT_{LOAD}	50% load to/from 100% load	4, 5, 6	All		25	us
		No load to 50% load	4, 5, 6	All		500	us
		50% load to no load	4, 5, 6	All		7	ms
Output response to transient step line changes 5/ 12/	VO_{TLINE}	Input step from 18 to 40VDC	4, 5, 6	All		+180	mV pk
		Input step from 40 to 18VDC	4, 5, 6	All		-600	mV pk
Recovery time transient step line changes 1/ 5/ 12/	TT_{LINE}	Input step from 18 to 40VDC	4, 5, 6	All		400	us
		Input step from 40 to 18VDC	4, 5, 6	All		400	us
Turn-on overshoot	$VTON_{OS}$	I_{OUT} = 0, 2000mA	4, 5, 6	All		750	mV pk
Turn-on delay 2/	TON_D	I_{OUT} = 0, 2000mA	4, 5, 6	All		12	ms
Load fault recovery 12/	Tr_{LF}	V_{IN} = 18 to 40 VDC	4, 5, 6	All		12	
Weight		Flange				75	grams

Notes:

1/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of V_{OUT} at 50% load.
2/ Turn-on delay time measurement is for either a step application of power at the input or the removal of a ground signal from the inhibit pin (pin 8) while power is applied to the input.
3/ An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
4/ Above +125°C case, derate output power linearly to 0 at +135°C case.
5/ Input step transition time between 2 and 10 microseconds.
6/ Capacitive load may be any value from 0 to the maximum limit without compromising DC performance. A capacitive load in excess of the maximum limit will not disturb loop stability but will interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn on.
7/ Load step transition time between 2 and 10 microseconds.
8/ Bandwidth guaranteed by design. Tested for 20 KHz.
9/ Load current split equally between $+V_{OUT}$ and $-V_{OUT.}$
10/ When operating with unbalanced loads, at least 25% of the load must be on the positive output to maintain regulation.
11/ Parameter guaranteed by line and load regulation tests.
12/ Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified in Table II.
13/ Up to 90% of full power is available from either output provided the total output does not exceed 30 watts.

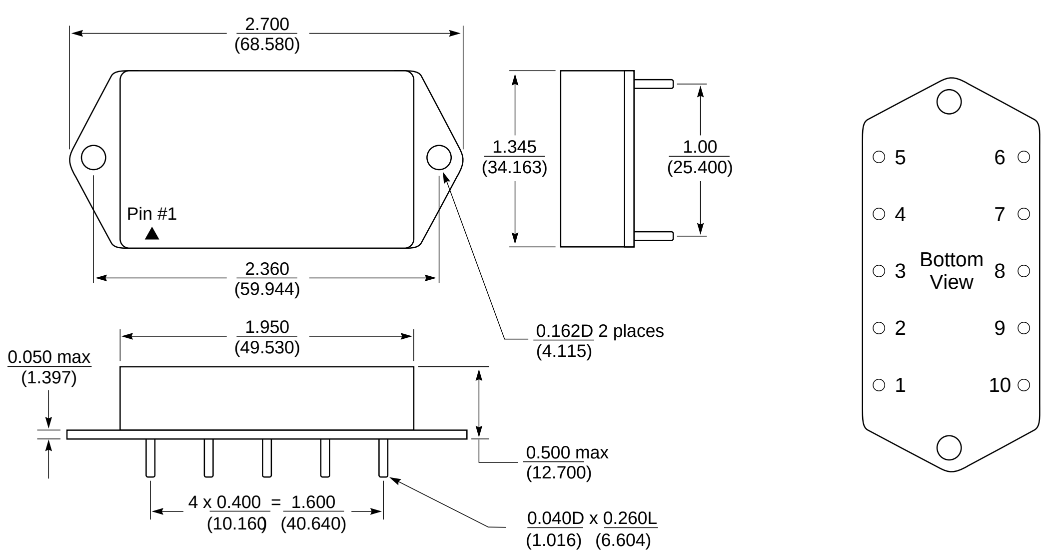
BLOCK DIAGRAM



PIN DESIGNATION

Pin 1	Positive input	Pin 10	Input common
Pin 2	N/C standard or Synchronization (optional)	Pin 9	N/C
Pin 3	Positive output	Pin 8	Inhibit
Pin 4	Output common	Pin 7	Case ground
Pin 5	Negative output	Pin 6	N/C

MECHANICAL OUTLINE



PART NUMBER

ATW 28 xx D / x - xxx

Model

Input Voltage

Output Voltage

12 = 12VDC

15 = 15VDC

Dual Output

Synchronization Option

Omit for standard

MSTR = Master

S:V = Slave

Temperature Range

Omit for -55°C to +85°C

ES = -55°C to +105°C

HB = -55°C to 125°C

CH = -55°C to 125°C

Available Screening Levels and Process Variations for ATW 2800D Series

Requirement	MIL-STD-883 Method	No Suffix	ES Suffix	HB Suffix	CH Suffix
Temperature Range		-55°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Element Evaluation					MIL-PRF-38534
Internal Visual	2017	✶	✓	✓	✓
Temperature Cycle	1010, Cond C		Cond A	✓	✓
Constant Acceleration	2001, Cond A		500g	5,000g	5,000g
Burn-in	1015		96hrs @ 105°C	160hrs @ 125°C	160hrs @ 125°C
Final Electrical (Group A)	Specification	25°C	25°C	-55, +25, +125°C	-55, +25, +125°C
Seal, Fine & Gross	1014		✓	✓	✓
External Visual	2009	✶	✓	✓	✓

✶ per Commercial Standards

STANDARDIZED MILITARY DRAWING CROSS REFERENCE

Standardized Military Drawing PIN	Vendor CAGE Number	Vendor Similar PIN
5962-9210901HZX	52467	ATW2812D/CH
5962-9210902HZX	52467	ATW2812D/CH-SLV
5962-9210903HZX	52467	ATW2812/CH-MSTR
5962-9161301HZX	52467	ATW2815D/CH
5962-9161302HZX	52467	ATW2815D/CH-SLV
5962-9161303HZX	52467	ATW2815D/CH-MSTR

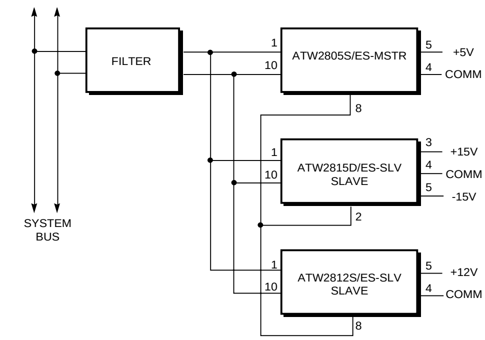
APPLICATION INFORMATION

Device Synchronization

Whenever multiple DC/DC converters are utilized in a single system, significant low frequency noise may be generated due to slight differences in the switching frequencies of the converters (beat frequency noise). Because of the low frequency nature of this noise (typically less than 10 KHz), it is difficult to filter out and may interfere with proper operation of sensitive systems (communications, radar or telemetry). Lambda Advanced Analog offers an option which provides synchronization of multiple AHE/ATW type converters, thus eliminating this type of noise.

To take advantage of this capability, the system designer must assign one of the converters as the master. Then, by definition, the remaining converters become slaves and will operate at the masters' switching frequency. The user should be aware that the synchronization system is fail-safe; that is, the slaves will continue operating should the master frequency be interrupted for any reason. The layout must be such that the synchronization output (pin 2) of the master device is connected to the synchronization input (pin 2) of each slave device. It is advisable to keep this run short to minimize the possibility of radiating the 250 KHz switching frequency.

The appropriate parts must be ordered to utilize this feature. After selecting the converters required for the system, a 'MSTR' suffix is added for the master converter part number and a 'SLV' suffix is added for slave part number. See Part Number section.



Typical Synchronization Connection Diagram

Inhibit Function

Connecting the inhibit input (Pin 8) to input common (Pin 10) will cause the converter to shut down. It is recommended that the inhibit pin be driven by an open collector device capable of sinking at least 400 µA of current. The open circuit voltage of the inhibit input is 11.5 ±1 VDC.

EMI Filter

An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461B CEO3.

NOTES

 The information in this data sheet has been carefully checked and is believed to be accurate; however no responsibility is assumed for possible errors. These specifications are subject to change without notice. 9847

LAMBDA ADVANCED ANALOG INC.

MIL-PRF-38534 Certified
ISO9001 Registered

2270 Martin Avenue
Santa Clara CA 95050-2781
(408) 988-4930 FAX (408) 988-2702