HB56A432 Series — HITACHI/ LOGIC/ARRAYS/MEM

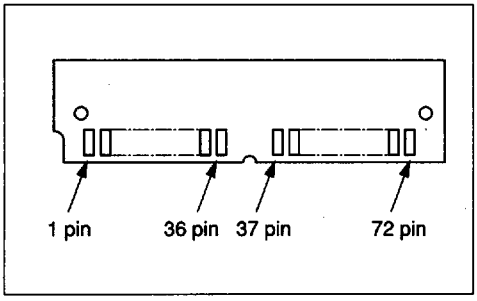
4,194,304-Word × 32-Bit High Density Dynamic RAM Module

The HB56A432 is a 4 M × 32 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117400J) sealed in SOJ package. An outline of the HB56A432 is 72-pin single in-line package. Therefore, the HB56A432 makes high density mounting possible without surface mount technolgy. The HB56A432 provides common data inputs and outputs.
Decoupling capacitors are mounted beneath each SOJ.

Features

- 72-pin single in-line package
  - Lead pitch : 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - Access time : 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode : 4.62 W/4.20 W/3.78 W (max)
  - Standby mode : 84 mW (max)
- Fast page mode capability
- 2,048 refresh cycle/32 ms
- 2 variations of refresh
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
- TTL compatible

Pin Arrangement



Ordering Information

Type No.	Access time	Package	Contact pad
HB56A432B-6	60ns	72-pin SIP socket type	gold
HB56A432B-7	70 ns		
HB56A432B-8	80 ns		
HB56A432SB-6	60ns	72-pin SIP socket type	solder
HB56A432SB-7	70 ns		
HB56A432SB-8	80 ns		

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

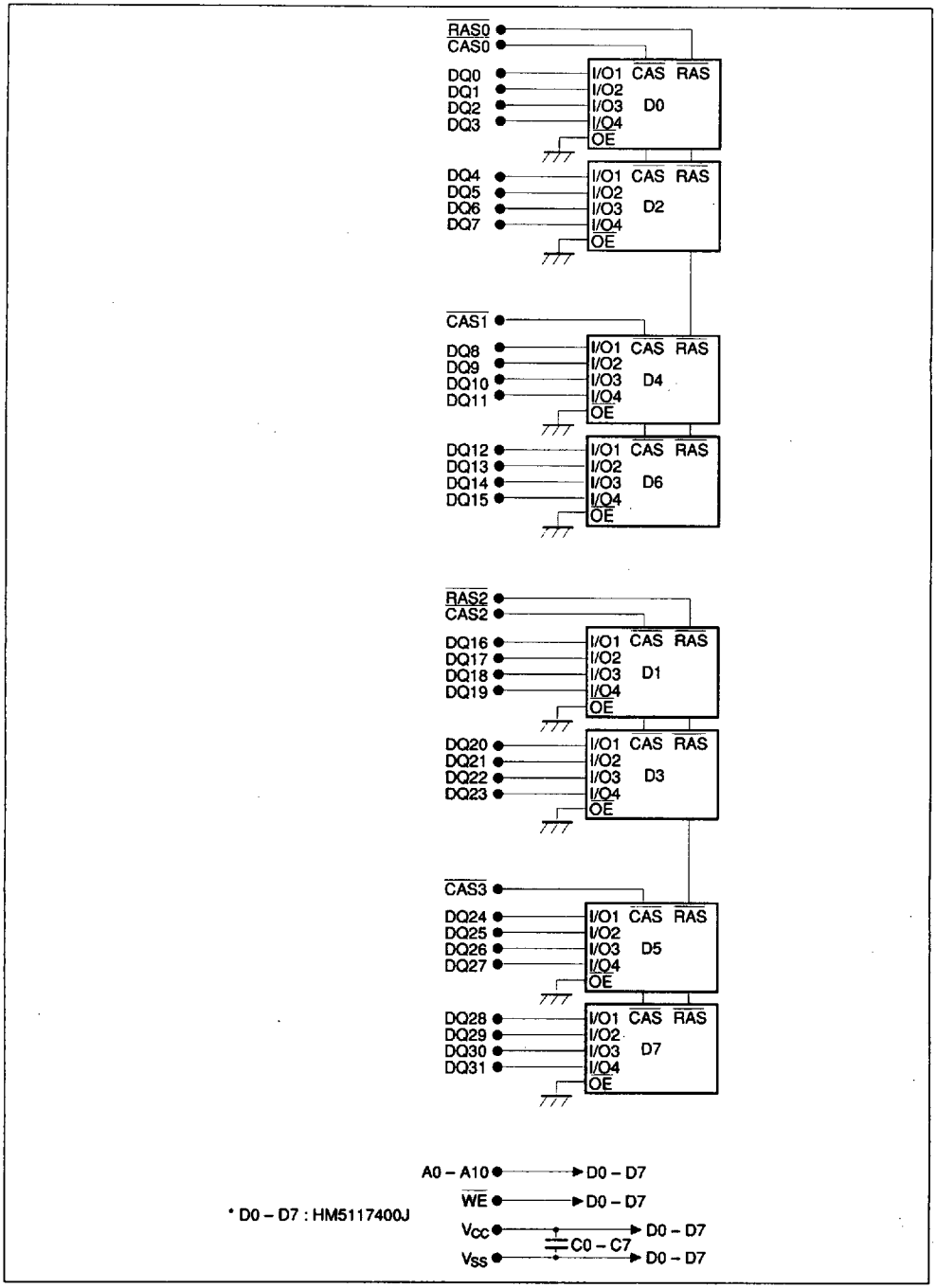
Pin Description

Pin name	Function
A0–A10	Address input
A0–A10	Refresh address input
DQ0–DQ31	Data-in/data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS2}$	Raw address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1–PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56A432B/SB		
Pin No.	Pin name	60 ns	70 ns	80 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

Block Diagram



HB56A432 Series

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin	(Input)	Vin	–1.0 to +7.0	V
relative to V_{SS}	(Output)	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	8	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56A432B/SB								
		-6		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test condition	Notes
Operating current	I_{CC1}	—	880	—	800	—	720	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	880	—	800	—	720	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	880	—	800	—	720	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	640	—	560	—	520	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
Output capacitance (DQ0 – DQ31)	$C_{I/O}$	—	17	pF	1, 2

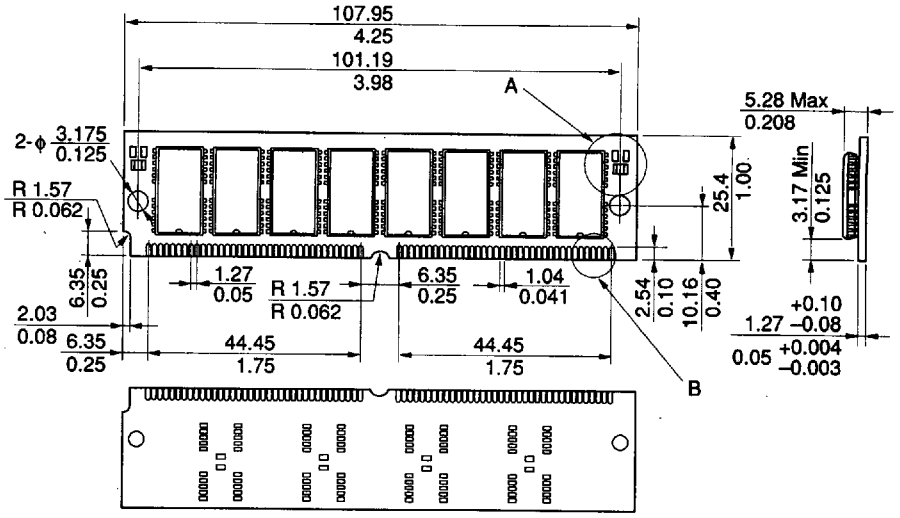
Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

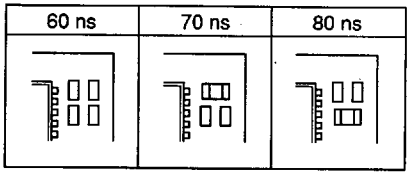
- Refer to the HM5117400 data sheet.
- The HB56A432 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available. ($\overline{OE}$ pin is fixed to V_{SS}).

Physical Outline

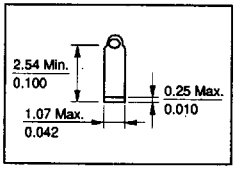
Unit : mm/inch



Detail A



Detail B



Note: Following the specification of the contact pads.

Type no.	Contact pad
HB56A432B-XX	gold
HB56A432SB-XX	solder