AT&T

Preliminary

DATA SHEET

439C Sub-Band Decoder

FEATURES

- 64 x 8-bit input FIFO memory buffer
- 64 x 8-bit output FIFO memory buffer
- Decodes 16 kb/s or 24 kb/s
- 1.67 MHz maximum parallel input data rate
- Input FIFO and output FIFO flags
- Serial data access to DSP, bypassing input FIFO
- TTL-compatible inputs and outputs
- FCC part 68.308 protection circuitry
- Multichannel operation under host control
- μ-law 64 kb/s PCM speech output
- Supports AT&T Voice Store and Forward Standards

DESCRIPTION

The 439C Sub-Band Decoder is a single-package integrated circuit. The device combines a CMOS memory buffer and a *WE*® DSP20 Digital Signal Processor (DSP) in a single dual-cavity ceramic 40-pin DIP. It is capable of producing high quality speech at either 16 kb/s or 24 kb/s under the control of a channel-encoded token. The 439C Sub-Band Decoder requires a single 5 V supply.

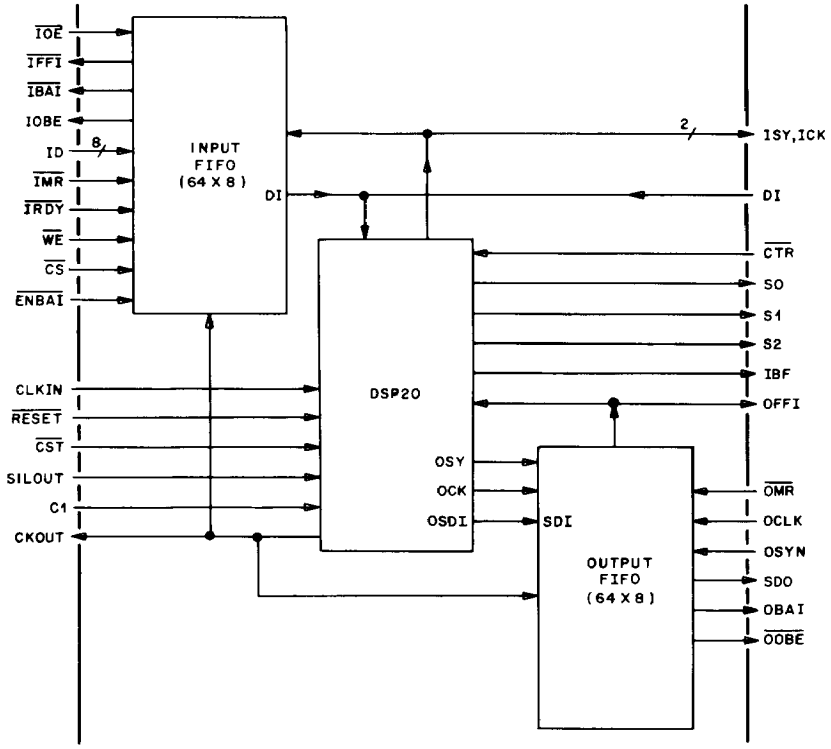
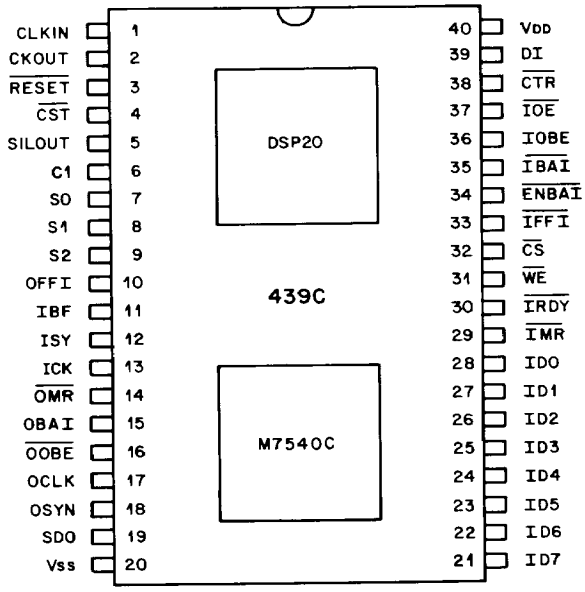


Figure 1. 439C Sub-Band Decoder Block Diagram

The information contained herein is preliminary and subject to change.

USER INFORMATION

Pin Descriptions



Symbols					
Sym	**Pin**	**Sym**	**Pin**	**Sym**	**Pin**
CKOUT	2	ID4	24	$\overline{OMR}$	14
CLKIN	1	ID5	23	$\overline{OOBE}$	16
$\overline{CS}$	32	ID6	22	OSYN	18
$\overline{CST}$	4	ID7	21	$\overline{RESET}$	3
$\overline{CTR}$	38	$\overline{IFFI}$	33	SDO	19
DI	39	$\overline{IMR}$	29	SILOUT	5
$\overline{ENBAI}$	34	IOBE	36	S0	7
$\overline{IBAI}$	35	$\overline{IOE}$	37	S1	8
IBF	11	$\overline{IRDY}$	30	S2	9
ICK	13	ISY	12	VDD	40
ID0	28	C1	6	VSS	20
ID1	27	OBAI	15	$\overline{WE}$	31
ID2	26	OCLK	17		
ID3	25	OFFI	10		

Figure 2. 439C Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. 439C Pin Descriptions

Pin	Symbol	Type	Name/Function
1	CLKIN	I	**Clock Input.**
2	CKOUT	O	**Clock Output.** System clock.
3	$\overline{RESET}$	I	**Reset (Active Low).** Suspends all DSP operations. After rising edge, DSP responds to new speech instructions, disregarding inputs prior to $\overline{RESET}$.
4	$\overline{CST}$	I	**Control Strobe (Active Low).** When low, SILOUT (pin 5) and C1 (pin 6) are transparent to the DSP. When high, the values of SILOUT and C1 at the time of $\overline{CST}$'s rising edge are latched into the DSP.
5	SILOUT	I	**Silence Output.** When tied to OBAI (pin 15), permits automatic output of silence when input FIFO is empty. When tied low, output is unpredictable when $\overline{OOBE}$ goes low.
6	C1	I	**FCC Part 68 Select.** When C1 is high, the FCC part 68 protection circuit is active; when C1 is low, it is inactive.
7 8 9	S0 S1 S2	O	**Status Register Outputs, Bits 0, 1, and 2.** No connection.

Table 1. 439C Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
10	OFFI	O	**Output FIFO Full Indicator.** When high, indicates output FIFO contains 64 bytes of data (full). If high for more than 500 μs, DSP could be in an indeterminate state.
11	IBF	O	**Input Buffer Full.** Indicates state of DSP input buffer. Set after 8 bits have been written into the DSP input buffer; cleared after the DSP has read the buffer.
12	ISY	O	**Input Sync.** Indicates start of data transfer to input buffer. Generated by DSP. ISY has a weak pull-down (50 kΩ nominal) to ground to prevent ISY from floating when $\overline{\text{CTR}}$ is high.
13	ICK	O	**Input Clock.** One-half CLKIN. Data shifted into the input buffer is latched on rising edge of ICK. Generated by DSP. ICK has a weak pull-down (50 kΩ nominal) to ground to prevent ICK from floating when $\overline{\text{CTR}}$ is high.
14	$\overline{\text{OMR}}$	I	**Output FIFO Master Reset (Active Low).** Resets all of the counters and pointers in the output FIFO.
15	OBAI	O	**Output FIFO Bytes Available Indicator.** High when less than 8 bytes are in output FIFO.
16	$\overline{\text{OOBE}}$	O	**Output FIFO Output Buffer Empty (Active Low).** Low when last bit of last byte has been shifted out of output FIFO.
17	OCLK	I	**Output Clock.** Output FIFO serial data output clock. Must be continuous.
18	OSYN	I	**Output FIFO Serial Data Output Sync Pulse.** Initiates transfer of data out of output FIFO.
19	SDO	O	**Serial Data Output.** Data is shifted out of the output FIFO on the negative edge of OCLK.
20	V_{SS}	—	**Ground.**
21 22 23 24 25 26 27 28	ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0	I	**Input Data Bus.**
29	$\overline{\text{IMR}}$	I	**Input FIFO Master Reset (Active Low).** Resets all counters and pointers in the input FIFO.
30	$\overline{\text{IRDY}}$	I	**Input Ready (Active Low).** Verifies that data on the input data bus is valid. Used with slower microprocessors. Can be tied low if it is not needed.

Table 1. 439C Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
31	$\overline{WE}$	I	**Write Enable (Active Low).** When low, input data is transferred from the input data bus to the input FIFO if $\overline{CS}$ and $\overline{IRDY}$ are low and $\overline{IFFI}$ is high.
32	$\overline{CS}$	I	**Chip Select (Active Low).** When low, input FIFO is selected.
33	$\overline{IFFI}$	O	**Input FIFO Full Indicator (Active Low).** Indicates input FIFO is full (contains 64 bytes of data). When low, further writes to input FIFO are ignored.
34	$\overline{ENBAI}$	I	**Enable Bytes Available Indicator (Active Low).** Disables $\overline{IBAI}$ until the next data write.
35	$\overline{IBAI}$	O	**Input FIFO Bytes Available Indicator (Active Low).** Goes low when there are less than 32 bytes in the input FIFO.
36	IOBE	O	**Input FIFO Output Buffer Empty.** Indicates when the last bit of the last byte has been shifted out of the input FIFO.
37	$\overline{IOE}$	I	**Input FIFO Output Enable (Active Low).** When low, input FIFO serial data output is input to the DSP. When high, serial data of input FIFO is in high-impedance state, allowing external hardware to provide data, via pin 39, coordinated with DSP-generated sync and clock lines (pins 12 and 13).
38	$\overline{CTR}$	I	**Clear to Read (Active Low).** Enables data reception by the DSP.
39	DI	I	**Data Input.** Receives serial data for DSP from input FIFO or external input.
40	V_{DD}	—	**5 V Supply.**

Operation

The 439C Sub-Band Decoder corresponds to the sub-band code (SBC) standard, Voice Store and Forward Standards, authorized by the AT&T Chief Architect's Division.

The 439C device can provide high quality speech at either 16 kb/s or 24 kb/s , corresponding to the AT&T standard. As shown on Figure 1, the device consists of an input and output FIFO and a *WE* DSP20 Digital Signal Processor (DSP). Figure 3 shows a simplified block diagram of the input and output FIFOs.

Parallel data is entered via the input FIFO input data bus (ID0—ID7) and written to the dual-port RAM. The RAM can buffer up to sixty-four 8-bit words. At the same time, the DSP can read the RAM through the parallel-to-serial shift register of the input FIFO. The output of the shift register is the input data to the DSP. The dual-port RAM used for the FIFO implementation facilitates simultaneous reading and writing of the memory.

To reset the counter and pointers in the input and output FIFOs, $\overline{IMR}$, and $\overline{OMR}$ are brought low. The RAM data is then overwritten with the new input data. All DSP operations are suspended by bringing $\overline{RESET}$ low.

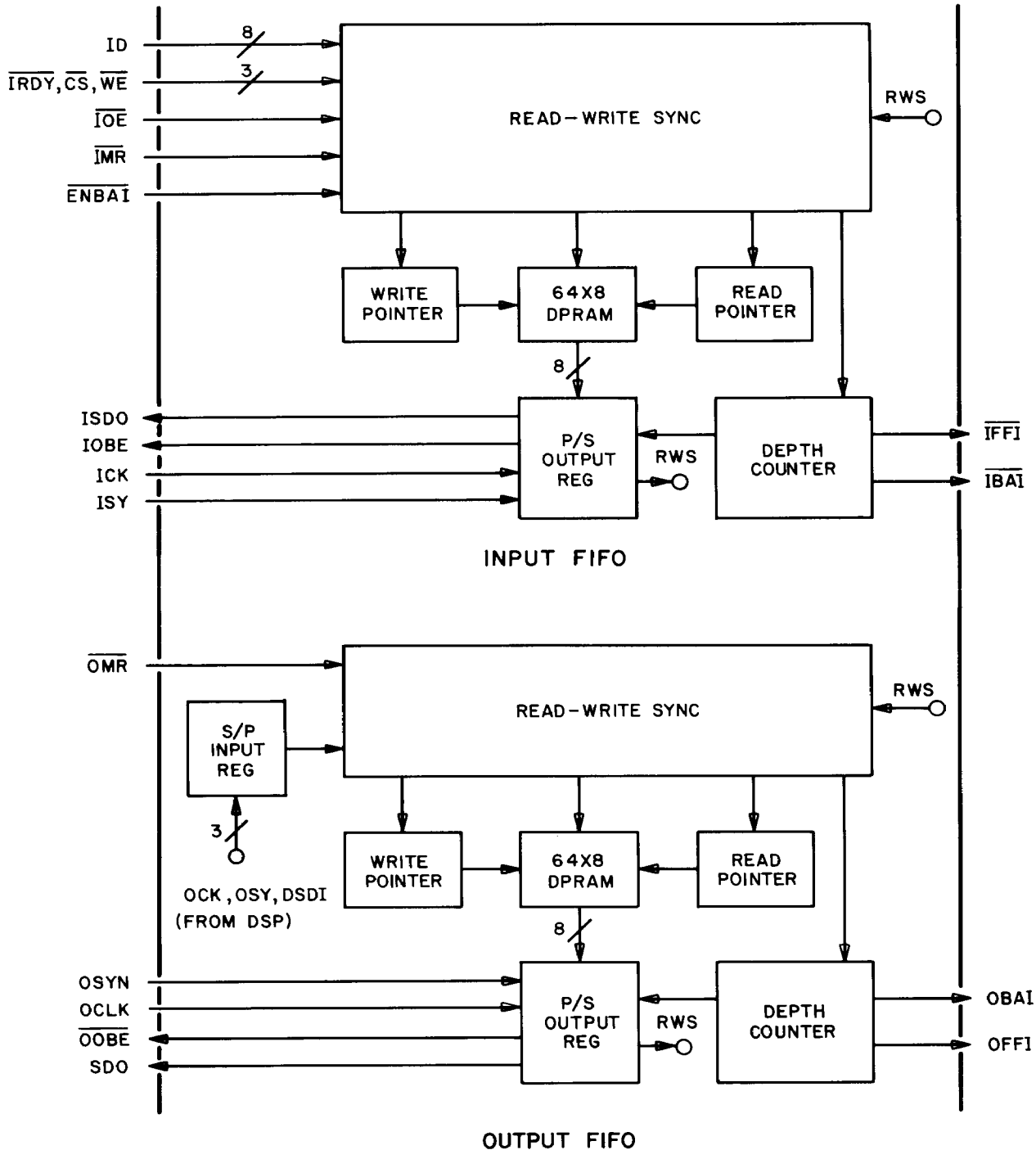


Figure 3. Input and Output FIFOs Simplified Block Diagram

Data can be entered either in parallel form through the input FIFO or in serial form directly to the DSP. To write to the input FIFO, $\overline{CS}$, $\overline{IRDY}$, and $\overline{WE}$ must be active. $\overline{IOE}$ must be active for serial data to be output to the DSP from the input FIF0 (see **Timing Characteristics**).

To enter serial data into the DSP, bypassing the input FIFO, DSP-generated ISY and ICK provide the timing to input data through DI (see **Timing Characteristics**). During parallel data input, DI should not be driven.

The 439C has six flags or indicators. $\overline{IBAI}$ goes low when there are less than 32 bytes in the input FIFO. A pulse signal on $\overline{ENBAI}$ disables this function. As long as $\overline{ENBAI}$ remains active, $\overline{IBAI}$ remains disabled. $\overline{IBAI}$ starts to function normally upon the next completed write.

$\overline{IFFI}$ goes low (active) when the input FIFO contains 64 bytes of data in memory. When active, $\overline{IFFI}$ indicates that the input FIFO is full. Further writes are ignored until $\overline{IFFI}$ goes high as a result of a DSP read or an $\overline{IMR}$ going low.

When the last bit of the last byte has been shifted out of the output shift register of the input FIFO, IOBE goes high (active).

OFFI goes high when the output FIFO contains 64 bytes of data in memory. The DSP could be in an indeterminate state if OFFI is high for more than 500 μs.

OBAI goes high when there are less than eight bytes in the output FIFO. When the last bit of the last byte is shifted out of the output shift register, $\overline{OOBE}$ goes low.

As an added feature, if OBAI is tied to SILOUT, the DSP starts writing data to the output FIFO when the output FIFO is nearly empty. It writes silence until more data is entered into the input FIFO.

Data transfer from the input FIFO to the DSP is controlled by connecting IOBE to $\overline{CTR}$.

CHARACTERISTICS

Clocks

Clock Input: 6—10 MHz (50% ± 2% duty cycle).
Input serial clock provided by DSP is 1/2 system clock.
Output serial clock provided by external hardware, maximum is 1/2 system clock (50% ± 2% duty cycle).

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 ± 0.25 V, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current	I_{DD}	—	225	mA	—
Input Current					
High Level (Logic 1)	I_{IH}	—	20	μA	V_{IH} = 5.25 V
Low Level (Logic 0)	I_{IL}	—	−20	μA	V_{IL} = 0.4 V
Output Current					
High Level (Logic 1)	I_{OH}	—	−400	μA	V_{OH} = 2.7 V
Low Level (Logic 0)	I_{OL}	—	1.6	mA	V_{OL} = 0.5 V
Input Voltage					
High Level (Logic 1)	V_{IH}	2.4	—	V	—
Low Level (Logic 0)	V_{IL}	—	0.7	V	—
Output Voltage					
High Level (Logic 1)	V_{OH}	2.7	—	V	—
Low Level (Logic 0)	V_{OL}	—	0.5	V	—
Power Dissipation	PD	—	1.5	W	V_{DD} = 5.0 V

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD}) ..... V_{SS} −0.5 to V_{SS} +6 V
Input Voltage Range (V_I) ..... V_{SS} −0.5 to V_{DD} +0.5 V
Power Dissipation (PD) ..... 2 W
Ambient Operating Temperature Range (T_A) ..... −40 to +95 °C
Storage Temperature Range (Tstg) ..... −40 to +95 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Timing characteristics refer to the behavior of the device under specified conditions and to the requirements imposed on the user for proper operation of the device. All timing data is valid for the following conditions:

T_A = 0 to 70 °C; V_{DD} = 5 ± 0 .25 V; V_{SS} = 0 V; capacitive load on outputs = 50 pF.

Timing Characteristics for Clocks and Control (See Figure 4)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tCKILCKIL	CLKIN Period	100	170	ns
tCKILCKIH	CLKIN Low Time	46	—	ns
tCKIHCKIL	CLKIN High Time	46	—	ns
tCKILCKOL	CKOUT Delay	—	40	ns
tCKOLCKOH	CKOUT Low Time	tCKILCKIH−2	tCKILCKIH+2	ns
tS2HS2L	S2 Pulse Width	tCKILCKIL−10	tCKILCKIL+30	ns
tCSTLCSTH	$\overline{CST}$ Pulse Width	25	—	ns
tCVCSTH	SILOUT or C1 Set-Up Time	25	—	ns
tCSTHCX	SILOUT or C1 Hold Time	0	—	ns
tREST	$\overline{RESET}$ Pulse Width	6tCKILCKIL	—	ns

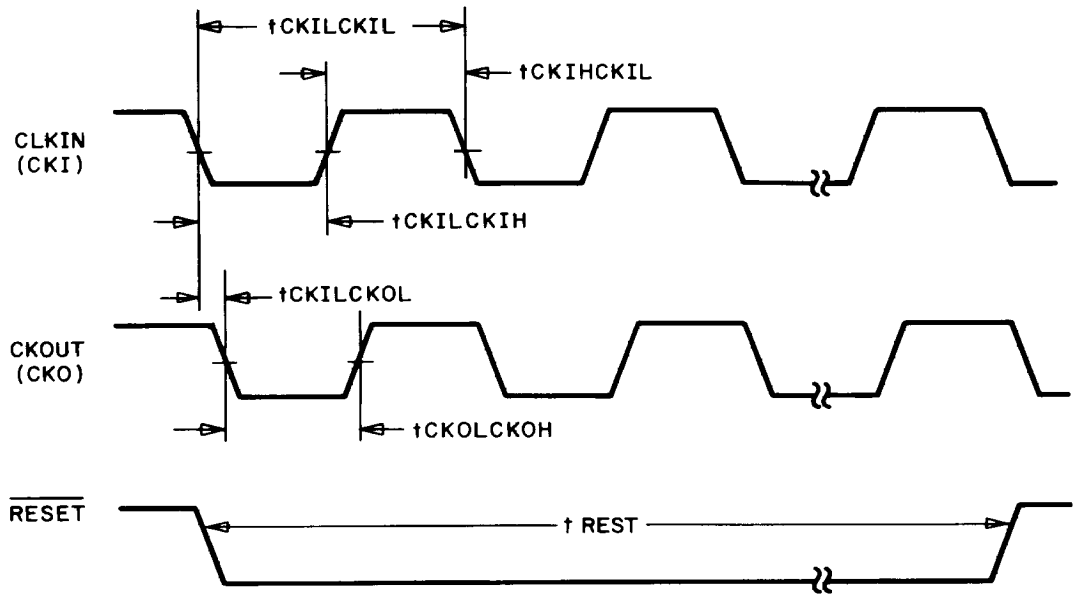
Timing Characteristics for Parallel Data Input (See Figure 5)				
Symbol	**Description**	**Min**	**Max**	**Unit**
tIMRL	$\overline{IMR}$ Pulse Width	2tCKILCKIL	—	ns
tIMRHWE/IRDYL	$\overline{IMR}$ High to $\overline{WE}$/$\overline{IRDY}$ Low	2tCKILCKIL	—	ns
tCSSU	$\overline{CS}$ Set-Up Time	20		ns
tCSLCSH	$\overline{CS}$ Pulse Width	2tCKILCKIL	—	ns
tWELWEH	$\overline{WE}$ Pulse Width	2tCKILCKIL	—	ns
tWELWEL	$\overline{WE}$ Low to $\overline{WE}$ Low	6tCKILCKIL	—	ns
tIRDYLIRDYH	$\overline{IRDY}$ Pulse Width	2tCKILCKIL	—	ns
tIRDYLIRDYL	$\overline{IRDY}$ Low to $\overline{IRDY}$ Low	6tCKILCKIL5	—	ns
tDSU	Data Set-Up Time	0	—	ns
tDH	Data Hold Time	2tCKILCKIL	—	ns
tEBALEBAH	$\overline{ENBAI}$ Pulse Width	2tCKILCKIL	—	ns
tEBALIBAH	$\overline{ENBAI}$ Low to $\overline{IBAI}$ High	—	2tCKILCKIL	ns
tWELIBAH	$\overline{WE}$ Low to $\overline{IBAI}$ High	—	5tCKILCKIL	ns
tWELIFFL	$\overline{WE}$ Low to $\overline{IFFI}$ Low	—	4tCKILCKIL	ns
tWELIOBEL	$\overline{WE}$ Low to IOBE Low	—	9tCKILCKIL	ns

Timing Characteristics for Serial Data Input (See Figure 6)				
Symbols	**Description**	**Min**	**Max**	**Unit**
tICKLICKL	ICK Period	2tCKILCKIL	–	ns
tICKLICKH	ICK Low Time	0.5tICKLICKL–10	.5tICKLICKL+10	ns
tISYHISYL	ISY Pulse Width	0.75tICKLICKL	1.1tICKLICKL	ns
tCTRLISYH	Delay to SYNC	20	tCKILCKIL+50	ns
tDIVICKH	DI Set-Up Time	20	–	ns
tICKHDIX	DI Hold Time	15	–	ns
tICKLIBFH	Delay of IBF	0	60	ns
tCTRLSV	Input Enable Delay	–	90	ns
tCTRHSZ	Input Disable Delay	–	70	ns
tISYHIBAL	ISY High to $\overline{\text{IBAI}}$ Low	–	6.5tICKLICKL + 5tCKILCKIL	ns
tISYHIFFH	ISY High to $\overline{\text{IFFI}}$ High	–	6.5tICKLICKL + 5tCKILCKIL	ns
tISYHIOBEH	ISY High to IOBE High	–	8.5tICKLICKL + 3tCKILCKIL	ns

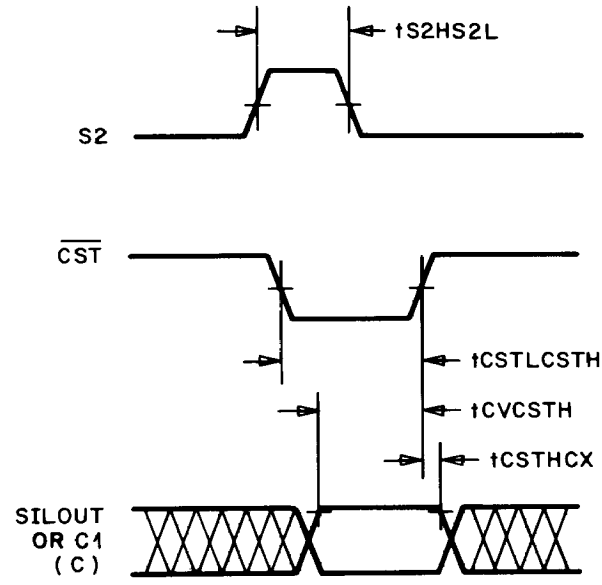
Timing Characteristics for Serial Data Output (See Figure 7)				
Symbols	**Description**	**Min**	**Max**	**Unit**
tOMRL	$\overline{\text{OMR}}$ Pulse Width	2tOCKLOCKL	–	ns
tOCKLOCKL	OCLK Period	2tCKILCKIL	–	ns
tOCKLOCKH	OCLK Low	0.5tOCKLOCKL–10	0.5tOCKLOCKL+10	ns
tOSYHOSYL	OSYN Pulse Width	tOCKLOCKL	5tOCKLOCKL	ns
tOSYHOSYH	OSYN High	11tOCKLOCKL	–	ns
tOCKLOSYL*	OCLK Low to OSYN Low	10	–	ns
tOCKLSDOX	SDO Hold Time	0	–	ns
tOCKLSDOV	SDO Delay	–	100	ns
tOSYHOBEL	OSYN High to $\overline{\text{OOBE}}$ Low	–	9tOCKLOCKL	ns
tOSYHOBAH	OSYN High to OBAI High	–	6.5tOCKLOCKL + 5tCKILCKIL	ns
tOSYHOFFL	OSYN High to OFFI Low	–	6.5tOCKLOCKL + 5tCKILCKIL	ns

*Clock under sync.

Timing Diagrams



A. Clocks



B. Control Timing

Figure 4. Clocks and Control Timing

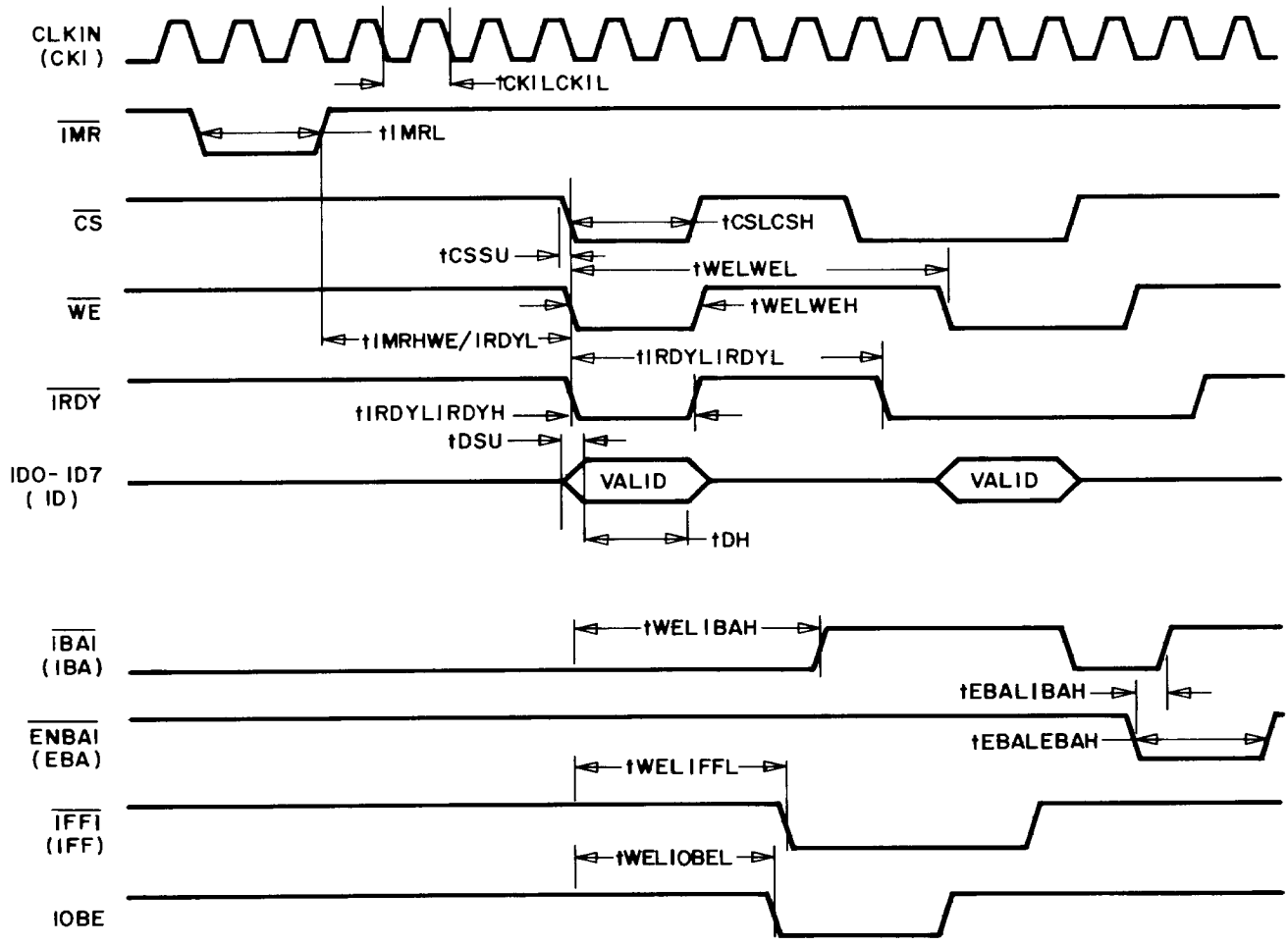


Figure 5. Parallel Data Input Timing

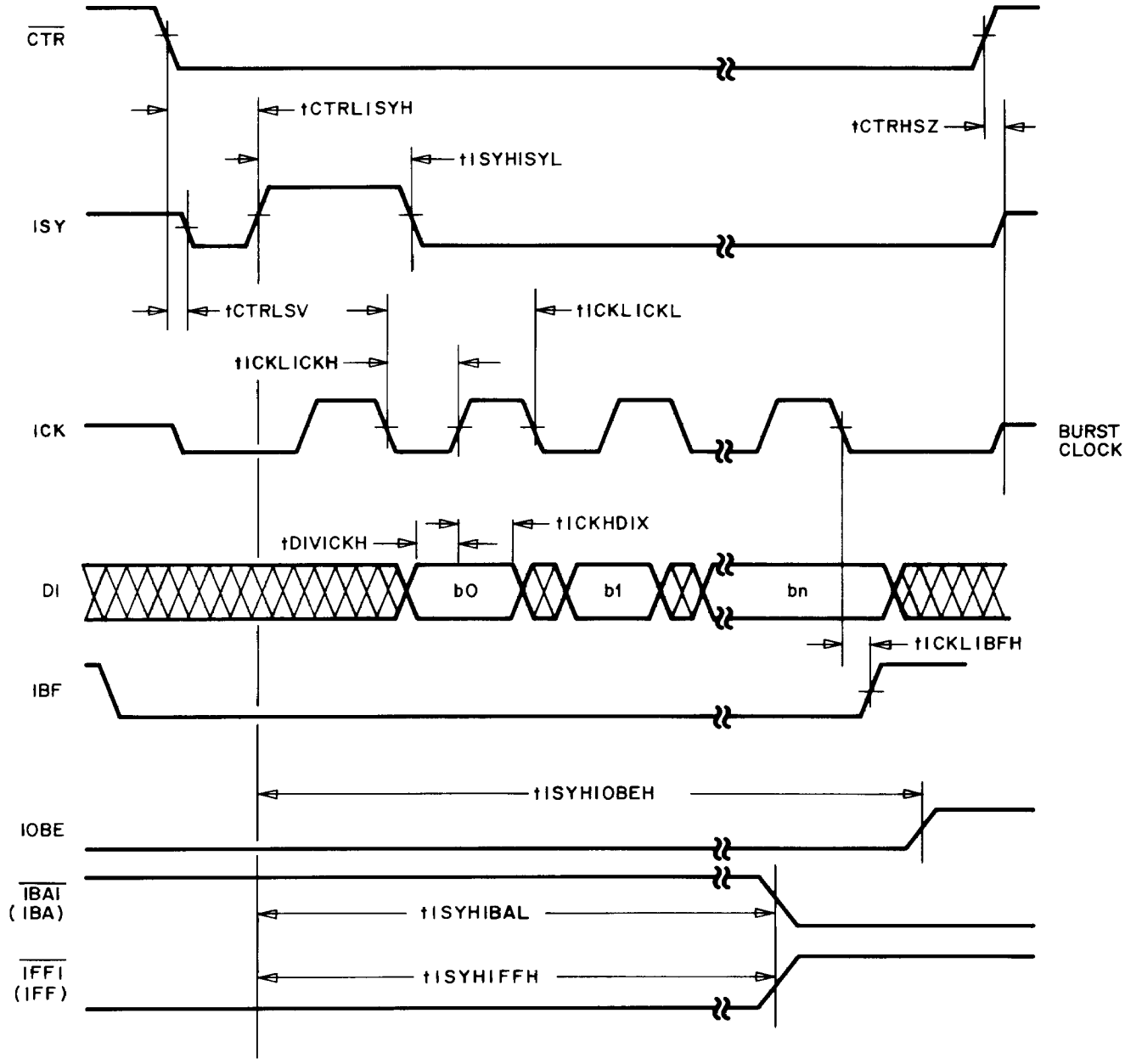


Figure 6. Serial Data Input Timing

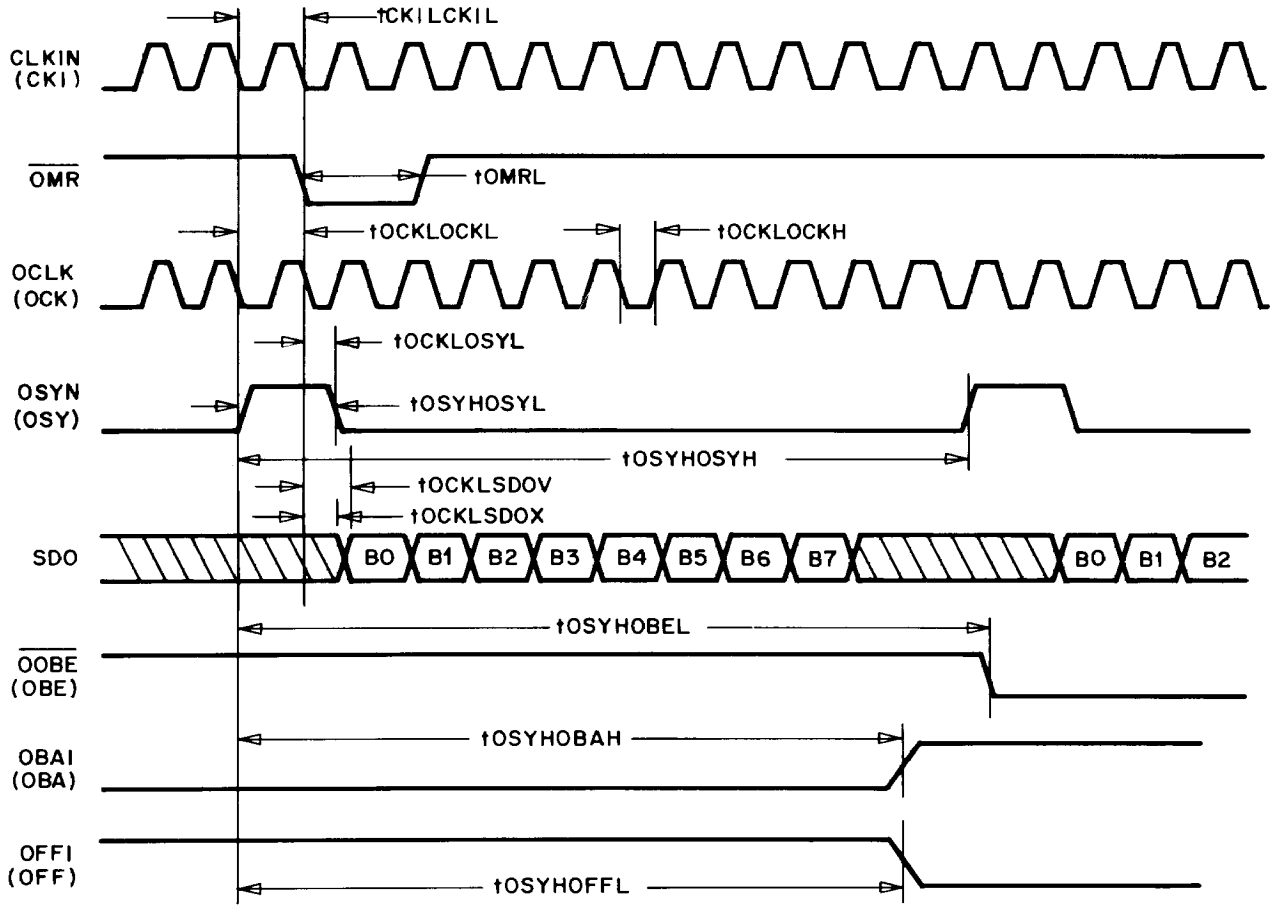
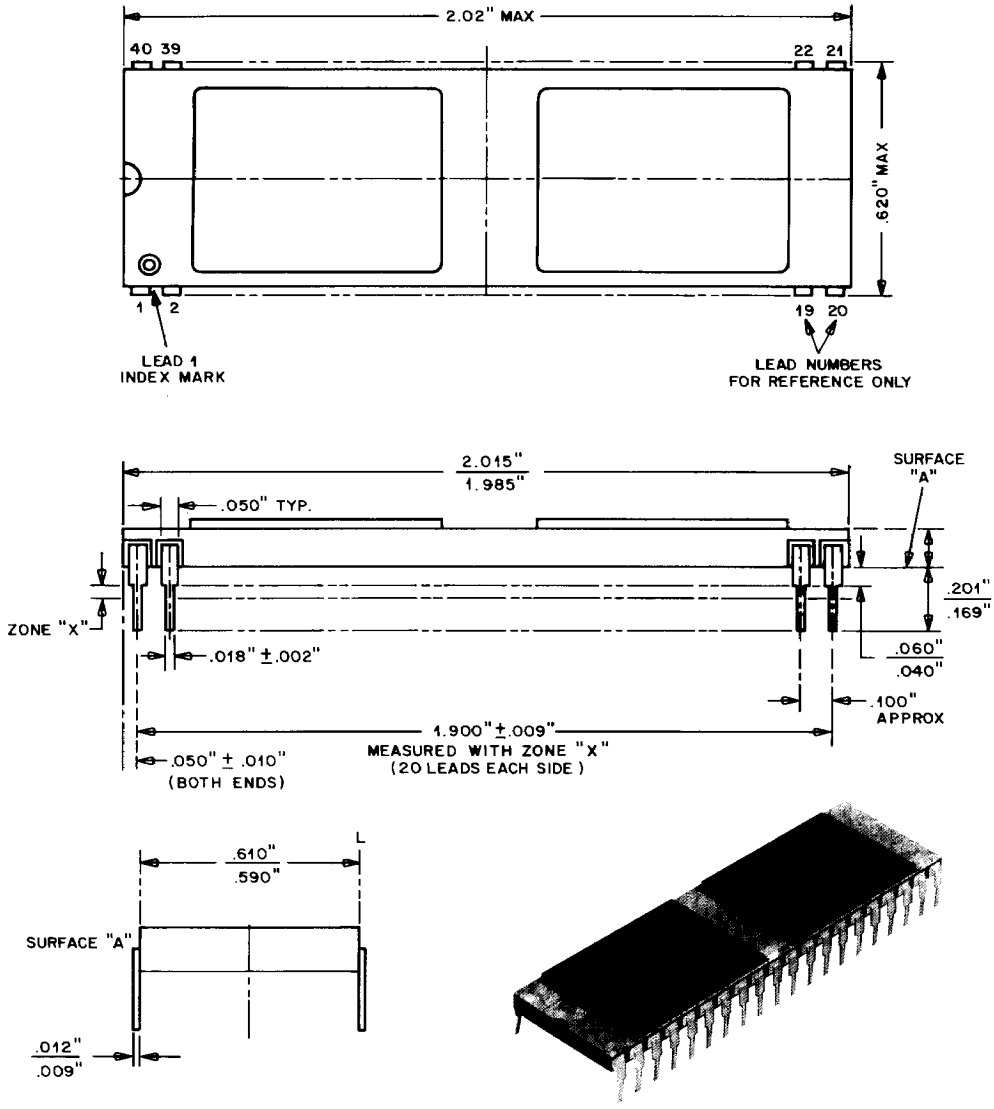


Figure 7. Serial Data Output Timing

Outline Diagram



NOTE: MEASUREMENTS ARE IN INCHES.

ORDERING INFORMATION

Device Code	Package	Temperature	COMCODE
439C	40-pin dual-cavity ceramic DIP	0 to 70 °C	104189675