CYPRESS SEMICONDUCTOR

Expandable 256K x 1 Static R/W RAM with Separate I/O

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **Five chip enables ($\overline{CE}_{1,2,3}$ and $CE_{4,5}$) to expand memory**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 770 mW**
- **Low standby power**
  - **— 330 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B163 is a high-performance BiCMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided five chip enables for each part ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$, CE_4, and CE_5). The active HIGH and active LOW chip enables provide on-chip address decoding, eliminating the need for external decoder logic.

The CY7B163 has an automatic power-down feature, reducing the power consumption by more than 50% when deselected by any CE input.

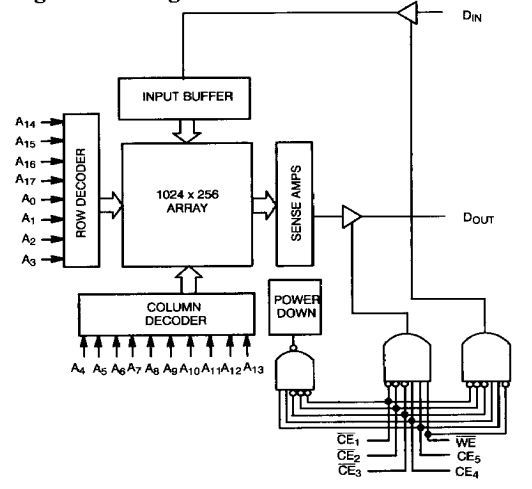
Writing to the device is accomplished when $\overline{CE}_{1,2,3}$ and $\overline{WE}$ are LOW, and $CE_{4,5}$ are HIGH. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enables $\overline{CE}_{1,2,3}$ LOW while $\overline{WE}$ and chip enables $CE_{4,5}$ remain HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output pin (D_{OUT}).

The output pin (D_{OUT}) is in a high-impedance state when the device is deselected (any of: $\overline{CE}_{1,2,3}$ HIGH or $CE_{4,5}$ LOW), or during a write operation ($\overline{WE}$ and $\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH).

The CY7B163 is available in leadless chip carriers and space-saving 300-mil-wide DIPs and SOJs.

Logic Block Diagram



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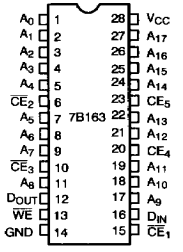
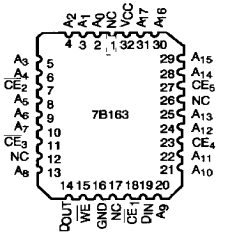
Pin Configurations

DIP/SOJ Top View



B163-2

LCC Top View



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Selection Guide

		7B163-10	7B163-12	7B163-15	7B163-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	150	130	125	
	Military		130	125	120
Maximum Standby Current (mA)	Commercial	30	30	30	
	Military		40	40	40

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} relative to GND[1] .. − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... − 0.5V to +7.0V

DC Input Voltage[1] ..... − 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		7B163−10 Min.	7B163−10 Max.	7B163−12 Min.	7B163−12 Max.	7B163−15, 20 Min.	7B163−15, 20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 0.8 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		150		130		125	mA
			Mil				130		125	
I_{SB}	Automatic CE Power-Down Current −CMOS Inputs	Max. V_{CC}, $CE_{1,2,3}$ ≥ V_{CC} − 0.3V, or $CE_{4,5}$ ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤0.3V, f=0	Com'l		40		30		30	mA
			Mil				40		40	

Shaded area contains advanced information.

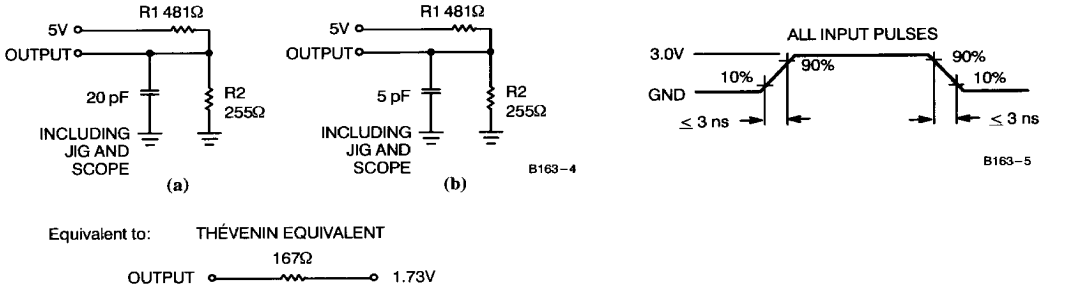
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. $V_{IL\,(Min)}$ = −3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 6]

Parameters	Description	7B163–10		7B163–12		7B163–15		7B163–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}_{1,2,3}$ HIGH or $CE_{4,5}$ LOW to High Z[7, 8]		6		7		8		10	ns
t_{PU}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}_{1,2,3}$ HIGH or $CE_{4,5}$ LOW to Power-Down		10		12		15		20	ns
WRITE CYCLE[9]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		5		7		7		10	ns

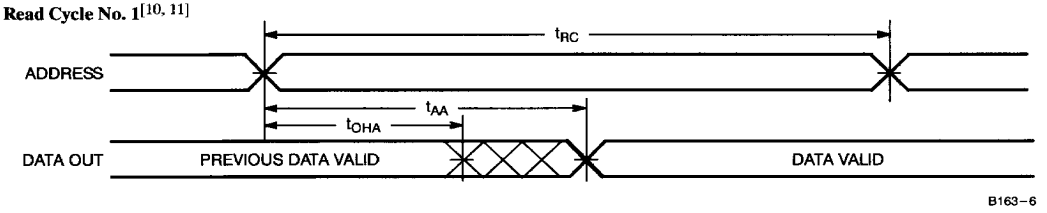
Shaded area contains advanced information.

Notes:

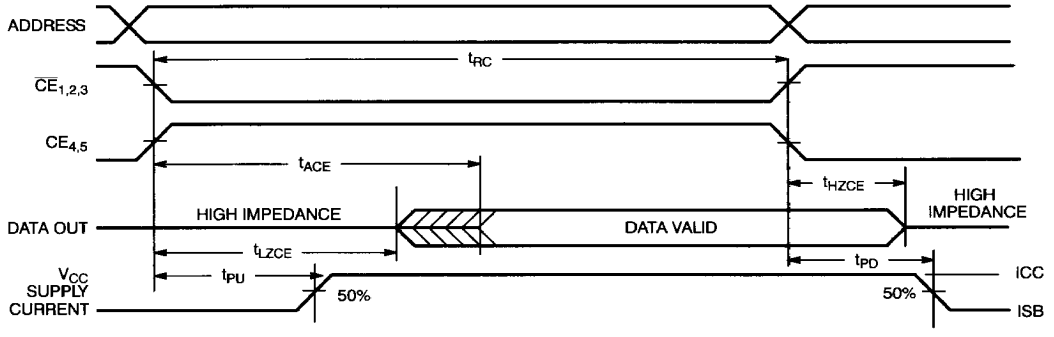
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH, and $\overline{WE}$ LOW. All signals must be asserted to initiate a write, and by being deasserted, any signal can terminate a write. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

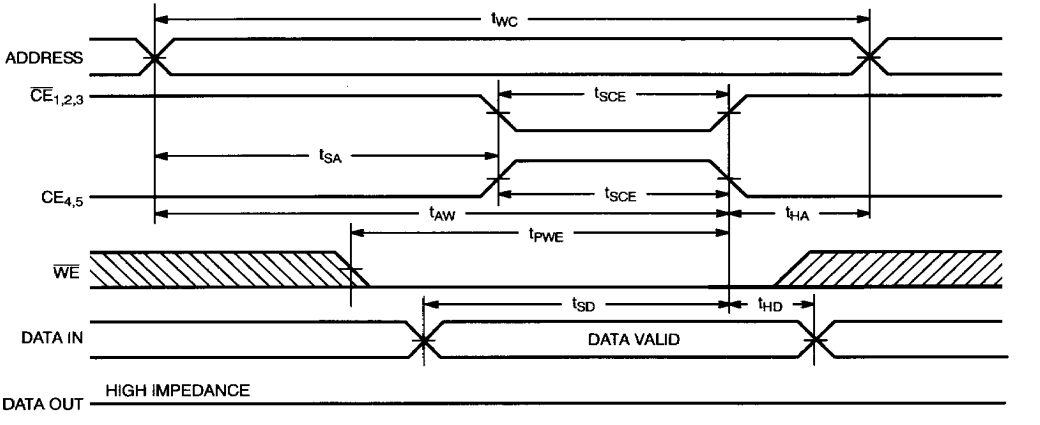
Read Cycle No. 1[10, 11]



Read Cycle No. 2[12]



Write Cycle No. 1 ($\overline{CE}$ Controlled)[13]

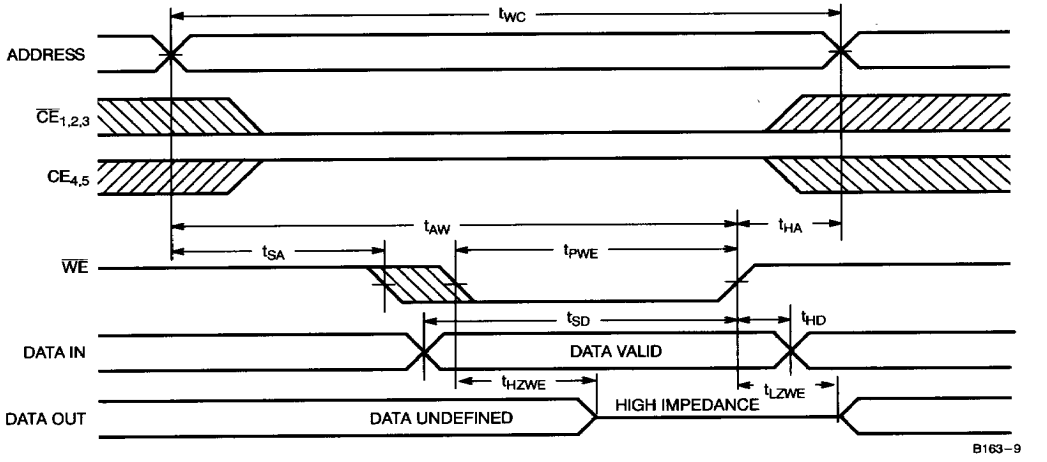


Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}_{1,2,3} \leq V_{IL}$ and $CE_{4,5} \geq V_{IH}$.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If any of $\overline{CE}_{1,2,3}$ goes HIGH or $CE_{4,5}$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled)[13]



Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	CE_4	CE_5	$\overline{WE}$	D_{OUT}	Mode	Power
L	L	L	H	H	H	Data Out	Read	Active (I_{CC})
L	L	L	H	H	L	High Z	Write	Active (I_{CC})
H	X	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	L	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	X	L	X	High Z	Power-Down	Standby (I_{SB})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B163–10DC	D22	Commercial
	CY7B163–10LC	TBD	
	CY7B163–10PC	P21	
	CY7B163–10VC	V21	
12	CY7B163–12DC	D22	Commercial
	CY7B163–12LC	TBD	
	CY7B163–12PC	P21	
	CY7B163–12VC	V21	
	CY7B163–12DMB	D22	Military
	CY7B163–12LMB	TBD	
15	CY7B163–15DC	P21	Commercial
	CY7B163–15LC	TBD	
	CY7B163–15PC	D22	
	CY7B163–15VC	V21	
	CY7B163–15DMB	D22	Military
	CY7B163–15LMB	TBD	
20	CY7B163–20DMB	D22	Military
	CY7B163–20LMB	TBD	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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