STEL-1175
Data Sheet

STEL-1175+125
(125 MHz)
32-Bit Resolution CMOS Phase Modulated Numerically Controlled Oscillator

FEATURES

- **VERY HIGH CLOCK FREQUENCY**
  - **125 MHz MAXIMUM OVER FULL MILITARY TEMPERATURE RANGE**
- **HIGH FREQUENCY RESOLUTION**
  - **32-BITS, 30 milli-Hz @ 125 MHz**
- **WIDE OUTPUT BANDWIDTH**
  - **0 TO 50 MHz @ 125 MHz CLOCK**
- **SHORT CLOCK TO OUTPUT DELAY FOR DIRECT CLOCK CONNECT TO 1175 AND DAC**
- **PRECISION PHASE MODULATION**
  - **12-BITS, 0.09° RESOLUTION, CAN BE USED FOR LINEAR PM OR PULSE-SHAPED PSK**
- **SINE OR COSINE SIGNAL GENERATION**
  - **12-BIT OUTPUTS**
- **HIGH SPECTRAL PURITY**
  ALL SPURS < -75 dBc
  (AT DIGITAL OUTPUT)
- **MICROPROCESSOR COMPATIBLE INPUTS**
- **LOW POWER DISSIPATION**
- **68 PIN PLCC PACKAGE**
  (COMMERCIAL TEMPERATURE RANGE)
- **68 PIN CERAMIC LCC PACKAGE**
  (MILITARY TEMPERATURE RANGE)

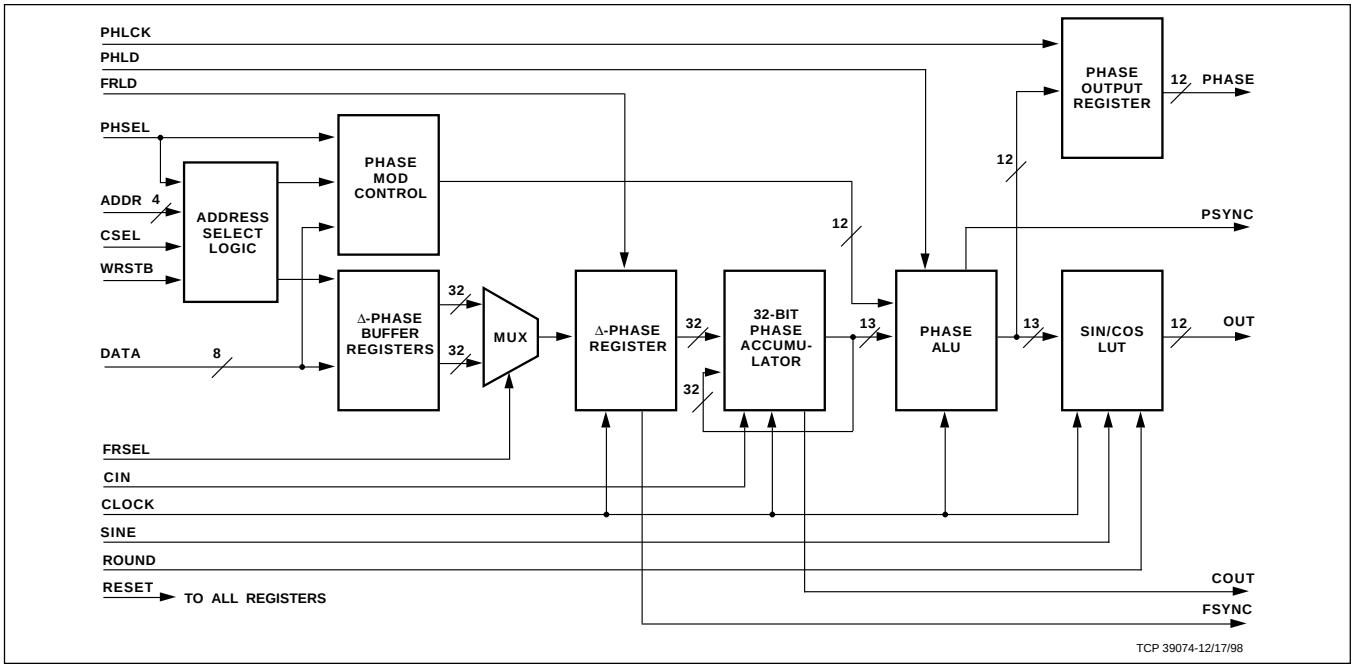
TYPICAL APPLICATIONS

- **FREQUENCY SYNTHESIZERS**
- **PSK MODULATORS**
- **DIGITAL SIGNAL PROCESSORS**
- **FAST HOPPED FREQUENCY SOURCES**

FUNCTIONAL DESCRIPTION

The STEL-1175 Modulated Numerically Controlled Oscillator (MNCO) uses digital techniques to provide a cost-effective solution for low noise signal sources. The device can operate at clock frequency up to 125 MHz and provides high frequency resolution and high spectral purity of outputs up to 50 MHz. The STEL-1175 also features phase modulation at rates up to 25% of the clock frequency. The 12-bit output can be selected to be a sine or cosine function, so that two STEL-1175 NCOs can be used to generate quadrature signals with independent phase modulation. Two independent frequency control registers are provided, allowing high speed frequency hopping or binary FSK at rates to 25% of the clock frequency. The device combines low power 0.5µ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoidal waveform generator able to achieve fine tuning resolution and high spectral purity at clock frequencies up to 125 MHz. The NCO is designed to provide a simple interface to an 8-bit microprocessor bus.

BLOCK DIAGRAM



The NCO maintains a record of phase which is accurate to 32 bits. At each clock cycle, the number stored in the 32-bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-Phase register represents the phase change for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

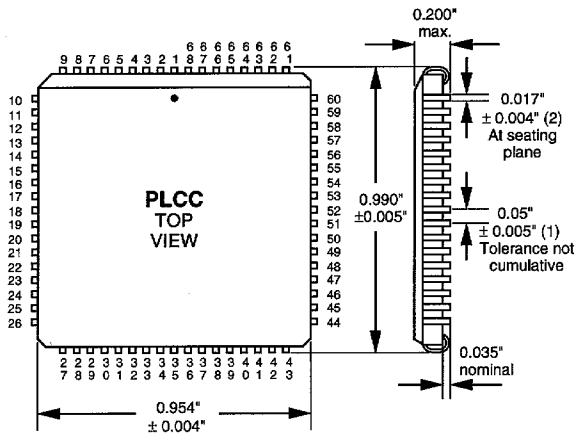
The sine and cosine functions are generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-Phase Register, which may be programmed by an 8-bit microprocessor.

The NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at frequencies greater than half the clock frequency and can be removed by filtering.

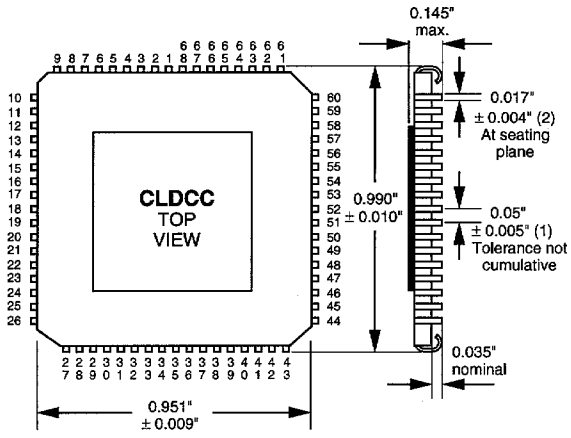
The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock

PIN CONFIGURATION

Package: 68 pin PLCC
Thermal coefficient, θ_{ja} = 35°/W



Package: 68 pin CLDCC
Thermal coefficient, θ_{ja} = 34°C/W



PIN CONNECTIONS

1	$PHASE_1$	15	$PHASE_7$	29	FRLD				
2	$PHASE_2$	16	$PHASE_8$	30	COUT	43	V_{DD}	56	FSYNC
3	$PHASE_3$	17	$PHASE_9$	31	CSEL	44	OUT_5	57	PSYNC
4	$PHASE_4$	18	$PHASE_{10}$	32	PHLD	45	OUT_6	58	$ADDR_0$
5	$PHASE_5$	19	$PHASE_{11}$	33	PHCLK	46	OUT_7	59	V_{SS}
6	$DATA_0$	20	WRSTB	34	V_{SS}	47	OUT_8	60	V_{DD}
7	$DATA_1$	21	PHSEL	35	V_{DD}	48	OUT_9	61	$ADDR_1$
8	$DATA_2$	22	I.C.	36	$OUT_{0(LSB)}$	49	OUT_{10}	62	$ADDR_2$
9	$DATA_3$	23	RESET	37	OUT_1	50	OUT_{11}	63	$ADDR_3$
10	$DATA_4$	24	ROUND	38	OUT_2	51	V_{SS}	64	CLOCK
11	$DATA_5$	25	SINE	39	OUT_3	52	V_{DD}	65	CIN
12	$DATA_6$	26	FRSEL	40	OUT_4	53	N.C.	66	V_{DD}
13	$DATA_7$	27	V_{DD}	41	N.C.	54	N.C.	67	V_{SS}
14	$PHASE_6$	28	V_{SS}	42	V_{SS}	55	N.C.	68	$PHASE_0$

Notes: 1. I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.
2. Connect all unused inputs to Vss, leave unused outputs unconnected.

frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 19 clock cycles. The dual Δ-Phase registers used in the STEL-1175 allow the frequency to be updated as rapidly as every fourth clock cycle, i.e. at 25% of the clock frequency. The pipeline delay associated with the phase modulator is only 12 clock cycles, since the phase modulating function is at the output of the accumulator. The phase modulation may also be changed as rapidly as every fourth clock cycle, at 25% of the clock frequency, resulting in a maximum modulation rate of 30 MHz with a clock frequency of 125 MHz. Note that when a phase or frequency change occurs at the output the change is instantaneous, i.e., it occurs in one clock cycle, with complete phase coherence.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the **$DATA_{7-0}$** inputs. The data is written into the device on the rising edge of the **WRSTB** input, and the register into which the data is written is selected by the **$ADDR_{3-0}$** inputs. The **CSEL** input can be used to selectively enable the writing of data from the bus.

PHASE MODULATION CONTROL BLOCK

This block includes the Phase Modulation Buffer Register and controls the source of the phase modulation (PM) data by means of the **PHSEL** input. When this signal is low, data from the **$DATA_{7-0}$** and **$ADDR_{3-0}$** inputs is written directly into the Phase ALU after a falling edge on the **PHLD** input. When **PHSEL** is high, data is written into the Phase Modulation Buffer Register from the **$DATA_{7-0}$** bus on the rising edge of the **WRSTB** input. The data will then be transferred into the Phase ALU after the next falling edge of **PHLD**. The source of the PM data applied to the Phase ALU will be the Phase Buffer Register in this mode.

Δ-PHASE BUFFER REGISTERS A & B BLOCK

The two Δ-Phase Buffer Registers are used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as four bytes per 32-bit Δ-Phase word. The data is transferred from these registers into the Δ-Phase Register after a falling edge on the **FRLD** input.

MUX BLOCK

This block is used to select which Δ-Phase Buffer Register is used as the source of frequency data for the Δ-Phase Register, by means of the **FRSEL** input.

Δ-PHASE REGISTER BLOCK

This block controls the updating of the Δ-Phase word used in the Accumulator. The frequency data from the Mux Block is loaded into this block after a falling edge on the **FRLD** input. This block also generates the **FSYNC** output, which indicates the instant at which any frequency change made at the inputs affects the **OUT_{11-0}** signals.

PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed, pipelined, 32-bit parallel accumulator, generating a new sum in every clock cycle. A carry input (the **CIN** input) allows the resolution of the accumulator to be expanded by means of an auxiliary NCO or phase accumulator. The overflow signal is discarded (and is available at the **COUT** pin), since the required output is the modulo(2^{32}) sum only. This represents the modulo(2þ) phase angle.

PHASE ALU BLOCK

The Phase ALU performs the addition of the PM data to the Phase Accumulator output. The PM data word is 12 bits wide, and this is added to the 13 most significant bits from the Phase Accumulator to form the modulated phase used to address the lookup table. This block also generates the **PSYNC** output, which indicates the instant at which any phase change made at the inputs affects the **OUT_{11-0}** signals.

SINE/COSINE LOOKUP TABLE BLOCK

This block is the sine/cosine memory. The 13 bits from the Phase ALU are used to address this memory to generate the 12-bit **OUT_{11-0}** outputs. The output will be a sine signal when the **SINE** input is high, and will be a cosine signal when this input is low.

PHASE OUTPUT REGISTER BLOCK

The twelve most significant bits from the Phase ALU Block are latched into the Phase Output Register on the rising edges of the **PHCLK** input. The output of this register is available on the **$PHASE_{11-0}$** pins.

INPUT SIGNALS

RESET

The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns high. The data on the **OUT_{11-0}** bus will then be invalid for 6 rising

clock edges, and thereafter will remain at the value corresponding to zero phase (801_H) until new frequency or phase modulation data is loaded with the **FRLD** or **PHLD** inputs after the **RESET** returns high.

CLOCK

All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 125 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 4 nanoseconds.

CSEL

The **C**hip **Sel**ect input is used to control the writing of data into the chip. It is active low. When this input is high all data writing via the $\mathbf{DATA_{7-0}}$ bus is inhibited.

$\mathbf{DATA_7}$ through $\mathbf{DATA_0}$

The 8-bit $\mathbf{DATA_{7-0}}$ bus is used to program the two 32-bit Δ-Phase Registers and the 12-bit Phase Modulation Register. $\mathbf{DATA_0}$ is the least significant bit of the bus. The data programmed into the Δ-Phase registers in this way determines the output frequency of the NCO.

$\mathbf{ADDR_3}$ through $\mathbf{ADDR_0}$

The four address lines $\mathbf{ADDR_{3-0}}$ control the use of the $\mathbf{DATA_{7-0}}$ bus for writing frequency data to the Δ-Phase Buffer Registers, and phase data to the Phase Buffer Register, as shown in the tables:

$\mathbf{ADDR_3}$	$\mathbf{ADDR_1}$	$\mathbf{ADDR_0}$	Register Field
0	0	0	Δ-Phase Bits 7 –0(LSB)
0	0	1	Δ-Phase Bits15 – 8
0	1	0	Δ-Phase Bits 23 – 16
0	1	1	Δ-Phase Bits 31 – 24
1	0	0	Phase Bits 3*– 0(LSB)
1	0	1	Phase Bits 11* – 4

$\mathbf{ADDR_3}$	$\mathbf{ADDR_2}$	Register Selected
0	0	Δ-Phase Buffer Register 'A'
0	1	Δ-Phase Buffer Register 'B'
1	X	Phase Buffer Register

* Note: The Phase Buffer Register is a 12-bit register. When the least significant byte of this register is selected ($\mathbf{ADDR_{3-0}}$ =1X00), $\mathbf{DATA_{7-4}}$ is written into Bits 3–0 of the register. In all cases, it is not necessary to reload unchanged bytes, and the byte loading sequence may be random.

WRSTB

The **Wr**ite **St**ro**b**e input is used to latch the data on the $\mathbf{DATA_{7-0}}$ bus into the device. On the rising edge of the **WRSTB** input, the information on the 8-bit data bus is transferred to the buffer register selected by the $\mathbf{ADDR_{3-0}}$bus.

FRSEL

The **F**requency **R**egister **Sel**ect line controls the mux which selects the Δ-Phase Buffer Register in use. When this signal is high Δ-Phase Buffer Register 'A' is selected as the source for the Δ-Phase Register, and the frequency corresponding to the data stored in this register will be generated by the NCO after the next **FRLD** command. When this line is low, Δ-Phase Buffer Register 'B' is selected as the source.

FRLD

The **Fr**equency **L**oa**d** input is used to control the transfer of the data from the Δ-Phase Buffer Registers to the Δ-Phase Register. The data at the output of the Mux Block must be valid during the clock cycle following the falling edge of **FRLD**. The data is then transferred during the subsequent cycle. The frequency of the NCO output will change 19 rising clock edges after the **FRLD** command due to pipelining delays.

PHSEL

The **Ph**ase Source **Sel**ect input selects the source of data for the Phase ALU. When it is high the source is the Phase Buffer Register. It is loaded from the $\mathbf{DATA_{7-0}}$ bus by setting address line $\mathbf{ADDR_3}$ high, as shown in the tables. When **PHSEL** is low, the sources for the phase modulation data are the $\mathbf{DATA_{7-0}}$ and $\mathbf{ADDR_{3-0}}$ inputs, and the data will be loaded independently of the states of **WRSTB** and **CSEL**. The data on these 12 inputs is presented directly as a parallel 12-bit word to the Phase ALU, allowing high-speed phase modulation. The 12-bit value is latched into the Phase ALU by means of the **PHLD** input. The data on the $\mathbf{ADDR_{3-0}}$ lines is mapped onto Phase Bits 3 to 0 and the data on the $\mathbf{DATA_{7-0}}$ lines are mapped onto Phase Bits 11 to 4 in this case. When using the parallel phase load mode **CSEL** and/or **WRSTB** should remain high to ensure that the phase data is not written into the phase and frequency buffer registers of the STEL-1175.

PHLD

The **Ph**ase **L**oa**d** input is used to control the latching of the Phase Modulation data into the Phase ALU. The 12-bit data at the output of the Phase Modulation Control Block must be valid during the clock cycle following the falling edge of **PHLD**. The data is then transferred during the subsequent cycle. The 12-bit phase data is added to the 12 most significant bits of the accumulator output, so that the MSB of the phase data represents a 180° phase change. The source of this data will be determined by the state of

PHSEL. The phase of the NCO output will change 12 rising clock edges after the **PHLD** command, due to pipeline delays.

CIN

The **C**arry **In**put is an arithmetic carry to the least significant bit of the Phase Accumulator. Normal operation of the NCO requires that **CIN** be set at a logic 0. When **CIN** is set at a logic 1 the effective value of the Ð-Phase register is increased by one. This allows the resolution of the accumulator to be expanded for higher frequency resolution by connecting the **COUT** pin of the lower order NCO to this input.

SINE

When the **SINE** input signal is set low the output signal appearing on the **OUT** pin will be a cosine function and when it is set high the DDS output will be a sine function. After a reset the device will always start at a phase angle of zero, irrespective of the status of the **SINE** input. In this way, by using two devices, one set in the sine mode and the other set in the cosine mode, quadrature outputs may be obtained. The quadrature phase relationship of the two outputs will be maintained at all times provided the two devices are operated from common **RESET**, **FRLD** and **CLOCK** signals. The use of phase modulation will, of course, modify this relationship, unless the devices are also phase modulated together.

ROUND

The **ROUND** input controls the precision of the $\mathbf{OUT_{11\text{-}0}}$ output. When the **ROUND** input is set high, the sine or cosine signals appearing on the $\mathbf{OUT_{11\text{-}0}}$ bus are accurate to 12 bits. In some instances it may be desirable to use only the 8 MSBs of this output. In such circumstances the signals appearing on the $\mathbf{OUT_{11\text{-}0}}$ bus can be rounded to present a more accurate 8-bit representation of the signal on $\mathbf{OUT_{11\text{-}4}}$ by setting the **ROUND** input low.

PHCLK

The register at the $\mathbf{PHASE_{11\text{-}0}}$ outputs allow the data appearing on these lines to be strobed and frozen on the rising edges of the **Ph**ase **Cl**oc**k** input. For continuous operation the **PHCLK** line and the **CLOCK** line should be tied together. When the $\mathbf{PHASE_{11\text{-}0}}$ outputs are not used **PHCLK** should be set low.

OUTPUT SIGNALS

$\mathbf{OUT_{11\text{-}0}}$

The signal appearing on the $\mathbf{OUT_{11\text{-}0}}$ output bus is derived from the 13 most significant bits of the Phase Accumulator. The 12-bit sine or cosine function is presented in offset binary format. When the phase modulation is zero and the **SINE** input is set high, the value of the output for a given phase value follows the relationship:

$\mathbf{OUT_{11\text{-}0}}$=2047 x sin (360 x (phase+0.5)/8192)°+2048

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 (801_H). However, when **ROUND** is set low, the value appearing on the $\mathbf{OUT_{11\text{-}0}}$ output will be rounded and will follow the relationship:

$\mathbf{OUT_{11\text{-}4}}$=127 x sin (360 x (phase+0.5)/8192)°+128

The data appearing on the $\mathbf{OUT_{3\text{-}0}}$ outputs will not be meaningful under these circumstances.

When the phase modulation is zero and the **SINE** input is set low, the value of the output for a given phase value follows the relationship:

$\mathbf{OUT_{11\text{-}0}}$=2047 x cos (360 x (phase+0.5)/8192)°+2048

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 4095 (FFF_H). However, when **ROUND** is set low, the value appearing on the $\mathbf{OUT_{11\text{-}0}}$ outputs will be rounded and will follow the relationship:

$\mathbf{OUT_{11\text{-}4}}$=127 x cos (360 x (phase+0.5)/8192)°+128

The data appearing on the $\mathbf{OUT_{3\text{-}0}}$ output will not be meaningful under these circumstances.

$\mathbf{PHASE_{11\text{-}0}}$

The 12 MSBs of the Phase ALU output are available on the $\mathbf{PHASE_{11\text{-}0}}$ lines. This signal is clocked on the rising edges of the **PHCLK** line.

COUT

Each time the value of the phase accumulator exceeds the maximum value that can be represented by a 32 bit number the **C**arry **Out** signal goes high for one clock cycle.

FSYNC

The **F**requency **Sync** output indicates the instant in time when a frequency change made at the inputs affects the $\mathbf{OUT_{11\text{-}0}}$ signals. The normally high **FSYNC** output goes low for one clock cycle 18 clock cycles after an **FRLD** command to indicate the end of the pipeline delay and the start of the new steady state condition.

PSYNC

The **P**hase **Sync** output indicates the instant in time when a phase change made at the inputs affects the $\mathbf{OUT_{11\text{-}0}}$ signals. The normally high **PSYNC** output goes low for one clock cycle 11 clock cycles after a **PHLD** command, to indicate the end of the pipeline delay and the start of the new steady state condition.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

***Warning:** Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.*

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125	°C (Plastic package)
		–65 to +150	°C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

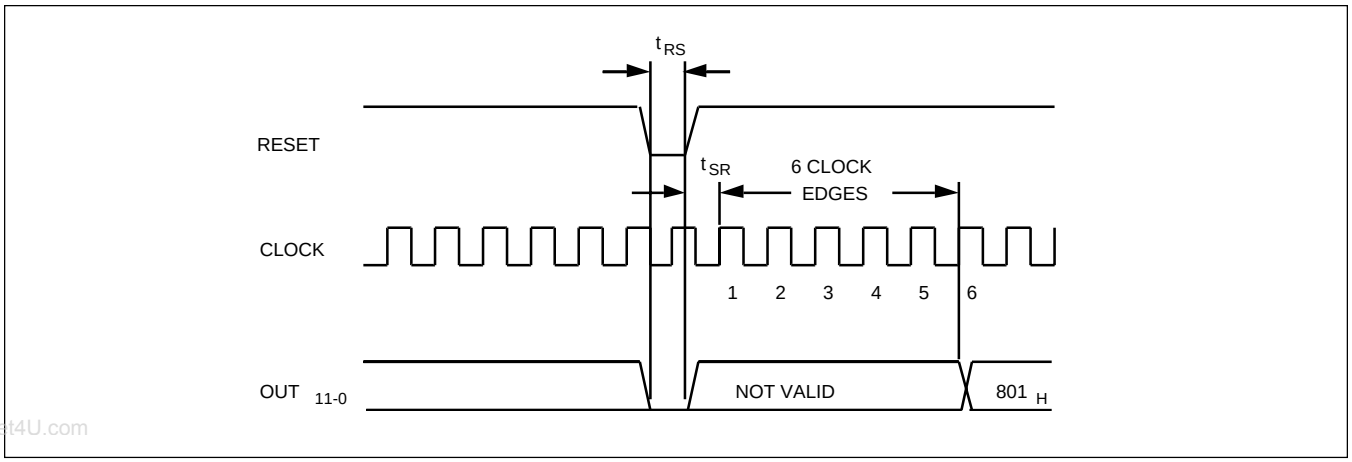
Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5%	Volts	(Commercial)
		+5 ± 10%	Volts	(Military)
T_a	Operating Temperature (Ambient)	0 to +70	°C	(Commercial)
		–55 to +125	°C	(Military)

D.C. CHARACTERISTICS

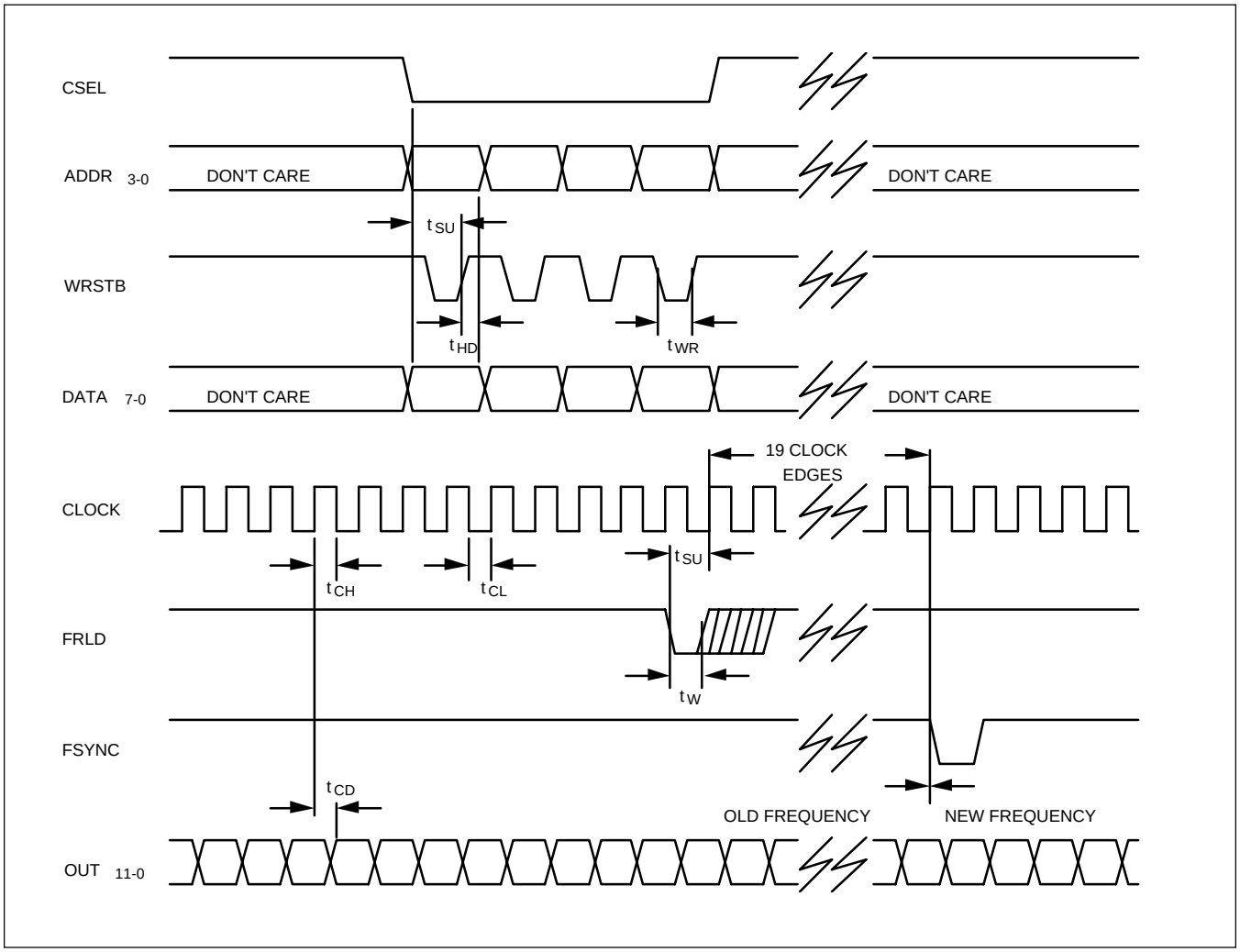
(Operating Conditions: V_{DD}= 5.0 V ±5%, VSS = 0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, VSS = 0 V, Ta = –55° to 125°C,Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**CIN** and **CSEL**, $V_{IN} = V_{DD}$
$I_{IH(min)}$	High Level Input Current			10	µA	All other inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			–10	µA	**CIN** and **CSEL**, $V_{IN} = V_{SS}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –8.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +8.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

NCO RESET SEQUENCE

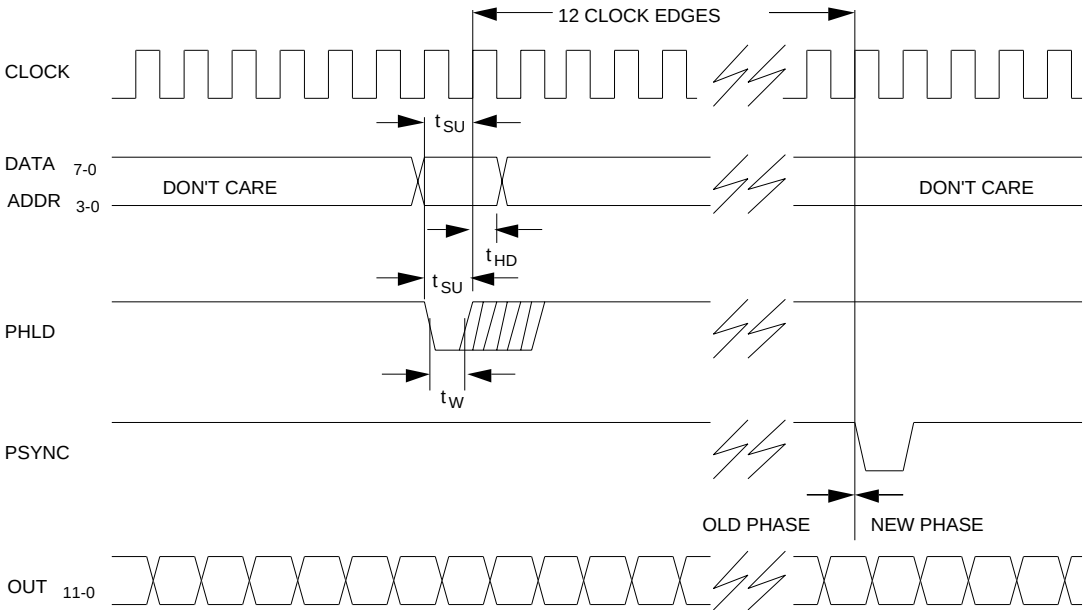


NCO FREQUENCY CHANGE SEQUENCE



NCO PHASE CHANGE SEQUENCE

1. PHSEL=0. DIRECT LOADING.



ELECTRICAL CHARACTERISTICS

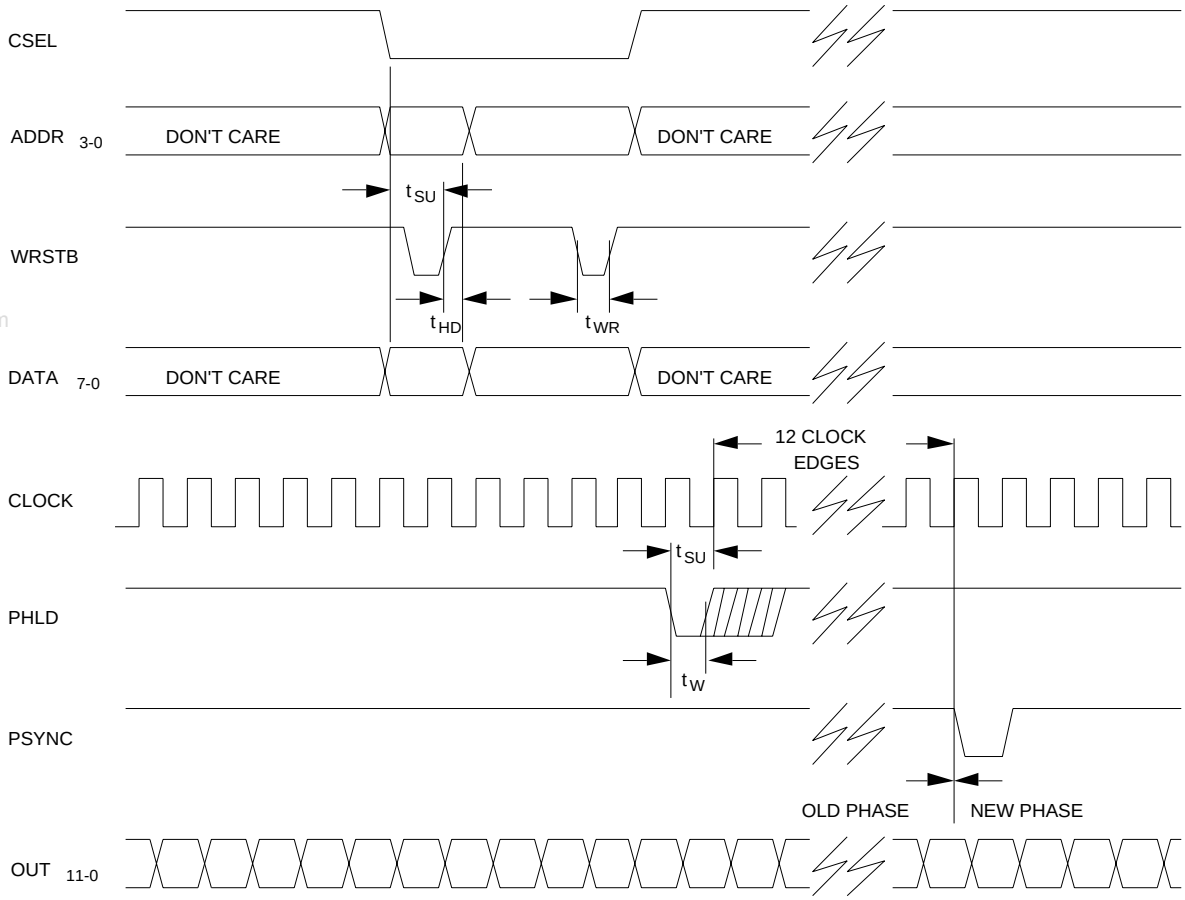
A.C. CHARACTERISTICS

(Operating Conditions: V_{DD}= 5.0 V ±5%, VSS = 0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, VSS = 0 V, Ta = –55° to 125° C, Military)

		STEL-1175+125					
		(Commercial)		(Military)			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Conditions
t_{RS}	**RESET** pulse width	10		25		nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	2		3		nsec.	
t_{SU}	**DATA**, **ADDR** or **CSEL** to **WRSTB** or **PHLD** Setup, and **FRLD** or **PHLD** to **CLOCK** Setup	3		3		nsec.	
t_{HD}	**DATA**, **ADDR** or **CSEL** to **WRSTB** or **PHLD** Hold, and **DATA** and **ADDR** to **CLOCK** Hold	3		3		nsec.	
t_{CH}	**CLOCK** high	3		4		nsec.	f_{CLK} = 125 MHz
t_{CL}	**CLOCK** low	3		4		nsec.	f_{CLK} = 125 MHz
t_W	**WRSTB**, **FRLD** or **PHLD** pulse width	3		5		nsec.	
t_{CD}	**CLOCK** to output delay	3	6	2	6	nsec.	Load = 15 pF

NCO PHASE CHANGE SEQUENCE

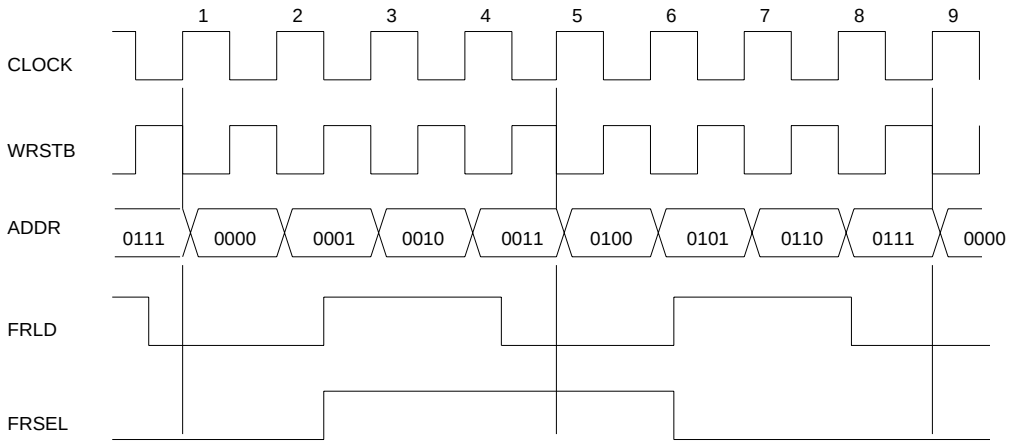
2. PHSEL=1. BUS LOADING.



HIGH-SPEED FREQUENCY CHANGE

The frequency of the STEL-1175 NCO can be changed as rapidly as 25% of the clock frequency. This is done by synchronizing the writing to the two Δ-Phase Buffer Registers, and updating both every eight clock cycles. The timing for this procedure is shown below. Each Δ-Phase Buffer Register is loaded while the contents of the other are being transferred into the Δ-Phase Register. The sequence for a load cycle begins on the rising edge of the clock following a falling edge of **FRLD**. In the diagram on page 11, Δ-Phase Buffer Register A is being loaded in cycles 1 through 4, while the contents of Δ-Phase Buffer Register B are being transferred, because **FRSEL** was low during the falling edge of **FRLD**. The reverse process happens during cycles 5 through 8, and the process then repeats starting in cycle 9. The **FRLD** signal can be used to clock a bistable latch to generate the **FRSEL** signal. The maximum update rate is 25%.

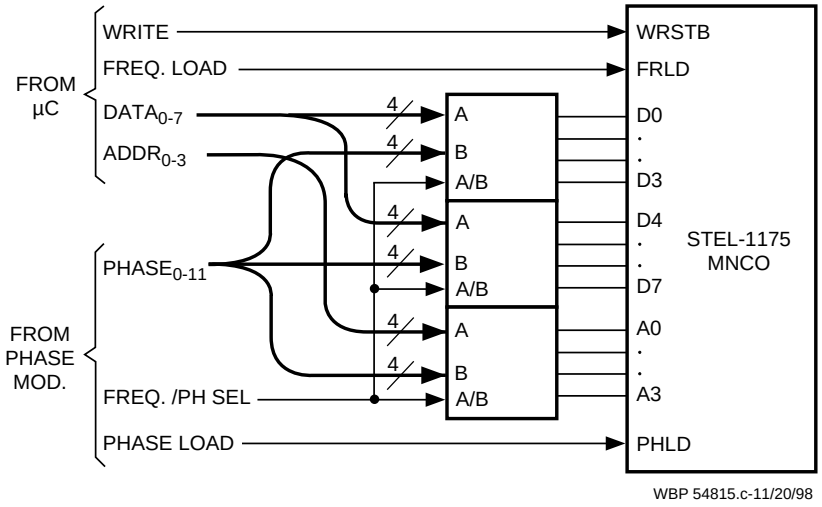
HIGH-SPEED FREQUENCY CHANGE



APPLICATIONS INFORMATION

USING THE STEL-1175 IN A HIGH-SPEED PHASE MODULATOR

By routing the data and address lines from the microcontroller via 2:1 multiplexers (e.g. 74HC157) the MNCO can be set up from the microcontroller and then phase modulated at high-speed from an external source. The **PHSEL** line should be set to a logic 0 to enable this mode of operation. The system shown modulates all 12 bits. In a typical PSK system only 1 to 4 bits of modulation will be used, simplifying the system considerably.



WBP 54815.c-11/20/98

SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

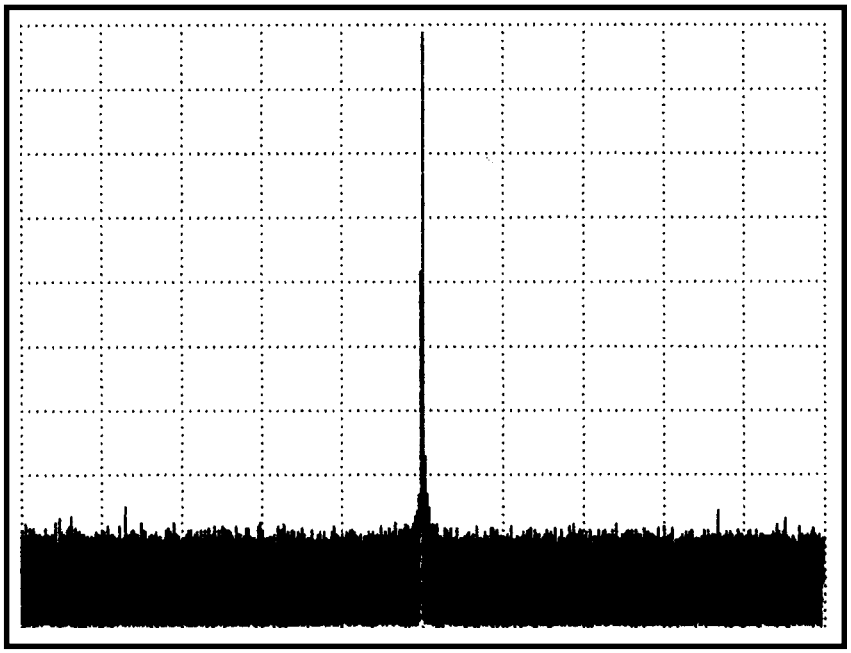
The sine or cosine signals generated by the STEL-1175 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically at least 75 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering.

As the output frequency f_o of the NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 60 MHz and the output frequency is programmed to 6.789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 10 or 20 MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –74 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	6.7 MHz
Frequency Span:	10.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	60 MHz

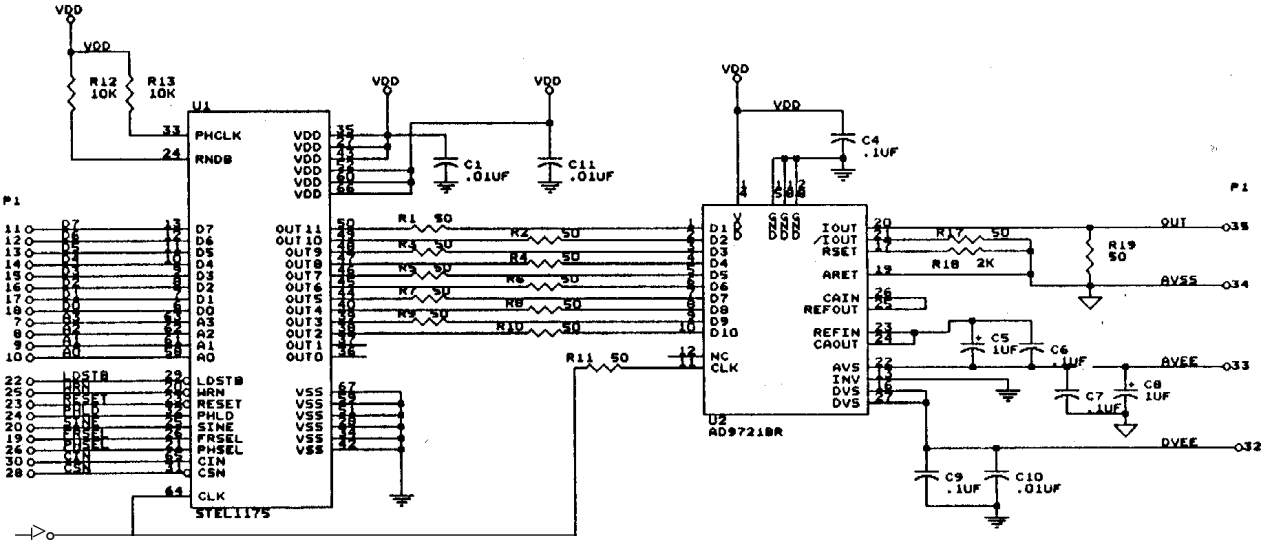


STEL-1175 TO DAC INTERFACE

Care must be taken in interfacing the STEL-1175 with the DAC. The clock to output delay in the STEL-1175 is typically 4 nS, but does change with processing variations, voltage, temperature, and loading. The circuit design must take this delay into account so that the input to the DAC is stable at the instant it is clocked into the DAC. The hold time of the DAC must be less than the minimum clock to output delay. The set-up time of the DAC must be less than the clock period minus the maximum clock to output delay.

For example, for 125 MHz, the set-up of the DAC must be less than 2 nS and the hold time less than 2 nS. For 80 MHz operation, the set-up time of the DAC must be less than 6.5 nS and the hold time less than 2 nS. This allows operation with most commercial DACs, such as the Harris HI5721.

TYPICAL SCHEMATIC DIAGRAM



For Further Information Call or Write

INTEL CORPORATION
Cable Network Operation
350 E. Plumeria Drive, San Jose, CA 95134
Customer Service Telephone: (408) 545-9700
Technical Support Telephone: (408) 545-9799
FAX: (408) 545-9888

WCP 970301A
015-140258