National Semiconductor

ADVANCE INFORMATION

TP3451 ISDN HDLC and GCI Controller

General Description

The TP3451 is a microprocessor peripheral communications device designed as both a full-duplex HDLC Framing and formatting controller, and a serial GCI (General Circuit Interface) frame controller. It is built on National's advanced M2CMOS process.

On the bus side of the device, full compatibility is provided for multiplexed and non-multiplexed microprocessor busses from National, Intel and Motorola, including DMA support. 64-byte FIFOs buffer the data in each direction of transmission. The HDLC functions include framing, address field control, and CRC processing for both LAPB and LAPD protocols. Also, in multi-protocol applications, the data paths may be switched to a transparent mode, bypassing the HDLC functions. 4 Status registers are also provided.

On the serial side of the device the data may be synchronously clocked in any of 4 distinct modes:

— Continuous unformatted data up to 4 Mb/s;

— Time-division multiplexed in a time-slot at 8, 16, 56 or 64 kb/s, with programmable time-slot assignment;

— GCI format in either of the 2 B channels or the D channel;

— The extended GCI-SCIT mode for ISDN Terminals.

In GCI mode, the TP3451 supports up to 8 GCI channels and also provides access to the GCI Monitor and Command/Indicate channels. The GCI-SCIT mode provides additional channels for control of local peripheral devices in TE applications.

Features

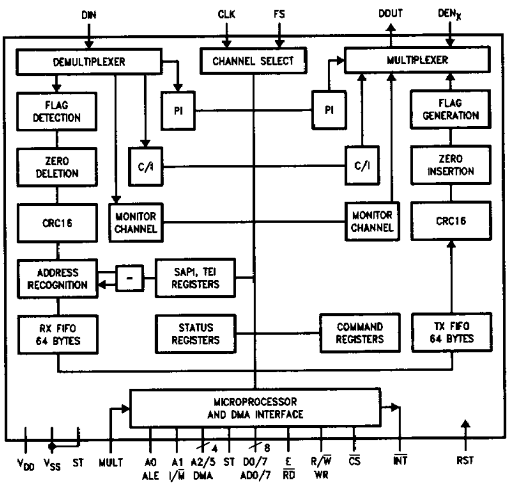
- LAPB and ISDN LAPD controller
- GCI and GCI-SCIT controller for M and C/I channels
- Full-duplex HDLC up to 4 Mb/s (non-GCI)
- Time-slot assigner for up to 64 TDM slots
- Formatter for 8, 16, 56 and 64 kb/s channels
- 4 SAPI and 3 TEI address filtering (LAPD)
- 64-byte FIFOs, with queueing for up to 8 receive frames and 2 transmit frames
- Protocol transparent mode (HDLC bypass)
- Compatible with National, Intel and Motorola μP busses
- DMA support with multiplexed bus
- Comprehensive status reporting
- 28-pin package

Applications

- X.25 terminals and controllers
- ISDN BRI/PRI D channel controller
- ISDN terminal adapters for X.25 and V.120
- ISDN Layer 2 controller for S/T and U BRI line-cards
- Easy interface to:

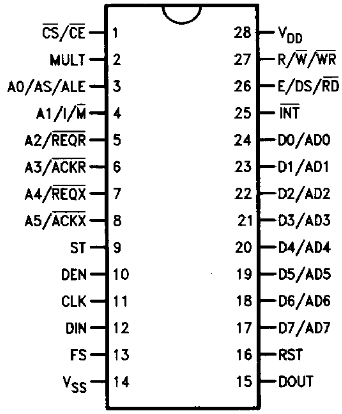
"S" interface device	TP3421
"U" interface device	TP3410
Codec/filter combos	TP3054/7 and TP3075/6
LAPD processor	HPC16400

Block Diagram



TL/H/10727-1

Connection Diagram



TL/H/10727-2

Order Number
TP3451J or TP3451N
NS Package Number J28A or N28B

Pin Descriptions

Name	Pin	Type	Function
V_{DD}	28	I	Positive Power Supply = 5V ± 5%.
V_{SS}	14	I	Signal Ground.
RST	16	I	Reset.
ST	9	I	Special Test (Reserved). Must be tied to V_{SS}.
$\overline{CS}$	1	I	Chip Select. A low level enables the device for read/write operations.
$\overline{INT}$	25	O	Interrupt request is asserted by the device when it requests service. Open drain active low output.
MULT	2	I	Multiplexed Bus. Indicates the μP bus interface selected. MULT = 1: multiplexed bus and DMA available. MULT = 0: address and data bus are separate.
I/$\overline{M}$	4	I	When MULT = 1, I/$\overline{M}$ = 1 selects Intel/National bus timing, and I/$\overline{M}$ = 0 selects Motorola 6803 bus timing.
DEMULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 0)			
A0/A5	3–8	I	Address Bus. Transfers addresses from μP to TP3451.
D0/D7	17–24	I/O	Data Bus. Transfers data between μP and TP3451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
E	26	I	Enable. Read/Write operations are synchronized with this signal; its falling edge marks the end of an operation.
MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 1)			
AD0/AD7	17–24	I/O	Address/Data Bus. Transfers addresses and data between μP and TP3451.
$\overline{WR}$	27	I	Write. A low on this input indicates a write operation.
$\overline{RD}$	26	I	Read. A low on this input indicates a read operation.
ALE	3	I	Falling edge latches the address from the external A/D bus.

Pin Descriptions (Continued)

Name	Pin	Type	Function
MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 0)			
AD0/AD7	17–24	I/O	Address/Data Bus. Transfers addresses and data between μP and TP3451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
DS	26	I	Data Strobe. Read/Write operations are synchronized with this signal: its falling edge marks the end of an operation.
AS	3	I	Address Strobe. Falling edge latches the address from the external A/D Bus.
DMA (Direct Memory Access): Only when MULT = 1			
$\overline{\text{DMA REQ X}}$ $\overline{\text{DMA REQ R}}$	7 5	O O	Direct Memory Access Requests: these outputs are asserted by the device to request an exchange of byte from the memory; in burst mode only, they are level sensitive.
$\overline{\text{DMA ACK X}}$ $\overline{\text{DMA ACK R}}$	8 6	I I	Direct Memory Access Acknowledge: these inputs are asserted by the DMA controller to signal to the HDLC controller that a byte is being transferred in response to a previous transfer request.
SERIAL PORT IN GCI MODES			
D_{OUT}	15	I/O	Data Output for B and D channels. In GCI mode it outputs B1, B2, M and C/I channels. In GCI-SCIT mode it also functions as D_{IN} for M' and C/I' channels (see Table II).
D_{IN}	12	I/O	Data Input for B and D channels. In GCI mode it inputs B1, B2 M and C/I channels. In GCI-SCIT mode (in TE applications) it also functions as D_{OUT} from M" and C/I" channels (see Table II).
CLK	11	I	Data Clock which determines the data shift rate for GCI channels on the serial interface, at 2 cycles per bit.
FS	13	I	Frame synchronization. This signal is a 8 kHz signal for frame synchronization. The front edge gives the time reference of the first bit in the frame.
DEN_X	10	I	Transmit Data Enable. In TE mode, this pin is a normally low input pulsing high to indicate the active bit times for D channel transmit at the D_{OUT} pin. It is gated with CLK and the internal time-slot strobes to control the shifting of data from the HDLC controller to an S interface device.
SERIAL PORT IN NON-GCI MODES			
D_{OUT}	15	O	Data Output for B and D channels, clocked by CLK input.
D_{IN}	12	I	Data Input for B and D channels, clocked by CLK.
CLK	11	I	Data Clock, which determines the data shift rate. Two modes: Single or double bit rate.
FS	13	I	Frame synchronization. Used in the time-division multiplexed mode, the rising edge gives the time reference of the first bit of the 8 kHz frame.
DEN_X	10	I	Transmit Data Enable. When high, enables the data at DOUT.

Functional Description

MICROPROCESSOR PORT

Any of 3 microprocessor bus interface standards may be selected by strapping the MULT and I/M pins. Multiplexed bus mode is selected by strapping MULT = 1; Intel/National bus compatibility can then be selected by I/M = 1, or Motorola bus compatibility is selected by strapping I/M = 0. The non-multiplexed Motorola bus mode is selected by strapping MULT = 0. Table I lists the registers which are accessed via the microprocessor port.

DATA FIFOs

The transmit and receive data paths between the microprocessor port and the HDLC section are buffered by means of independent 64-byte FIFOs. Each FIFO is accessible in blocks of up to 32 bytes, and demands service from the μP by generating interrupts. The data transferred through the FIFOs always consists of the address field, control field and information field of each HDLC packet (frame). In the receive direction a status byte is also appended at the end of the frame, containing indicators such as CRC pass/fail, frame abort and data overflow.

SERIAL PORT

This is a synchronous interface consisting of a single data shift clock input, CLK, transmit data output D_{OUT} and receive data input D_{IN}. CLK may run with either 1 or 2 cycles per data bit, selected via register CR2. Data passes between the Serial Port and the FIFOs either via the HDLC section or without HDLC processing (HDLC Bypass), selected via the MODE register. Data is transferred lsb first.

Two additional control input pins are provided. FS is a frame sync input which defines the start of the 8 kHz frame when any of the time-division multiplexed formats (including GCI) are used. DEN_X is an enable/disable control for transmit data at D_{OUT}, for use in ISDN Terminal applications when interfacing the device to the 16 kb/s D channel of an S/T Interface Transceiver (e.g., TP3420/1). The transceiver must exercise flow control for D channel access contention resolution at the S/T interface (for the Passive Bus). Transmit data shifting at D_{OUT} is inhibited when DEN_X is pulled low and enabled when DEN_X is pulled high.

Four different modes are available for data at the serial interface, with selection via register CR1. In the TDM and GCI modes, when the device is operating in a B channel (8-bit time-slot), the data may occupy the complete time-slot at 64 kb/s, or only a partial time-slot for data rates <64 kb/s. Options available are:

- 56 kb/s in the 7 msb's of the time-slot (lsb is not used);
- 16 kb/s, programmable into a 2-bit sub-slot in bits 1 and 2, 3 and 4, 5 and 6 or 7 and 8 of the time-slot;
- 8 kb/s using any 1 bit of the time-slot.

Selection is made in registers CR1 and TSR.

Continuous Mode

In this mode, there is no time-division multiplexing of data, and the FS input is not used. Data may be shifted at rates up to 4 Mb/s continuously in this mode (although the microprocessor routines to service the FIFOs may limit the net throughput to less than this). The DENx input must be pulled high to enable the D_{OUT} pin.

Time-Division Multiplexed (TDM) Mode

In this mode the FS input defines the start of an 8 kHz frame which may consist of up to 64 8-bit time-slots (with CLK shifting at up to 4.096 Mb/s). A programmable time-slot assignment circuit, programmed via the TSR register, allows the data to be programmed to shift only during one of these time-slots (same slot for transmit and receive).

GCI (General Circuit Interface) Mode

When the GCI format is used, the FS input is used for 8 kHz frame synchronization; the data shift clock at CLK must be selected to run at 2 cycles per data bit in register CR2. *Figure 3* shows the GCI frame format, which may have from 1 to 8 GCI channels multiplexed in the frame. The HDLC controller may use either of the B channels or the D channel in any of these GCI channels, selected in the TSR register. In addition, the device provides transmit and receive registers for access to the GCI Monitor channel and Command/Indicate channel. For applications which do not require HDLC, the device may function as a GCI formatter and controller for the Monitor and C/I channels by disabling the HDLC sections (see MODE register). For more details, see the section on GCI Registers.

GCI-SCIT (Special Circuit Interface for Terminals) Mode

The GCI-SCIT mode is an extension of the GCI mode for use in ISDN Terminals, with 3 GCI channels as shown in *Figures 3* and *4*. Channel 0 is used for 2B + D access to the Layer 1 interface and control of the transceiver, and channels 1 and 2 are added for local control of other devices. For more details, see the section on GCI Registers.

HDLC TRANSMITTER

A typical HDLC frame consists of the following data fields:

Flag	Address	Control	Information	CRC	Flag

The HDLC transmit section performs the following functions:

— Flag Generation

A flag (01111110) is generated to delimit the beginning and end of every frame; as an option, the closing flag of one frame may be shared with the opening flag of the next, selected via the MODE register.

— Zero Insertion

A zero is inserted after 5 consecutive ones within an HDLC frame (between flags) to prevent emulation of the flag;

— CRC Generation

The 2-byte CRC (Cyclic Redundancy Check) field transmitted in the frame is generated according to the polynominal $X^{16} + X^{12} + X^5 + 1$;

— Abort Sequence Generator

An HDLC frame may be terminated with an abort sequence under microprocessor control (see CMDR register).

— Interframe Fill

Flags or idle (consecutive ones) may be transmitted during the interframe time (see MODE register).

Functional Description (Continued)

HDLC RECEIVER

The HDLC receive section performs the following functions and reports status on received frames in the RFIFO register:

— Flag Detection

Opening and closing flags (01111110) are detected; shared opening and closing flags are acceptable.

— Zero Deletion

A zero following 5 consecutive ones within the frame is deleted;

— Address Field Recognition

An address filter, with either 1 or 2 bytes, may be selected to determine if a received HDLC frame is accepted or rejected based on the contents of the HDLC address field. Up to 4 SAPI values (0, 63 and 2 user programmable) and/or 3 TEI values (127 and 2 user programmable) may be selected (see registers ACA, ACB, ACC, ACD and ACE). The complete address field is also passed to the RFIFO for address filtering in the μP.

— CRC Checking

The CRC is recalculated on the received frame and compared with the received CRC according to the polynominal $X^{16} + X^{12} + X^5 + 1$;

— Checking for Idle

Fifteen or more consecutive ones are interpreted as "idle";

— Minimum Length Checking.

Register Descriptions

Registers in the TP3451 are accessed via the Microprocessor Port using the addresses shown in Table I. Tables II and III then show how Register CR1 configures the various channels at the Serial Port.

TABLE I. Register Address Map

Address Hex	Read Register Name	Write Register Name
CONFIGURATION REGISTERS		
2B	CR1 (Serial Port)	CR1 (Serial Port)
3E	CR2 (Serial Port)	CR2 (Serial Port)
25		TSR (Time-Slot Register)
HDLC CONTROL REGISTERS		
00	RFIFO	XFIFO
23	STAR (General Status)	CMDR (Command Register)
24	MODE	MODE (HDLC Modes)
25	RFBC (Receive Frame Byte Counter)	
26	ACA (Address Checking)	ACA (Address Checking)
27	ACB	ACB (SAPI x)
28	ACC	ACC (SAPI y)
29	ACD	ACD (TEI a)
2A	ACE	ACE (TEI b)
STATUS REGISTERS WHICH GENERATE INTERRUPTS		
20	ISTA0 (HDLC Status)	ISTA0
21	ISTA1 (GCI Status)	ISTA1
22	ISTA2 (GCI Status)	ISTA2
32	—	MASK0
33	—	MASK1
34	—	MASK2
GCI MONITOR AND C/I CHANNEL ACCESS REGISTERS		
2C	CIR1 (Rx C/I Channel)	CIX1 (Tx C/I Channel)
2D	CIR2 (Rx C/I' Channel)	CIX2 (Tx C/I' Prime Channel)
2E	MONR1 (Rx M Channel)	MONX1/0 (Tx M Channel)
2F	—	MONX1/1 (Tx M Channel Last Byte)
30	MONR2 (Rx M' Channel)	MONX2/0 (Tx M' Channel)
31	—	MONX2/1 (Tx M' Channel Last Byte)

Register Description (Continued)

TABLE II. Serial Port Channel Assignment

Serial Port Mode	CR1 Register								C/I		M		16 kb/s D Channel		64 kb/s (Note 1)		CI′		M′		CI″ (CMS)
	TE	MAS/SSC	CCs	CMS/SC	PI	VZ D_{OUT}	MDS1	MDS0	CIR1	CIX1	MONR1	MONX1	DR	DX	BR	BX	CIR2	CIX2	MONR2	MONX2	
Continuous	X	X	X	X	X	X	X	0	← HDLC Frame →												
Time-Division Multiplexed	X	See Table III			X	X	0	1					See Table III								
GCI (Not SCIT)	0	See Table III			X	0/1	1	1	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	See Table III								
GCI-SCIT	1	1	0	0	0	0/1	1	1	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}							
D Channel Data				1	0	0/1			D_{IN}	D_{OUT}^*	D_{IN}	D_{OUT}^*	D_{IN}	D_{OUT}^*							D_{OUT}^*
SCIT Master				0	1	0/1			D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}			D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	
				1	1	0/1			D_{IN}	D_{OUT}^*	D_{IN}	D_{OUT}^*	D_{IN}	D_{OUT}^*			D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}^*
GCI-SCIT	1	0	0	0	0	0/1	1	1	D_{IN}	D_{OUT}			D_{IN}	D_{OUT}							
D Channel Data				1	0	0/1			D_{IN}	D_{OUT}^*			D_{IN}	D_{OUT}^*							D_{OUT}^*
SCIT Slave				0	1	0/1			D_{IN}	D_{OUT}			D_{IN}	D_{OUT}			D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	
				1	1	0/1			D_{IN}	D_{OUT}^*			D_{IN}	D_{OUT}^*			D_{IN}	D_{OUT}	D_{IN}	D_{OUT}^*	
GCI-SCIT	1	X	1	0	0	0/1	1	1	D_{IN}	D_{OUT}					D_{IN}	D_{OUT}					
B Channel Data				0	1	0/1			D_{IN}	D_{OUT}					D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	
See also Table III																					

D_{OUT}^*: CMS = 1 and access procedure valid on D and C/I channels.

Note 1: See Table III for sub-multiplexing within a 64 kb/s time-slot.

Note 2: *Figures 4* and *5* identify the GCI and GCI-SCIT channels.

Register Descriptions (Continued)

TABLE III. 64 kb/s Time-Slot Submultiplexing

Serial Port Mode	Time-Slot Submultiplex	TSR Register Assignment	CR1 Register		
			MAS/SSC	CCS	CMS/SC
Time-Division Multiplexed	64 kb/s (Complete B Channel)	Select 1/64 Time-Slots	X	1	0
	16 kb/s (2-Bit Sub-Slot)	Select 1/256 Sub-Slots	X	0	0
	8 kb/s in msb of 16 kb/s Sub-Slot	Select 1/256 Sub-Slots	0	0	1
	8 kb/s in lsb of 16 kb/s Sub-Slot	Select 1/256 Sub-Slots	1	0	1
	8 kb/s in lsb of Time-Slot Only	Select 1/64 Time-Slots	0	1	1
	56 kb/ in 7 msb's of Time-Slot	Select 1/64 Time-Slots	1	1	1
GCI and GCI-SCIT	D Channel	Select GCI Channel	X	0	X
	64 kb/s (Complete B Channel)	Select GCI Channel and B1/B2	X	1	0
	8 kb/s in lsb of Time-Slot Only	Select GCI Channel and B1/B2	0	1	1
	56 kb/s in 7 msb/s of Time-Slot	Select GCI Channel and B1/B2	1	1	X

For all registers the MSB is on the left and LSB on the right.

CR1 Configuration Register 1

After Reset 00

This register configures the Serial Port. See Tables II and III.

TE	MAS	CCS	CMS/8	PI	VZ DOUT	MDS1	MDS0

TE TE Mode.

TE = 1: GCI-SCIT mode selected (must also set MDS0/1 = 1).

TE = 0: Not GCI-SCIT mode.

MAS/SSC In GCI-SCIT mode with D channel operation, this bit selects Master or Slave of the C/I' and M' channels. In other modes it selects sub-slots. See Tables II and III.

CCS Channel Capacity Selection

CCS = 1: 64 kb/s

CCS = 0: 16 kb/s

CMS/SC In GCI and GCI-SCIT D channel modes, this bit controls if access to the D and C/I channels is restricted to the Master only, or is accessible by Peripheral devices using local contention resolution. In other modes it selects sub-slots. See Tables II and III.

PI Peripheral Interface (if TE = 1 only)

PI = 1: CIX2, CIR2, MONX2 and MONR2 registers are enabled for GCI-SCIT mode.

PI = 0: CIX2, CIR2, MONX2 and MONR2 registers are disabled.

VZ DOUT DOUT forced to zero (to power-up the TP3421 SID or other GCI transceiver).

VZ DOUT = 1: If TIM = 0000 is stored in CIX1 register by the μP, and if CIR1 = DI = 1111 (level is inactive), DOUT is forced to zero when FS and CLK are not detected.

VZ DOUT = 0: If TIM = 0000 is stored in CIX1 and if CIR1 = DI, DOUT functions normally.

MDS1 Mode Bit 1

MDS1 = 1: GCI mode (M and C/I channels are valid).

MDS1 = 0: Time-division multiplexed mode

MDS0 Mode Bit 0

MDS0 = 1: TDM or GCI mode (FS input and time-slot multiplexers are active).

MDS0 = 0: Continuous mode (no TDM)

CR2 Configuration Register 2

After Reset 00

TLP	ADDR	AD3	AD2	AD1	AD0	CRS	TRI

TLP Test Loop

TLP = 1: The transmitter is internally connected to the receiver; the transmit output is not activated. The Serial Port must be activated to provide the bit clock and frame Synchronization.

TLP = 0: No test loop.

ADDR GCI Address Recognition in GCI-SCIT mode. If TE = 1 and PI = 1:

ADDR = 1: The first byte of the message received in MONR2 register is compared with AD0/3. If the bytes match, the message is accepted, otherwise it is ignored.

ADDR = 0: The message in MONR2 is always accepted.

AD0/3 Address 0/3

When PI = 1, these 4 bits are the GCI address of the device.

AD0/2 Address bit used by the access procedure to D and C/I channels (TE = CMS = CCS = 1)

CRS Clock Rate Selection

CRS = 1: Clock frequency is twice the data rate; (GCI).

CRS = 0: Clock frequency and data rate are identical.

TRI TRI-STATE®

TRI = 1: DOUT is a TRI-STATE output

TRI = 0: DOUT is open drain output

Register Descriptions (Continued)

TSR **Time Slot Register**

After Reset 00

See also Table III.

TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

In TDM Mode:
(MDS1 = 0 in CRI Register)

a) CCS = 1 in CRI Reg. (64 kbit/s)
Then: TSR2/7 select time-slot relative to FS input (from 0 to 63)

b) CCS = 0 in CRI Reg. (16 kbit/s)
Then: TSR0/7 select 2-bit sub-slot relative to FS input (from 0 to 255).

In GCI mode (MDS1 = 1 in CRI Register):

a) CCS = 1 in CRI Reg. (64 kbit/s)
Then: TSR2 selects B1 or B2:
TSR4/6 select GCI channel (from 0 to 7)

b) CCS = 0 in CRI Reg. (16 kbit/s)
Then: TSR4/6 select GCI channel (from 0 to 7) in D channel.

MODE **HDLC Mode Register**

After Reset 00

DMA	FL1	FL0	ITF	RAC	CAC	NHF	FLA

DMA — DMA Interface
DMA = 1: the DMA interface is active

FL1/0 — HDLC Frame Length
Minimum frame length accepted:

	FL1	FL0
3 bytes	0	0
4 bytes	0	1
5 bytes	1	0
6 bytes	1	1

ITF — Interframe Time Fill
ITF = 1: Flags are transmitted
ITF = 0: IDLE is transmitted

RAC — Receiver Active
RAC = 1: Receiver is enabled
RAC = 0: Receiver is disabled

CAC — Channel Activation
CAC = 1: Receiver and transmitter are active
CAC = 0: Receiver and transmitter are inactive

NHF — HDLC Function Select
NHF = 1: HDLC function disabled (Bypass mode)

FLA — Flag
FLA = 1: Shared flags are transmitted between HDLC frames
FLA = 0: Transmit two flags between HDLC frames

CMDR **Command Register**

After Reset 00H

XHF	XME	RMC	RMD	RHR	XRES	M2RES	M1RES

XHF — Transmit HDLC Frame
Must be set, after loading XFIFO, to start HDLC frame transmission.

XME — Transmit Message End
Must be set when the last byte of the frame is entered in XFIFO.

RMC — Receive Message Complete
Normally used in response to RPF or RME interrupt. Acknowledges that the received frame (or one pool of data) has been read and the corresponding RFIFO is freed.

RMD — Receive Message Delete
May be used in response to RPF or RME interrupt. The entire frame will be ignored by the receiver. The part of frame already stored is deleted.

RHR — Receive HDLC Reset
HDLC receiver is reset.

XRES — Transmit HDLC Reset
HDLC transmitter is reset; XFIFO is cleared and the transmitted frame (if any) is aborted.

M2RES — Monitor 2 Reset
Receive and transmit M' channel controllers are reset.

M1RES — Monitor 1 Reset
Receive and transmit M' channel controllers are reset.

FIFOs **RFIFO (Read), XFIFO (Write).**

The address of the currently accessible byte is always 00H. Data is transferred between the FIFOs and the Serial Port with LSB first. When the closing flag of a receive frame is detected, a status byte is added to the data in the RFIFO. This byte is read last and has the following format:

RBC	RDO	CRC	RAB	0	0	0	0

RBC — Receive Byte Count
The length of the received frame is not an integer number of bytes

RDO — Receive Data Overflow
A part of the frame has been lost because the receive FIFO was full

CRC — CRC Check
The received CRC bytes were correct

RAB — Receive Abort
The received frame was aborted

A status byte equal to A0H indicates a correctly received frame (for LAPD).

Register Descriptions (Continued)

ISTA0 **Interrupt Status Register 0**

After Reset 10H

The $\overline{INT}$ pin is activated only when any of the unmasked bits in this register is set = 1. The software should make a copy of this register, since it must be cleared by writing 00H before writing to any of the HDLC and/or GCI registers.

RME	RPF	RFO	XPR	XDU	EXI2	EXI1	0

RME Receive Message End
One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes is stored in the RFIFO.

RPF Receive Pool Full
32 bytes of a frame are in RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow
A complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready
One data block (32 bytes max) may be entered into the XFIFO.

XDU Transmit Data Underrun
A transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME command was issued. It is not possible to transmit a new frame when this interrupt remains unacknowledged.

EXI1 Extended Interrupt 1
This bit is set if any of the unmasked bits in register ISTA1 is set.

EXI2 Extended Interrupt 2
This bit is set if any of the unmasked bits in register ISTA2 is set.

ISTA1 **Interrupt Status Register 1 (GCI Mode only)**

After Reset 01H

0	0	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1

CIC1 Command/Indicate Change
A change in the contents of CIR1 is detected.

EOM1 End of Message 1 (Monitor Channel)
The last byte of an M channel messge has been received in register MONR1.

XAB1 Monitor Transmit ABORT
The received byte has not been validated in two successive GCI frames. The M channel receiver has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register
A validated new byte has been received in register MONR1.

RAB1 Receive Abort
The M channel transmitter received an ABORT from the remote receiver.

XMR1 Transmit Monitor Register 1 Ready
A byte can be stored in register MONX1.

ISTA2 **Interrupt Status Register 2 (GCI-SCIT Mode only)**

After Reset 01H

0	0	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

CIC2 Command/Indicate Change
A change in the contents of CIR2 is detected.

EOM2 End of Message 2 (M' channel)
The last byte of an M' channel message has been received in register MONR2.

XAB2 Monitor Transmit ABORT
The received byte has not been validated in two successive GCI frames. The M' channel receiver has sent an ABORT (A bit) to the remote transmitter.

RMR2 Receiver Monitor Register
A byte has been received in register MONR2.

RAB2 Receive ABORT
The M' channel transmitter received an ABORT from the remote receiver.

XMR2 Transmit Monitor Register 2 Ready
A byte can be stored in register MONX2.

MASK0 **Interrupt Mask Registers.**
MASK1 After Reset FFH.
MASK2 The three mask registers MASK0, MASK1, MASK2 are associated with the three interrupt registers ISTA0, ISTA1 and ISTA2 respectively.

Each interrupt source in the ISTA registers can be selectively masked by setting to "1" the corresponding bit in the appropriate MASK register. The current status of all interrupt sources, regardless of masking, is indicated when an ISTA register is read by the microprocessor. However, only unmasked sources can generate an interrupt by pulling $\overline{INT}$ low.

STAR **Status Register**

After Reset 40H

XDOV	XFW	IDLE	RLA	DC10	0	0	0

XDOV Transmit Data Overflow
More than 32 bytes are queued in the XFIFO.

XFW Transmit FIFO Write Enable
Data can be entered into the XFIFO.

IDLE IDLE State
15 or more consecutive ones have been detected at DIN.

RLA Receive Line Active
RLA = 1: Indicates an HDLC frame is being received on the line
RLA = 0: Receive channel is idle.

DCIO D and C/I Channels Occupied
DCIO = 1: D and C/I Channels are busy.

Register Descriptions (Continued)

RFBC **Receive Frame Byte Counter**

After Reset 00

See also Table IV.

RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC 0/7 Receive Data Count

Total number of bytes in the received HDLC frame (without CRC).

RDC 0/4 Indicate the number of bytes in the current block available in RFIFO (m).

RDC 5/7 Indicate the number of 32 byte blocks received (n). If the frame exceeds 223 bytes, RDC 5/7 hold the value "111", and only RCD 0/4 continue to count modulo 32.

The contents of the register are valid after an RME interrupt. The μP must read n + 1 bytes to transfer the received data plus the status byte into memory.

TABLE IV. Receive Frame Byte Counter Operation

Number of Bytes in the Frame Received (without CRC)	RFBC Register		Number of 32 Byte Blocks Previously Read by the μP
	765	43210	
N (Note 1)	n	m	n
1 Min	000	00001	0
2	000	00010	0
3	000	00011	0
30	000	11110	0
31	000	11111	0
32	001	00000	1
33	001	00001	1
62	001	11110	1
63	001	11111	1
64	010	00000	2
222	110	11110	6
223	110	11111	6
224	111	00000	7
256	111	00000	7
257	111	00001	7
	111	—	7

Note 1: For received frames up to 255 bytes in length, N = 32 n + m. Longer frames may be received but only m will be valid; n will stop counting at 111.

ACA **Address Check Register A**

After Reset 00

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA0	SAPI 0 is recognized if CA0 = 1
CA1	SAPI 63 is recognized if CA1 = 1
CA2	SAPI x is recognized if CA2 = 1
CA3	SAPI y is recognized if CA3 = 1
CA4	TEI 127 is recognized if CA4 = 1
CA5	TEI a is recognized if CA5 = 1
CA6	TEI b is recognized if CA6 = 1
CA7	Address Filter Active if CA7 = 1

If CA0-3 all = 0, all received SAPI values are accepted; if any one or more of these bits = 1, only receive addresses matching the stored SAPI(s) are accepted. If CA4-6 all = 0, all received TEI values are accepted; if any one or more of these bits = 1, only receive addresses matching the stored TEI(s) are accepted. To disable all address filtering set CA7 = 0; registers ACB, ACC, ACD and ACE are then inactive and all received address fields are accepted.

ACB **Address Check Register B**

After Reset 00

The contents of ACB indicate the SAPI x value

SAPI	0	0

6 High Order Bits

ACC **Address Check Register C**

After Reset 00

The contents of ACC indicate the SAPI y value

SAPI	0	0

6 High Order Bits

ACD **Address Check Register D**

After Reset 00

The contents of ACD indicate the TEI a value

TEI	0

7 High Order Bits

ACE **Address Check Register E**

After Reset 00

The contents of ACE indicate the TEI b value

TEI	0

7 High Order Bits

CIX1 **Command/Indicate Transmit Register 1**

After Reset FFH

(GCI Selected Only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4 Code to be transmitted in the outgoing GCI C/I channel. C1 bit is transmitted first.

CIR1 Command/Indicate Receive Register 1

After Reset FFH

(GCI Selected Only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4 Data from the incoming GCI C/I channel. After CIC1 interrupt in ISTA1, the μP must read this register.

CIX2 **Command/Indicate Transmit Register 2**

After Reset FFH

1	1	P1	P2	P3	P4	P5	P6

P1/P6 Code transmitted in the 2nd GCI channel. P1 bit is transmitted first.

Register Descriptions (Continued)

CIR2 **Command/Indicate Receive Register 2**

After Reset 3FH

(GCI-SCIT in TE mode only)

0	0	P1	P2	P3	P4	P5	P6

P1/P6 The contents of the 2nd C/I channel, which are the different requests received from peripherals to local μP. Up to six peripherals can make simultaneous requests. After CIC2 interrupt in ISTA2, the μP must read this register.

MONX1/0 and MONX1/1 **Monitor Transmit Registers**

(GCI Selected Only)

After Reset FFH

M1	M2	M3	M4	M5	M6	M7	M8

After Reset FF.

The data written in MONX1/0 is transmitted in the outgoing GCI Monitor channel according to the GCI transfer protocol. M1 bit is transmitted first. The last byte of the message (or a single-byte message) must be written to register MONX1/1 to complete the M channel handshake. XMR1 interrupt indicates when these registers are ready for the next byte.

MONR1 **Monitor Receive Register 1**

(GCI Selected Only)

After Reset FFH

M1	M2	M3	M4	M5	M6	M7	M8

The data read from MONR1 is the byte received in the Monitor channel according to the GCI transfer protocol. RMR1 interrupt in ISTA1 indicates when a new byte is available in this register.

MONX2/0 and MONX2/1 **Monitor Transmit Registers**

(GCI-SCIT in TE Mode Only)

After Reset FFH

The data written in MONX2/0 is transmitted in the 2nd GCI M′ channel to a peripheral (if PI = MAX = 1 in register CR1). The last byte of the message (or a single-byte message) must be written to register MONX2/1 to complete the M′ channel handshake. XMR2 interrupt indicates when these registers are ready for the next byte.

MONR2 **Monitor Receive Registers**

(GCI-SCIT in TE Mode Only)

After Reset FFH

The data read from MONR2 is the byte received from the M′ channel in the 2nd GCI channel. RMR2 interrupt in ISTA2 indicates when a new byte is available in this register.

Transmit FIFO Operation

In the transmit direction (towards the HDLC transmitter) the μP may load a block of up to 32 bytes into XFIFO either after first polling the XFW bit in the STAR register, or after an XPR interrupt in ISTA0. To start transmission of a frame the XHF command must be written to the CMDR register. The TP3451 will request another data block by an XPR interrupt if the XFIFO contains less than 32 bytes (unless the XME bit has been set); thus, up to 64 bytes may be stored at any one time.

When the last block of the HDLC frame is loaded into XFIFO, the μP must set the XME bit. After transmission of all remaining XFIFO bytes, the CRC field and closing flag are then added, and the HDLC controller generates a final XPR interrupt.

The XFIFO is implemented as two buffers, each consisting of 32 byte FIFOs. The μP has access to one buffer at a time and passes control to the HDLC hardware by setting the XHF or XME bits in the CMDR register. The HDLC TX hardware empties the buffers and informs the availability of the buffers to the μP via the XPR bit in ISTA0.

The XDOV bit in the STAR register will be set if more than 32 bytes are written into one buffer. The bit will not generate an interrupt but it can be polled by software. If the XFIFO becomes empty while the XME bit has not been set, an abort sequence is generated, followed by interframe fill, and the XDU interrupt is generated. A frame may also be aborted by the XRES command.

Figure 1 shows a typical bus handshake during a transmit HDLC frame.

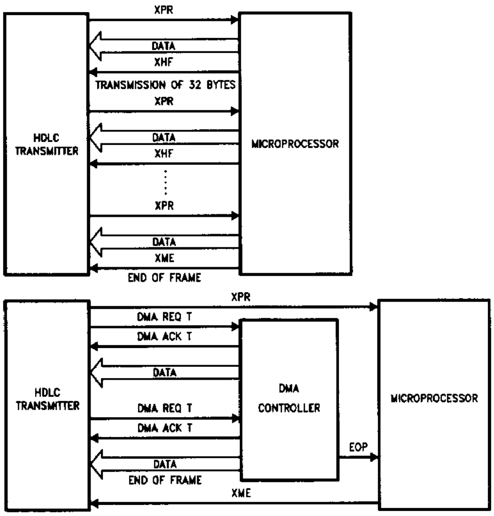


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FIGURE 1. Bus Handshake during Transmit HDLC Frame

2

Receive FIFO Operation

In the receive direction, data at the D_{IN} input may be accepted unconditionally, or may be filtered for HDLC address matching if selected in registers ACA, ACB, ACC, ACD and/or ACE. Each received frame which matches one of the enabled addresses, and satisifies the selected minimum length in the MODE register, is sent to the RFIFO with all bytes between the opening flag and the CRC field.

The RFIFO is implemented using eight separate buffers each consisting of eight byte FIFOs. The FIFO buffers are cascaded (or linked in a chain) automatically as required by the length of an incoming packet to form a FIFO up to 64 bytes deep.

Associated with each buffer is a set of registers containing information such as buffer status (full/empty), packet frame status (the packet status byte which can be read after the end of the packet data bytes) and the RFBC (which keeps count of the packet length).

An empty buffer is allocated to an incoming packet, and additional empty buffers (maximum 7) are automatically linked to it as required. After four buffers are full, the RPF Receive Pool Full (a Pool consists of four buffers containing 32 bytes) interrupt is asserted to request service. The detection of a closing flag will freeze the buffer and the associated status registers while asserting the RME interrupt via ISTA0. A short message of 8 bytes or less (including CRC) can be contained in each of the 8 buffers and the complete packet status information can be stored in the 8 sets of associated status registers. Eight RME interrupts may also be queued in this stack.

As data is received, the RFBC keeps track of the number of received bytes even if the packet occupies multiple buffers. RFBC bits 0 to 4 indicate the number of data bytes, m, stored in the current block. At each RFIFO read access by the μP, m is decremented, reaching 0 when the complete block is read. RFBC bits 5 to 7 indicate the total number of 32 byte blocks already received, n. Bits 5 to 7 remain unchanged at each read access. Also, they do not overflow; when a count of n = 7 is reached, a frame length greater than 223 bytes is indicated (see Table IV).

In response to an RME interrupt, the μP must read the RFBC and then read m + 1 bytes from the RFIFO. The μP then releases the buffer(s) by setting the RMC bit in the CMDR register. For a RPF interrupt, the μP must read 32 bytes and then release the four FIFO buffers by setting the RMC bit in the CMDR register. If more than 32 read accesses are performed after an RPF interrupt, the last data byte will be repeated. If more than m + 1 read accesses are performed after an RME interrupt, the packet status byte will be repeated.

The μP can ignore received frame by writing the RMD command to the CMDR register in response to an RPF or RME interrupt. The part of the frame already stored is deleted and the remainder of the frame is ignored. To check if the receive HDLC channel is idle, the IDLE bit in the STAR register can be polled.

Figure 2 shows a typical bus handshake while receiving an HDLC frame.

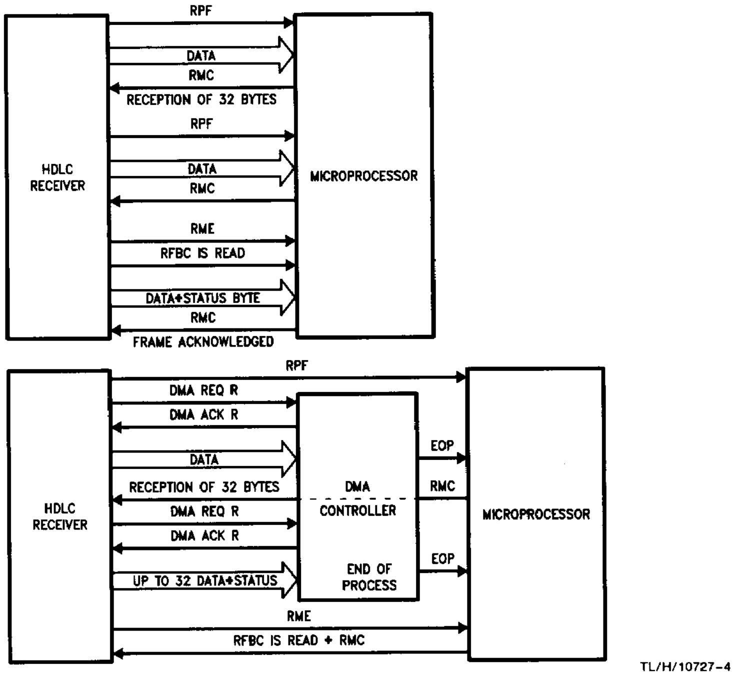

FIGURE 2. Bus Handshake during Receive HDLC Frame

FIFO Access Using DMA

The TP3451 has a DMA interface which can be enabled by the DMA bit in the MODE register. The DMA interface is available only when multiplexed bus is selected. When DMA is enabled, the TP3451 asserts $\overline{\text{DMA REQR}}$ or $\overline{\text{DMA REQX}}$ to request an exchange of bytes between the FIFOs and the external memory.

The external DMA controller asserts $\overline{\text{DMA ACKR}}$ or $\overline{\text{DMA ACKX}}$ to access the FIFOs.

These signals are equivalent to the E/DS/RD functions. During DMA access, the $\overline{\text{CS}}$ pin must be inactive (high); AS and E/DS/RD signals can be present. Outside DMA Access, all registers are accessible by the μP except the FIFOs.

FRAME TRANSMISSION

When a 32 byte block is free in XFIFO, $\overline{\text{DMA REQX}}$ goes low and XPR interrupts the μP. The DMA controller can write data in the XFIFO. At the end of the frame, the μP sends XME to the HDLC controller; CRC and closing flag will be sent by the HDLC controller.

FRAME RECEPTION

When one block has been stored in RFIFO, the $\overline{\text{DMA REQR}}$ pin goes low and RPF (or RME) interrupts the μP. The DMA controller reads the RFIFO. After the RME interrupt, the frame length will be available in RFBC register. The block is acknowledged by an RMC command.

GCI Registers

GCI COMMAND/INDICATE PROCEDURE

The two circuits communicating on the GCI interface (e.g., TP3451 and TP3421 SID) send each other a continuous four bit command code in the C/I field.

Receive C/I

The TP3451 stores in every frame the four bits of C/I channel coming from register CIR. This value is compared with the previous one. If a new value appears during two consecutive frames, this new value is loaded in register CIR1 and a CIC1 interrupt is generated.

Transmit C/I

The transmit register CIX1 can be written at any time by the μP. Its content is continuously sent in the C/I channel.

Note: The TIM command (0000) forces a low level on DOUT, if CIR1 = DI (1111) when VZ DOUT = 1, to request FS and CLK.

GCI MONITOR CHANNEL

THE GCI Monitor channel procedure allows bi-directional transmission of control messages in each direction, with acknowledgement using the A bit.

Receive Monitor Channel

An interrupt (bit RMR1 in ISTA1 register) is generated when a new byte is available in register MONR1.

The TP3451 generates an interrupt bit (XAB1 in ISTA1) if it does not receive twice the same byte; it also sends an ABORT to the remote transmitter. An interrupt is also generated (EOM in ISTA1) when it has received an End Of Message indicator via the E bit. Acknowledgement to the remote transmitter is sent if:

- the byte was received twice with the same value:
- the microprocessor reads the previous byte stored in register MONR1.

Transmit Monitor Channel

The TP3451 generates an interrupt (XMR1 in ISTA1) when the MONX1 registers are ready for a message byte. ISTA1 and ISTA0 must be cleared before writing to the MONX1 registers.

A Monitor Channel message must be loaded into register MONX1/0 one byte at a time. When the last message byte is written in register MONX1/1, the device sends the End Of Message indicator (via the E bit) to the remote receiver. If an Abort is received, one interrupt (RAB1) is generated.

GCI-SCIT OPERATION IN M′ AND C/I′ CHANNELS

A procedure is provided which allows bi-directional message transmission between the microprocessor and peripheral devices connected on C/I′ and M′ channels through GCI-SCIT channel 1.

Receive Interrupt on C/I′ (DOUT is an input).

A new value on C/I′ indicates to the TP3451 that one peripheral device in the terminal wants to send a message. Up to six peripherals may generate such an interrupt to the microprocessor.

Each GCI frame, the six bits of the C/I′ channel coming from peripherals are loaded in register CIR′. This value is compared with the previous one and, if a new value appears during two consecutive frames, it is loaded in register CIR2, and a CIC2 interrupt (ISTA2 register) is generated.

The μP may send a message on the M′ channel (DIN becomes an output) to allow the peripheral device to transmit.

Message Transmission on M′ Channel

The TP3451 sets interrupt XMR2 (ISTA2 register) if the MONX2 registers are available. ISTA2 and ISTA0 must be cleared before writing to the MONX2 registers. Writing MONX2 generates a message transmission. When the last byte is stored in register MONX2/1, the device sends the End Of Message indicator (via the E bit) to the remote peripheral.

If an ABORT is received, interrupt RAB2 (ISTA2 register) is generated; the microprocessor must repeat the message.

Message Reception on M′ Channel

Interrupt bit RMR2 (ISTA2 register) is generated when a new byte is available in MONR2 register. Interrupt bit XAB2 (ISTA2 register) is set if it does not read the same byte twice; in this case, it sends an ABORT to the remote peripheral.

The controller generates interrupt bit EOM2 (ISTA2 register) when the End Of Message indicator is received.

GCI Registers (Continued)

ACCESS PROCEDURE TO D AND C/I CHANNELS

Up to eight HDLC controllers may be connected to the D channel and C/I channel in GCI Channel 0. A contention resolution mechanism is provided by CMS (Contention Mode Selection) in GCI Channel 2, see *Figures 3* and *4*. This mechanism allows granting an access without losing data.

An access request may be generated if CIX1 (Command/Indicate Register 1) contains any code except DI (1111). During the procedure the M channel (with A and E bits) may be used. On input DIN, the GCI controller checks the CMS4 bit, which indicates the status of C/I and D channels.

CMS4 = 1 indicates channels free;
CMS4 = 0 indicates channels busy.

If the channels are free, the HDLC controller starts transmitting its individual address, AD2 on CMS1, AD1 on CMS2, AD0 on CMS3. If an erroneous address is detected, the procedure is terminated immediately. If the complete address can be read without error, the D and C/I channels are occupied and the TP3451 transmits CMS4 = 0. The HDLC controller which has the lowest address has priority over the others.

The access request is withdrawn if the HDLC controller transmits code DI = 1111, and the CMS4 bit is set = 1.

Figure 5 shows flow charts of these procedures.

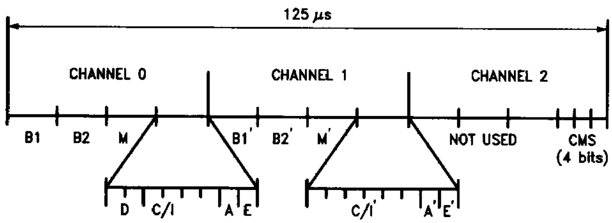

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FIGURE 3. GCI-SCIT Frame Format

GCI Registers (Continued)

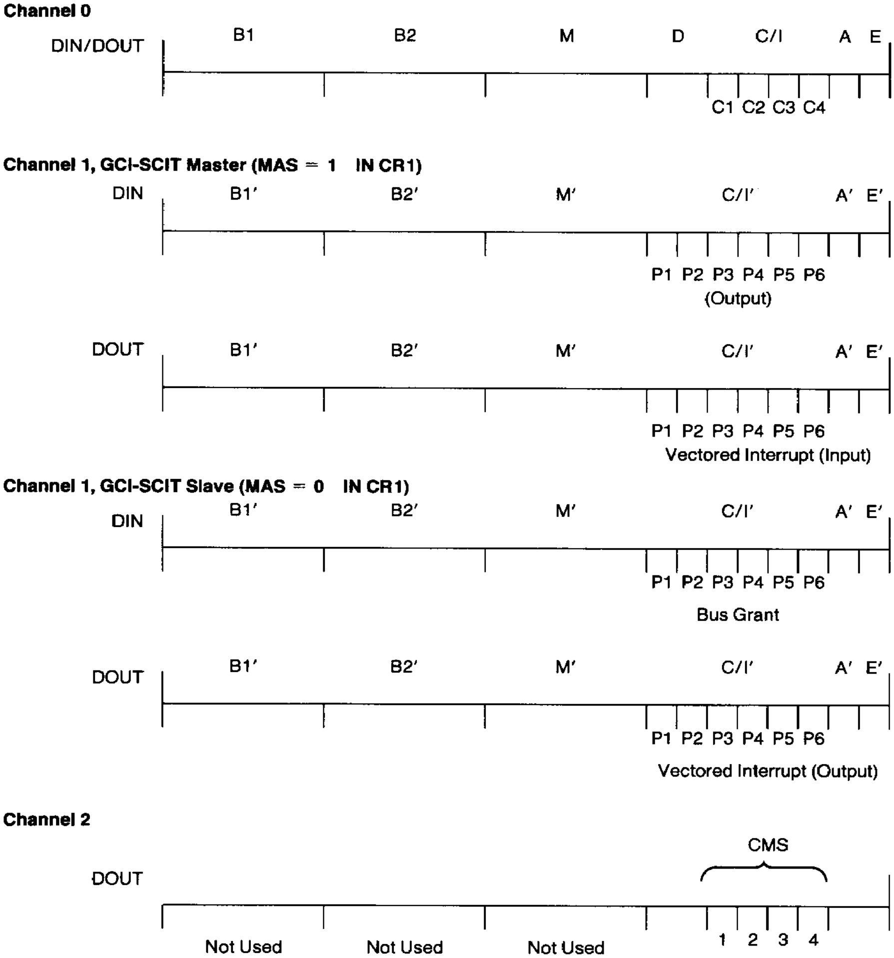


FIGURE 4. GCI-SCIT Channel Format

GCI Registers (Continued)

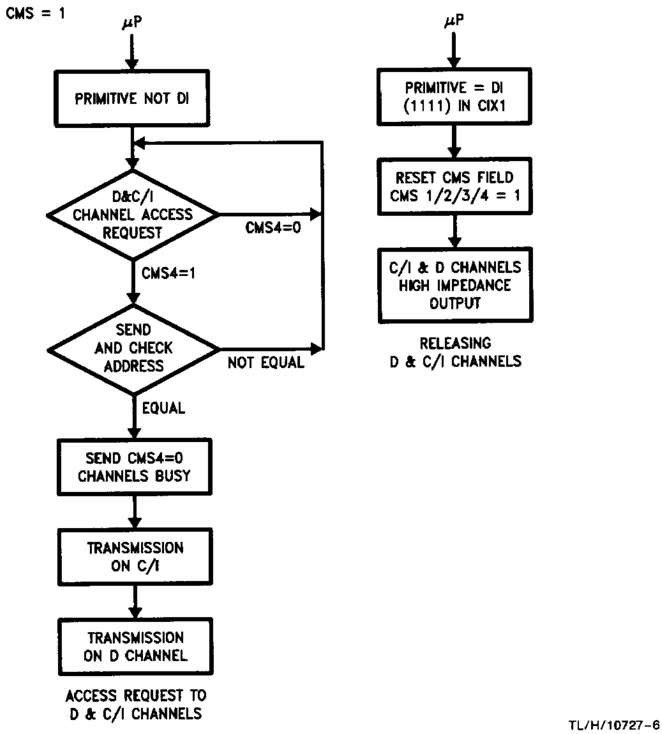


FIGURE 5. D and C/I Channels Access Procedure in GCI-SCIT Mode

Applications Information

The TP3451 HDLC controller may be used in a variety of applications, including ISDN TE's and TA's, NT-2's and LT's, both for Basic Rate and Primary Rate.

Figures 6 through *8* illustrate typical TE applications. *Figure 6* shows the TP3451 as the Basic Rate D channel LAPD controller, which may be handling all the traffic for multiple SAPIs (Service Access Point Indicator). The transceiver may be the TP3421 SID or TP3410 UID, in which case GCI mode would be used for the serial interface, or a non-GCI transceiver such as the TP3420 can be used with the programmable TSA on the HDLC controller.

Figure 7 shows a more modular arrangement which takes advantage of the GCI-SCIT mode. One TP3451 handles only the Layer 2 management and signaling logical links (SAPIs 0 and 63), while another module may be added as an option to handle packet data (SAPI 16). The GCI-SCIT mode provides the contention resolution for the 2 (or more) HDLC controllers to access the D channel in GCI channel 0, with one of the devices always assured of using the D channel without loss of data.

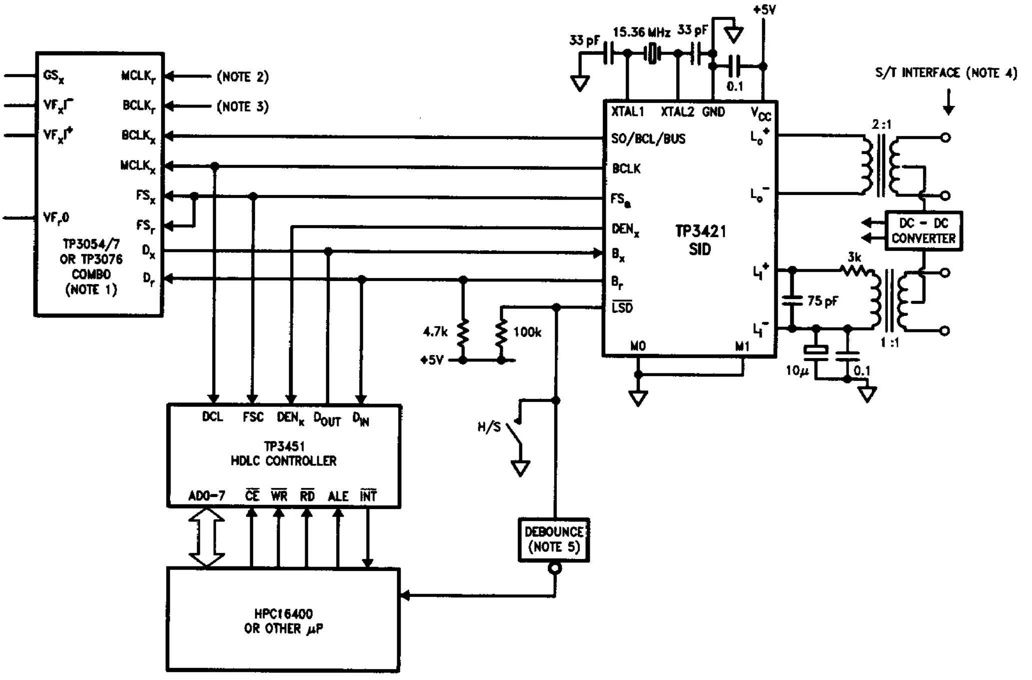
Figure 8 can be applied either to a Basic Rate interface, using the TP3421 transceiver, or to a Primary Rate interface with suitable Layer 1 devices. One TP3451 always handles the D channel traffic (at 16 kb/s or 64 kb/s, as appropriate), with another TP3451 assigned to a B channel for X.25 or V.120 circuit-switched data calls. If a call is received from a non-HDLC TE, the HDLC By pass mode can be selected to allow protocol processing in software. A DMA controller may be added as shown to improve data throughput.

In each of these TE/TA applications for Basic Rate, the TP3421 S Interface Device provides the D channel access contention resolution at the S/T interface and exercises local flow control of the D channel HDLC controller by means of the DEN_X pin. This is required only in the direction towards the network; the D channel received from the network is continuously clocked into the D_{IN} input. *Figure 9* illustrates the procedure.

Applications showing the device used for D channel processing in the network are shown in *Figures 10* and *11*. *Figure 10* shows an 8 channel line card with 8 TP3451's multiplexed on the GCI interface, using the GCI channel assigner. Any GCI compatible transceiver may be used, e.g., TP3421 for S/T or TP3410 for U. A GCI compatible exchange circuit may implement the system interface.

Figure 11 shows a centralized processing arrangement. Using a switching network the channels can be concentrated to connect either:

i. Up to 32 64 kb/s channels on a 2 Mb/s highway;
ii. up to 64 64 kb/s channels on a 4 Mb/s highway;
iii. up to 256 Basic Rate D channels on a 4 Mb/s highway.



Note 1: The TP3076 Combo must be connected to MICROWIRE Interface on the µP to control the programmable gain etc.

Note 2: To power-up the TP3054/7 Combo, MCLK, /PDN must be pulled low.

Note 3: For TP3054 (µ-law) leave $BCLK_r$ open-circuit. For TP3057 (A-law) connect $BCLK_r$ low for 1.536 MHz MCLK operation. $BCLK_X$ operates at 768 kHz.

Note 4: See TP3421 User's Manual for Line interface protection.

Note 5: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.

FIGURE 6. Low Cost ISDN Phone Application

Applications Information (Continued)

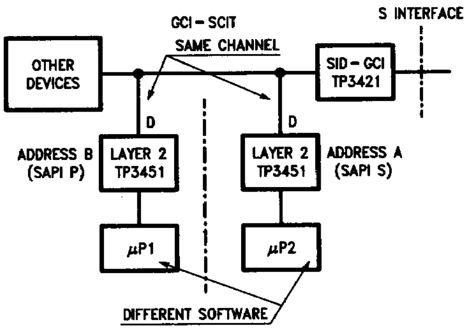


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FIGURE 7. LAPB and LAPD Protocol on the Same D Channel Handled with 2 Different HDLC Controllers

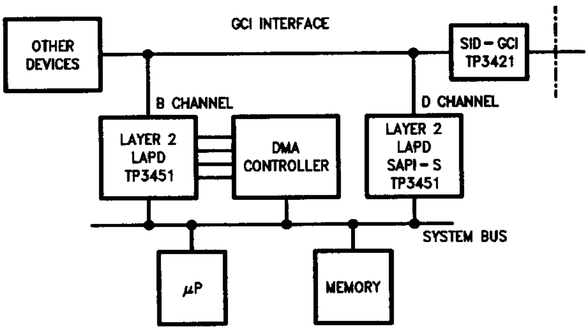

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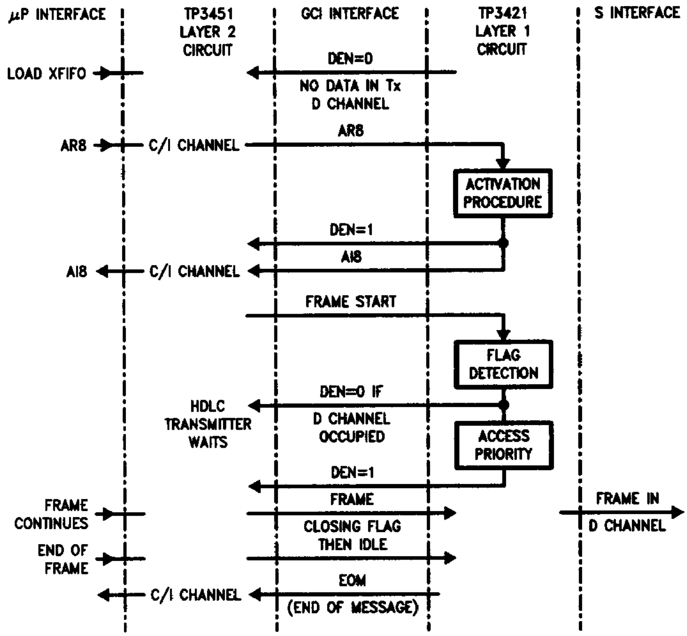
FIGURE 8. LAPB and LAPD Protocol Handling on B and D Channel

Applications Information (Continued)



Note: ARB—Activation Request 8
AIB—Activation Indication with Priority 1

FIGURE 9. Basic Rate Terminal D Channel Transmission Procedure

Applications Information (Continued)

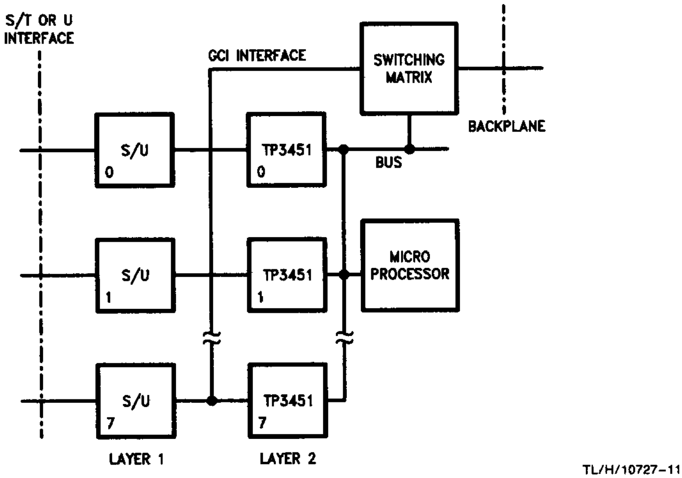


FIGURE 10. Decentralized D Channel Handling in NT2 or LT

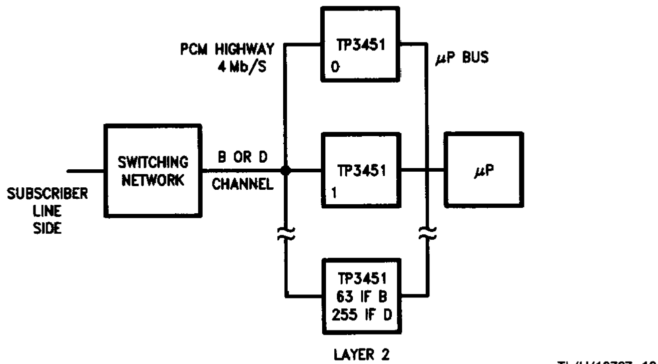


FIGURE 11. Centralized D Channel Handling in NT2 or LT

Absolute Maximium Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{DD} to V_{SS}	7V
Voltage at any Digital Input	V_{DD} + 1V to V_{SS} −1V
Storage Temp. Range	−65°C to +150°C
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating to be Determined	

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0°C to +70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage	Maximum Leakage Current: ±10 μA	2	V_{DD} + 0.4	V
V_{IL}	Low Level Input Voltage	Maximum Leakage Current: ±10 μA	V_{SS} − 0.4	0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 μA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.45	V
V_{OL} D_{OUT}	Low Level Output Voltage D_{OUT}	I_{OL} = 7 mA		0.45	V
C	Input/Output Capacitance			10	pF
C_{OUT}	Load Capacitance D_{IN}/D_{OUT}			150	pF
	Load Capacitance $\overline{INT}$			150	pF
	Load Capacitance ADD/T			100	pF
I_{DD}	Supply Current				mA

Timing Characteristics

SERIAL PORT (see *Figures 12* and *13*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FSync	FS Frequency		0	8		kHz
F_{CLK}	CLK Frequency	GCI Mode; 64 x n x FSync; 1 ≤ n ≤ 8	512		4096	kHz
		Double Clock Mode (Non-GCI); 16 x n x FSync; 1 ≤ n ≤ 64	128		8192	kHz
		Single Clock Mode; 8 x n x FSync; 1 ≤ n ≤ 64	64		4096	kHz
t_{WCH}	Period of CLK High		80			ns
t_{WCL}	Period of CLK Low		80			ns
t_{RC}	Rise Time of CLK				30	ns
t_{FC}	Fall Time of CLK				30	ns
t_{HCF}	Hold Time: CLK to FS		0			ns
t_{SFC}	Set-Up Time: FS to CLK		30			ns
t_{DCD}	Delay Time: CLK High to Data Valid	C_L = 150 pF			80	ns
t_{DCZ}	Delay Time: CLK to Data Disabled		0		80	ns
t_{DFD}	Delay Time: FS High to Data Valid	Applies only if FS Rises Later than CLK Rising Edge. C_L = 150 pF			80	ns
t_{SDC}	Set-Up Time: Data Valid to CLK		20			ns
t_{HCD}	Hold Time: CLK Low to Data Invalid		0			ns

Timing Characteristics (Continued)

DEN$_X$ Timing (See *Figure 14*)

Symbol	Parameter	Conditions	Min	Max	Units
t_{SDXC}	DEN Setup to CLK		0		ns
t_{HCDX}	DEN Hold from CLK		30		ns

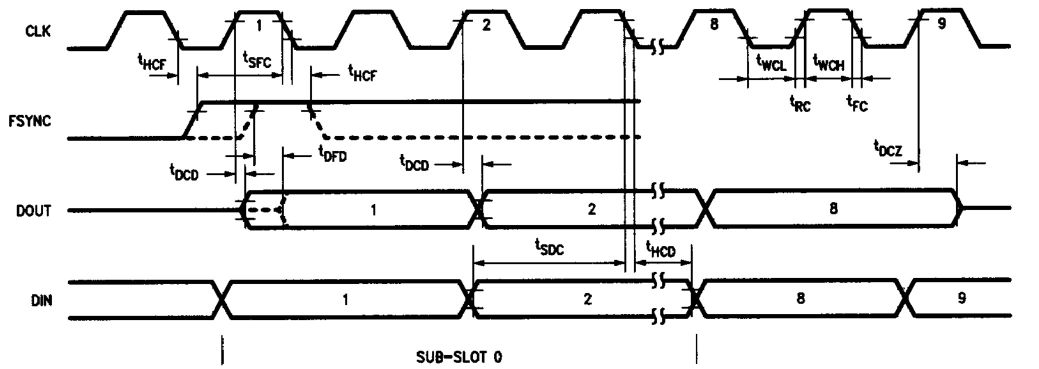


FIGURE 12. GCI and Double Clock Timing Diagram

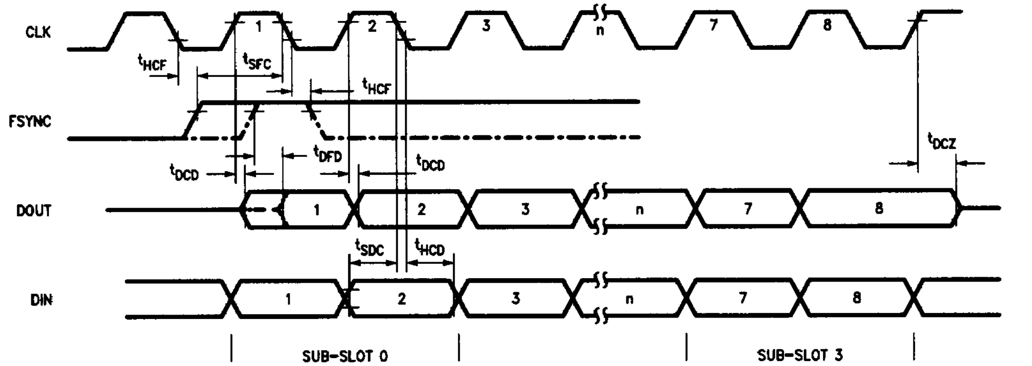


FIGURE 13. Single Clock Timing Diagram

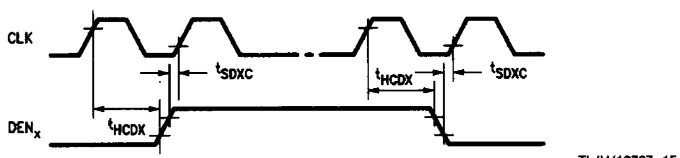


FIGURE 14. DEN$_X$ Timing

Note: DEN$_X$ normally defines 2-bit periods per frame at D_{OUT} for the D Channel.

Timing Characteristics (Continued)

Microprocessor Bus Timing

READ CYCLE (Non-Multiplexed Mode, *Figure 15*)

Symbol	Parameter	Min	Max	Units
t_{EAH}	Address Hold after E	10		ns
t_{EAH}	R/$\overline{W}$ Hold after E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. Setup	20		ns
t_{ACC}	Data Delay from E		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WE}	Minimum Width of E	110		ns

WRITE CYCLE (Non-Multiplexed Mode, *Figure 15*)

Symbol	Parameter	Min	Max	Units
t_{EAH}	Address Hold after E	10		ns
t_{EAH}	R/$\overline{W}$ Hold after E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. CS Setup	20		ns
t_{DES}	Data to End of E Setup	35		ns
t_{EDH}	End of E. CS to Data Hold	10		ns
t_{WE}	Minimum Width of E	60		ns
t_{RW}	Minimum Width of Reset	100		ns
t_{RW}	Reset (Load Max 100 pF)	100		ns

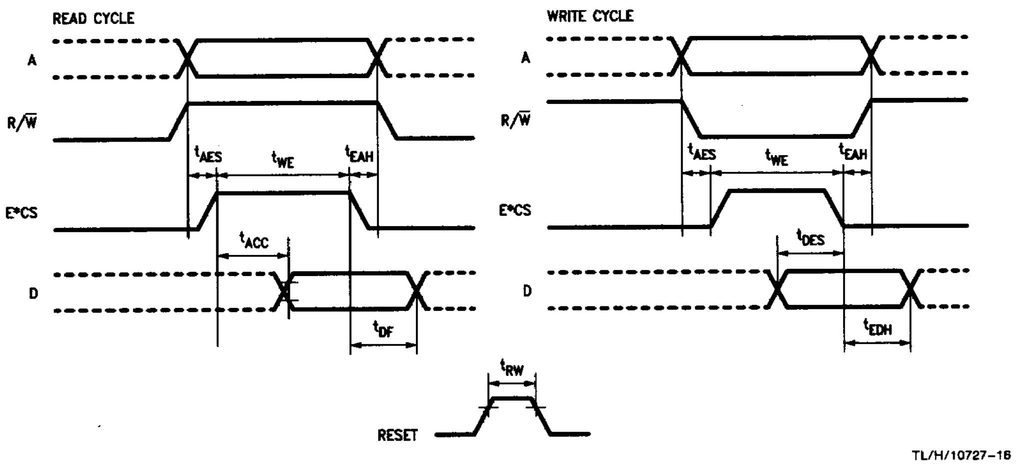


FIGURE 15. Non-Multiplexed μP Bus Timing

Microprocessor Bus Timing (Continued)

READ CYCLE (Multiplexed Intel/National Mode, *Figure 16*)

Symbol	Parameter	Min	Max	Units
t_{LA}	Address Hold after ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		110	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	$\overline{CE}$ to $\overline{RD}$ or $\overline{WR}$ Set-Up t_{CSS}	20		ns
t_{CSH}	$\overline{CE}$ Hold after $\overline{RD}$ to $\overline{WR}$ t_{CSH}	10		ns

WRITE CYCLE (Multiplexed Intel/National Mode, *Figure 16*)

Symbol	Parameter	Min	Max	Units
t_{WR}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns
t_{RW}	Reset Pulse Width	100		ns

RESET CYCLE (Demultiplexed Mode)

Symbol	Parameter	Min	Max	Units
t_{RW}	Reset Pulse Width	100		ns

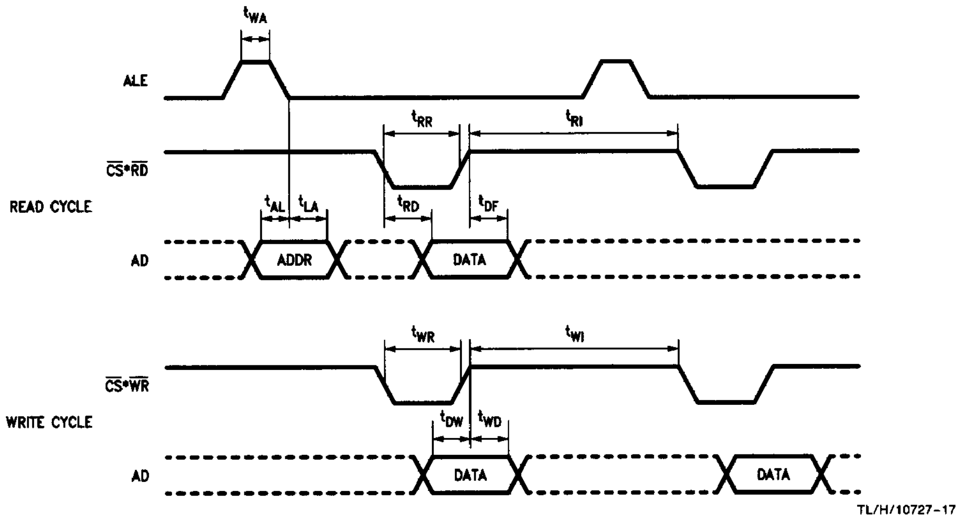


FIGURE 16. Multiplexed Intel/National μP Bus Timing

Microprocessor Bus Timing (Continued)

MULTIPLEXED MOTOROLA-LIKE μP BUS TIMING *(Figure 17)*

Symbol	Parameter	Min	Max	Units
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS Low to DS High	10		ns
t_{RWS}	RW to DS Setup	20		ns
t_{RWH}	RW Hold after DS	10		ns
t_{CSS}	$\overline{CS}$ to DS Setup	20		ns
t_{CSH}	$\overline{CS}$ Hold after DS	10		ns
t_{AAS}	Address to AS Setup	20		ns
t_{AAH}	Address Hold after AS	10		ns
READ CYCLE				
t_{DV}	Data Valid after DS		110	ns
t_{DF}	Output Flat Delay		25	ns
WRITE CYCLE				
t_{DWS}	Data to DS Setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

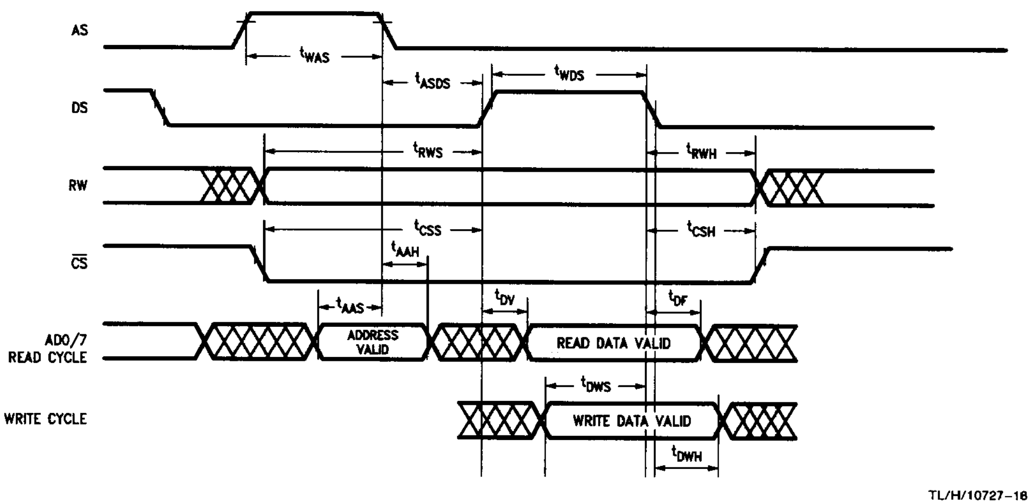


FIGURE 17. Multiplexed Motorola-Like μP Bus Timing

Microprocessor Bus Timing (Continued)

DMA BUS TIMING (Reception Mode, *Figure 18*)

Symbol	Parameter	Min	Max	Units
t_{ACC}	Data Delay from ACKR		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WARL}	Minimum Width ACKR Low	110		ns
t_{WARH}	Minimum Width ACKR High	70		ns
t_{DRAR}	REQR Delay from ACKR		80	ns

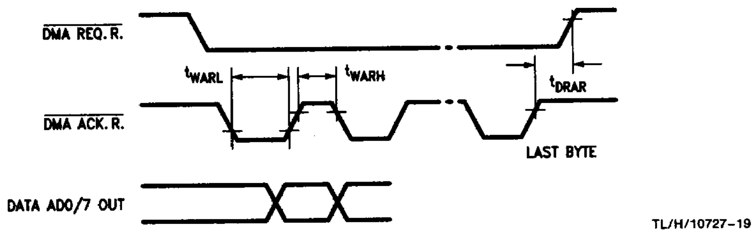


FIGURE 18. DMA Frame Reception Timing

DMA BUS TIMING (Transmission Mode, *Figure 19*)

Symbol	Parameter	Min	Max	Units
t_{DAS}	Data Setup to ACKX	35		ns
t_{DAH}	Data Hold from ACKX	10		ns
t_{WAXL}	Minimum Width ACKX Low	60		ns
t_{WAXH}	Minimum Width ACKX High	70		ns
t_{DRAX}	REQX Delay from ACKX	80		ns

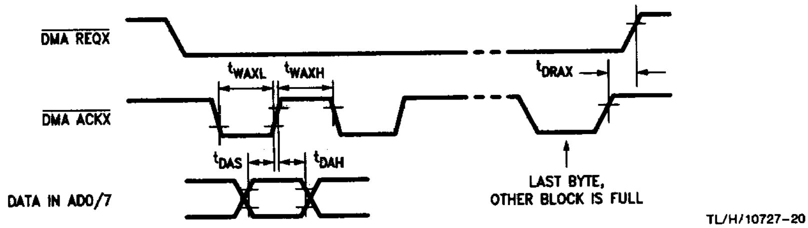


FIGURE 19. DMA Frame Transmission Timing